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ภาคผนวก ก

คุณสมบัติของ IC เบอร์ LH0022CH

LH0022/LH0022C, LH0042/LH0042C, LH0052/LH0052C

National Semiconductor

Operational Amplifiers/Buffers

LH0022/LH0022C High Performance FET Op Amp
LH0042/LH0042C Low Cost FET Op Amp
LH0052/LH0052C Precision FET Op Amp

general description

The LH0022/LH0042/LH0052 are a family of FET input operational amplifiers with very closely matched input characteristics, very high input impedance, and ultra-low input currents with no compromise in noise, common mode rejection ratio, open loop gain, or slew rate. The internally laser nulled LH0052 offers 500 microvolts maximum offset and 5 $\mu V/^{\circ}C$ offset drift. Input offset current is less than 500 femtoamps at room temperature and 100 pA maximum at 125°C. The LH0022 and LH0042 are not internally nulled but offer comparable matching characteristics. All devices in the family are internally compensated and are free of latch-up and unusual oscillation problems. The devices may be offset nulled with a single 10k trimpot with neglible effect in CMRR.

The LH0022, LH0042 and LH0052 are specified for operation over the −55°C to +125°C military temperature range. The LH0022C, LH0042C and LH0052C are specified for operation over the −25°C to +85°C temperature range.

features

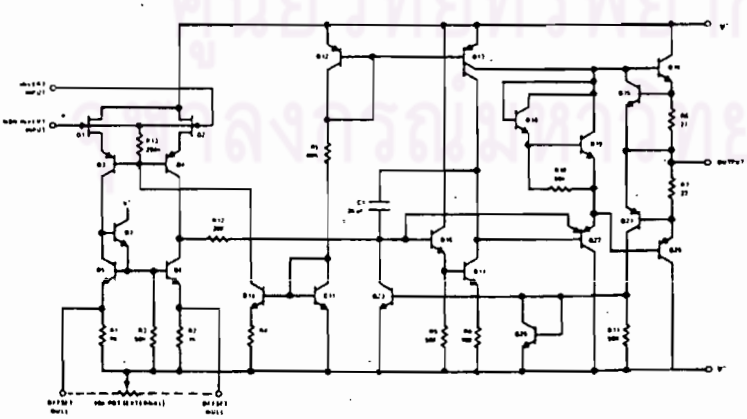
- Low input offset current—500 femtoamps max. (LH0052)
- Low input offset drift—5 $\mu V/^{\circ}C$ max (LH0052)
- Low input offset voltage — 100 microvolts-typ.
- High open loop gain — 100 dB typ.
- Excellent slew rate — 3.0 V/μs typ.
- Internal 6 dB/octave frequency compensation
- Pin compatible with standard IC op amps (TO-5 package)

The LH0022/LH0042/LH0052 family of IC op amps are intended to fulfill a wide variety of applications for process control, medical instrumentation, and other systems requiring very low input currents and tightly matched input offsets. The LH0052 is particularly suited for long term high accuracy integrators and high accuracy sample and hold buffer amplifiers. The LH0022 and LH0042 provide low cost high performance for such applications as electrometer and photocell amplification, pico-ammeters, and high input impedance buffers.

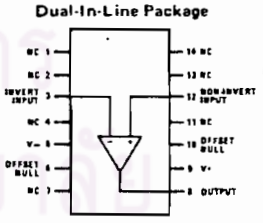
Special electrical parameter selection and custom built circuits are available on special request.

For additional application information and information on other National operational amplifiers, see *Available Linear Applications Literature.*

schematic and connection diagrams

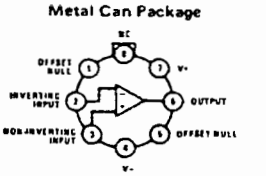


Dual-In-Line Package



Order Number LH0022D, LH0022CD, LH0042D, LH0042CD, LH0052D or LH0052CD
See Package D14E

Metal Can Package



Order Number LH0022H, LH0022CH, LH0042H, LH0042CH, LH0052H or LH0052CH
See Package H08A

*Previously Called NH0022/NH0022C

absolute maximum ratings

Supply Voltage	±22V
Power Dissipation (see graph)	500 mW
Input Voltage (Note 1)	±15V
Differential Input Voltage (Note 2)	±30V
Voltage Between Offset Null and V^-	±0.5V
Short Circuit Duration	Continuous
Operating Temperature Range	
LH0022, LH0042, LH0052	-55°C to +125°C
LH0022C, LH0042C, LH0052C	-25°C to +85°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

dc electrical characteristics For LH0022/LH0022C (Note 3)

PARAMETER	CONDITIONS	LIMITS						UNITS
		LH0022			LH0022C			
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$R_S \leq 100\ k\Omega$; $T_A = 25°C$, $V_S = \pm 15V$		2.0	4.0		3.5	6.0	mV
	$R_S \leq 100\ k\Omega$, $V_S = \pm 15V$			5.0			7.0	mV
Temperature Coefficient of Input Offset Voltage	$R_S \leq 100\ k\Omega$		5	10		5	15	µV/°C
Offset Voltage Drift with Time			3			4		µV/week
Input Offset Current	(Note 4)		0.2	2.0		1.0	5.0	pA
				2.0			0.5	nA
Temperature Coefficient of Input Offset Current		Doubles every 10°C			Doubles every 10°C			
Offset Current Drift with Time			0.1			0.1		pA/week
Input Bias Current	(Note 4)		5	10		10	25	pA
				10			2.5	nA
Temperature Coefficient of Input Bias Current		Doubles every 10°C			Doubles every 10°C			
Differential Input Resistance			10^{12}			10^{12}		Ω
Common Mode Input Resistance			10^{12}			10^{12}		Ω
Input Capacitance			4.0			4.0		pF
Input Voltage Range	$V_S = \pm 15V$	±12	±13.5		±12	±13.5		V
Common Mode Rejection Ratio	$R_S \leq 10\ k\Omega$, $V_{IN} = \pm 10V$	80	90		70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\ k\Omega$, $\pm 5V \leq V_S \leq \pm 15V$	80	90		70	90		dB
Large Signal Voltage Gain	$R_L = 2\ k\Omega$, $V_{OUT} = \pm 10V$, $T_A = 25°C$, $V_S = \pm 15V$	100	200		75	160		V/mV
	$R_L = 2\ k\Omega$, $V_{OUT} = \pm 10V$, $V_S = \pm 15V$	50			50			V/mV
Output Voltage Swing	$R_L = 1\ k\Omega$, $T_A = 25°C$, $V_S = \pm 15V$	±10	±12.5		±10	±12		V
	$R_L = 2\ k\Omega$, $V_S = \pm 15V$	±10			±10			V
Output Current Swing	$V_{OUT} = \pm 10V$, $T_A = 25°C$	±10	±15		±10	±15		mA
Output Resistance			75			75		Ω
Output Short Circuit Current			25			25		mA
Supply Current	$V_S = \pm 15V$		2.0	2.5		2.4	2.8	mA
Power Consumption	$V_S = \pm 15V$			75			85	mW

dc electrical characteristics for LH0042/LH0042C (Note 3)

(V_S = ±15V; unless otherwise specified)

PARAMETER	CONDITIONS	LIMITS						UNITS
		LH0042			LH0042C			
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$R_S \leq 100\ k\Omega$		5.0	20		6.0	20	mV
Temperature Coefficient of Input Offset Voltage	$R_S \leq 100\ k\Omega$		5			10		µV/°C
Offset Voltage Drift with Time			7			10		µV/week
Input Offset Current	(Note 4)		1	5		2	10	pA
Temperature Coefficient of Input Offset Current		Doubles every 10°C			Doubles every 10°C			
Offset Current Drift with Time			0.1			0.1		pA/week
Input Bias Current	(Note 4)		10	25		15	50	pA
Temperature Coefficient of Input Bias Current		Doubles every 10°C			Doubles every 10°C			
Differential Input Resistance			10^{12}			10^{12}		Ω
Common Mode Input Resistance			10^{12}			10^{12}		Ω
Input Capacitance			4.0			4.0		pF
Input Voltage Range		±12	±13.5		±12	±13.5		V
Common Mode Rejection Ratio	$R_S \leq 10\ k\Omega$, V_{IN} = ±10V	70	86		70	80		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\ k\Omega$, ±5V ≤ V_S ≤ ±15V	70	86		70	80		dB
Large Signal Voltage Gain	R_L = 1 kΩ, V_{OUT} = ±10V	50	150		25	100		V/mV
Output Voltage Swing	R_L = 1 kΩ	±10	±12.5		±10	±12		V
Output Current Swing	V_{OUT} = ±10V	±10	±15		±10	±15		mA
Output Resistance			75			75		Ω
Output Short Circuit Current			20			20		mA
Supply Current			2.5	3.5		2.8	4.0	mA
Power Consumption				105			120	mW

dc electrical characteristics For LH0052/LH0052C (Note 3)

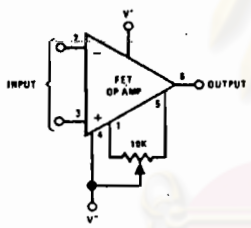
PARAMETER	CONDITIONS	LIMITS						UNITS
		LH0052			LH0052C			
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$R_S \leq 100\ k\Omega$; V_S = ±15V, T_A = 25°C		0.1	0.5		0.2	1.0	mV
	$R_S \leq 100\ k\Omega$, V_S = ±15V			1.0			1.5	mV
Temperature Coefficient of Input Offset Voltage	$R_S \leq 100\ k\Omega$, V_S = ±15V		2	5		5	10	µV/°C
Offset Voltage Drift with Time			2			4		µV/week
Input Offset Current	(Note 4)		0.01	0.5		0.02	1.0	pA
				100			100	pA
Temperature Coefficient of Input Offset Current		Doubles every 10°C			Doubles every 10°C			
Offset Current Drift with Time			<0.1			<0.1		pA/week
Input Bias Current	(Note 4)		0.5	2.5		1.0	5.0	pA
				2.5			0.5	nA
Temperature Coefficient of Input Bias Current		Doubles every 10°C			Doubles every 10°C			
Differential Input Resistance			10^{12}			10^{12}		Ω
Common Mode Input Resistance			10^{12}			10^{12}		Ω
Input Capacitance			4.0			4.0		pF
Input Voltage Range	V_S = ±15V	±12	±13.5		±12	±13.5		V
Common Mode Rejection Ratio	$R_S \leq 10\ k\Omega$, V_{IN} = ±10V	74	90		70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\ k\Omega$, ±5V ≤ V_S ≤ ±15V	74	90		70	90		dB
Large Signal Voltage Gain	R_L = 2 kΩ, V_{OUT} = ±10V, V_S = ±15V, T_A = 25°C	100	200		75	160		V/mV
	R_L = 2 kΩ, V_{OUT} = ±10V, V_S = ±15V	50			50			V/mV
Output Voltage Swing	R_L = 1 kΩ, T_A = 25°C V_S = ±15V	±10	±12.5		±10	±12		V
	R_L = 2 kΩ, V_S = ±15V	±10			±10			V
Output Current Swing	V_{OUT} = ±10V, T_A = 25°C	±10	±15		±10	±15		mA
Output Resistance			75			75		Ω
Output Short Circuit Current			25			25		mA
Supply Current	V_S = ±15V		3.0	3.5		3.0	3.8	mA
Power Consumption	V_S = ±15V			105			114	mW

ac electrical characteristics For all amplifiers (T_A = 25°C, V_S = ±15V)

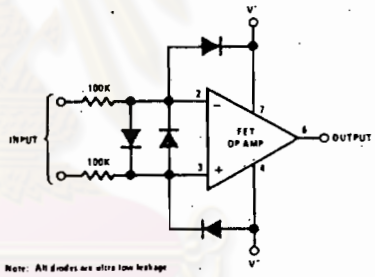
PARAMETER	CONDITIONS	LIMITS						UNITS
		LH0022/42/52			LH0022C/42C/52C			
		MIN	TYP	MAX	MIN	TYP	MAX	
Slew Rate	Voltage Follower	1.5	3.0		1.0	3.0		V/μs
Large Signal Bandwidth	Voltage Follower		40			40		kHz
Small Signal Bandwidth			1.0			1.0		MHz
Rise Time			0.3	1.5		0.3	1.5	μs
Overshoot			10	30		15	40	%
Settling Time (0.1 %)	ΔV_{IN} = 10V		4.5			4.5		μs
Overload Recovery			4.0			4.0		μs
Input Noise Voltage	R_S = 10 kΩ, f_o = 10 Hz		150			150		nV/√Hz
Input Noise Voltage	R_S = 10 kΩ, f_o = 100 Hz		55			55		nV/√Hz
Input Noise Voltage	R_S = 10 kΩ, f_o = 1 kHz		35			35		nV/√Hz
Input Noise Voltage	R_S = 10 kΩ, f_o = 10 kHz		30			30		nV/√Hz
Input Noise Voltage	BW = 10 Hz to 10 kHz, R_S = 10 kΩ		12			12		μVrms
Input Noise Current	BW = 10 Hz to 10 kHz		<.1			<.1		pArms

Note 1: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
Note 2: Rating applies for minimum source resistance of 10 kΩ, for source resistances less than 10 kΩ, maximum differential input voltage is ±5V.
Note 3: Unless otherwise specified, these specifications apply for ±5V ≤ V_S ≤ ±20V and -55° C ≤ T_A ≤ ±125°C for the LH0022 and LH0052 and -25°C ≤ T_A ≤ +85°C for the LH0022 and LH0052C. Typical values are given for T_A = 25°C.
Note 4: Input currents are a strong function of temperature. Due to high speed testing they are specified a junction temperature T_j = 25° C, self heating will cause an increase in current in manual tests.

auxiliary circuits (shown for TO-5 pin out)

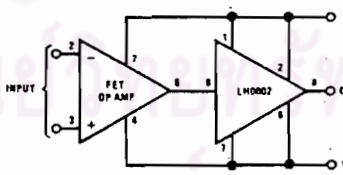


Offset Null



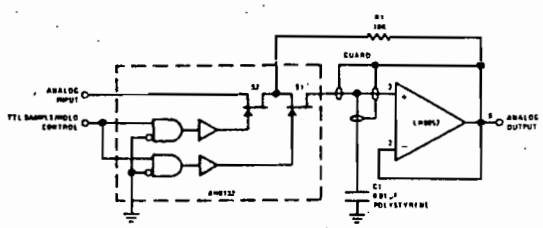
Note: All diodes are ultra low leakage

Protecting Inputs From ±150V Transients

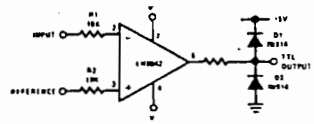


Boosting Output Drive to ±100 mA

typical applications

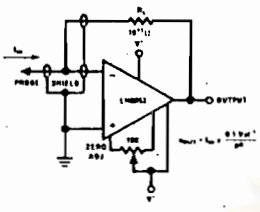


Low Drift Sample and Hold

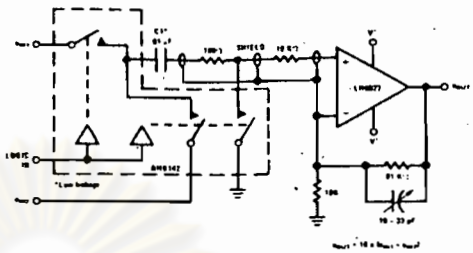


Precision Voltage Comparator

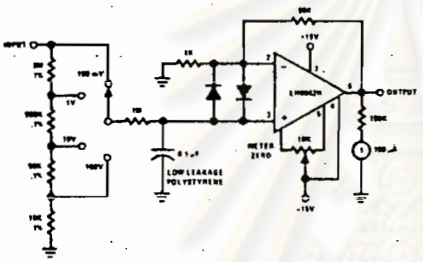
typical applications (con't)



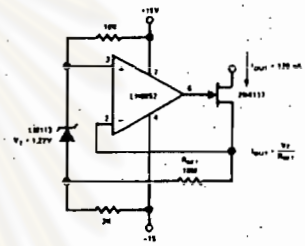
Picoamp Amplifier for pH Meters and Radiation Detectors



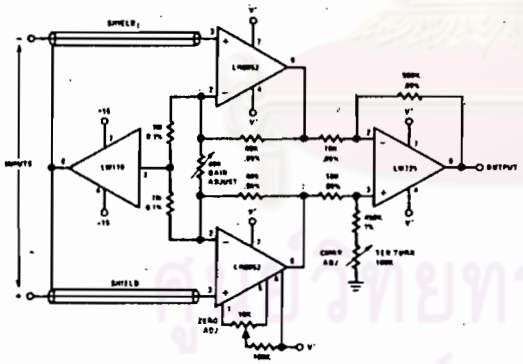
Precision Subtractor for Automatic Test Gear



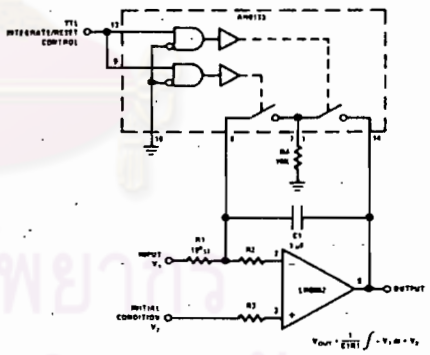
Sensitive Low Cost "VTVM"



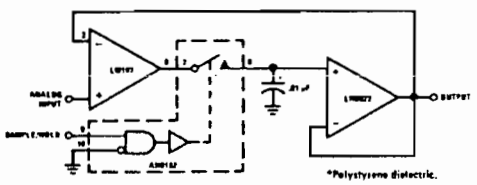
Ultra Low Level Current Source



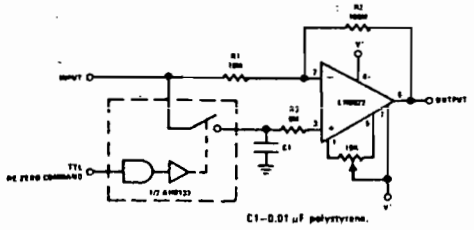
True Instrumentation Amplifier



Precision Integrator



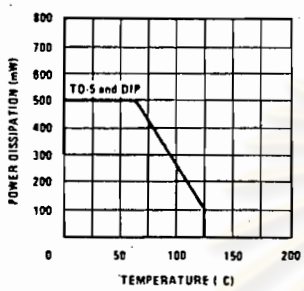
Precision Sample and Hold



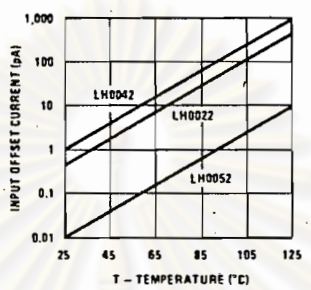
Re-Zeroing Amplifier

typical performance characteristics

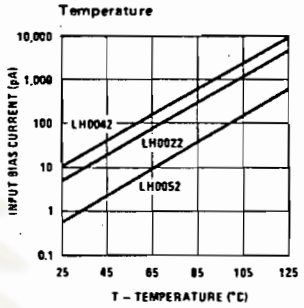
Maximum Power Dissipation



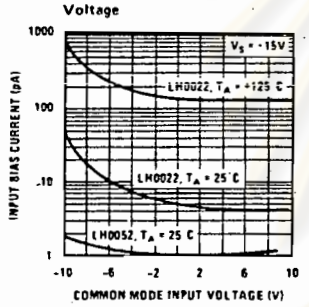
Input Offset Current vs Temperature



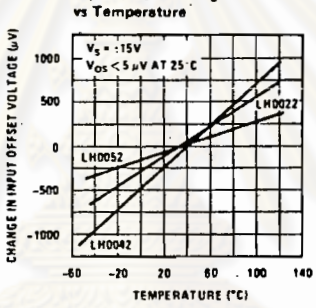
Input Bias Current vs Temperature



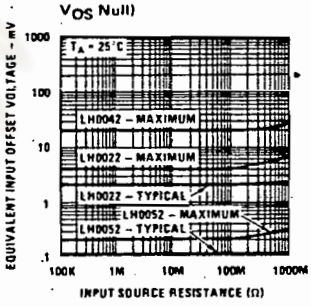
Input Bias Current vs Input Voltage



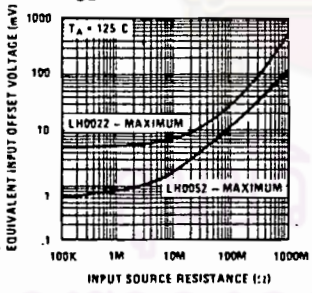
Input Offset Voltage vs Temperature



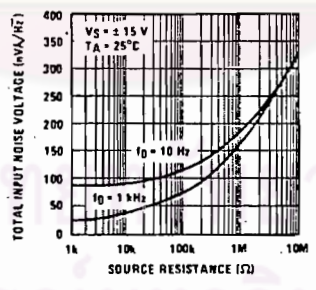
Offset Error (Without V_{OS} Null)



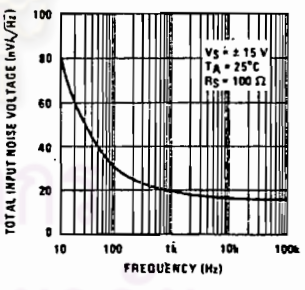
Offset Error (Without V_{OS} Null)



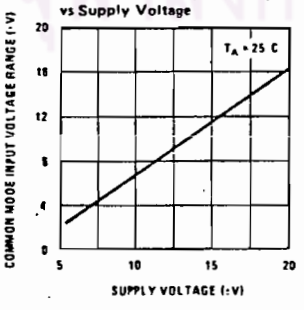
Total Input Noise Voltage* vs Source Resistance



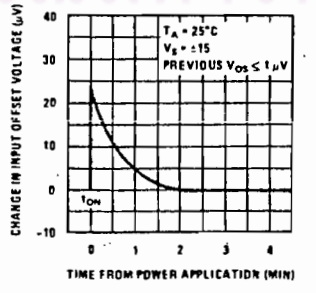
Total Input Noise Voltage* vs Frequency



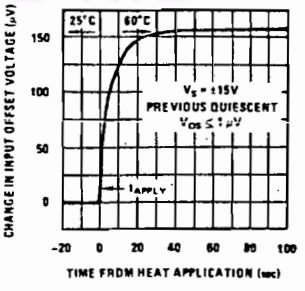
Common Mode Input Voltage vs Supply Voltage



Stabilization Time of Input Offset Voltage from Power Turn-On



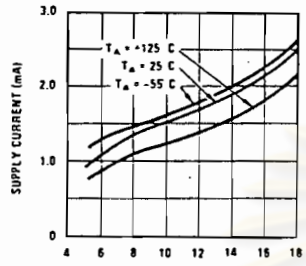
Change in Input Offset Voltage Due to Thermal Shock vs Time



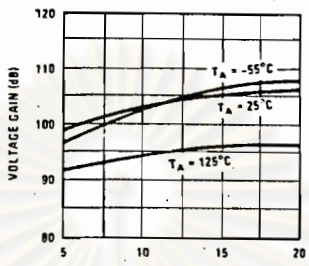
*Noise Voltage Includes Contribution from Source Resistance

typical performance characteristics (con't)

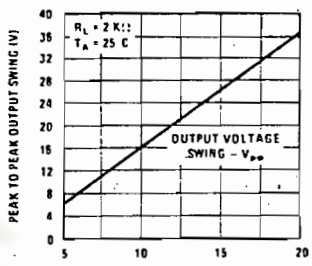
Supply Voltage vs Supply Current



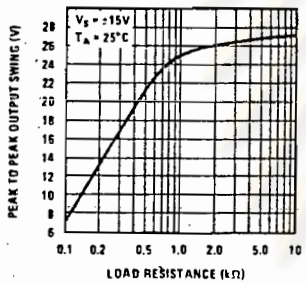
Voltage Gain



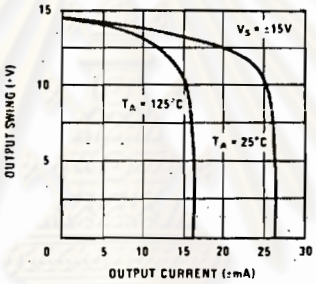
Output Swing vs Supply Voltage



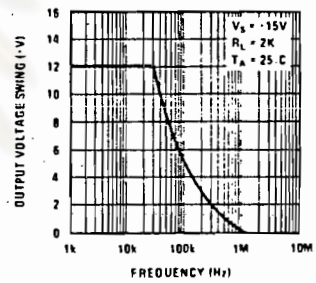
Output Voltage Swing vs Load Resistance



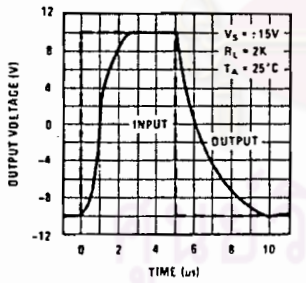
Current Limiting



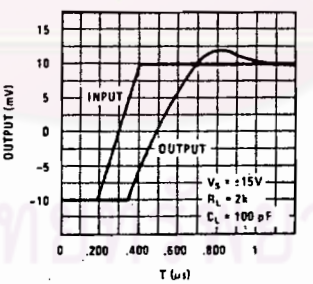
Output Voltage Swing vs Frequency



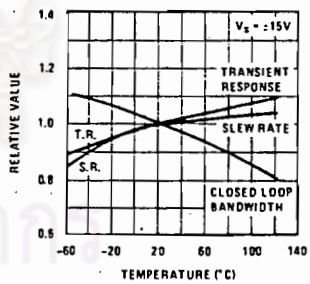
Voltage Follower Large Signal Response



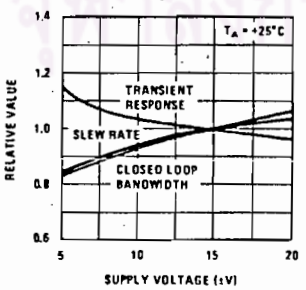
Transient Response



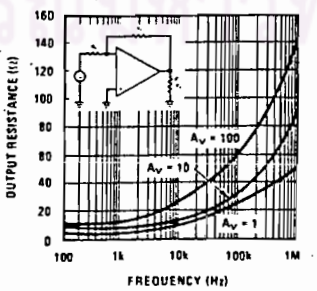
Frequency Characteristics vs Ambient Temperature



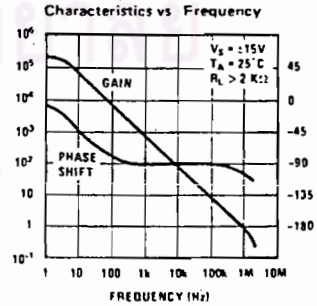
Frequency Characteristics vs Supply Voltage



Output Resistance vs Frequency



Open Loop Transfer Characteristics vs Frequency



ภาคผนวก ข

คุณสมบัติของ IC เบอร์ LM4250CN

LM4250/LM4250C

National Semiconductor

Operational Amplifiers/Buffers

LM4250/LM4250C Programmable Operational Amplifier

General Description

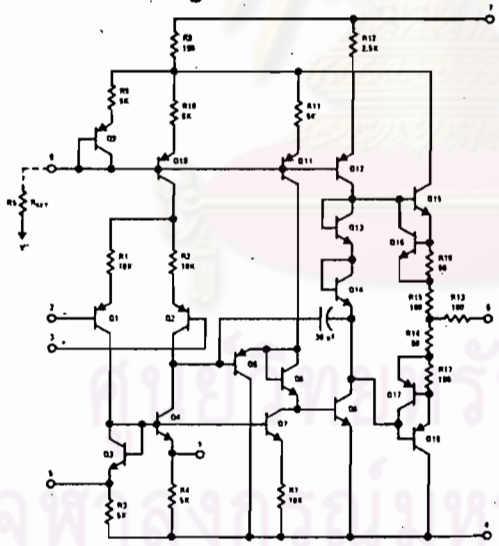
The LM4250 and LM4250C are extremely versatile programmable monolithic operational amplifiers. A single external master bias current setting resistor programs the input bias current, input offset current, quiescent power consumption, slew rate, input noise, and the gain-bandwidth product. The device is a truly general purpose operational amplifier.

Features

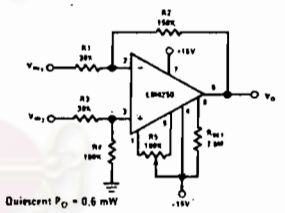
- ±1V to ±18V power supply operation
- 3 nA input offset current
- Standby power consumption as low as 500 nW
- No frequency compensation required
- Programmable electrical characteristics
- Offset Voltage nulling capability
- Can be powered by two flashlight batteries
- Short circuit protection

The LM4250C is identical to the LM4250 except that the LM4250C has its performance guaranteed over a 0°C to 70°C temperature range instead of the −55°C to +125°C temperature range of the LM4250.

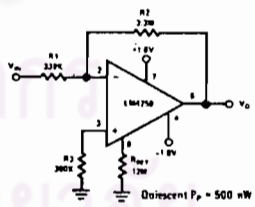
Schematic Diagrams



Typical Applications



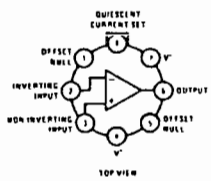
X5 Difference Amplifier



500 Nano-Watt X10 Amplifier

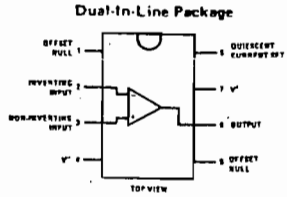
Connection Diagrams

Metal Can Package



Order Number LM4250H or LM4250CH
See NS Package H08C

Dual-In-Line Package



Order Number LM4250CN
See NS Package N08B
Order Number LM4250J
or LM4250CJ
See NS Package J08A

Absolute Maximum Ratings

Supply Voltage	±18V	Output Short-Circuit Duration		Indefinite
Power Dissipation (Note 1)	500 mW	Operating Temperature Range	LM4250	$-55°C \leq T_A \leq 125°C$
Differential Input Voltage	±30V		LM4250C	$0°C \leq T_A \leq 70°C$
Input Voltage (Note 2)	±15V	Storage Temperature Range		-65°C to 150°C
I_{SET} Current	150 μA	Lead Temperature (Soldering,10 sec)		300°C

Electrical Characteristics

LM4250 ($-55°C \leq T_A \leq 125°C$ unless otherwise specified)

PARAMETERS	CONDITIONS	$V_S = \pm 1.5V$			
		$I_{SET} = 1\ \mu A$		$I_{SET} = 10\ \mu A$	
		MIN	MAX	MIN	MAX
V_{OS}	$T_A = 25°$ $R_S \leq 100\ k\Omega$		3 mV		5 mV
I_{OS}	$T_A = 25°$		3 nA		10 nA
I_{bias}	$T_A = 25°$		7.5 nA		50 nA
Large Signal Voltage Gain	$T_A = 25°$ $R_L = 100\ k\Omega$	40k			
	$V_O = \pm 0.6$, $R_L = 10\ k\Omega$			50k	
Supply Current	$T_A = 25°C$		7.5 μA		80 μA
Power Consumption	$T_A = 25°C$		23 μW		240 μW
V_{OS}	$R_S \leq 100\ k\Omega$		4 mV		6 mV
I_{OS}	$T_A = 125°C$		5 nA		10 nA
	$T_A = -55°C$		3 nA		10 nA
I_{bias}			7.5 nA		50 nA
Input Voltage Range		±0.7V		±0.7V	
Large Signal Voltage Gain	$V_O = \pm 0.6V$ $R_L = 100\ k\Omega$	30k			
	$R_L = 10\ k\Omega$			30k	
Output Voltage Swing	$R_L = 100\ k\Omega$	±0.6V			
	$R_L = 10\ k\Omega$			±0.6V	
Common Mode Rejection Ratio	$R_S \leq 10\ k\Omega$	70 dB		70 dB	
Supply Voltage Rejection Ratio	$R_S \leq 10\ k\Omega$	76 dB		76 dB	
Supply Current			8 μA		90 μA
Power Consumption			24 μW		270 μW

PARAMETERS	CONDITIONS	$V_S = \pm 15V$			
		$I_{SET} = 1\ \mu A$		$I_{SET} = 10\ \mu A$	
		MIN	MAX	MIN	MAX
V_{OS}	$T_A = 25°C$ $R_S \leq 100\ k\Omega$		3 mV		5 mV
I_{OS}	$T_A = 25°C$		3 nA		10 nA
I_{bias}	$T_A = 25°C$		7.5 nA		50 nA
Large Signal Voltage Gain	$T_A = 25°C$ $R_L = 100\ k\Omega$	100k			
	$V_O = \pm 10V$ $R_L = 10\ k\Omega$			100k	
Supply Current	$T_A = 25°C$		10 μA		90 μA
Power Consumption	$T_A = 25°C$		300 μW		2.7 mW
V_{OS}	$R_S \leq 100\ k\Omega$		4 mV		6 mV
I_{OS}	$T_A = 125°C$		25 nA		25 nA
	$T_A = -55°C$		3 nA		10 nA
I_{bias}			7.5 nA		50 nA
Input Voltage Range		±13.5V		±13.5V	
Large Signal Voltage Gain	$V_O = \pm 10V$ $R_L = 100\ k\Omega$	50k			
	$R_L = 10\ k\Omega$			50k	
Output Voltage Swing	$R_L = 100\ k\Omega$	±12V			
	$R_L = 10\ k\Omega$			±12V	
Common Mode Rejection Ratio	$R_S \leq 10\ k\Omega$	70 dB		70 dB	
Supply Voltage Rejection Ratio	$R_S \leq 10\ k\Omega$	76 dB		76 dB	
Supply Current			11 μA		100 μA
Power Consumption			330 μW		3 mW

Note 1: The maximum junction temperature of the LM4250 is 150°C, while that of the LM4250C is 100°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W junction to ambient, or 45°C/W junction to case. The thermal resistance of the dual-in-line package is 125°C/W.

Note 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Electrical Characteristics LM4250C ($0°C \leq T_A \leq 70°C$ unless otherwise specified)

PARAMETERS	CONDITIONS	$V_S = \pm 1.5V$			
		$I_{SET} = 1\ \mu A$		$I_{SET} = 10\ \mu A$	
		MIN	MAX	MIN	MAX
V_{OS}	$T_A = 25°C$ $R_S \leq 100\ k\Omega$		5 mV		6 mV
I_{OS}	$T_A = 25°C$		6 nA		20 nA
I_{bias}	$T_A = 25°C$		10 nA		75 nA
Large Signal Voltage Gain	$T_A = 25°C$ $R_L = 100\ k\Omega$	25k			
	$V_O = \pm 0.6V$ $R_L = 10\ k\Omega$			25k	
Supply Current	$T_A = 25°C$		8 μA		90 μA
Power Consumption	$T_A = 25°C$		24 μW		270 μW
V_{OS}	$R_S \leq 10\ k\Omega$		6.5 mV		7.5 mV
I_{OS}			8 nA		25 nA
I_{bias}			10 nA		80 nA
Input Voltage Range		±0.6V		±0.6V	
Large Signal Voltage Gain	$V_O = \pm 0.6V$ $R_L = 100\ k\Omega$	25k			
	$R_L = 10\ k\Omega$			25k	
Output Voltage Swing	$R_L = 100\ k\Omega$	±0.6V			
	$R_L = 10\ k\Omega$			±0.6V	
Common Mode Rejection Ratio	$R_S \leq 10\ k\Omega$	70 dB		70 dB	
Supply Voltage Rejection Ratio	$R_S \leq 10\ k\Omega$	74 dB		74 dB	
Supply Current			8 μA		90 uA
Power Consumption			24 μW		270 uW

PARAMETERS	CONDITIONS	$V_S = \pm 15V$			
		$I_{SET} = 1\ \mu A$		$I_{SET} = 10\ \mu A$	
		MIN	MAX	MIN	MAX
V_{OS}	$T_A = 25°C$ $R_S \leq 100\ k\Omega$		5 mV		6 mV
I_{OS}	$T_A = 25°C$		6 nA		20 nA
I_{bias}	$T_A = 25°C$		10 nA		75 nA
Large Signal Voltage Gain	$T_A = 25°C$ $R_L = 100\ k\Omega$	60k			
	$V_O = \pm 10V$ $R_L = 10\ k\Omega$			60k	
Supply Current	$T_A = 25°C$		11 μA		100 μA
Power Consumption	$T_A = 25°C$		330 μW		3 mW
V_{OS}	$R_S \leq 10\ k\Omega$		6.5 mV		7.5 mV
I_{OS}			8 nA		25 nA
I_{bias}			10 nA		80 nA
Input Voltage Range		±13.5V		±13.5V	
Large Signal Voltage Gain	$V_O = \pm 10V$ $R_L = 100\ k\Omega$	50k			
	$R_L = 10\ k\Omega$			50k	
Output Voltage Swing	$R_L = 100\ k\Omega$	±12V			
	$R_L = 10\ k\Omega$			±12V	
Common Mode Rejection Ratio	$R_S \leq 10\ k\Omega$	70 dB		70 dB	
Supply Voltage Rejection Ratio	$R_S \leq 10\ k\Omega$	74 dB		74 dB	
Supply Current			11 uA		100 uA
Power Consumption			300 uW		3 mW

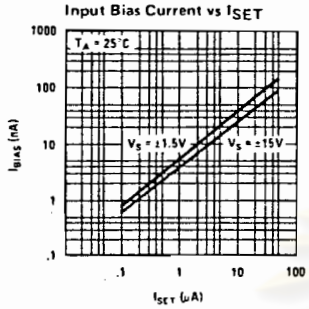
Resistor Biasing

Set Current Setting Resistor to V^-

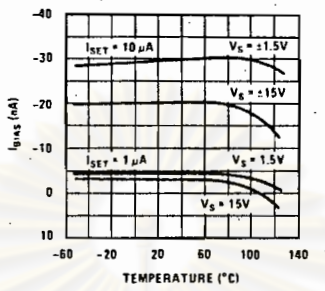
	I_{SET}				
V_S	0.1 μA	0.5 μA	1.0 μA	5 μA	10 μA
±1.5V	25.6 MΩ	5.04 MΩ	2.5 MΩ	492 kΩ	244 kΩ
±3.0V	55.6 MΩ	11.0 MΩ	5.5 MΩ	1.09 MΩ	544 kΩ
±6.0V	116 MΩ	23.0 MΩ	11.5 MΩ	2.29 MΩ	1.14 MΩ
±9.0V	176 MΩ	35.0 MΩ	17.5 MΩ	3.49 MΩ	1.74 MΩ
±12.0V	236 MΩ	47.0 MΩ	23.5 MΩ	4.69 MΩ	2.34 MΩ
±15.0V	296 MΩ	59.0 MΩ	29.5 MΩ	5.89 MΩ	2.94 MΩ

Typical Performance Characteristics

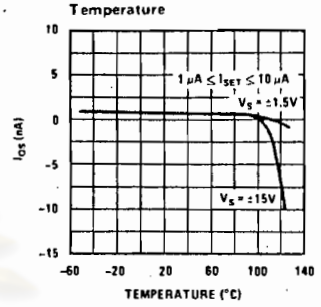
Input Bias Current vs I_{SET}



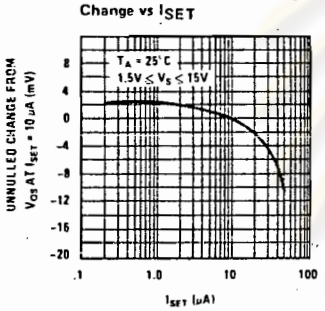
Input Bias Current vs Temperature



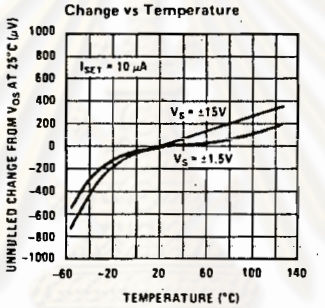
Input Offset Current vs Temperature



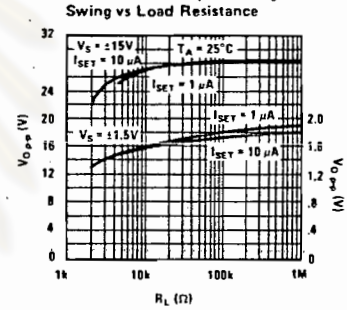
Unnulled Input Offset Voltage Change vs I_{SET}



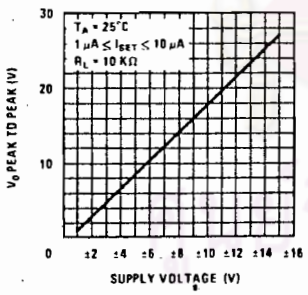
Unnulled Input Offset Voltage Change vs Temperature



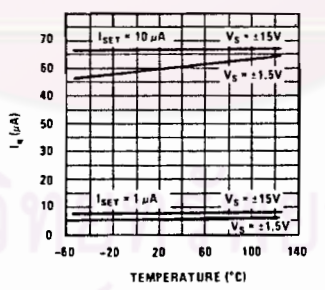
Peak to Peak Output Voltage Swing vs Load Resistance



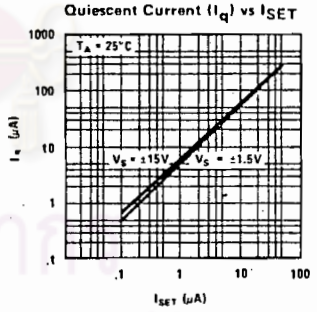
Peak to Peak Output Voltage Swing vs Supply Voltage



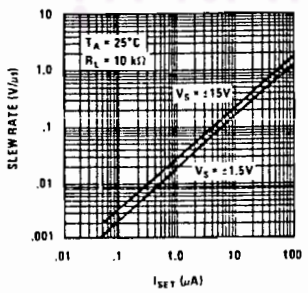
Quiescent Current (I_Q) vs Temperature



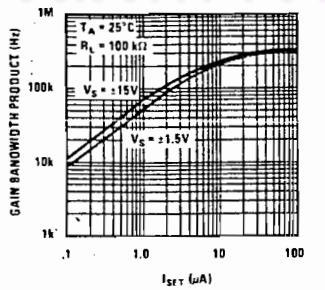
Quiescent Current (I_Q) vs I_{SET}



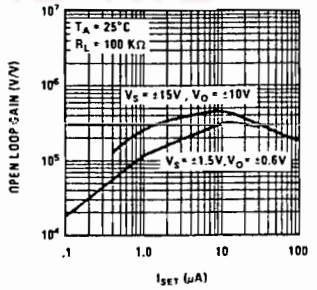
Slew Rate vs I_{SET}



Gain Bandwidth Product vs I_{SET}

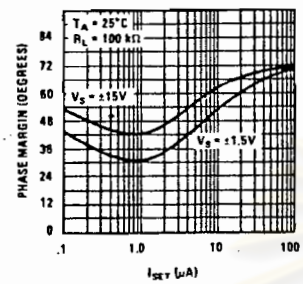


Open Loop Voltage Gain vs I_{SET}

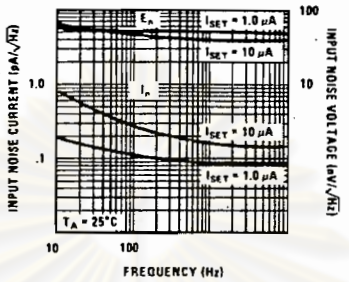


Typical Performance Characteristics (Continued)

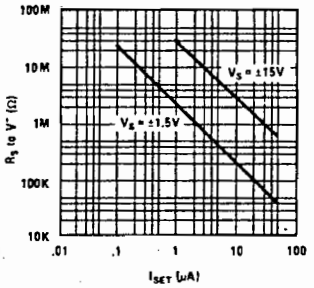
Phase Margin vs I_{SET}



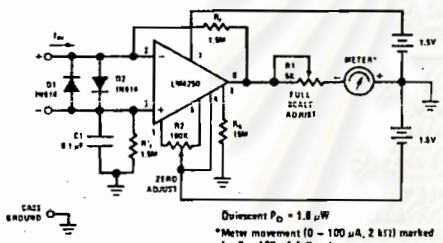
Input Noise Current (I_n) and Voltage (E_n) vs Frequency



R_{SET} vs I_{SET}



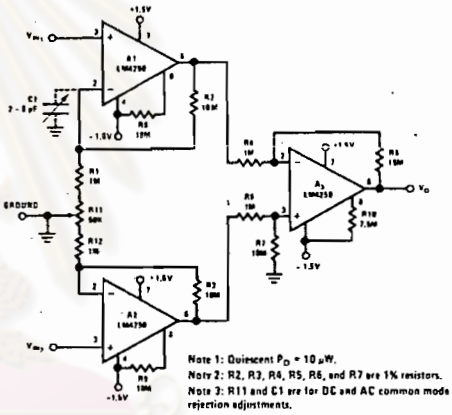
Typical Applications (Continued)



Quiescent P_D = 1.8 μW

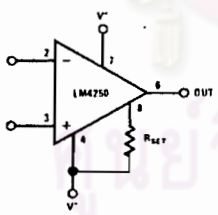
*Meter movement (0 – 100 μA, 2 kΩ) marked for 0 – 100 nA full scale.

Floating Input Meter Amplifier
100 Nano-Ampere Full Scale

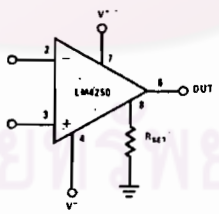


Note 1: Quiescent P_D = 10 μW.
Note 2: R2, R3, R4, R5, R6, and R7 are 1% resistors.
Note 3: R11 and C1 are for DC and AC common mode rejection adjustments.

X100 Instrumentation Amplifier 10 μW



R_{SET} Connected to V⁻

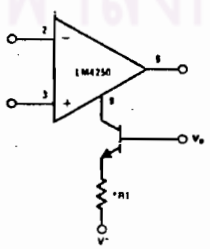


R_{SET} Connected to Ground

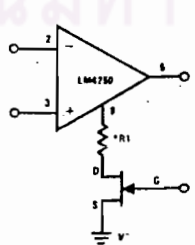
I_{SET} EQUATIONS:

$I_{SET} \approx \frac{V^+ + |V^-| - 0.5}{R_{SET}}$ where R_{SET} is connected to V⁻.

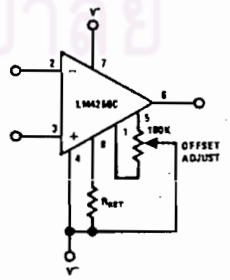
$I_{SET} \approx \frac{V^+ - 0.5}{R_{SET}}$ where R_{SET} is connected to ground.



Transistor Current Source Biasing



FET Current Source Biasing



Offset Null Circuit

*R1 limits I_{SET} maximum

ภาคผนวก ค

คุณสมบัติของ IC เบอร์ ICL7116CPL

INTERSIL

ICL7116/ICL7117
3½ Digit Single Chip A/D Converter with Display Hold

FEATURES

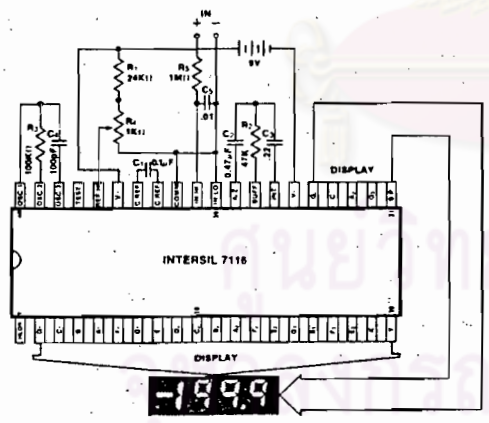
- **HOLD Reading Input allows indefinite display hold**
- **Guaranteed zero reading for 0 volts input on all scales.**
- **True polarity at zero for precise null detection.**
- **1 pA input current typical.**
- **True differential input and reference.**
- **Direct display drive - no external components required. — LCD ICL7116**
  — LED ICL7117
- **Low noise - less than 15 μV pk-pk typical.**
- **On-chip clock and reference.**
- **Low power dissipation - typically less than 10mW.**
- **No additional active circuits required.**

GENERAL DESCRIPTION

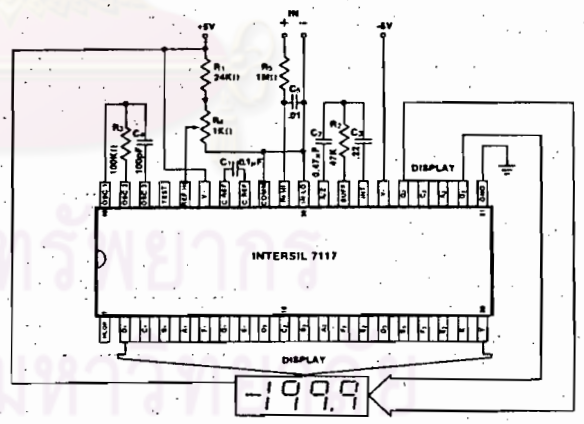
The Intersil ICL7116 and 7117 are high performance, low power 3-1/2 digit A/D converters. All the necessary active devices are contained on a single CMOS I.C., including seven segment decoders, display drivers, reference, and a clock. The 7116 is designed to interface with a liquid crystal display (LCD) and includes a backplane drive; the 7117 will directly drive an instrument-size light emitting diode (LED) display.

The 7116 and 7117 have almost all of the features of the 7106 and 7107 with the addition of a HOLD Reading input. With this input, it is possible to make a measurement and then retain the value on the display indefinitely. To make room for this feature the reference input has been referenced to Common rather than being fully differential. These circuits retain the accuracy, versatility, and true economy of the 7106 and 7107. High accuracy like auto-zero to less than 10μV, zero drift of less than 1μV/°C, input bias current of 10pA maximum, and roll over error of less than one count. The versatility of true differential input is of particular advantage when measuring load cells, strain gauges and other bridge-type transducers. And finally the true economy of single power supply operation (7116), enabling a high performance panel meter to be built with the addition of only seven passive components and a display.

TYPICAL CONNECTION DIAGRAMS



ICL7116 with Liquid Crystal Display

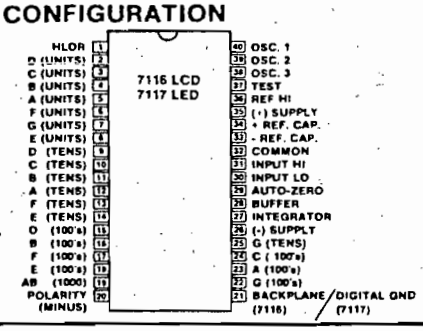


ICL7117 with LED Display

ORDERING INFORMATION

Part	Package	Temp. Range	Order Part #
7116	40 pin ceramic DIP	0°C to +70°C	ICL7116CDL
7116	40 pin plastic DIP	0°C to +70°C	ICL7116CPL
7117	40 pin ceramic DIP	0°C to +70°C	ICL7117CDL
7117	40 pin plastic DIP	0°C to +70°C	ICL7117CPL

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

ICL7116

Supply Voltage (V^+ to V^-) 15V
Analog Input Voltage (either input) (Note 1) ..... V^+ to V^-
Reference Input Voltage (either input) ..... V^+ to V^-
Clock Input ..... Test to V^+
Power Dissipation (Note 2)
Ceramic Package ..... 1000 mW
Plastic Package ..... 800 mW
Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... −65°C to +160°C
Lead Temperature (Soldering, 60 sec) ..... 300°C

ICL7117

Supply Voltage V^+ ..... +6V
V^- ..... −9V
Analog Input Voltage (either input) (Note 1) ..... V^+ to V^-
Reference Input Voltage (either input) ..... V^+ to V^-
Clock Input ..... Gnd to V^+
Power Dissipation (Note 1)
Ceramic Package ..... 1000 mW
Plastic Package ..... 800 mW
Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... −65°C to +160°C
Lead Temperature (Soldering, 60 sec) ..... 300°C

Note 1: Input voltages may exceed the supply voltages provided the input current is limited to ±100μA.

Note 2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

ELECTRICAL CHARACTERISTICS (Note 3)

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Zero Input Reading	Vin = 0.0V Full Scale = 200.0mV	-000.0	±000.0	+000.0	Digital Reading
Ratiometric Reading	Vin = Vref Vref = 100mV	999	999/1000	1000	Digital Reading
Rollover Error (Difference in reading for equal positive and negative reading near Full Scale)	-Vin = +Vin ≈ 200.0mV	−1	±.2	+1	Counts
Linearity (Max. deviation from best straight line fit)	Full scale = 200mV or full scale = 2.000V	−1	±.2	+1	Counts
Common Mode Rejection Ratio (Note 4)	Vcm = ±1V, Vin = 0V, Full Scale = 200.0mV		50		μV/V
Noise (Pk - Pk value not exceeded 95% of time)	Vin = 0V Full Scale = 200.0mV		15		μV
Leakage Current @ Input	Vin = 0V		1	10	pA
Zero Reading Drift	Vin = 0 0° < T_A < 70°C		0.2	1	μV/°C
Scale Factor Temperature Coefficient	Vin = 199.0mV 0 < T_A < 70°C (Ext. Ref. 0 ppm/°C)		1	5	ppm/°C
Supply Current (Does not include LED current for 7117)	Vin = 0		0.8	1.8	mA
Analog Common Voltage (With respect to pos. supply)	25kΩ between Common & pos. Supply	2.4	2.8	3.2	Volts
Temp. Coeff. of Analog Common (with respect to pos. Supply)	25kΩ between Common & pos. Supply		80		ppm/°C
Input Resistance, Pin 1 (Note 6)		30	70		kΩ
V_{IL}, Pin 1 (7116 only)				Test +1.5	Volts
V_{IL}, Pin 1 (7117 only)				GND +1.5	Volts
V_{IH}, Pin 1 (Both)		V^+ −1.5			Volts
7116 ONLY Pk-Pk Segment Drive Voltage (Note 5)	V Supply = 9V	4	5	6	Volts
7116 ONLY Pk-Pk Backplane Drive Voltage (Note 5)	V Supply = 9V	4	5	6	Volts
7117 ONLY Segment Sinking Current (Except Pin 19)	+Supply = 5.0V Segment voltage = 3V	5	8.0		mA
7117 ONLY Segment Sinking Current (Pin 19 only)	+Supply = 5.0V Segment voltage = 3V	10	16		mA

Note 3: Unless otherwise noted, specifications apply to both the 7116 and 7117 at T_A = 25°C, f_{clock} = 48kHz. 7116 is tested in the circuit of Figure 1. 7117 is tested in the circuit of Figure 2.

Note 4: Refer to "Differential Input" discussion on page 4.

Note 5: Back plane drive is in phase with segment drive for 'off' segment, 180° out of phase for 'on' segment. Frequency is 20 times conversion rate. Average DC component is less than 50mV.

Note 6: The 7116 logic input has an internal pull-down resistor connected from HLDR, pin 1, to TEST, pin 37. The 7117 logic input has an internal pull-down resistor connected from HLDR, pin 1 to GROUND, pin 21.

TEST CIRCUITS

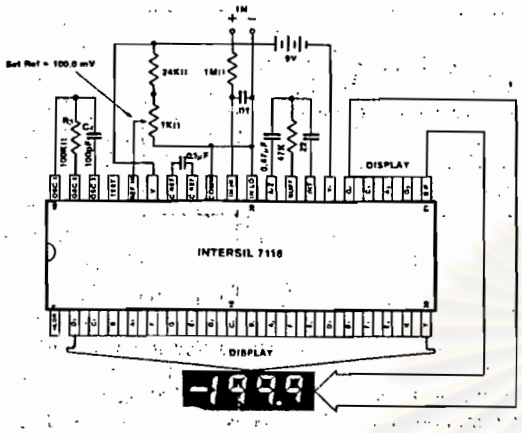


Figure 1: 7116

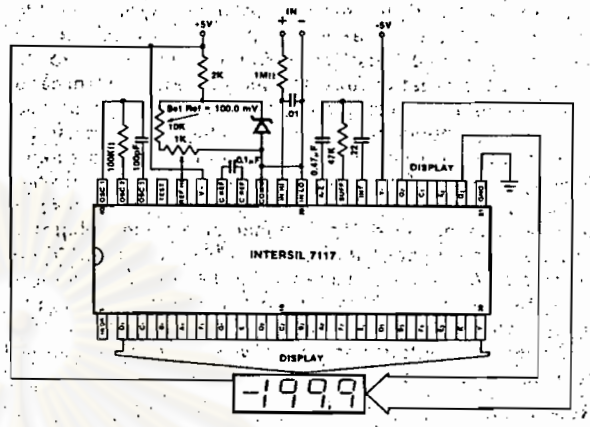


Figure 2: 7117

DETAILED DESCRIPTION

ANALOG SECTION

Figure 3 shows the Block Diagram of the Analog Section for the ICL7116 and 7117. Each measurement cycle is divided into three phases. They are (1) auto-zero (A-Z), (2) signal integrate (INT) and (3) deintegrate (DE).

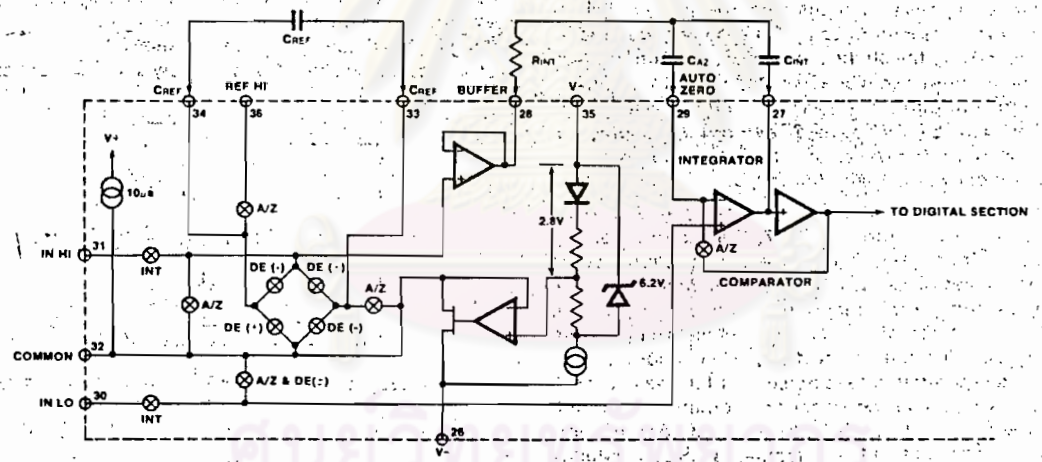


Figure 3: Analog Section of 7116/7117

1. Auto-zero phase

During auto-zero three things happen. First, input high and low are disconnected from the pins and internally shorted to analog common. Second, the reference capacitor is charged to the reference voltage. Third, a feedback loop is closed around the system to charge the auto-zero capacitor C_{AZ} to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the A-Z accuracy is limited only by the noise of the system. In any case, the offset referred to the input is less than 10μV.

2. Signal integrate phase

During signal integrate, the auto-zero loop is opened, the internal short is removed, and the internal input high and low are connected to the external pins. The converter then integrates the differential voltage between input high and input low for a fixed time. This differential voltage can be within a wide common mode range; within one volt of either supply. If, on the other hand, the input signal has no return with respect to the converter power supply, input low can be tied to analog common to establish the correct common-mode voltage. At the end of this phase, the polarity of the integrated signal is determined.

3. De-integrate phase

The final phase is de-integrate, or reference integrate. Input low is internally connected to analog common and input high is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal. Specifically the digital reading displayed is 1000 $(\frac{Vin}{Vref})$.

Differential Input

The input can accept differential voltages anywhere within the common mode range of the input amplifier; or specifically from 0.5 volts below the positive supply to 1.0 volt above the negative supply. In this range the system has a CMRR of 86 dB typical. However, since the integrator also swings with the common mode voltage, care must be exercised to assure the integrator output does not saturate. A worse case condition would be a large positive common-mode voltage with a near full-scale negative differential input voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common mode voltage. For these critical applications the integrator swing can be reduced to less than the recommended 2V full scale swing with little loss of accuracy. The integrator output can swing within 0.3 volts of either supply without loss of linearity.

Reference

The reference input must be generated as a positive voltage with respect to Common.

Analog Common

This pin is included primarily to set the common mode voltage for battery operation (7116) or for any system where the input signals are floating with respect to the power supply. The common pin sets a voltage that is approximately 2.8 volts more negative than the positive supply. This is selected to give a minimum end-of-life battery voltage of about 6V. However, the analog common has some of the attributes of a reference voltage. When the total supply voltage is large enough to cause the zener to regulate (>7V), the common voltage will have a low voltage coefficient (.001%/%), low output impedance (≈15Ω), and a temperature coefficient typically less than 80ppm/°C.

The limitations of the on-chip reference should also be recognized, however. With the 7117, the internal heating which results from the LED drivers can cause some degradation in performance. Due to their higher thermal resistance, plastic parts are poorer in this respect than ceramic. The combination of reference Temperature Coefficient (TC), internal chip dissipation, and package thermal resistance can increase noise near full scale from 25 μV to 80 μVpk-pk. Also the linearity in going from a high dissipation count such as 1000 (20 segments on) to a low dissipation count such as 1111 (8 segments on) can suffer by a count or more. Devices with a positive TC reference may require several counts to pull out of an overload condition. This is because overload is a low dissipation mode, with the three least significant digits blanked. Similarly, units with a negative TC may cycle between overload and a non-overload count as the die alternately heats and cools. All these problems are of course eliminated if an external reference is used.

The 7116, with its negligible dissipation, suffers from none of these problems. In either case, an external reference can easily be added, as shown in Fig. 4.

Analog common is also the voltage the input returns to during auto-zero and de-integrate. If signal low is different from analog common, a common mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. However, in some applications input low will be set at a fixed known voltage (power supply common for instance). In this application, analog common should be tied to the same point, thus removing the common mode voltage from the converter.

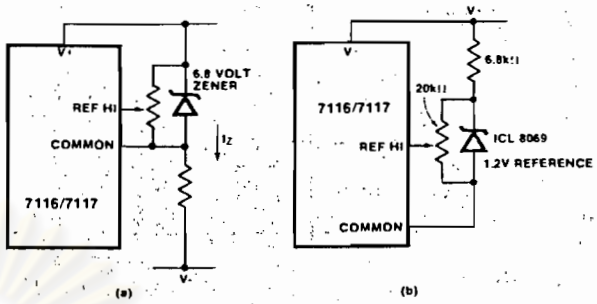


Figure 4: Using an External Reference

Within the IC, analog common is tied to an N channel FET that can sink 30mA or more of current to hold the voltage 2.8 volts below the positive supply (when a load is trying to pull the common line positive). However, there is only 10μA of source current, so common may easily be tied to a more negative voltage thus over-riding the internal reference.

Test

The test pin serves two functions. On the 7116 it is coupled to the internally generated digital supply through a 500Ω resistor. Thus it can be used as the negative supply for externally generated segment drivers such as decimal points or any other presentation the user may want to include on the LCD display. Figures 5 and 6 show such an application.

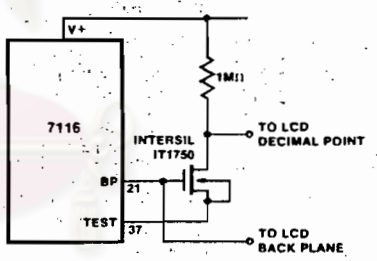


Figure 5: Simple Inverter for Fixed Decimal Point

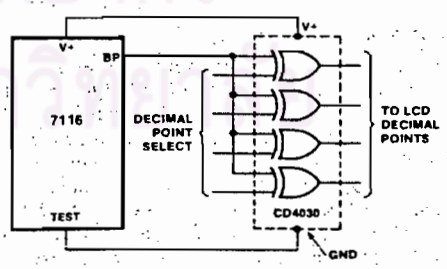


Figure 6: Exclusive 'OR' Gate for Decimal Point Drive

The second function is a "lamp test". When Test is pulled high (to + supply) all segments will be turned on and the display should read - 1888. Caution: on the 7116, in the lamp test mode, the segments have a constant d-c voltage (no square-wave) and will burn the LCD display if left in this mode for several minutes.

DIGITAL SECTION

Figures 7 and 8 show the digital section for the 7116 and 7117, respectively. In the 7116, an internal digital ground is generated from a 6 volt Zener diode and a large P channel source follower. This supply is made stiff to absorb the relative large capacitive currents when the back plane (BP) voltage is switched. The BP frequency is the clock frequency divided by 800. For three readings/second this is a 60 Hz square wave with a nominal amplitude of 5 volts. The segments are driven at the same frequency and amplitude and are in phase with BP when OFF, but out of phase when ON. In all cases neglible d-c voltage exists across the segments.

Figure 8 is the Digital Section of the 7117. It is identical except the regulated supply and back plane drive have been eliminated and the segment drive has been increased from 2 to 8 mA, typical for instrument size common anode LED displays. Since the 1000 output (pin 19) must sink current from two LED segments, it has twice the drive capability or 16 mA.

HOLD Reading Input

The HLDR input will prevent the latch from being updated when this input is at a logic "HI". The chip will continue to make A/D conversions, however, the results will not be updated to the internal latches until this input goes low. This input can be left open or connected to TEST (7116) or GROUND (7117) to continuously update the display. This input has been implemented as a CMOS compatible input with a 70K typical resistance to either TEST (7116) or GROUND (7117).

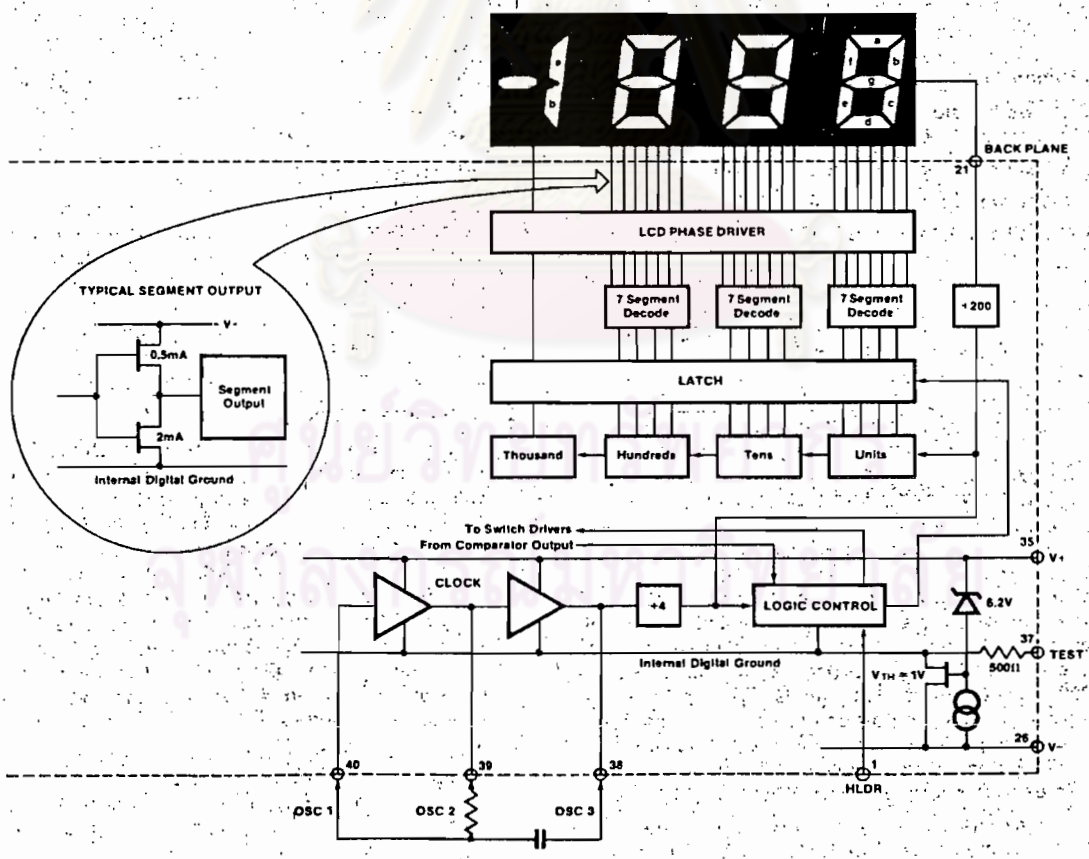


Figure 7: Digital Section 7116

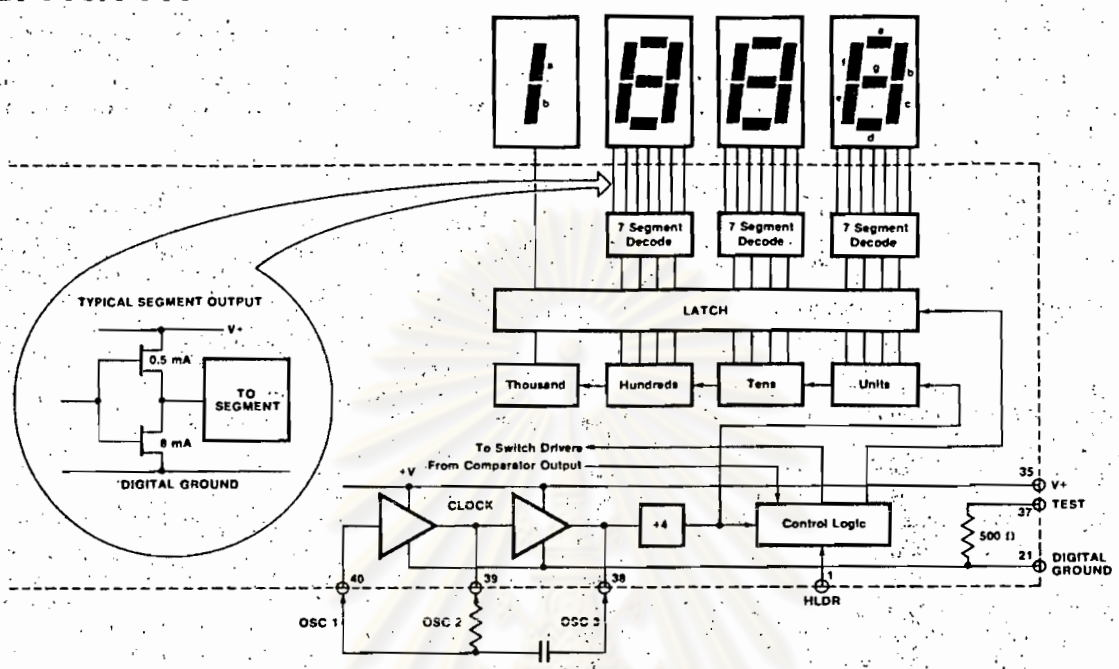


Figure 8: Digital Section 7117

System Timing

Figure 9 shows the clocking arrangement used in the 7116 and 7117. Three basic clocking arrangements can be used:

1. An external oscillator connected to pin 40.
2. A crystal between pins 39 and 40.
3. An R-C oscillator using all three pins.

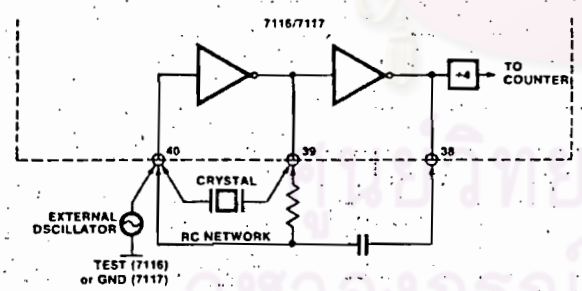


Figure 9: Clock Circuits

The oscillator frequency is divided by four before it clocks the decade counters. It is then further divided to form the three convert-cycle phases. These are signal integrate (1000 counts), reference de-integrate (0 to 2000 counts) and auto-zero (1000 to 3000 counts). For signals less than full scale, auto-zero gets the unused portion of reference deintegrate. This makes a complete measure cycle of 4,000 (16,000 clock pulses) independent of input voltage. For three readings/second, an oscillator frequency of 48kHz would be used.

To achieve maximum rejection of 60 Hz pickup, the signal integrate cycle should be a multiple of 60 Hz. Oscillator frequencies of 240kHz, 120kHz, 80kHz, 60kHz, 48kHz, 40kHz, 33 ⅓ kHz, etc. should be selected. For 50Hz rejection, Oscillator frequencies of 200kHz, 100kHz, 66 ⅔ kHz, 50kHz, 40kHz, etc. would be suitable. Note that 40kHz (2.5 readings/second) will reject both 50 and 60 Hz (also 400 and 440 Hz).

COMPONENT VALUE SELECTION

1. Integrating Resistor

Both the buffer amplifier and the integrator have a class A output stage with 100μA of quiescent current. They can supply 20μA of drive current with negligible non-linearity. The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small enough that undue leakage requirements are not placed on the PC board. For 2 volt full scale, 470kΩ is near optimum and similarly a 47kΩ for a 200.0 mV scale.

2. Integrating Capacitor

The integrating capacitor should be selected to give the maximum voltage swing that ensures tolerance build-up will not saturate the integrator swing (approx. 0.3 volt from either supply). In the 7116 or the 7117, when the analog common is used as a reference, a nominal ±2 volt full scale integrator swing is fine. For the 7117 with ±5 volt supplies and analog common tied to supply ground, a ±3.5 to ±4 volt swing is nominal. For three readings/second (48kHz clock), nominal values for C_{int} are .22 and .10μF, respectively. Of course, if different oscillator frequencies are used, these values should be changed in inverse proportion to maintain the same output swing.

An additional requirement of the integrating capacitor is it have low dielectric absorption to prevent roll-over errors. While other types of capacitors are adequate for this application, polypropylene capacitors give undetectable errors at reasonable cost.

3. Auto-Zero Capacitor

The size of the auto-zero capacitor has some influence on the noise of the system. For 200 mV full scale where noise

is very important, a 0.47μF capacitor is recommended. On the 2 volt scale, a 0.047μF capacitor increases the speed of recovery from overload and is adequate for noise on this scale.

4. Reference Capacitor

A 0.1μF capacitor gives good results in most applications. If rollover errors occur a larger value, up to 1.0μF may be required.

5. Oscillator Components

For all ranges of frequency a 100kΩ resistor is recommended and the capacitor is selected from the equation $f = \frac{45}{RC}$. For 48kHz clock (3 readings/second), C = 100pF.

6. Reference Voltage

The analog input required to generate full-scale output (2000 counts) is: Vin = .2Vref. Thus, for the 200.0 mV and 2.000 volt scale, Vref should equal 100.0 mV and 1.000 volt, respectively. However, in many applications where the A/D is connected to a transducer, there will exist a scale factor other than unity between the input voltage and the digital reading. For instance, in a weighing system, the designer might like to have a full scale reading when the voltage from the transducer is 0.682V. Instead of dividing the input down to 200.0 mV, the designer should use the input voltage directly and select Vref = .341V. Suitable values for integrating resistor and capacitor would be 120kΩ and .22μF. This makes the system slightly quieter and also avoids a divider network on the input. The 7117 with ±5 volts supplies can accept input signals up to ±4 volts. Another advantage of this system occurs when a digital reading of zero is desired for Vin ≠ 0. Temperature and weighing systems with a variable tare are examples. This offset reading can be conveniently generated by connecting the voltage transducer between analog high and common and the variable (or fixed) offset voltage between common and analog low.

7. 7117 Power Supplies

The 7117 is designed to work from ±5 volt supplies. However, if a negative supply is not available, it can be generated from the clock output with 2 diodes, 2 capacitors, and an inexpensive I.C. Figure 10 shows this application.

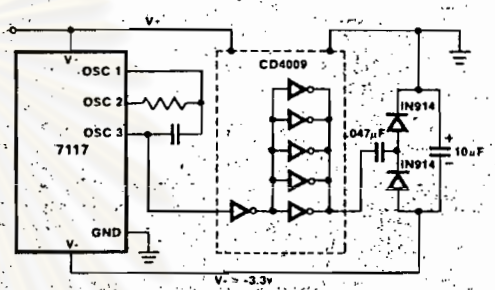


Figure 10: Generating Negative Supply from +5v

In fact, in selected applications no negative supply is required. The conditions to use a single +5V supply are:

1. The input signal can be referenced to the center of the common mode range of the converter.
2. The signal is less than ±1.5 volts.
3. An external reference is used.

4

TYPICAL APPLICATIONS

The 7116 and 7117 may be used in a wide variety of configurations. The circuits which follow show some of the possibilities, and serve to illustrate the exceptional versatility of these A/D converters.

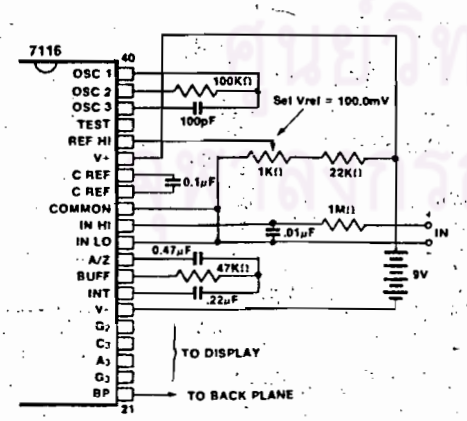


Figure 11: 7116 using the internal reference. Values shown are for 200.0 mV full scale, 3 readings per second, floating supply voltage (9V battery).

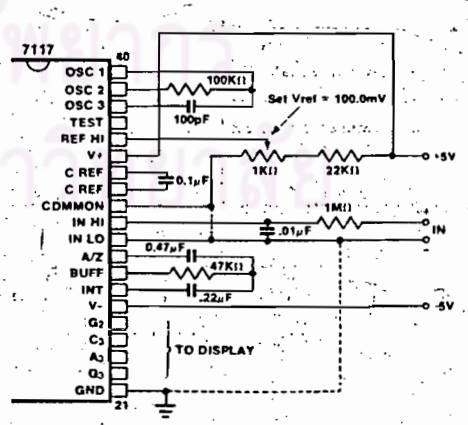


Figure 12: 7117 using the internal reference. Values shown are for 200.0 mV full scale, 3 readings per second. IN LO may be tied to either COMMON for inputs floating with respect to supplies, or GND for single ended inputs. (See discussion under Analog Common on page 4).

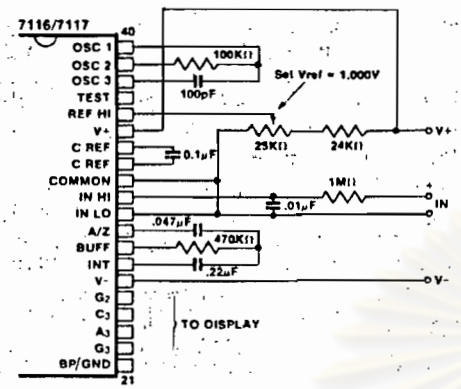


Figure 13: 7116/7117: Recommended component values for 2.000V full scale.

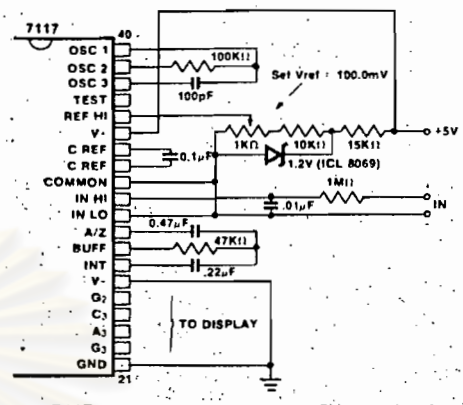


Figure 14: 7117 operated from single +5V supply. An external reference must be used in this application, since the voltage between V+ and V- is insufficient for correct operation of the internal reference.

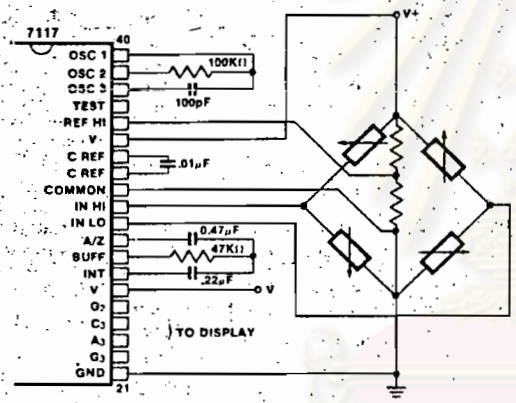


Figure 15: 7117 measuring ratiometric values of Quad Load Cell. The resistor values within the bridge are determined by the desired sensitivity.

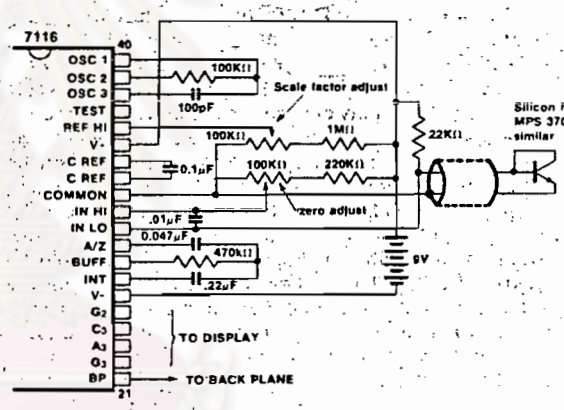
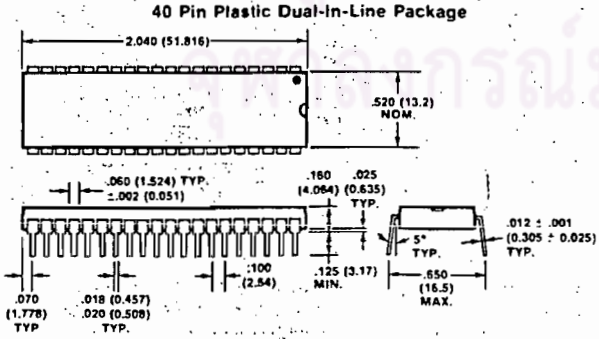


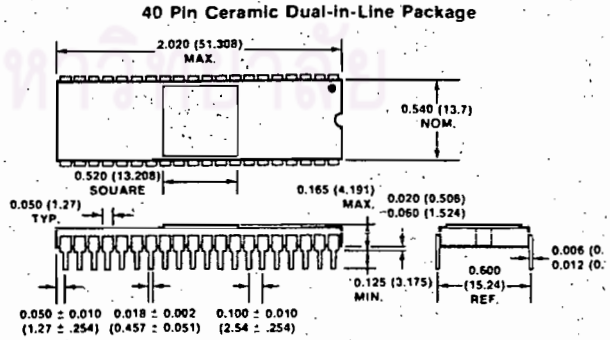
Figure 16: 7116 used as a digital centigrade thermometer. A silicon diode-connected transistor has a temperature coefficient of about -2mV/°C. Calibration is achieved by placing the sensing transistor in ice water and adjusting the zeroing potentiometer for a 000.0 reading. The sensor should then be placed in boiling water and the scale-factor potentiometer adjusted for 100.0 reading.

PACKAGE DIMENSIONS

40 Pin Plastic Dual-In-Line Package



40 Pin Ceramic Dual-In-Line Package



ประวัติ

นางสาวนวลรัตน์ สีกุหลาบ เกิดเมื่อวันที่ 2 ธันวาคม 2496 ที่ตำบลลุมพินี เขตปทุมวัน กรุงเทพมหานคร สำเร็จการศึกษาขั้นปริญญาวิทยาศาสตรบัณฑิต สาขาฟิสิกส์ จากคณะวิทยาศาสตร์ จุฬาลงกรณ์มหาวิทยาลัย เมื่อปีการศึกษา 2518 เข้าทำงานในสถาบันส่งเสริมการสอนวิทยาศาสตร์และเทคโนโลยี ให้ลาศึกษาต่อในชั้นปริญญาวิทยาศาสตร์มหาบัณฑิต ณ แผนกวิชาฟิสิกส์ จุฬาลงกรณ์มหาวิทยาลัย เมื่อปีการศึกษา 2522