## Chapter 6

## Description of DSP-Based Signal Averager Hardware

Introduction

From block diagram 4-1, a typical signal averager configuration has shown some disadvantages for using in NMR imaging. On arithmetic unit, a fixed hardware is often used to perform the specific algorithm which is also depended on the memory configuration. Thus, the arithmetic unit and the configuration of memory must be concurrently considered in the design. These make signal averagers, that based on fixed hardware, applicable in specific applications. Any changing in specifications means that redesigning the system is mandatory.

In the DSP-based signal averager, a digital signal processor and an appropriate software are used instead of the fixed hardware described above. The discussed limitations are overridden since the operations are concentrated in software. A block diagram of DSP-based signal averager hardware is illustrated in Fig. 6-1.

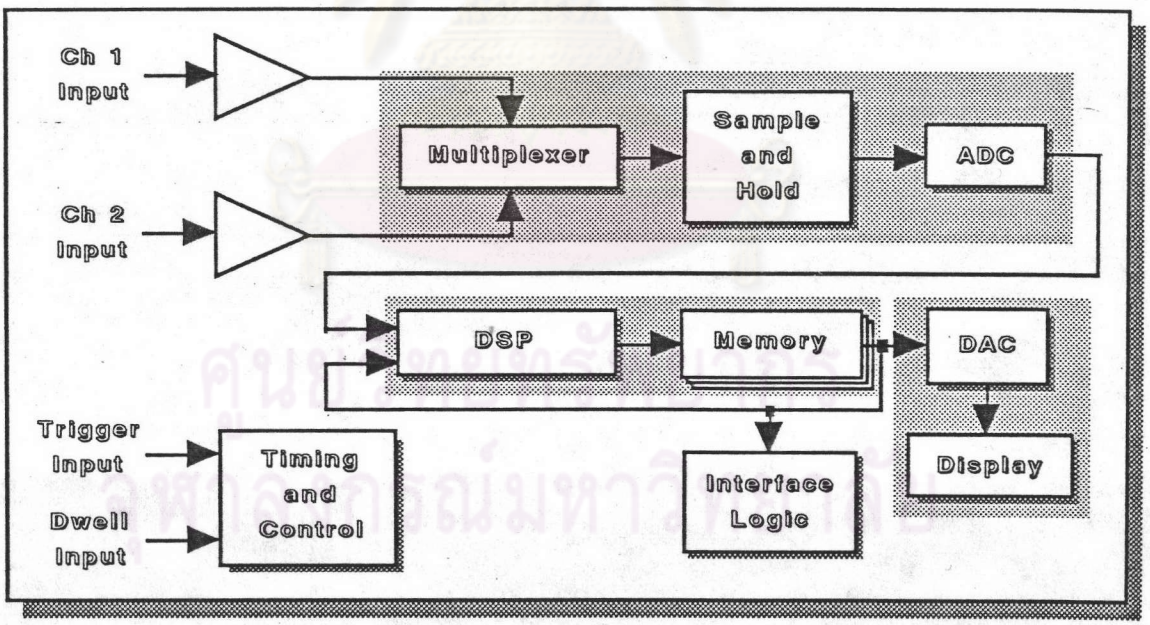


Fig. 6-1 Block diagram of DSP-based signal averager hardware.

The DSP-based signal averager for NMR imaging systems based on TMS32010 has been developed. Averaging computation is implemented through the developed software which described in chapter 7. The structure of memory can be defined to satisfy the specific case. Operating procedures are controlled by a microprocessor. In the following sections, the required specifications are presented. The descriptions of each parts are also demonstrated.

Specifications

1) Signal Input

- 2 channels input with sensitivity, polarity, and offset control.
- Variable-frequency low-pass filter on each input.
- 1 external trigger input with threshold and slope control.
- 1 external dwell time input.

2) Memory

- 2 dimensional definable array structure.
- 2048 words maximum memory length.

3) Signal Processing

- Linear summation averaging algorithm.
- DC offset post processing.

4) System Operational Controls

- Menu-driven style in operating procedures.
- Liquid crystal display and optical encoder for interactive input.
- Simple modifications of control software.

5) System Output Functions

- Oscilloscope interfacing for using as a display unit.
- Computer interfacing logic for processing and recording.

Description of the Hardware Section

The signal averager have been constructed from 5 parts: memory part, MCS32 part, TMS320 part, TMS320 IO part, and analog part. The relation of each parts is shown in Fig 6-2.

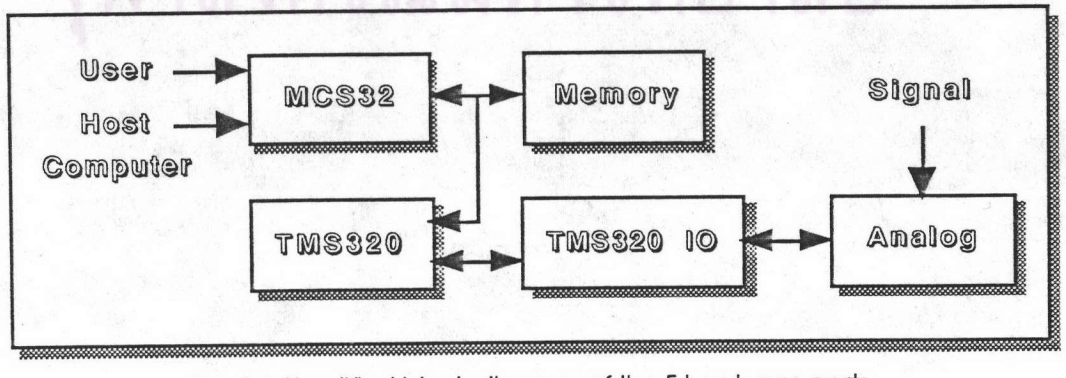


Fig. 6-2 Simplified block diagram of the 5 hardware parts.

1) Memory Part

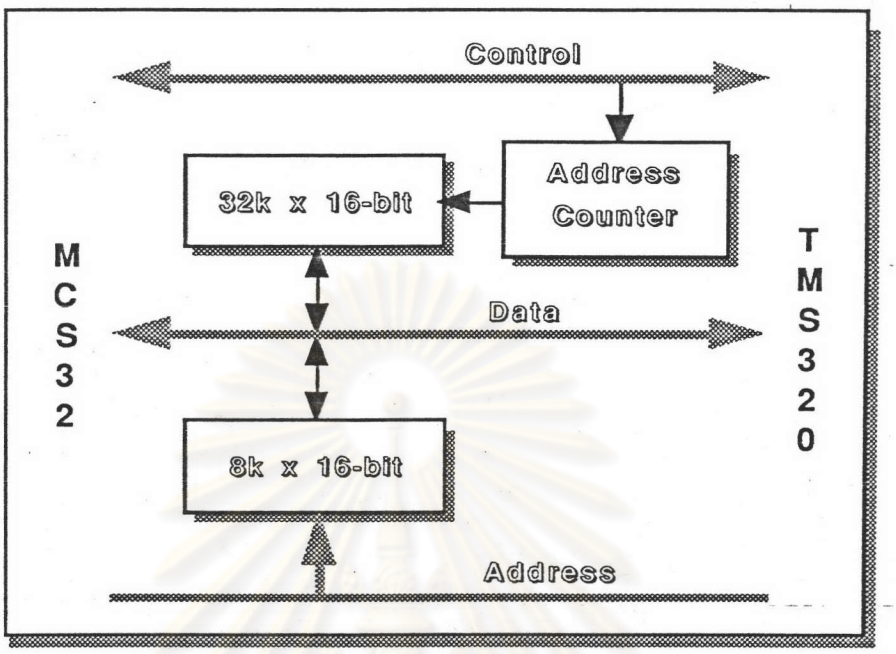


Fig. 6-3 Block diagram of the memory parts.

The memory part is 16-bit width which compose of two separate units: 32k words and 8k words. The first unit is used to store the acquired data which can be defined the structure by the processor. Since a typical read only memory (ROM) is not fast enough for the program memory of TMS32010, the random access memory (RAM) of 8k words is used to store the instructions. The memory part can be accessed individually by MCS32 or TMS320 part.

1.1) TMS320 Program Memory

As mentioned in chapter 5, fast memories with access times of under 100ns are required for the program memory of TMS32010. For the local market, ROMs with access times above 200ns are only available. However, RAMs with the access times of 100 ns and above can be found in general store. Two integrated circuits (IC) of 6264 type which are 8k x 8-bit are used to form the 16-bit program memory. On the power-on sequence, MCS32 part uploads the program from its ROM into this area.

1.2) Data Memory

By the limitation of TMS32010, the capacity of on chip data memory is 144 words which is not enough for performing the task required by NMR imaging. To overcome this problem, external memory extension technique is implemented. Two 62256 RAMs are used to build 32k x 16-bit data memory. A set of external address counters is controlled by making use of data bus and I/O capability of TMS32010. To access the data memory, the desired beginning

address must be presented to the memory part. The further operation of read or write in memory part will increment the address by one.

2) MCS32 Part

The heart of MCS32 part is 8032 microprocessor which is one of the MCS-51 family. The most interesting aspect of this microprocessor is its BASIC interpreter which resided in a separate ROM. This means that a control program can be easily developed by using simple and effective BASIC language. For the MCS32 part, 8032 with a developed BASIC program is used to interface with users and control the operating sequences of other parts.

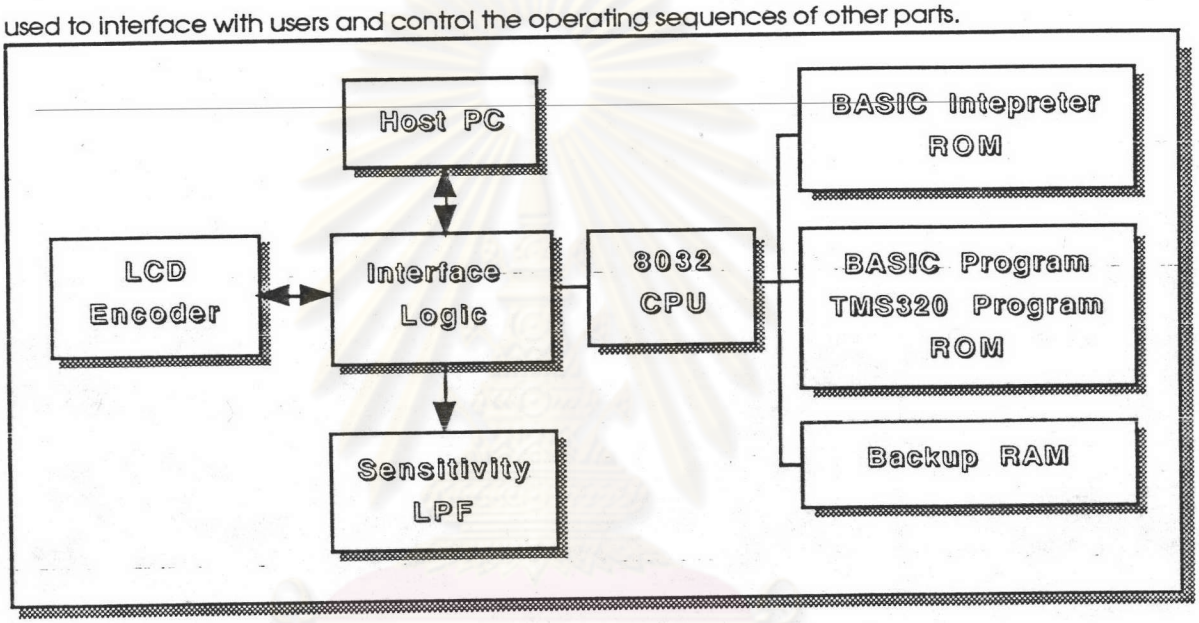


Fig. 6-4 Block diagram of the MCS32 parts.

2.1) 8032 and BASIC Interpreter ROM

8032 microprocessor is one of the MCS-51 family. It is designed primarily for using as an embedded controller. The capability of using BASIC as a development language makes it popular among developers. However, in some applications where execution speed is required, assembly language is an essential. In this application, BASIC is used in menu-driven control program whereas assembly is used in LCD and encoder interfacing program.

2.2) BASIC Program ROM and TMS320 Program ROM

A BASIC program ROM is the memory area that the control program written in BASIC language resides. TMS320 program ROM contains the signal processing program of TMS32010 which transferred to the memory unit in the power-on sequence.

2.3) Backup RAM

Random access memory (RAM) is a kind of volatile memory in which its memory will lost when power down. In some situation where some variables must be often modified and

saved, a battery is used to supply the power for RAM in power down mode. For example, many of setting parameters in this design is saved by using this technique.

2.4) Interface Logic

Interface logic is the unit that makes the connection of microprocessor to the real world possible. For interactive input, a liquid crystal display (LCD) and an optical encoder are used to simplify the operating procedures.

3) TMS320 Part

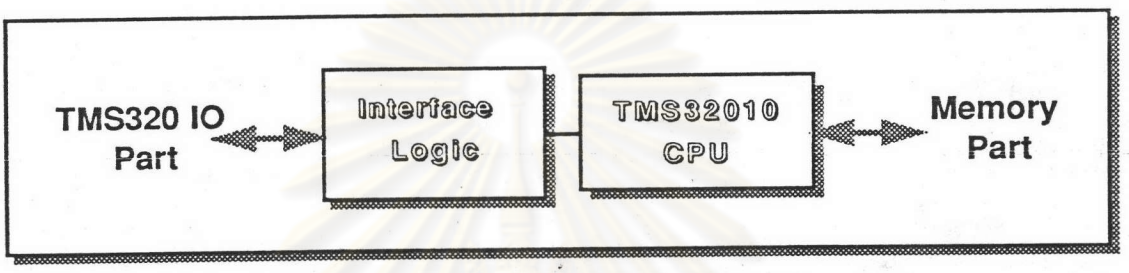


Fig. 6-5 Block diagram of the TMS320 parts.

The averaging process is performed in this part. TMS32010 digital signal processor executes the processing algorithm by the control program written in assembly language. However, the content of program is saved in the MCS32 ROM which transferred to the memory part on power up.

4) TMS320 IO Part

The TMS320 IO part is the input and output buffer between the digital section of TMS320 part and the analog section of analog part.

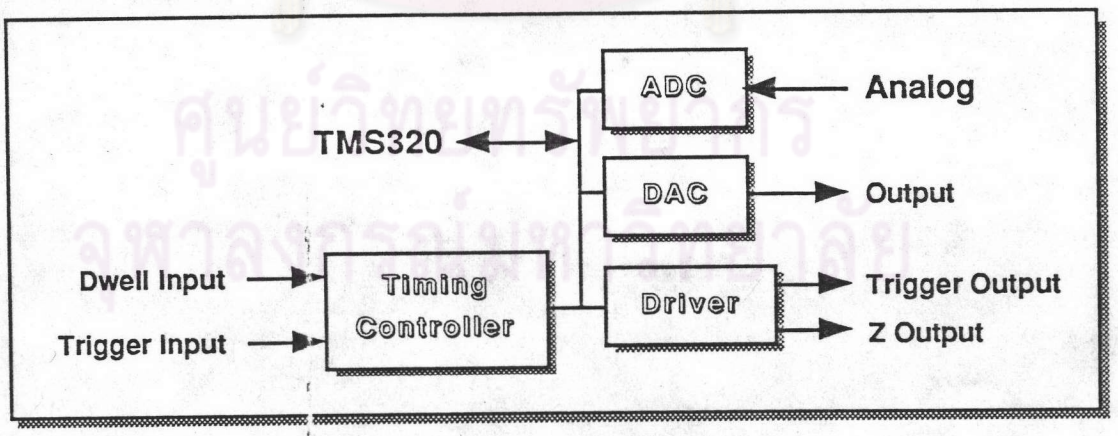


Fig. 6-6 Block diagram of the TMS320 IO parts.

4.1) Analog to Digital Convertor

An ADC is a device that convert analog signal into digital representation. In TMS320 IO part, a flash ADC of CA3318 is used to convert the output signal from the analog part which is in 0 - 5 V. range.

4.2) Digital to Analog Convertor

A DAC is a device that convert digital representation into analog signal. After averaging process of each sample is completed, TMS32010 will sent the result to this DAC whereas its output can be connected to an oscilloscope. Thus, the processed signal can be observed during the averaging process.

4.3) Timing Control

An external trigger signal is applied is this unit to initiate the sequence. The signal is converted in to digital level and transferred to the TMS320 part. An external dwell signal which is in digital level are buffered and sent to the TMS320 part.

5) Analog Part

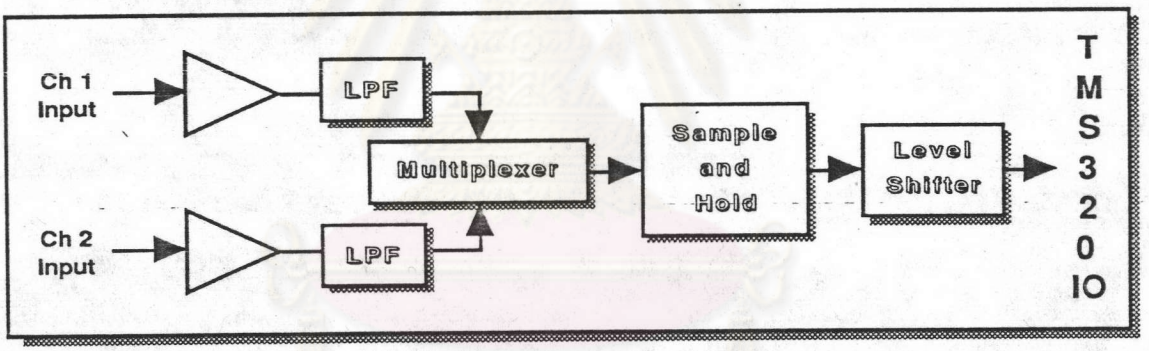


Fig. 6-7 Block diagram of the analog parts.

The analog part consists of 2 channels input which is amplified by the input preamplifiers. The sensitivity of input are selected by the MCS32 part. The amplified signals are sent to the low-pass filter. After selected channel from the multiplexer is held by the sample-and-hold circuit, the level shifter will shift the acquired signal which is bipolar into unipolar form that is appropriate for the ADC input.