

## CHAPTER III

### RESULTS AND DISCUSSIONS

#### Introduction

Data translator has been tested for both analog and digital signals. The range of analog signal is between 0 - 500 Hz at the interval of 50 Hz, and the range of squarewave signal is between 0 - 1,000 Hz at the interval of 100 Hz.

#### Test Procedure

##### 1. In "WRITE" Mode

The input signal is applied by the low-distortion oscillator to the signal input of the data translator, and the output of data translator is connected to the input of the tape recorder for signal storage in the cassette tape. The set-up of equipment is shown in Figure 15.

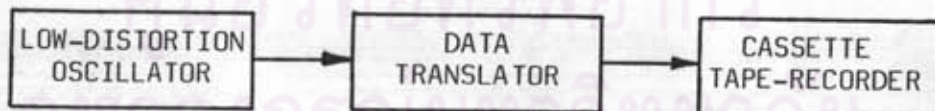


Figure 15 : Equipment set-up in "WRITE" mode

##### 2. In "READ" Mode

The signal from cassette tape recorder is applied to the data input of data translator. The reproduced data from data translation is connected to one input of dual-trace storage oscilloscope in order to compare the magnitude and waveshape with the

original signal from low-distortion oscillator, which is applied to another input of the oscilloscope.

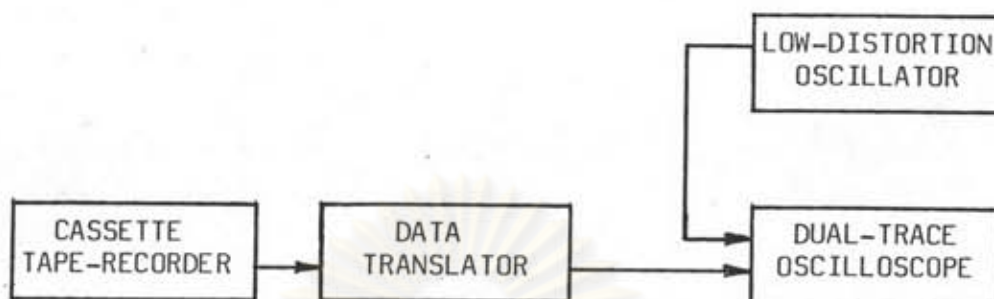


Figure 16 : Equipment set-up in "READ" mode

### 3. Performance Test

The double-pole network is selected to be tested by the data translator. By choosing the value of  $R_1 = R_2 = 5 \text{ k}\Omega$  and  $C_1 = C_2 = 0.2 \mu\text{f}$ , the diagram of network is shown in Figure 17.

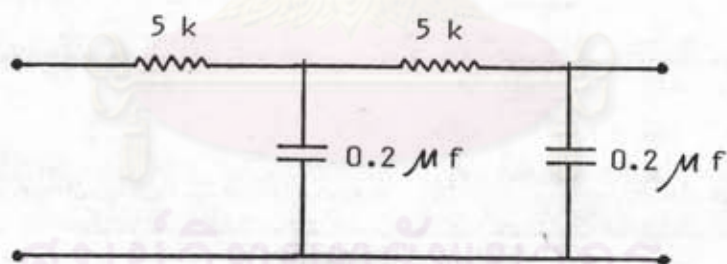


Figure 17 : RC low-pass network

Apply a  $0.775 \text{ V}_{\text{rms}}$  squarewave ranging from  $0 - 300 \text{ Hz}$  at the interval of  $50 \text{ Hz}$  to the input of network and then record the output signal via data translator for a period of time and compare the reproduced signal with the original output signal from the network. The set-up of performance test is shown in Figure 18.

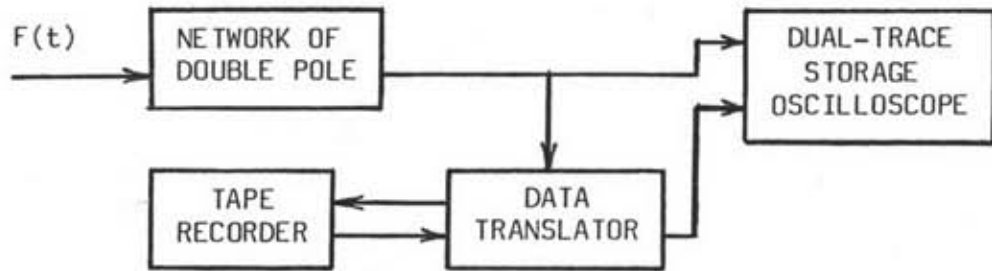


Figure 18 : Equipment set-up for performance test

### Testing Results

#### 1. Results of Analog Test

The testing results of analog signal input is tabulated below.

Table 1 : Gain vs. frequency of analog signal

Frequency (Hz)	Amplitude (V)		Time (msec)	Ao (dB)
	Recording	Reproducing		
5	0.775	0.770	200	-0.056
10	0.775	0.765	100	-0.112
15	0.775	0.765	66.6	-0.112
20	0.775	0.765	50	-0.112
25	0.775	0.765	40	-0.112
30	0.775	0.763	33.3	-0.134
35	0.775	0.763	28.6	-0.134
40	0.775	0.763	25	-0.134
45	0.775	0.760	22.2	-0.168
50	0.775	0.760	20	-0.168
60	0.775	0.760	16.6	-0.168

Table 1 : Gain vs. frequency of analog signal

Frequency (Hz)	Amplitude (V)		Time (msec)	Ao (dB)
	Recording	Reproducing		
50	0.775	0.760	20	-0.168
60	0.775	0.760	16.6	-0.168
80	0.775	0.758	12.5	-0.192
100	0.775	0.752	10	-0.26
150	0.775	0.739	6.6	-0.412
200	0.775	0.734	5	-0.472
250	0.775	0.713	4	-0.724
300	0.775	0.713	3.3	-0.724
350	0.775	0.678	2.8	-1.16
400	0.775	0.642	2.5	-1.634
450	0.775	0.618	2.2	-1.966
500	0.775	0.591	2	-2.354
600	0.775	0.538	1.6	-3.17
800	0.775	0.436	1.2	-4.996
1000	0.775	0.346	1	-7.004

The abovementioned results are plotted in semi-logarithmic graph as shown in Figure 19 and the photographs of the comparison between recorded and reproduced signal for frequency ranging from 0 - 500 Hz at the interval of 100 Hz are shown in Figure 20 to Figure 24.

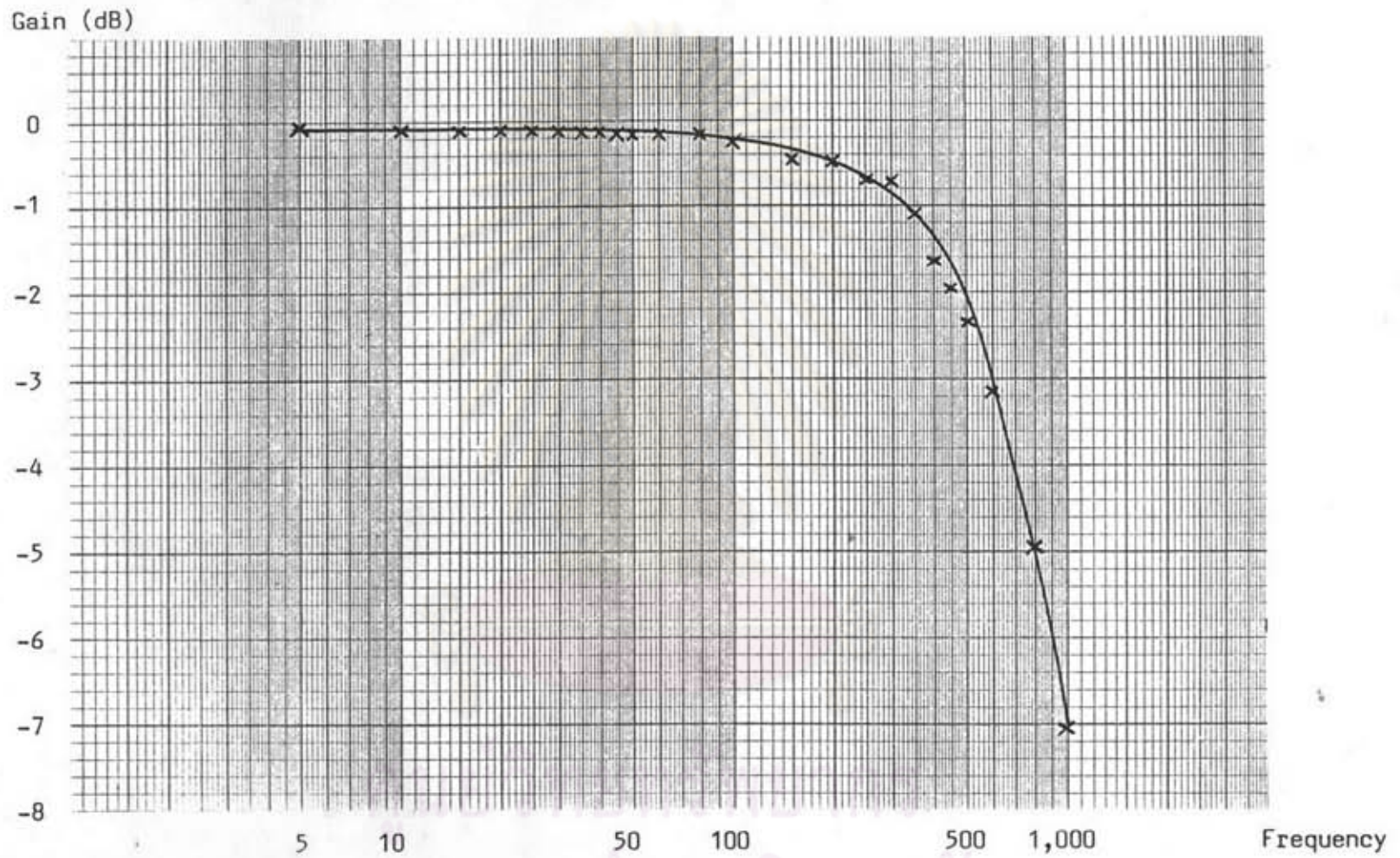
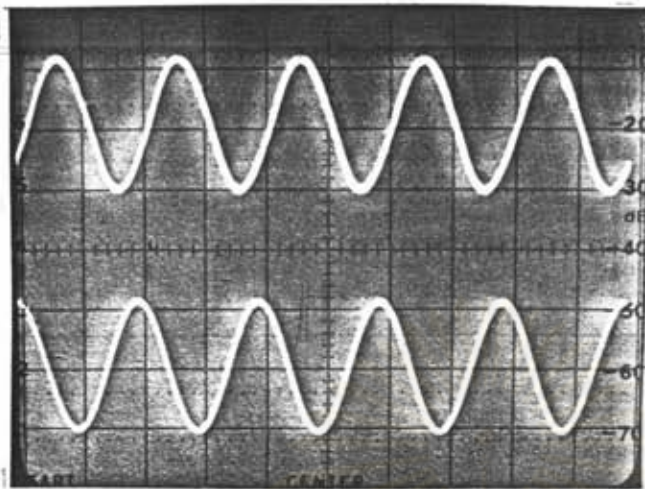


Figure 19 : Frequency response of the data translator



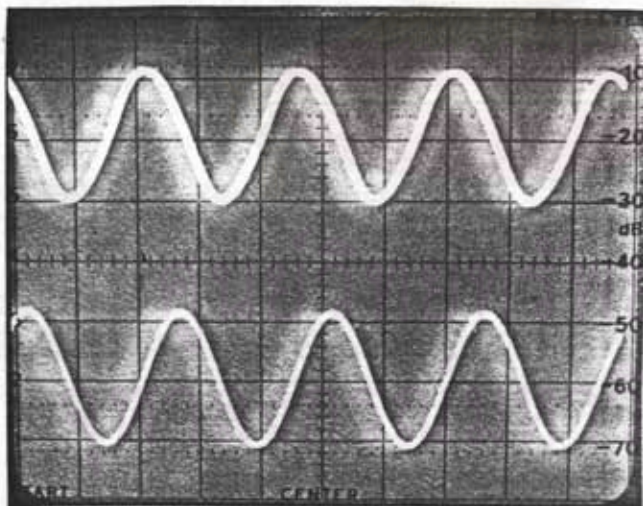
reproduced signal

recorded signal

Figure 20 : Test result of analog signal at 100 Hz

$$V/\text{div} = 1 \text{ V/cm}$$

$$\text{Time/div} = 5 \text{ msec/cm}$$



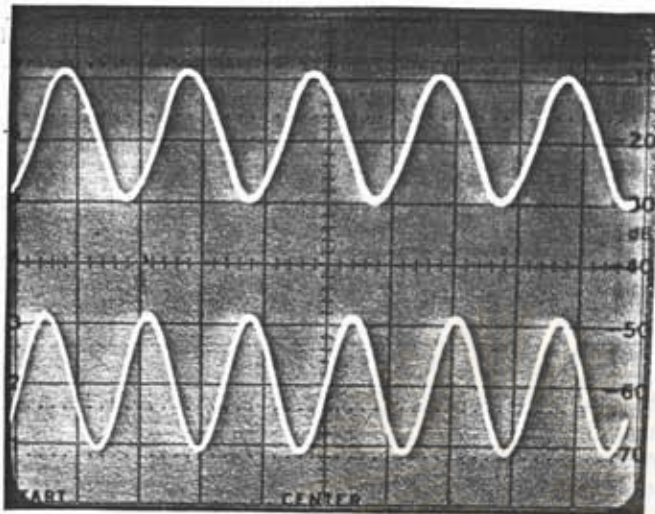
reproduced signal

recorded signal

Figure 21 : Test result of analog signal at 200 Hz

$$V/\text{div} = 1 \text{ V/cm}$$

$$\text{Time/div} = 2 \text{ msec/cm}$$



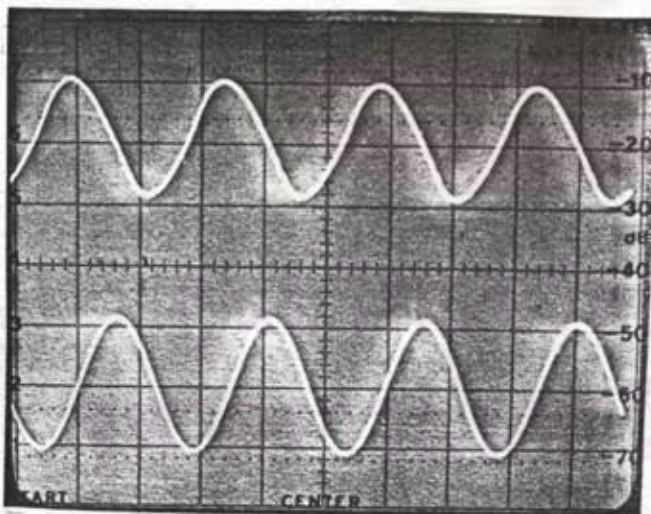
reproduced signal

recorded signal

Figure 22 : Test result of analog signal at 300 Hz

$$V/\text{div} = 1 V/\text{cm}$$

$$\text{Time}/\text{div} = 2 \text{ msec}/\text{cm}$$



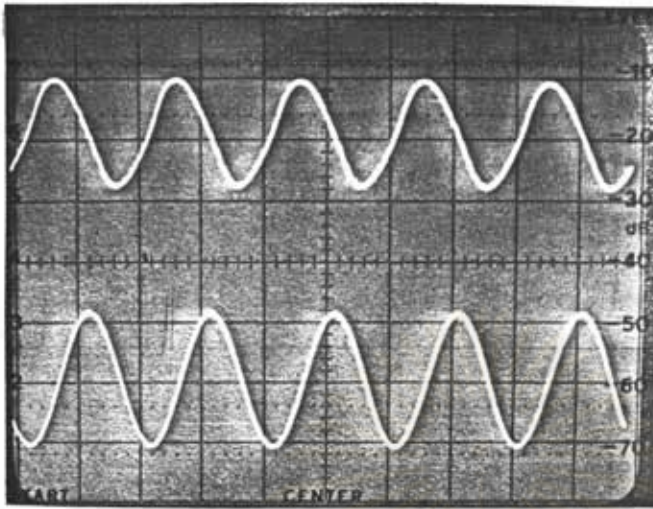
reproduced signal

recorded signal

Figure 23 : Test result of analog signal at 400 Hz

$$V/\text{div} = 1 V/\text{cm}$$

$$\text{Time}/\text{div} = 1 \text{ msec}/\text{cm}$$



reproduced signal

recorded signal

Figure 24 : Test result of analog signal at 500 Hz

$$V/\text{div} = 1 \text{ V/cm}$$

$$\text{Time/div} = 1 \text{ msec/cm}$$



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## 2. Results of Squarewave Test

The testing result of squarewave signal input with TTL interface frequency range from 0 - 2,800 bits/sec at the interval of 400 bits/sec are shown in Figure 25 to Figure 31.

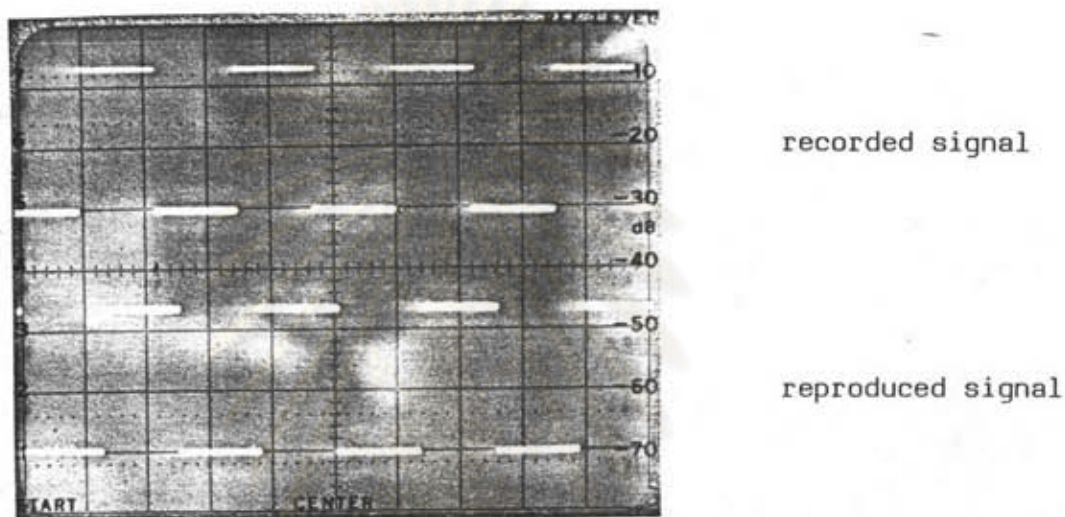


Figure 25 : Test result of digital signal at 400 bits/sec

$$V/\text{div} = 2 \text{ V/cm}$$

$$\text{Time}/\text{div} = 2 \text{ msec/cm}$$

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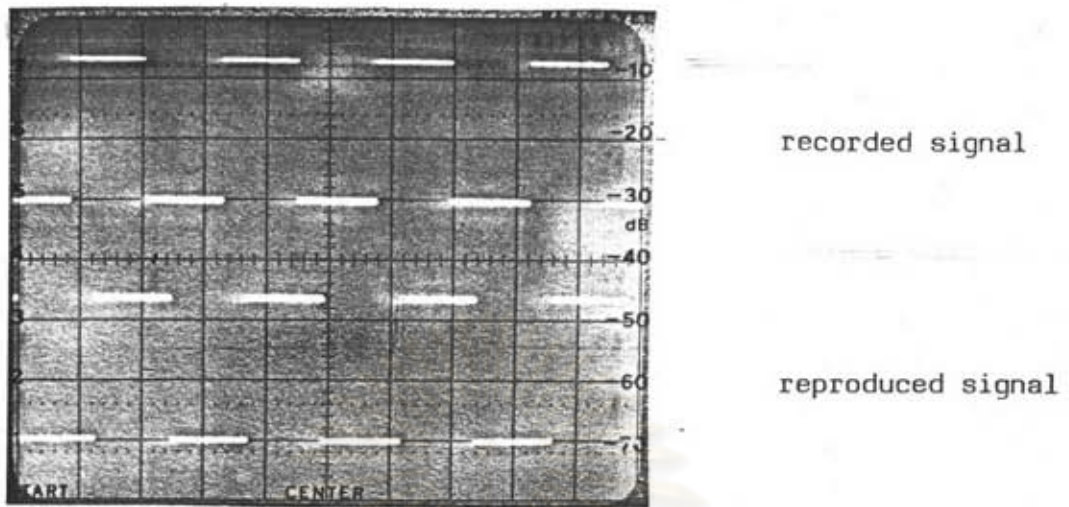


Figure 26 : Test result of digital signal at 800 bits/sec

$$V/\text{div} = 2 V/\text{cm}$$

$$\text{Time}/\text{div} = 1 \text{ msec}/\text{cm}$$

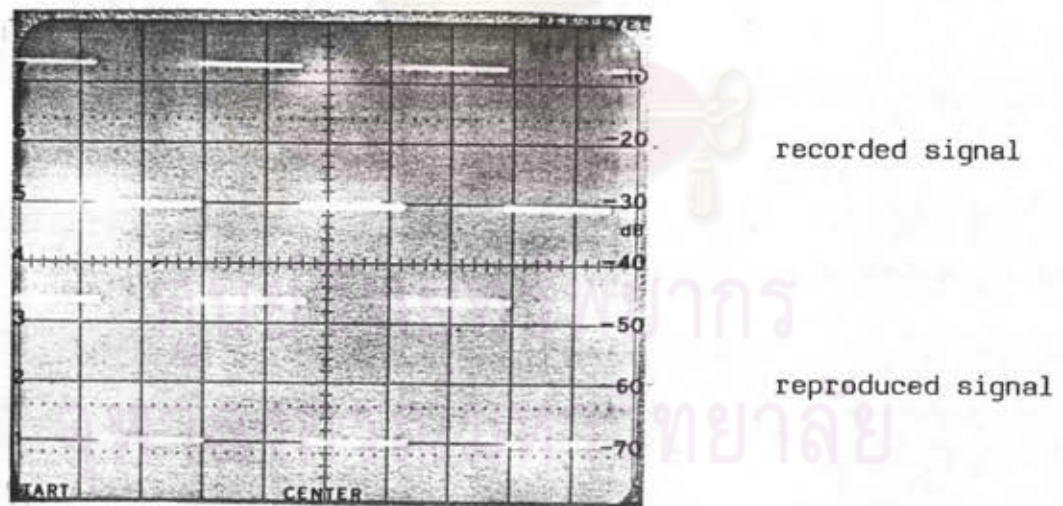
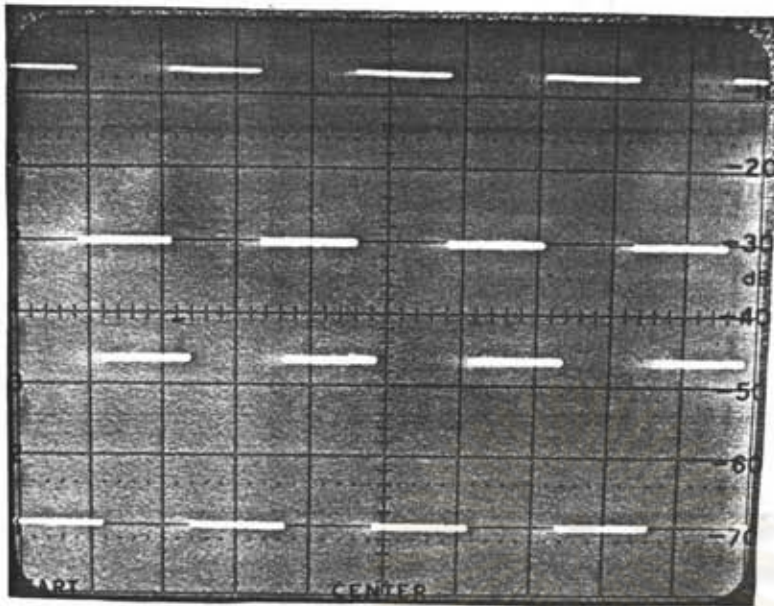


Figure 27 : Test result of digital signal at 1,200 bits/sec

$$V/\text{div} = 2 V/\text{cm}$$

$$\text{Time}/\text{div} = 5 \text{ msec}/\text{cm}$$



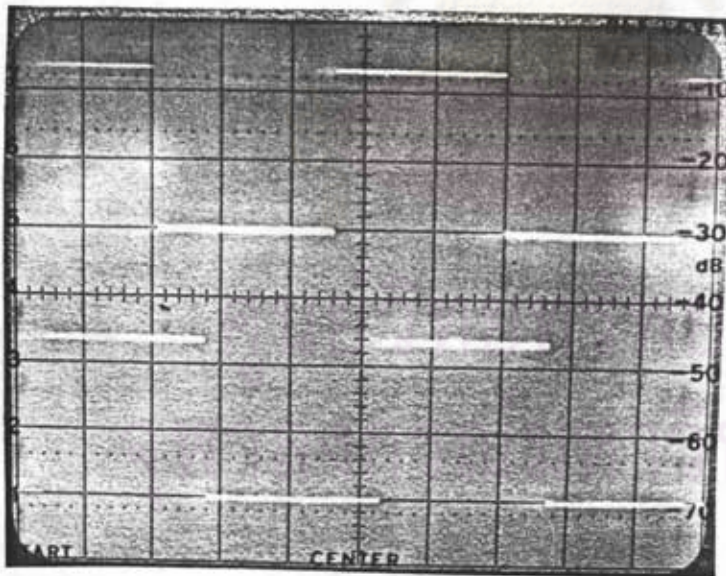
recorded signal

reproduced signal

Figure 28 : Test result of digital signal at 1,600 bits/sec

$$V/\text{div} = 2 V/\text{cm}$$

$$\text{Time}/\text{div} = 5 \text{ msec}/\text{cm}$$



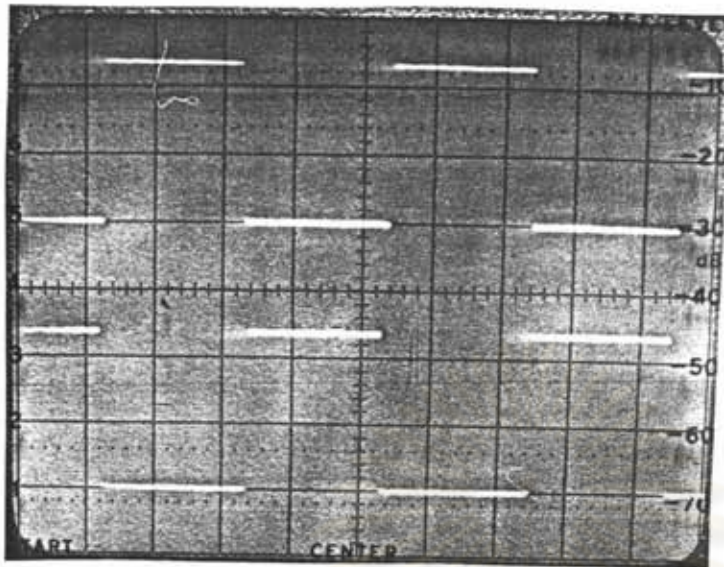
recorded signal

reproduced signal

Figure 29 : Test result of digital signal at 2,000 bits/sec

$$V/\text{div} = 2 V/\text{cm}$$

$$\text{Time}/\text{div} = 2 \text{ msec}/\text{cm}$$



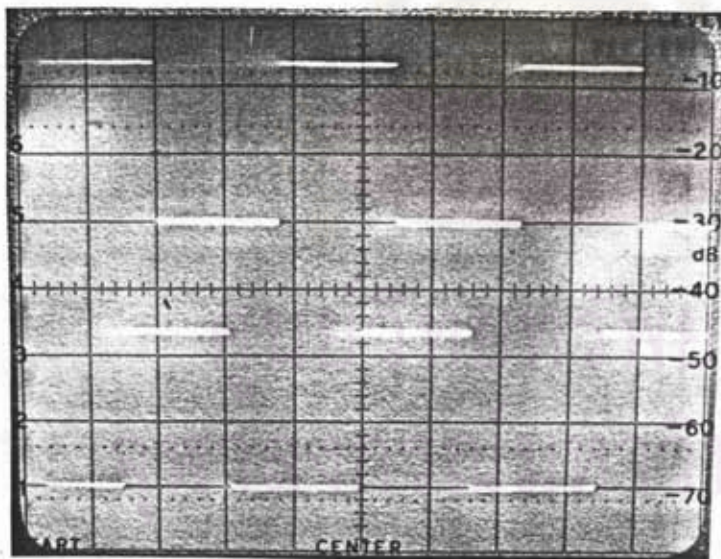
recorded signal

reproduced signal

Figure 30 : Test result of digital signal at 2,400 bits/sec

$$V/\text{div} = 2 \text{ V/cm}$$

$$\text{Time/div} = 2 \text{ msec/cm}$$



recorded signal

reproduced signal

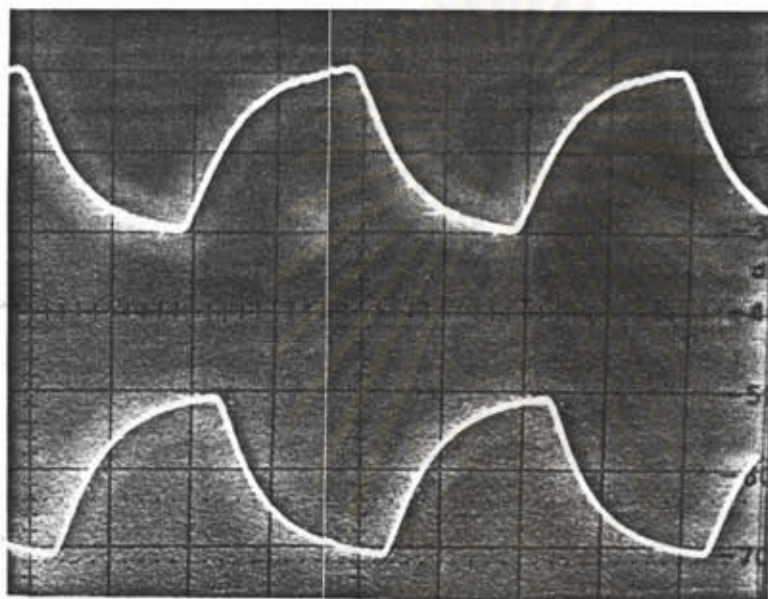
Figure 31 : Test result of digital signal at 2,800 bits/sec

$$V/\text{div} = 2 \text{ V/cm}$$

$$\text{Time/div} = 2 \text{ msec/cm}$$

### 3. Results of Performance Test

The squarewave signal input to the RC network varies from 20 ms to 2 msec and testing results are shown in Figure 32 to Figure 41.



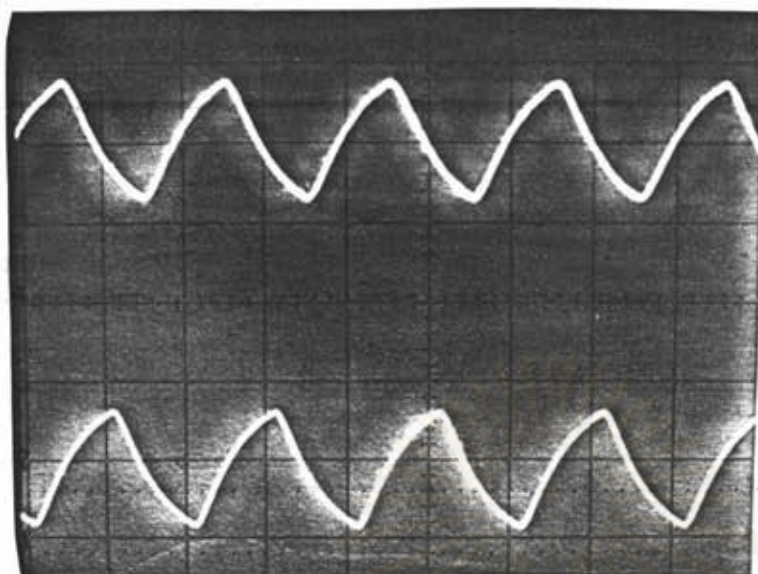
reproduced signal

recorded signal

Figure 32 : Test result of network at a period of 20 msec

$$\begin{aligned} V/\text{div} &= 1 \text{ V/cm} \\ \text{Time}/\text{div} &= 5 \text{ msec/cm} \end{aligned}$$

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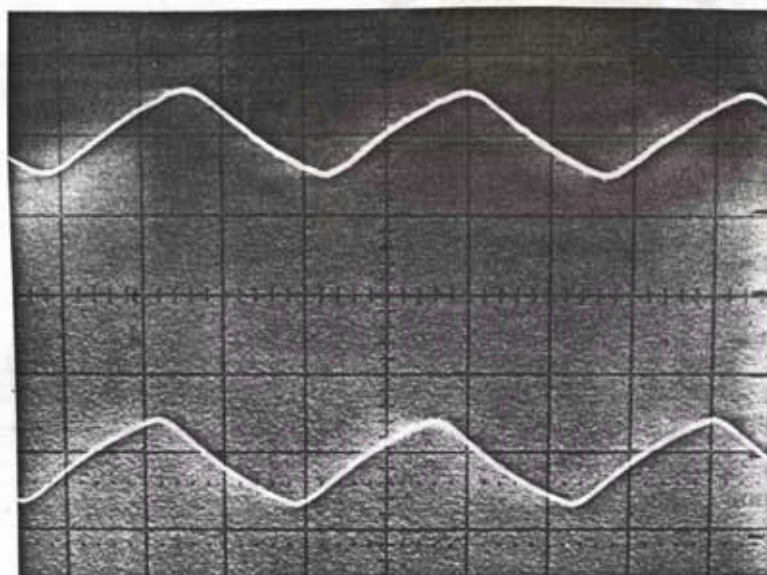
reproduced signal

recorded signal

Figure 33 : Test result of network at a period of 10 msec

$$V/\text{div} = 1 \text{ V/cm}$$

$$\text{Time/div} = 5 \text{ msec/cm}$$



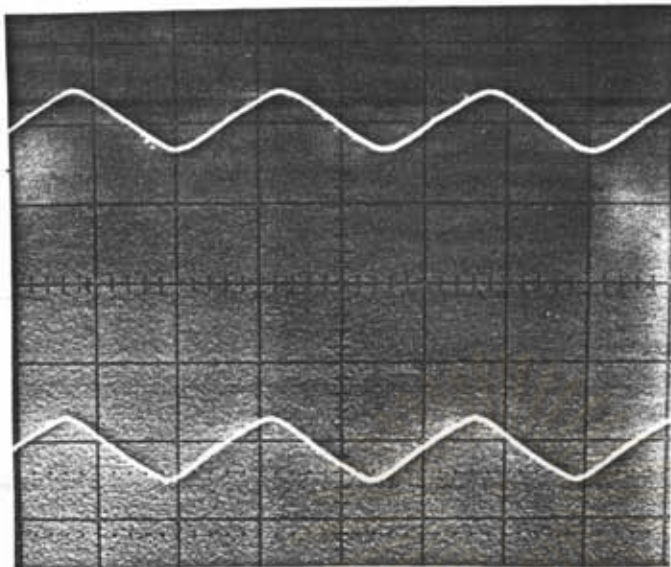
reproduced signal

recorded signal

Figure 34 : Test result of network at a period of 6.6 msec

$$V/\text{div} = 1 \text{ V/cm}$$

$$\text{Time/div} = 2 \text{ msec/cm}$$



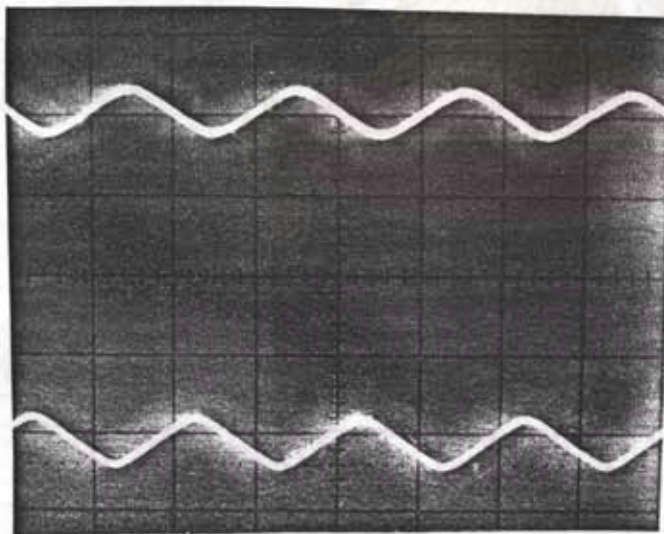
reproduced signal

recorded signal

Figure 35 : Test result of network at a period of 5 msec

$$V/\text{div} = 1 \text{ V/cm}$$

$$\text{Time/div} = 2 \text{ msec/cm}$$



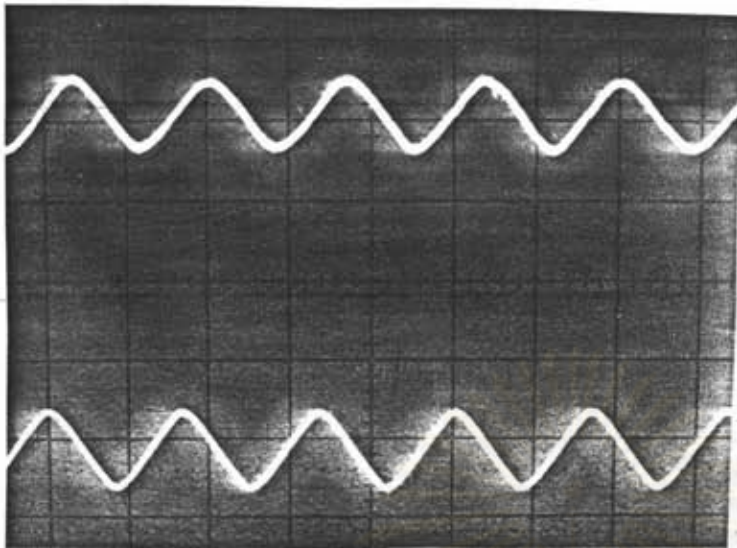
reproduced signal

recorded signal

Figure 36 : Test result of network at a period of 4 msec

$$V/\text{div} = 1 \text{ V/cm}$$

$$\text{Time/div} = 2 \text{ msec/cm}$$



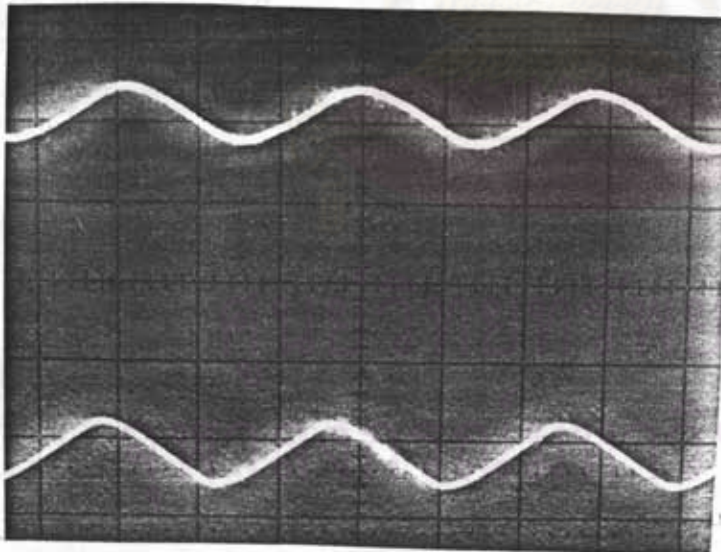
reproduced signal

recorded signal

Figure 37 : Test result of network at a period of 3.3 msec

$$V/\text{div} = .5 \text{ V/cm}$$

$$\text{Time/div} = 2 \text{ msec/cm}$$



reproduced signal

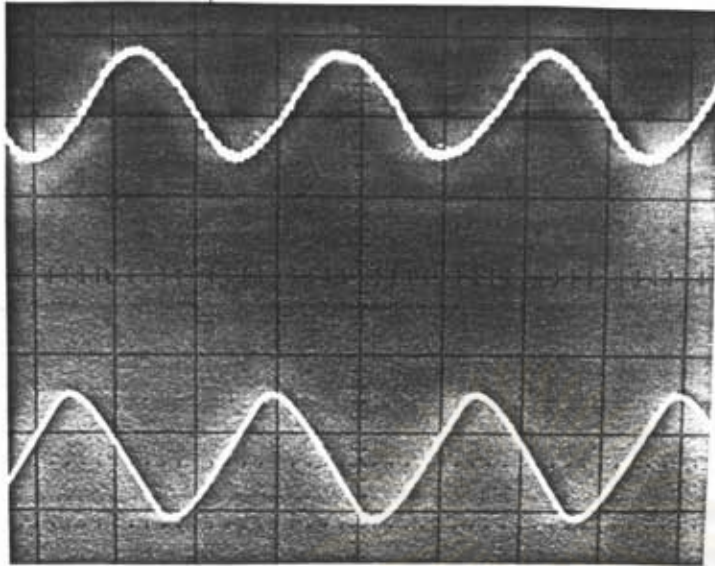
recorded signal

Figure 38 : Test result of network at a period of 2.8 msec

$$V/\text{div} = .5 \text{ V/cm}$$

$$\text{Time/div} = 1 \text{ msec/cm}$$





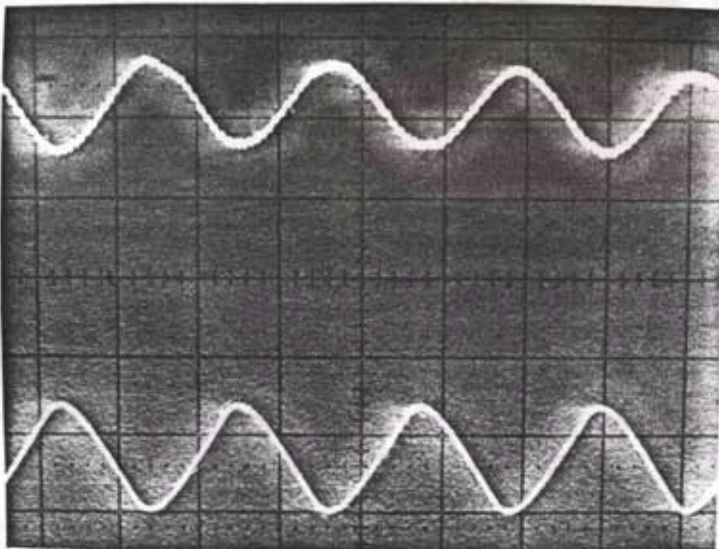
reproduced signal

recorded signal

Figure 39 : Test result of network at a period of 2.5 msec

$$V/\text{div} = 0.2 \text{ V/cm}$$

$$\text{Time/div} = 1 \text{ msec/cm}$$



reproduced signal

recorded signal

Figure 40 : Test result of network at a period of 2.2 msec

$$V/\text{div} = 0.2 \text{ V/cm}$$

$$\text{Time/div} = 1 \text{ msec/cm}$$

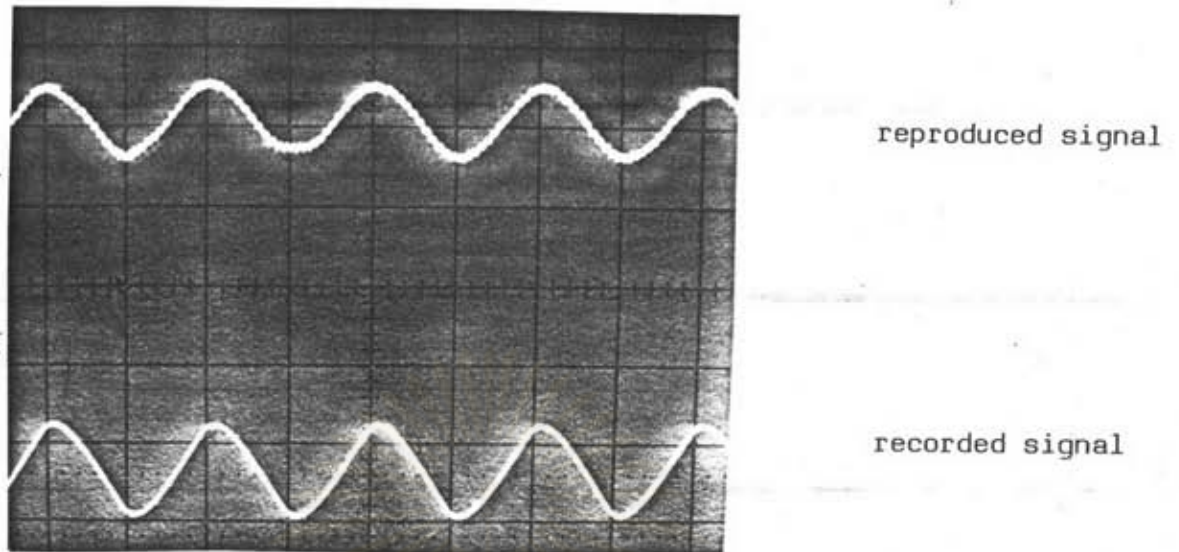


Figure 41 : Test result of network at a period of 2 msec

$$\begin{aligned} V/\text{div} &= .2 V/\text{cm} \\ \text{Time}/\text{div} &= 1 \text{ msec}/\text{cm} \end{aligned}$$

### Discussion

From Figure 19 it is shown that frequency response for analog data input of the data translator is flat for frequency ranging from 0 - 300 Hz which is quite satisfactory from the design point of view. However, for squarewave input with TTL interface, the reproduced signal is remarkable upto 2,800 bits/sec. This is because of the wide range of acceptability of logical TTL input. But for digital data input higher than 2,800 bits/sec, the duty cycle is decreased because of the design specification and the non-linearity of locked range of phase-locked loop. The performance test of data translator by double-pole network is also acceptable.