เอกสารอ้างอิง

1. สุพัฒน์ เอื้องพูลสวัสดิ์ , "การพัฒนาอุปกรณ์วิเคราะห์ความสูงของพัลซ์โดยใช้ไมโครโปรเซสเซอร์", วิทยานิพนธ์ปริญญามหาบัณฑิต ภาควิชานิวเคลียร์เทคโนโลยี บัณฑิตวิทยาลัย จุฬาลงกรณ์มหาวิทยาลัย, 2528.
2. Basic Counting Systems. 7th edition. CANBERRA.Canberra Industries ,Inc.
3. P.W.Nicholson. Nuclear Electronics. London,John Wiley & Sons ,Ltd., 1974.
4. Knoll G.F., Radiation Detection and Measurement, New York , John Wiley & Sons Ltd., 1979.
5. Winston Gayler, The APPLE II Circuit Description, Howard W.Sams & Co.,Inc., Indiana , 1983.
6. Steve Wozniak , The APPLE II , BYTE Publication, Inc. Peterborough,NH 30458,1977.
7. Marvin L. De Jong, APPLE II Assembly Language, Howard W. Sams & Co., Inc., Indiana , 1982.
8. Lon Poole With Martin Mc Niff & Steven Cook, APPLE II User's Guide , Osborn/Mc Graw-Hill, California.
9. ซีเอ็ดยูเคชั่น บริษัท , ไมโครคอมพิวเตอร์. เล่ม 8 . กทม. , บริษัท ซีเอ็ดยูเคชั่น จำกัด , ปี 2527 .

ภาคผนวก ก
ชุดคำสั่งแอสเซมบลีของ 6502 ไมโครโปรเซสเซอร์

6502 MICROPROCESSOR INSTRUCTIONS

ADC	Add Memory to Accumulator with Carry
AND	"AND" Memory with Accumulator
ASL	Shift Left One Bit (Memory or Accumulator)
BCC	Branch on Carry Clear
BCS	Branch on Carry Set
BEQ	Branch on Result Zero
BIT	Test Bits in Memory with Accumulator
BMI	Branch on Result Minus
BNE	Branch on Result not Zero
BPL	Branch on Result Plus
BRK	Force Break
BVC	Branch on Overflow Clear
BVS	Branch on Overflow Set
CLC	Clear Carry Flag
CLD	Clear Decimal Mode
CLI	Clear Interrupt Disable Bit
CLV	Clear Overflow Flag
CMP	Compare Memory and Accumulator
CPX	Compare Memory and Index X
CPY	Compare Memory and Index Y
DEC	Decrement Memory by One
DEX	Decrement Index X by One
DEY	Decrement Index Y by One
EOR	"Exclusive-Or" Memory with Accumulator
INC	Increment Memory by One
INX	Increment Index X by One
INY	Increment Index Y by One
JMP	Jump to New Location
JSR	Jump to New Location Saving Return Address
LDA	Load Accumulator with Memory
LDX	Load Index X with Memory
LDY	Load Index Y with Memory
LSR	Shift Right one Bit (Memory or Accumulator)
NOP	No Operation
ORA	"OR" Memory with Accumulator
PHA	Push Accumulator on Stack
PHP	Push Processor Status on Stack
PLA	Pull Accumulator from Stack
PLP	Pull Processor Status from Stack
ROL	Rotate One Bit Left (Memory or Accumulator)
ROR	Rotate One Bit Right (Memory or Accumulator)
RTI	Return from Interrupt
RTS	Return from Subroutine
SBC	Subtract Memory from Accumulator with Borrow
SEC	Set Carry Flag
SED	Set Decimal Mode
SEI	Set Interrupt Disable Status
STA	Store Accumulator in Memory
STX	Store Index X in Memory
STY	Store Index Y in Memory
TAX	Transfer Accumulator to Index X
TAY	Transfer Accumulator to Index Y
TSX	Transfer Stack Pointer to Index X
TXA	Transfer Index X to Accumulator
TXS	Transfer Index X to Stack Pointer
TYA	Transfer Index Y to Accumulator

THE FOLLOWING NOTATION APPLIES TO THIS SUMMARY:

A	Accumulator
X, Y	Index Registers
M	Memory
$\overline{C}$	Borrow
P	Processor Status Register
S	Stack Pointer
✓	Change
—	No Change
+	Add
∧	Logical AND
-	Subtract
∀	Logical Exclusive Or
↑	Transfer From Stack
↓	Transfer To Stack
←	Transfer To
→	Transfer To
V	Logical OR
PC	Program Counter
PCH	Program Counter High
PCL	Program Counter Low
OPER	Operand
#	Immediate Addressing Mode

FIGURE 1 ASL-SHIFT LEFT ONE BIT OPERATION

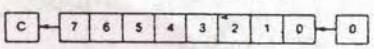
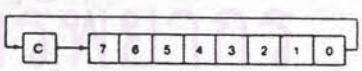


FIGURE 2 ROTATE ONE BIT LEFT (MEMORY OR ACCUMULATOR)

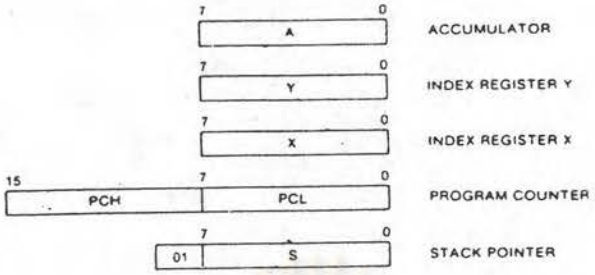
FIGURE 3

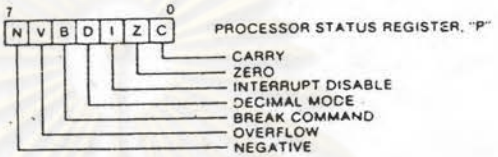


NOTE 1: BIT — TEST BITS

Bit 6 and 7 are transferred to the status register. If the result of A ∧ M is zero then Z=1, otherwise Z=0.

PROGRAMMING MODEL





INSTRUCTION CODES

Name Description	Operation	Addressing Mode	Assembly Language Form	HEX OP Code	No. Bytes	"P" Status Reg. N Z C I D V
ADC Add memory to accumulator with carry	A+M+C → A,C	Immediate Zero Page Zero Page,X Absolute Absolute,X Absolute,Y (Indirect,X) (Indirect),Y	ADC #Oper ADC Oper ADC Oper,X ADC Oper ADC Oper,X ADC Oper,Y ADC (Oper,X) ADC (Oper),Y	69 65 75 60 7D 79 61 71	2 2 2 3 3 3 2 2	√√√--√
AND "AND" memory with accumulator	A∧M → A	Immediate Zero Page Zero Page,X Absolute Absolute,X Absolute,Y (Indirect,X) (Indirect),Y	AND #Oper AND Oper AND Oper,X AND Oper AND Oper,X AND Oper,Y AND (Oper,X) AND (Oper),Y	29 25 35 20 30 39 21 31	2 2 2 3 3 3 2 2	√√----
ASL Shift left one bit (Memory or Accumulator)	(See Figure 1)	Accumulator Zero Page Zero Page,X Absolute Absolute,X	ASL A ASL Oper ASL Oper,X ASL Oper ASL Oper,X	0A 06 16 0E 1E	1 2 2 3 3	√√√---
BCC Branch on carry clear	Branch on C=0	Relative	BCC Oper	90	2	------
BCS Branch on carry set	Branch on C=1	Relative	BCS Oper	B0	2	------
BEQ Branch on result zero	Branch on Z=1	Relative	BEQ Oper	F0	2	------
BIT Test bits in memory with accumulator	A∧M, M_7 → N, M_6 → V	Zero Page Absolute	BIT* Oper BIT* Oper	24 2C	2 3	M_7√---M_6
BMI Branch on result minus	Branch on N=1	Relative	BMI Oper	30	2	------
BNE Branch on result not zero	Branch on Z=0	Relative	BNE Oper	D0	2	------
BPL Branch on result plus	Branch on N=0	Relative	BPL oper	10	2	------
BRK Force Break	Forced Interrupt PC-2↓P↓	Implied	BRK*	00	1	---1--
BVC Branch on overflow clear	Branch on V=0	Relative	BVC Oper	50	2	------

Name Description	Operation	Addressing Mode	Assembly Language Form	HEX OP Code	No Bytes	"P" Status Reg N Z C I D V
BVS Branch on overflow set	Branch on V=1	Relative	BVS Oper	70	2	
CLC Clear carry flag	0 → C	Implied	CLC	18	1	- - 0 -
CLD Clear decimal mode	0 → D	Implied	CLD	D8	1	- 0 - -
CLI	0 → I	Implied	CLI	58	1	- 0 -
CLV Clear overflow flag	0 → V	Implied	CLV	B8	1	0 - - -

CMP Compare memory and accumulator	A − M	Immediate
		Zero Page
		Zero Page, X
		Absolute
		Absolute X
		Absolute Y
		(Indirect,X)
		(Indirect),Y
			CMP #Oper
			CMP Oper
			CMP Oper,X
			CMP Oper
			CMP Oper,X
			CMP Oper,Y
			CMP (Oper,X)
			CMP (Oper),Y
				C9
				C5
				D5
				CD
				DD
				D9
				C1
				D1
					2
					2
					2
					3
					3
					3
					2
					2
						√√√ -

CPX Compare memory and index X	X − M	Immediate Zero Page Absolute	CPX #Oper CPX Oper CPX Oper	E0 E4 EC	2 2 3	√√√- - -
CPY Compare memory and index Y	Y − M	Immediate Zero Page Absolute	CPY #Oper CPY Oper CPY Oper	C0 C4 CC	2 2 3	√√√- - -
DEC Decrement memory by one	M − 1 → M	Zero Page Zero Page X Absolute Absolute,X	DEC Oper DEC Oper,X DEC Oper DEC Oper,X	C6 D6 CE DE	2 2 3 3	√√- - - -
DEX Decrement index X by one	X − 1 → X	Implied	DEX	CA	1	√√- - - -
DEY Decrement index Y by one	Y − 1 → Y	Implied	DEY	88	1	√√- - - -

Name Description	Operation	Addressing Mode	Assembly Language Form	HEX OP Code's	No. Bytes	"P" Status Reg N Z C I D V
EOR "Exclusive-Or" memory with accumulator	A ∨ M → A	Immediate Zero Page Zero Page X Absolute Absolute X Absolute Y (Indirect,X) (Indirect),Y	EOR #Oper EOR Oper EOR Oper,X EOR Oper EOR Oper X EOR Oper Y EOR (Oper,X) EOR (Oper),Y	49 45 55 4D 5D 59 41 51	2 2 2 3 3 3 2 2	√√ - - -
INC Increment memory by one	M + 1 → M	Zero Page Zero Page,X Absolute Absolute,X	INC Oper INC Oper,X INC Oper INC Oper,X	E6 F6 EE FE	2 2 3 3	√√- - - -
INX Increment index X by one	X + 1 → X	Implied	INX	E8	1	√√- - - -
INY Increment index Y by one	Y + 1 → Y	Implied	INY	C8	1	√√- - - -
JMP Jump to new location	(PC+1) → PCL (PC+2) → PCH	Absolute Indirect	JMP Oper JMP (Oper)	4C 6C	3 3	- - - - - -
JSR Jump to new location saving return address	PC+2 ↓ (PC+1) → PCL (PC+2) → PCH	Absolute	JSR Oper	20	3	- - - - - -

LDA Load accumulator with memory	M → A	Immediate
		Zero Page
		Zero Page,X
		Absolute
		Absolute,X
		Absolute,Y
		(Indirect,X)
		(Indirect),Y
			LDA #Oper
			LDA Oper
			LDA Oper,X
			LDA Oper
			LDA Oper,X
			LDA Oper,Y
			LDA (Oper,X)
			LDA (Oper),Y
				A9
				A5
				B5
				AD
				BD
				B9
				A1
				B1
					2
					2
					2
					3
					3
					3
					2
					2
						√√- - - -

LDX Load index X with memory	M → X	Immediate Zero Page Zero Page,Y Absolute Absolute,Y	LDX #Oper LDX Oper LDX Oper,Y LDX Oper LDX Oper,Y	A2 A6 B6 AE BE	2 2 2 3 3	√√- - - -
LDY Load index Y with memory	M → Y	Immediate Zero Page Zero Page,X Absolute Absolute,X	LDY #Oper LDY Oper LDY Oper,X LDY Oper LDY Oper,X	A0 A4 B4 AC BC	2 2 2 3 3	√√- - - -

Name Description	Operation	Addressing Mode	Assembly Language Form	HEX OP Code	No. Bytes	"P" Status Reg N Z C I D V
LSR Shift right one bit (memory or accumulator)	(See Figure 1)	Accumulator	LSR A	4A	1	0√√-- -
		Zero Page	LSR Oper	46	2	
		Zero Page,X	LSR Oper,X	56	2	
		Absolute	LSR Oper	4E	3	
		Absolute,X	LSR Oper,X	5E	3	
NOP No operation	No Operation	Implied	NOP	EA	1	------
ORA "OR" memory with accumulator	A ∨ M → A	Immediate	ORA #Oper	09	2	√√----
		Zero Page	ORA Oper	05	2	
		Zero Page,X	ORA Oper,X	15	2	
		Absolute	ORA Oper	0D	3	
		Absolute,X	ORA Oper,X	1D	3	
		Absolute,Y	ORA Oper,Y	19	3	
		(Indirect,X)	ORA (Oper,X)	01	2	
		(Indirect),Y	ORA (Oper),Y	11	2	
PHA Push accumulator on stack	A ↓	Implied	PHA	48	1	------
PHP Push processor status on stack	P ↓	Implied	PHP	08	1	------
PLA Pull accumulator from stack	A ↑	Implied	PLA	68	1	√√----
PLP Pull processor status from stack	P ↑	Implied	PLP	28	1	From Stack
ROL Rotate one bit left (memory or accumulator)	(See Figure 2)	Accumulator	ROL A	2A	1	√√√---
		Zero Page	ROL Oper	26	2	
		Zero Page,X	ROL Oper,X	36	2	
		Absolute	ROL Oper	2E	3	
		Absolute,X	ROL Oper,X	3E	3	
ROR Rotate one bit right (memory or accumulator)	(See Figure 3)	Accumulator	ROR A	6A	1	√√√---
		Zero Page	ROR Oper	66	2	
		Zero Page,X	ROR Oper,X	76	2	
		Absolute	ROR Oper	6E	3	
		Absolute,X	ROR Oper,X	7E	3	

Name Description	Operation	Addressing Mode	Assembly Language Form	HEX OP Code	No. Bytes	"P" Status Reg N Z C I D V
RTI Return from interrupt	P↑ PC↑	Implied	RTI	40	1	From Stack
RTS Return from subroutine	PC↑, PC+1 → PC	Implied	RTS	60	1	------
SBC Subtract memory from accumulator with borrow	A - M - C̄ → A	Immediate	SBC #Oper	E9	2	√√√---
		Zero Page	SBC Oper	E5	2	
		Zero Page,X	SBC Oper,X	F5	2	
		Absolute	SBC Oper	ED	3	
		Absolute,X	SBC Oper,X	FD	3	
		Absolute,Y	SBC Oper,Y	F9	3	
		(Indirect,X)	SBC (Oper,X)	E1	2	
		(Indirect),Y	SBC (Oper),Y	F1	2	
SEC Set carry flag	1 → C	Implied	SEC	38	1	---1---
SED Set decimal mode	1 → D	Implied	SED	F8	1	----1-
SEI Set interrupt disable status	1 → I	Implied	SEI	78		---1--
STA Store accumulator in memory	A → M	Zero Page	STA Oper	85	2	------
		Zero Page,X	STA Oper,X	95	2	
		Absolute	STA Oper	8D	3	
		Absolute,X	STA Oper,X	9D	3	
		Absolute,Y	STA Oper,Y	99	3	
		(Indirect,X)	STA (Oper,X)	81	2	
		(Indirect),Y	STA (Oper),Y	91	2	
STX Store index X in memory	X → M	Zero Page	STX Oper	86	2	------
		Zero Page,Y	STX Oper,Y	96	2	
		Absolute	STX Oper	8E	3	
STY Store index Y in memory	Y → M	Zero Page	STY Oper	84	2	------
		Zero Page,X	STY Oper,X	94	2	
		Absolute	STY Oper	8C	3	
TAX Transfer accumulator to index X	A → X	Implied	TAX	AA	1	√√----
TAY Transfer accumulator to index Y	A → Y	Implied	TAY	A8	1	√√----
TSX Transfer stack pointer to index X	S → X	Implied	TSX	BA	1	√√--- ---

Name Description	Operation	Addressing Mode	Assembly Language Form	HEX OP Code	No Bytes	"P" Status Reg. N Z C I D V
TXA Transfer index X to accumulator	X → A	Implied	TXA	8A	1	√√ - - - - -
TXS Transfer index X to stack pointer	X → S	Implied	TXS	9A	1	- - - - - -
TYA Transfer index Y to accumulator	Y → A	Implied	TYA	98	1	√√ - - - - -

HEX OPERATION CODES

00 — BRK
01 — ORA — (Indirect, X)
02 — NOP
03 — NOP
04 — NOP
05 — ORA — Zero Page
06 — ASL — Zero Page
07 — NOP
08 — PHP
09 — ORA — Immediate
0A — ASL — Accumulator
0B — NOP
0C — NOP
0D — ORA — Absolute
0E — ASL — Absolute
0F — NOP
10 — BPL
11 — ORA — (Indirect), Y
12 — NOP
13 — NOP
14 — NOP
15 — ORA — Zero Page, X
16 — ASL — Zero Page, X
17 — NOP
18 — CLC
19 — ORA — Absolute, Y
1A — NOP
1B — NOP
1C — NOP
1D — ORA — Absolute, X
1E — ASL — Absolute, X
1F — NOP
20 — JSR
21 — AND — (Indirect, X)
22 — NOP
23 — NOP
24 — BIT — Zero Page
25 — AND — Zero Page
26 — ROL — Zero Page
27 — NOP
28 — PLP
29 — AND — Immediate
2A — ROL — Accumulator
2B — NOP
2C — BIT — Absolute
2D — AND — Absolute
2E — ROL — Absolute
2F — NOP
30 — BMI
31 — AND — (Indirect), Y
32 — NOP
33 — NOP
34 — NOP
35 — AND — Zero Page, X
36 — ROL — Zero Page, X
37 — NOP
38 — SEC
39 — AND — Absolute, Y
3A — NOP
3B — NOP
3C — NOP
3D — AND — Absolute, X
3E — ROL — Absolute, X
3F — NOP
40 — RTI
41 — EOR — (Indirect, X)
42 — NOP
43 — NOP
44 — NOP
45 — EOR — Zero Page
46 — LSR — Zero Page
47 — NOP
48 — PHA
49 — EOR — Immediate
4A — LSR — Accumulator
4B — NOP
4C — JMP — Absolute
4D — EOR — Absolute
4E — LSR — Absolute
4F — NOP
50 — BVC
51 — EOR (Indirect), Y
52 — NOP
53 — NOP
54 — NOP
55 — EOR — Zero Page, X
56 — LSR — Zero Page, X
57 — NOP
58 — CLI
59 — EOR — Absolute, Y
5A — NOP
5B — NOP
5C — NOP
5D — EOR — Absolute, X
5E — LSR — Absolute, X
5F — NOP
60 — RTS
61 — ADC — (Indirect, X)
62 — NOP
63 — NOP
64 — NOP
65 — ADC — Zero Page
66 — ROR — Zero Page
67 — NOP
68 — PLA
69 — ADC — Immediate
6A — ROR — Accumulator
6B — NOP
6C — JMP — Indirect
6D — ADC — Absolute
6E — ROR — Absolute
6F — NOP
70 — BVS
71 — ADC — (Indirect), Y
72 — NOP
73 — NOP
74 — NOP
75 — ADC — Zero Page, X
76 — ROR — Zero Page, X
77 — NOP
78 — SEI
79 — ADC — Absolute, Y
7A — NOP
7B — NOP
7C — NOP
7D — ADC — Absolute, X NOP
7E — ROR — Absolute, X NOP
7F — NOP
80 — NOP
81 — STA — (Indirect, X)
82 — NOP
83 — NOP
84 — STY — Zero Page
85 — STA — Zero Page
86 — STX — Zero Page
87 — NOP
88 — DEY
89 — NOP
8A — TXA
8B — NOP
8C — STY — Absolute

8D — STA — Absolute
8E — STX — Absolute
8F — NOP
90 — BCC
91 — STA — (Indirect), Y
92 — NOP
93 — NOP
94 — STY — Zero Page, X
95 — STA — Zero Page, X
96 — STX — Zero Page, Y
97 — NOP
98 — TYA
99 — STA — Absolute, Y
9A — TXS
9B — NOP
9C — NOP
9D — STA — Absolute, X
9E — NOP
9F — NOP
A0 — LDY — Immediate
A1 — LDA — (Indirect, X)
A2 — LDX — Immediate
A3 — NOP
A4 — LDY — Zero Page
A5 — LDA — Zero Page
A6 — LDX — Zero Page
A7 — NOP
A8 — TAY
A9 — LDA — Immediate
AA — TAX
AB — NOP
AC — LDY — Absolute
AD — Absolute
AE — LDX — Absolute
AF — NOP
B0 — BCS
B1 — LDA — (Indirect), Y
B2 — NOP
B3 — NOP
B4 — LDY — Zero Page, X
B5 — LDA — Zero Page, X
B6 — LDX — Zero Page, Y
B7 — NOP
B8 — CLV
B9 — LDA — Absolute, Y
BA — TSX
BB — NOP
BC — LDY — Absolute, X
BD — LDA — Absolute, X
BE — LDX — Absolute, Y
BF — NOP
C0 — CPY — Immediate
C1 — CMP — (Indirect, X)
C2 — NOP
C3 — NOP
C4 — CPY — Zero Page
C5 — CMP — Zero Page
C6 — DEC — Zero Page
C7 — NOP
C8 — INY
C9 — CMP — Immediate
CA — DEX
CB — NOP
CC — CPY — Absolute
CD — CMP — Absolute
CE — DEC — Absolute
CF — NOP
D0 — BNE
D1 — CMP — (Indirect), Y
D2 — NOP
D3 — NOP
D4 — NOP
D5 — CMP — Zero Page, X
D6 — DEC — Zero Page, X
D7 — NOP
D8 — CLD
D9 — CMP — Absolute, Y
DA — NOP
DB — NOP
DC — NOP
DD — CMP — Absolute, X
DE — DEC — Absolute, X
DF — NOP
E0 — CPX — Immediate
E1 — SBC — (Indirect, X)
E2 — NOP
E3 — NOP
E4 — CPX — Zero Page
E5 — SBC — Zero Page
E6 — INC — Zero Page
E7 — NOP
E8 — INX
E9 — SBC — Immediate
EA — NOP
EB — NOP
EC — CPX — Absolute
ED — SBC — Absolute
EE — INC — Absolute
EF — NOP
F0 — BEQ
F1 — SBC — (Indirect), Y
F2 — NOP
F3 — NOP
F4 — NOP
F5 — SBC — Zero Page, X
F6 — INC — Zero Page, X
F7 — NOP
F8 — SED
F9 — SBC — Absolute, Y
FA — NOP
FB — NOP
FC — NOP
FD — SBC — Absolute, X
FE — INC — Absolute, X
FF — NOP

ภาคผนวก ข
ข้อมูลวงจรรวม

LOGIC DIVISION

JANUARY 1982

GATES

54/7408, LS08, S08

Quad Two-Input AND Gate

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
7408	15ns	16mA
74LS08	9ns	3.4mA
74S08	5ns	25mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ± 5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ± 10%; T_A = −55°C to +125°C
Plastic DIP	N7408N • N74LS08N N74S08N	
Ceramic DIP	N7408F • N74LS08F N74S08F	S54S08F • S54LS08F
Flatpack		S54S08W • S54LS08W

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

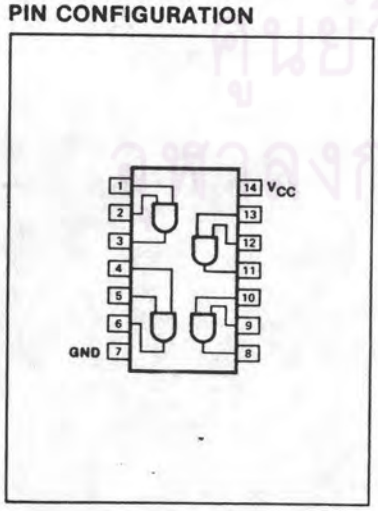
H = HIGH voltage level
L = LOW voltage level

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

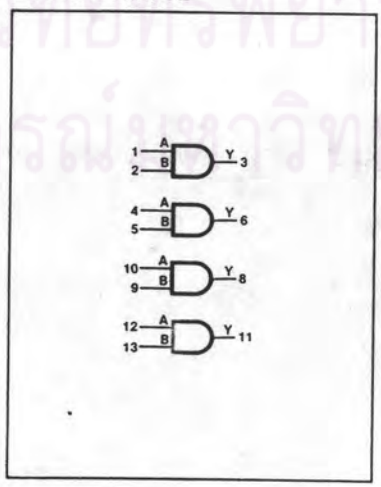
PINS	DESCRIPTION	54/74	54/74S	54/74LS
A, B	Inputs	1ul	1Sul	1LSul
Y	Output	10ul	10Sul	10LSul

NOTE
Where a 54/74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL}, a 54/74S unit load (Sul) is 50μA I_{IH} and −2.0mA I_{IL}, and 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

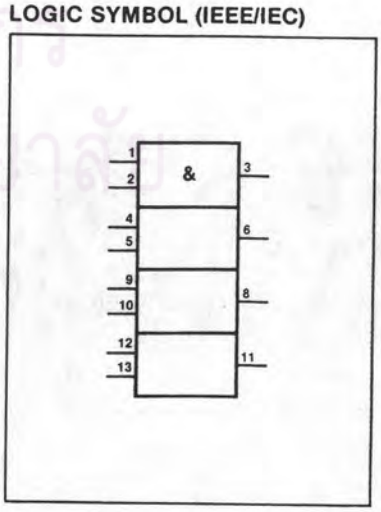
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Signetics

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54	54LS	54S	74	74LS	74S	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +5	−30 to +1	−30 to +5	−30 to +5	−30 to +1	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125			0 to 70			°C

3

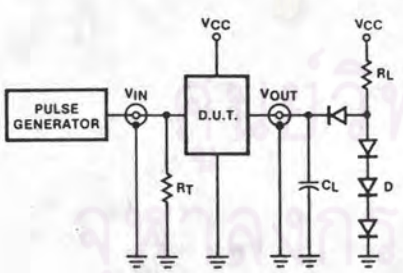
RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74			54/74LS			54/74S			UNIT
			Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			2.0			2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.8			+0.7			+0.8	V
		Com'l			+0.8			+0.8			+0.8	V
I_{IK}	Input clamp current				−12			−18			−18	mA
I_{OH}	HIGH-level output current				−800			−400			−1000	μA
I_{OL}	LOW-level output current	Mil			16			4			20	mA
		Com'l			16			8			20	mA
T_A	Operating free-air temperature	Mil	−55		+125	−55		+125	−55		+125	°C
		Com'l	0		70	0		70	0		70	°C

NOTE
V_{IL} = +0.7V MAX for 54S at T_A = +125°C only.

TEST CIRCUITS AND WAVEFORMS

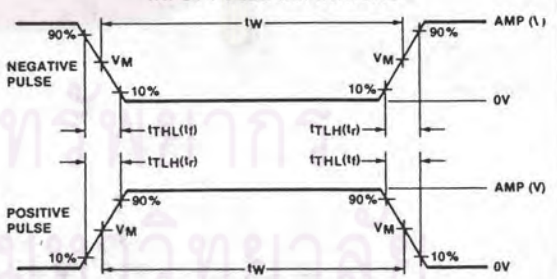
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

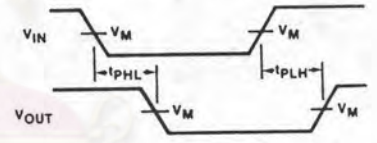
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS[1]			54/7408			54/74LS08			54/74S08			UNIT
				Min	Typ[2]	Max	Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH} HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, I_{OH} = MAX		Mil	2.4	3.4		2.5	3.4		2.5	3.4		V
			Com'l	2.4	3.4		2.7	3.4		2.7	3.4		V
V_{OL} LOW-level output voltage	V_{CC} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil		0.2	0.4		0.25	0.4			0.5[4]	V
			Com'l		0.2	0.4		0.35	0.5			0.5	V
		I_{OL} = 4mA	74LS					0.25	0.4				V
V_{IK} Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					– 1.5			– 1.5			– 1.2	V
I_I Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V				1.0						1.0	mA
		V_I = 7.0V							0.1				mA
I_{IH} HIGH-level input current	V_{CC} = MAX	V_I = 2.4V				40							μA
		V_I = 2.7V							20			50	μA
I_{IL} LOW-level input current	V_{CC} = MAX	V_I = 0.4V				– 1.6			– 0.4				mA
		V_I = 0.5V										– 2.0	mA
I_{OS} Short-circuit output current[3]	V_{CC} = MAX		Mil	– 20		– 55	– 20		– 100	– 40		– 100	mA
			Com'l	– 18		– 55	– 20		– 100	– 40		– 100	mA
I_{CC} Supply Current (total)	V_{CC} = MAX	I_{CCH} Outputs HIGH			11	21		2.4	4.8		18	32	mA
		I_{CCL} Outputs LOW			20	33		4.4	8.8		32	57	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. V_{OL} = + 0.45V MAX for 54S at T_A = + 125°C only.

AC WAVEFORMS

WAVEFORM FOR NON-INVERTING OUTPUTS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

Waveform 1

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	54/74		54/74LS		54/74S		UNIT
		C_L = 15pF, R_L = 400Ω		C_L = 15pF, R_L = 2kΩ		C_L = 15pF, R_L = 280Ω		
		Min	Max	Min	Max	Min	Max	
t_{PLH} Propagation delay	Waveform 1		27		15		7.0	ns
t_{PHL}			19		20		7.5	

SCHMITT TRIGGERS

54/7414, LS14

Hex Inverter Schmitt Trigger

DESCRIPTION

The '14 contains six logic inverters which accept standard TTL input signals and provide standard TTL output levels. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. In addition, they have greater noise margin than conventional inverters.

Each circuit contains a Schmitt trigger followed by a Darlington level shifter and a phase splitter driving a TTL totem-pole output. The Schmitt trigger uses positive feedback to effectively speed-up slow input transition, and provide different input threshold voltages for positive and negative-going transitions. This hysteresis between the positive-going and negative-going input thresholds (typically 800mV) is determined internally by resistor ratios and is essentially insensitive to temperature and supply voltage variations.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
7414	15ns	31mA
74LS14	15ns	10mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N7414N • N74LS14N	
Ceramic DIP	N7414F • N74LS14F	S5414F • S54LS14F
Flatpack		S5414W • S54LS14W

FUNCTION TABLE

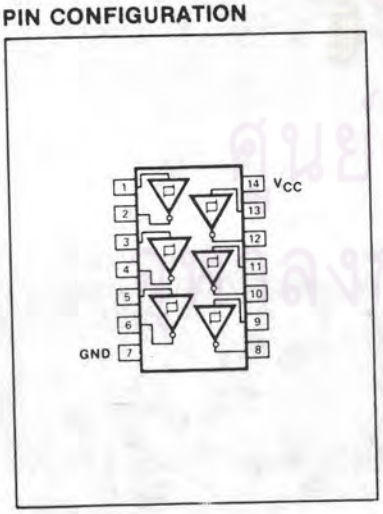
INPUT	OUTPUT
A	Y
0	1
1	0

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

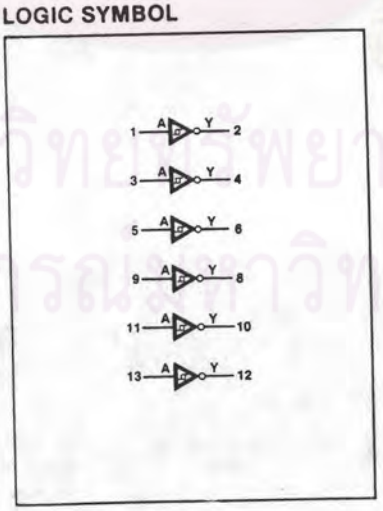
PINS	DESCRIPTION	54/74	54/74LS
A	Inputs	1ul	1LSul
Y	Output	10ul	10LSul

NOTE
Where a 54/74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL}, and a 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

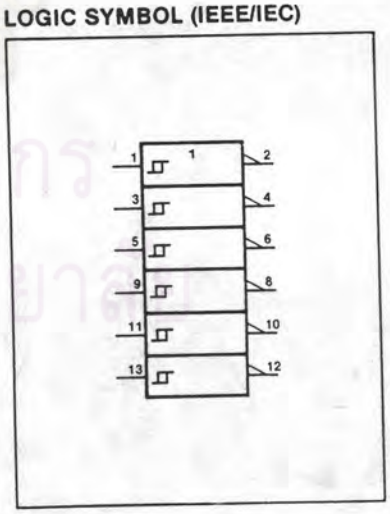
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Signetics

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54	54LS	74	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +1	−30 to +5	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125		0 to 70		°C

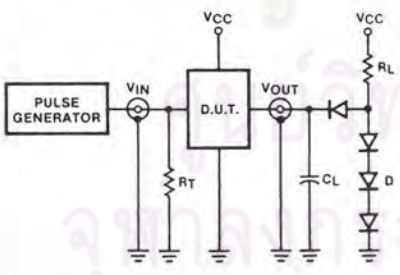
3

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74			54/74LS			UNIT
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
I_{IK}	Input clamp current				−12			−18	mA
I_{OH}	HIGH-level output current				−800			−400	μA
I_{OL}	LOW-level output current	Mil			16			4	mA
		Com'l			16			8	mA
T_A	Operating free-air temperature	Mil	−55		+125	−55		+125	°C
		Com'l	0		70	0		70	°C

TEST CIRCUITS AND WAVEFORMS

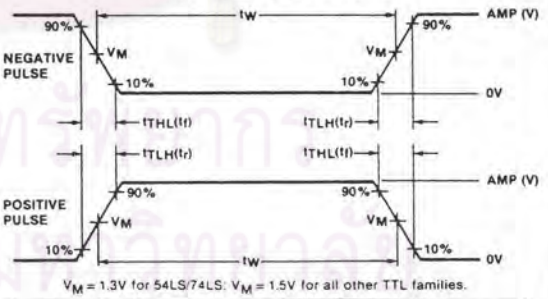
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

SCHMITT TRIGGERS

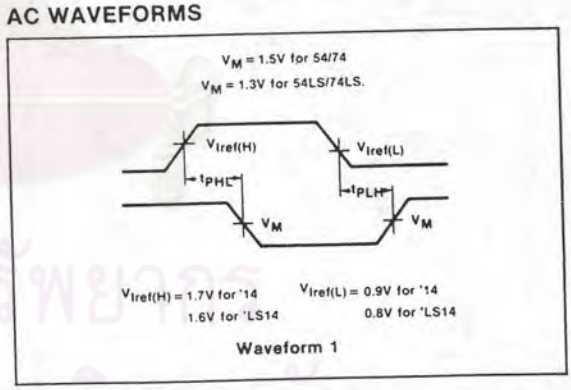
54/7414, LS14

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/7414			54/74LS14			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{T+}	Positive-going threshold	V_{CC} = 5.0V			1.5	1.7	2.0	1.4	1.6	1.9	V
V_{T-}	Negative-going threshold	V_{CC} = 5.0V			0.6	0.9	1.1	0.5	0.8	1.0	V
ΔV_T	Hysteresis ($V_{T+} - V_{T-}$)	V_{CC} = 5.0V			0.4	0.8		0.4	0.8		V
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, $V_I = V_{T-MIN}$, I_{OH} = MAX		Mil	2.4	3.4		2.5	3.4		V
				Com'l	2.4	3.4		2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, $V_I = V_{T+MAX}$	I_{OL} = MAX	Mil		0.2	0.4		0.25	0.4	V
				Com'l		0.2	0.4		0.35	0.5	V
			I_{OL} = 4mA	74LS					0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, $I_I = I_{IK}$					-1.5			-1.5	V
I_{T+}	Input current at positive-going threshold	V_{CC} = 5.0V, $V_I = V_{T+}$				-0.43			-0.14		mA
I_{T-}	Input current at negative-going threshold	V_{CC} = 5.0V, $V_I = V_{T-}$				-0.56			-0.18		mA
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V				1.0				mA
			V_I = 7.0V							0.1	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX	V_I = 2.4V				40				μA
			V_I = 2.7V							20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V					-1.2			-0.4	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		Mil	-20		-55	-20		-100	mA
				Com'l	-18		-55	-20		-100	mA
I_{CC}	Supply current (total)	V_{CC} = MAX	I_{CCH}	Outputs HIGH		22	36		8.6	16	mA
			I_{CCL}	Outputs LOW		39	60		12	21	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and $V_{CC} = V_{CC\,MAX} + 0.5V$. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

AC WAVEFORMS



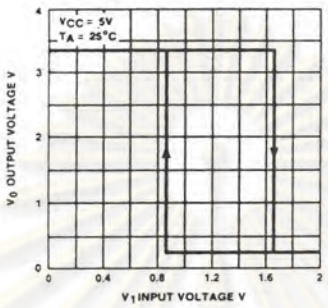
Waveform 1

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

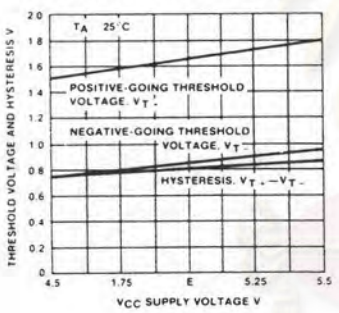
PARAMETER		TEST CONDITIONS	54/74		54LS/74LS		UNIT
			C_L = 15pF, R_L = 400Ω		C_L = 15pF, R_L = 2kΩ		
			Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay	Waveform 1		22 22		22 22	ns

TYPICAL CHARACTERISTICS

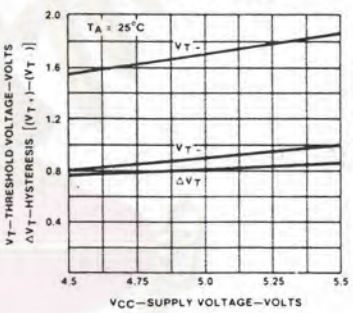
(54/74, 54LS/74LS)
V_{IN} vs V_{OUT}
TRANSFER FUNCTION



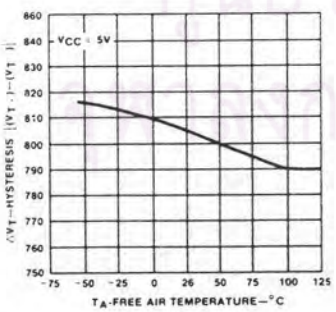
(54/74)
THRESHOLD VOLTAGE AND
HYSTERESIS vs
POWER SUPPLY VOLTAGE



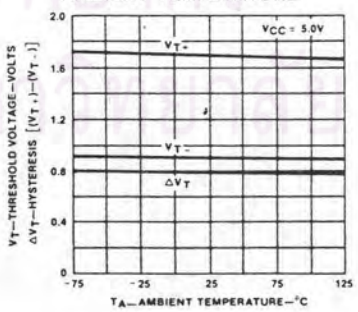
(54LS/74LS)
THRESHOLD VOLTAGE AND
HYSTERESIS vs
POWER SUPPLY VOLTAGE



(54/74)
HYSTERESIS vs TEMPERATURE



(54LS/74LS)
THRESHOLD VOLTAGE AND
HYSTERESIS vs
AMBIENT TEMPERATURE



GATES

54/7432, LS32, S32

Quad Two-Input OR Gate

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
7432	12ns	19mA
74LS32	14ns	4.0mA
74S32	4ns	28mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ± 5%; T_A = 0°C to + 70°C	MILITARY RANGES V_{CC} = 5V ± 10%; T_A = − 55°C to + 125°C
Plastic DIP	N7432N • N74LS32N N74S32N	
Ceramic DIP	N7432F • N74LS32F N74S32F	S5432F • S54LS32F
Flatpack		S5432W • S54LS32W

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	H

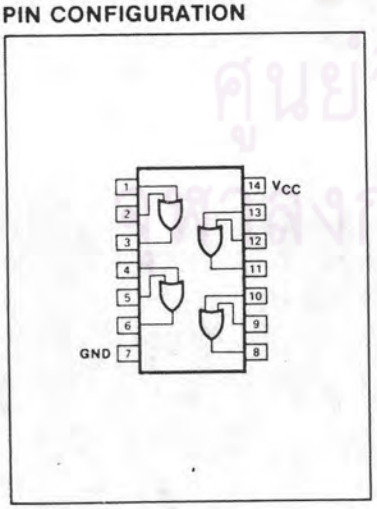
H = HIGH voltage level
L = LOW voltage level

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

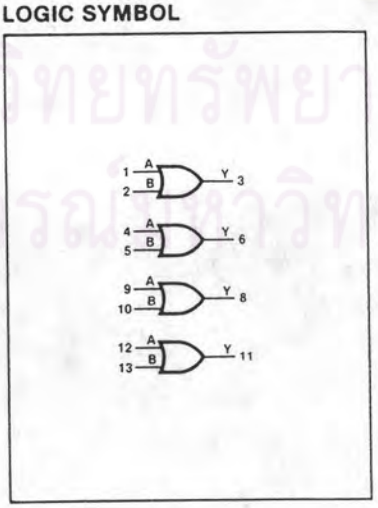
PINS	DESCRIPTION	54/74	54/74S	54/74LS
A, B	Inputs	1ul	1Sul	1LSul
Y	Output	10ul	10Sul	10LSul

NOTE
Where a 54/74 unit load (ul) is understood to be 40μA I_{IH} and − 1.6mA I_{IL}, a 54/74S unit load (Sul) is 50μA I_{IH} and − 2.0mA I_{IL}, and a 54/74LS unit load (LSul) is 20μA I_{IH} and − 0.4mA I_{IL}.

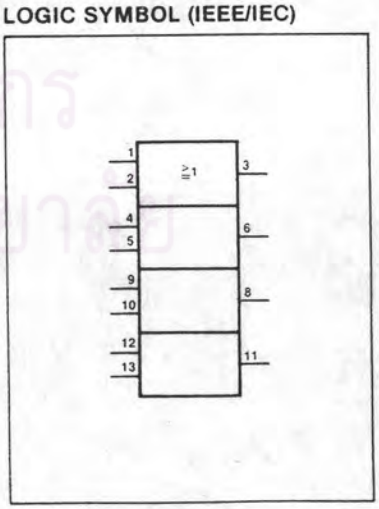
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

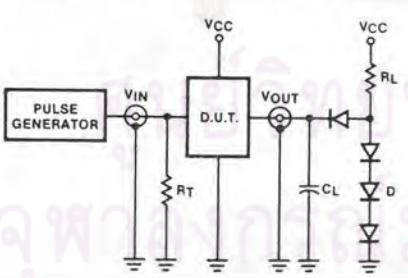
PARAMETER		54	54LS	54S	74	74LS	74S	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +5	−30 to +1	−30 to +5	−30 to +5	−30 to +1	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125			0 to 70			°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74			54/74LS			54/74S			UNIT
			Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			2.0			2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.8			+0.7			+0.8	V
		Com'l			+0.8			+0.8			+0.8	V
I_{IK}	Input clamp current				−12			−18			−18	mA
I_{OH}	HIGH-level output current				−800			−400			−1000	μA
I_{OL}	LOW-level output current	Mil			16			4			20	mA
		Com'l			16			8			20	mA
T_A	Operating free-air temperature	Mil	−55		+125	−55		+125	−55		+125	°C
		Com'l	0		70	0		70	0		70	°C

TEST CIRCUITS AND WAVEFORMS

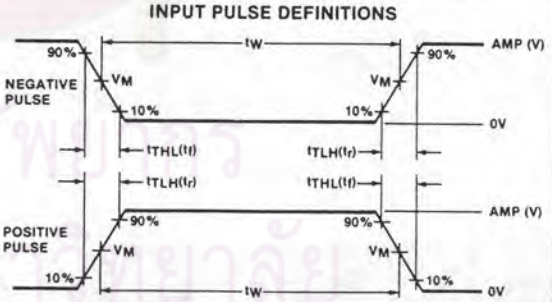
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

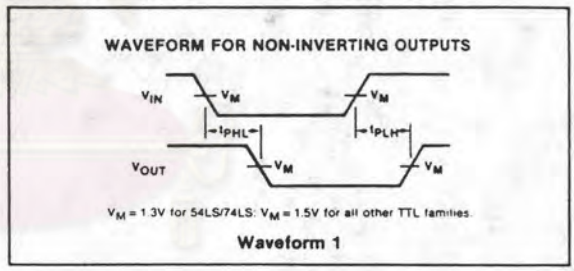
FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS[1]			54/7432			54/74LS32			54/74S32			UNIT
				Min	Typ[2]	Max	Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH} HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, I_{OH} = MAX		Mil	2.4	3.4		2.5	3.4		2.5	3.4		V
			Com'l	2.4	3.4		2.7	3.4		2.7	3.4		V
V_{OL} LOW-level output voltage	V_{CC} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil		0.2	0.4		0.25	0.4			0.5	V
			Com'l		0.2	0.4		0.35	0.5			0.5	V
		I_{OL} = 4mA	74LS					0.25	0.4				V
V_{IK} Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					– 1.5			– 1.5			– 1.2	V
I_I Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V				1.0						1.0	mA
		V_I = 7.0V							0.1				mA
I_{IH} HIGH-level input current	V_{CC} = MAX	V_I = 2.4V				40							μA
		V_I = 2.7V							20			50	μA
I_{IL} LOW-level input current	V_{CC} = MAX	V_I = 0.4V				– 1.6			– 0.4				mA
		V_I = 0.5V										– 2.0	mA
I_{OS} Short-circuit output current[3]	V_{CC} = MAX		Mil	– 20		– 55	– 20		– 100	– 40		– 100	mA
			Com'l	– 18		– 55	– 20		– 100	– 40		– 100	mA
I_{CC} Supply current (total)	V_{CC} = MAX	I_{CCH} Outputs HIGH			15	22		3.1	6.2		18	32	mA
		I_{CCL} Outputs LOW			23	38		4.9	9.8		38	68	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

AC WAVEFORM



Waveform 1

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	54/74		54/74LS		54/74S		UNIT
		C_L = 15pF, R_L = 400Ω		C_L = 15pF, R_L = 2kΩ		C_L = 15pF, R_L = 280Ω		
		Min	Max	Min	Max	Min	Max	
t_{PLH} Propagation delay	Waveform 1		15		22		7.0	ns
t_{PHL} Propagation delay	Waveform 1		22		22		7.0	ns

FLIP-FLOPS

54/7474, LS74A, S74

Dual D-Type Flip-Flop

DESCRIPTION

The '74 is a dual positive edge-triggered D-type flip-flop featuring individual Data, Clock, Set and Reset inputs; also complementary Q and $\overline{Q}$ outputs.

Set ($\overline{S}_D$) and Reset ($\overline{R}_D$) are asynchronous active-LOW inputs and operate independently of the Clock input. Information on the Data (D) input is transferred to the Q output on the LOW-to-HIGH transition of the clock pulse. The D inputs must be stable one setup time prior to the LOW-to-HIGH clock transition for predictable operation. Although the Clock input is level-sensitive, the positive transition of the clock pulse between the 0.8V and 2.0V levels should be equal to or less than the clock-to-output delay time for reliable operation.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
7474	25MHz	17mA
74LS74A	33MHz	4mA
74S74	100MHz	30mA

ORDERING CODE

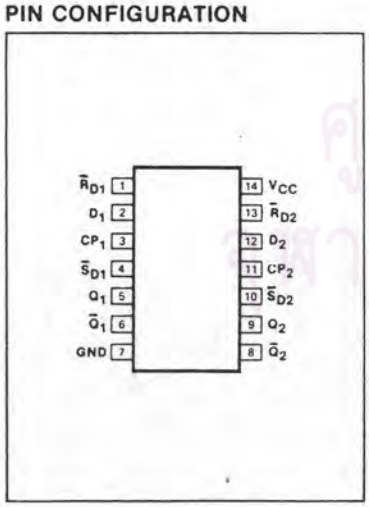
PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N7474N • N74LS74AN N74S74N	
Ceramic DIP	N7474F • N74LS74AF N74S74F	S5474F • S54LS74AF S54S74F
Flatpack		S5474W • S54LS74AW S54S74W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

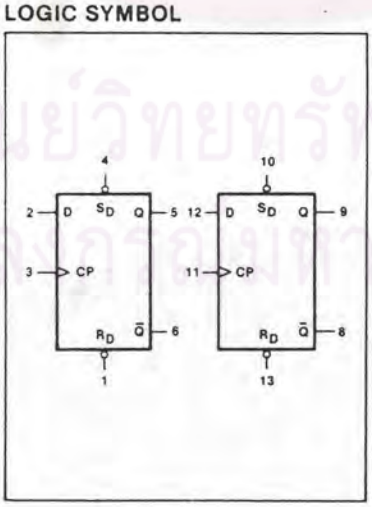
PINS	DESCRIPTION	54/74	54/74S	54/74LS
D	Input	1ul	1Sul	1LSul
$\overline{R}_D$	Input	2ul	3Sul	2LSul
$\overline{S}_D$	Input	1ul	2Sul	2LSul
CP	Input	2ul	2Sul	1LSul
Q, $\overline{Q}$	Outputs	10ul	10Sul	10LSul

NOTE
Where a 54/74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL}, a 54/74S unit load (Sul) is 50μA I_{IH} and −2.0mA I_{IL}, and 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

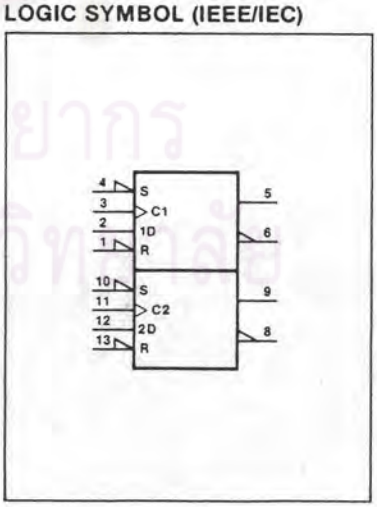
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)

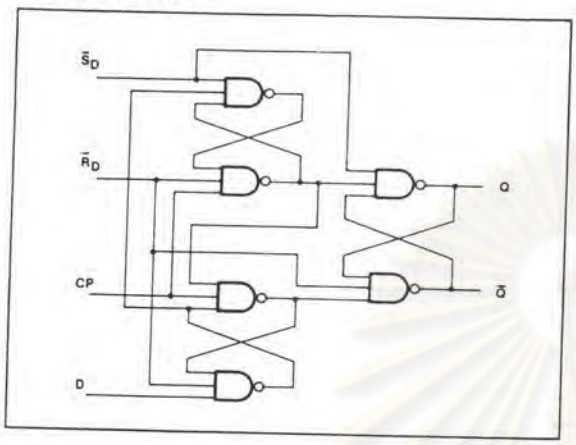


Signetics

FLIP-FLOPS

54/7474, LS74A, S74

LOGIC DIAGRAM



MODE SELECT—FUNCTION TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	$\overline{S}_D$	$\overline{R}_D$	CP	D	Q	$\overline{Q}$
Asynchronous Set	L	H	X	X	H	L
Asynchronous Reset (Clear)	H	L	X	X	L	H
Undetermined[a]	L	L	X	X	H	H
Load "1" (Set)	H	H	↑	h	H	L
Load "0" (Reset)	H	H	↑	l	L	H

H = HIGH voltage level steady state.
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
L = LOW voltage level steady state.
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
X = Don't care.
↑ = LOW-to-HIGH clock transition.

NOTE
(a) Both outputs will be HIGH while both $\overline{S}_D$ and $\overline{R}_D$ are LOW, but the output states are unpredictable if $\overline{S}_D$ and $\overline{R}_D$ go HIGH simultaneously.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54	54LS	54S	74	74LS	74S	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +5	−30 to +1	−30 to +5	−30 to +5	−30 to +1	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125			0 to 70			°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74			54/74LS			54/74S			UNIT
			Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			2.0			2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.8			+0.7			+0.8	V
		Com'l			+0.8			+0.8			+0.8	V
I_{IK}	Input clamp current				−12			−18			−18	mA
I_{OH}	HIGH-level output current				−400			−400			−1000	μA
I_{OL}	LOW-level output current	Mil			16			4			20	mA
		Com'l			16			8			20	mA
T_A	Operating free-air temperature	Mil	−55		+125	−55		+125	−55		+125	°C
		Com'l	0		70	0		70	0		70	°C

NOTE
V_{IL} = +0.7V MAX for 54S at T_A = +125°C only.

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/7474			54/74LS74A			54/74S74			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	2.4	3.4		2.5	3.4		2.5	3.4		V
				Com'l	2.4	3.4		2.7	3.4		2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil		0.2	0.4		0.25	0.4			0.5[6]	V
				Com'l		0.2	0.4		0.35	0.5			0.5	V
			I_{OL} = 4mA	74LS					0.25	0.4				V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					-1.5			-1.5			-1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V				1.0						1.0	mA
			V_I = 7.0V	D input						0.1				mA
				$\overline{R}_D$ input						0.2				mA
				$\overline{S}_D$ input						0.2				mA
				CP input						0.1				mA
I_{IH}	HIGH-level input current	V_{CC} = MAX	V_I = 2.4V	D input			40							μA
				$\overline{R}_D$ input			120							μA
				$\overline{S}_D$ input			80							μA
				CP input			80							μA
			V_I = 2.7V	D input						20			50	μA
				$\overline{R}_D$ input						40			150	μA
				$\overline{S}_D$ input						40			100	μA
				CP input						20			100	μA
I_{IL}	LOW-level input current[5]	V_{CC} = MAX	V_I = 0.4V	D input			-1.6			-0.4				mA
				$\overline{R}_D$ input			-3.2			-0.8				mA
				$\overline{S}_D$ input			-1.6			-0.8				mA
				CP input			-3.2			-0.4				mA
			V_I = 0.5V	D input									-2	mA
				$\overline{R}_D$ input									-6	mA
				$\overline{S}_D$ input									-4	mA
				CP input									-4	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		Mil	-20		-57	-20		-100	-40		-100	mA
				Com'l	-18		-57	-20		-100	-40		-100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX				17	30		4	8		30	50	mA

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the shorted circuit should not exceed one second.
4. Measure I_{CC} with the Clock inputs grounded and all outputs open, with the Q and $\overline{Q}$ outputs HIGH in turn.
5. Set is tested with reset HIGH and reset is tested with set HIGH.
6. V_{OL} = +0.45V MAX for 54S at T_A = +125°C only.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54/74		54LS/74LS		54S/74S		UNIT
			C_L = 15pF, R_L = 400Ω		C_L = 15pF, R_L = 2kΩ		C_L = 15pF, R_L = 280Ω		
			Min	Max	Min	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	15		25		75		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1		25 40		25 40		9 9	ns
t_{PLH} t_{PHL}	Propagation delay Set or Reset to output	Waveform 2		25 40		25 40		6 13.5	ns
		Waveform 2 CP = HIGH							
t_{PHL}	Set or Reset to output	Waveform 2 CP = LOW		0		40		8	ns

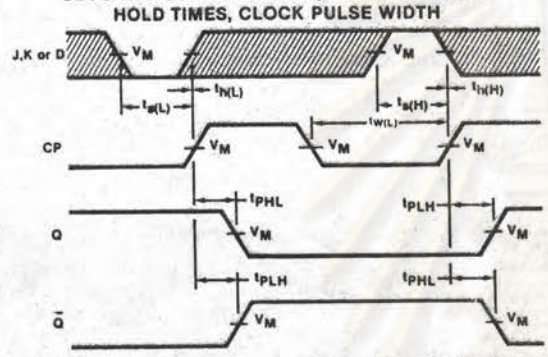
NOTE
Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

AC SETUP REQUIREMENTS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER	TEST CONDITIONS	54/74		54LS/74LS		54S/74S		UNIT
		Min	Max	Min	Max	Min	Max	
$t_W(H)$ Clock pulse width (HIGH)	Waveform 1	30		25		6		ns
$t_W(L)$ Clock pulse width (LOW)	Waveform 1	37				7.3		ns
$t_W(L)$ Set or reset pulse width (LOW)	Waveform 2	30		25		7		ns
$t_s(H)$ Setup time (HIGH) data to clock	Waveform 1	20		20		3		ns
$t_s(L)$ Setup time (LOW) data to clock	Waveform 1	20		20		3		ns
t_h Hold time data to clock	Waveform 1	5		5		2		ns

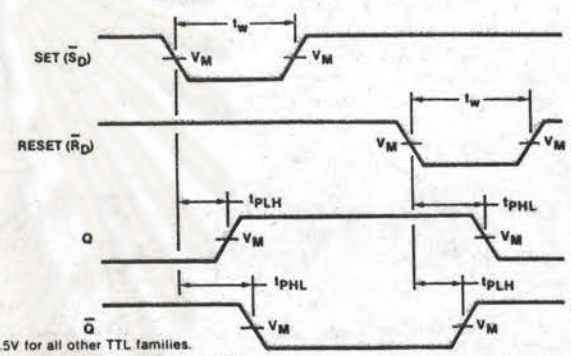
AC WAVEFORMS

CLOCK TO OUTPUT DELAYS, DATA SETUP AND HOLD TIMES, CLOCK PULSE WIDTH



Waveform 1

SET AND RESET TO OUTPUT DELAYS, SET AND RESET PULSE WIDTHS

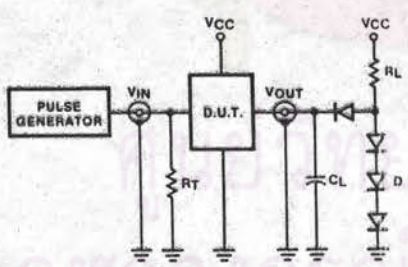


Waveform 2

V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUITS AND WAVEFORMS

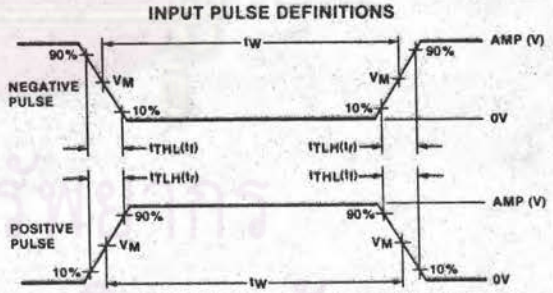
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

COUNTERS

54/7490, LS90

Decade Counter

DESCRIPTION

The '90 is a 4-bit, ripple-type Decade Counter. The device consists of four master-slave flip-flops internally connected to provide a divide-by-two section and a divide-by-five section. Each section has a separate Clock input to initiate state changes of the counter on the HIGH-to-LOW clock transition. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes.

A gated AND asynchronous Master Reset ($MR_1 \cdot MR_2$) is provided which overrides both clocks and resets (clears) all the flip-flops. Also provided is a gated AND asynchronous Master Set ($MS_1 \cdot MS_2$) which overrides the clocks and the MR inputs, setting the outputs to nine (HLLH).

Since the output from the divide-by-two section is not internally connected to the succeeding stages, the device may be operated in various counting modes. In a BCD (8421) counter the $\overline{CP}_1$ input must be externally connected to the Q_0 output. The $\overline{CP}_0$ input receives the incoming count producing a BCD count sequence. In a symmetrical Bi-quinary divide-by-ten counter the Q_3 output must be connected externally to the $\overline{CP}_0$ input. The input count is then applied to the CP_1 input and a divide-by-ten square wave is obtained at output Q_0. To operate as a divide-by-two and a divide-by-five counter no external interconnections are required. The first flip-flop is used as a binary element for the divide-by-two function ($\overline{CP}_0$ as the input and Q_0 as the output). The $\overline{CP}_1$ input is used to obtain a divide-by-five operation at the Q_3 output.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT
7490	30MHz	30mA
74LS90	42MHz	9mA

ORDERING CODE

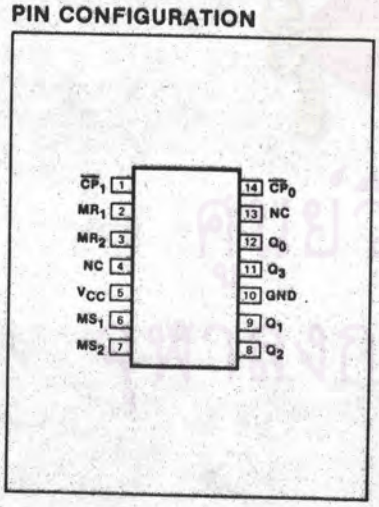
PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N7490N • N74LS90N	
Ceramic DIP	N7490F • N74LS90F	S54LS90F
Flatpack		S54LS90W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

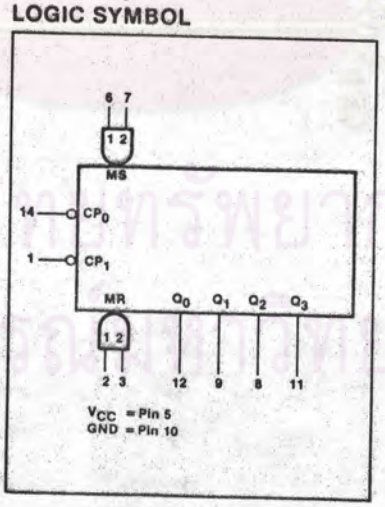
PINS	DESCRIPTION	54/74	54/74LS
$\overline{CP}_0$	Input	2ul	6LSul
$\overline{CP}_1$	Input	4ul	8LSul
MR, MS	Inputs	1ul	1LSul
Q_0-Q_3	Outputs	10ul	10LSul

NOTE
Where a 54/74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL}, and a 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

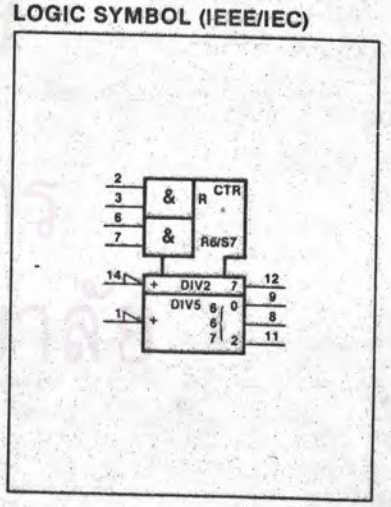
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)

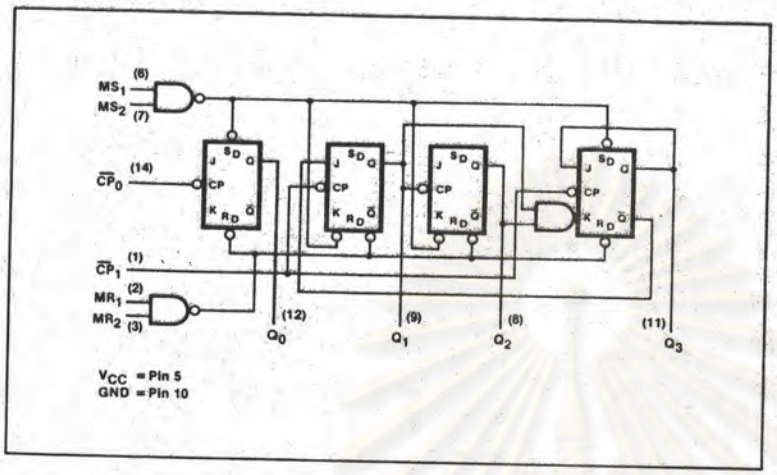


Signetics

COUNTERS

54/7490, LS90

LOGIC DIAGRAM



MODE SELECTION—FUNCTION TABLE

RESET/SET INPUTS				OUTPUTS			
MR_1	MR_2	MS_1	MS_2	Q_0	Q_1	Q_2	Q_3
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
L	X	L	X	Count			
X	L	X	L	Count			
L	X	X	L	Count			
H	L	L	X	Count			

H = HIGH voltage level
L = LOW voltage level
X = Don't care

BCD COUNT SEQUENCE—FUNCTION TABLE

COUNT	OUTPUTS			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

NOTE
Output Q_0 connected to input $\overline{CP}_1$.

ABSOLUTE MAXIMUM RATINGS

(Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54	54LS	74	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +1	−30 to +5	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125		0 to 70		°C

NOTE
V_{IN} is limited to +5.5V on $\overline{CP}_0$ and $\overline{CP}_1$ inputs on the 54/74LS90 only.

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74			54/74LS			UNIT
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.8			+0.7	V
		Com'l			+0.8			+0.8	V
I_{IK}	Input clamp current				−12			−18	mA
I_{OH}	HIGH-level output current				−800			−400	μA
I_{OL}	LOW-level output current	Mil			16			4	mA
		Com'l			16			8	mA
T_A	Operating free-air temperature	Mil	−55		+125	−55		+125	°C
		Com'l	0		70	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS[1]			54/7490			54/74LS90			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	2.4	3.4		2.5	3.4		V
				Com'l	2.4	3.4		2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil		0.2	0.4		0.25	0.4	V
				Com'l		0.2	0.4		0.35	0.5	V
			I_{OL} = 4mA	74LS					0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					– 1.5			– 1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V	All inputs '90			1.0				mA
			V_I = 7.0V	MR, MS inputs						0.1	mA
			V_I = 5.5V	$\overline{CP}_0$ input						0.2	mA
				$\overline{CP}_1$ input						0.4	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX	V_I = 2.4V	MR, MS inputs			40				μA
				$\overline{CP}_0$ input			80				μA
				$\overline{CP}_1$ input			160				μA
			V_I = 2.7V	MR, MS inputs						20	μA
				$\overline{CP}_0$ input[5]						40	μA
				$\overline{CP}_1$ input[5]						80	μA
I_{IL}	LOW-level input current	V_{CC} = MAX	V_I = 0.4V	MR, MS inputs			– 1.6			– 0.4	mA
				$\overline{CP}_0$ input			– 3.2			– 2.4	mA
				$\overline{CP}_1$ input			– 6.4			– 3.2	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		Mil	– 20		– 55	– 20		– 100	mA
				Com'l	– 18		– 55	– 20		– 100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX		Mil		30	46		9	15	mA
				Com'l		30	53		9	15	mA

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. I_{CC} is measured with all outputs open, both MR inputs grounded following momentary connection to 4.5V, and all other inputs grounded.
5. The maximum limit for the 54LS90 only is 80μA for $\overline{CP}_0$ and 160μA for $\overline{CP}_1$ inputs.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54/74		54/74LS		UNIT
			C_L = 15pF, R_L = 400Ω		C_L = 15pF, R_L = 2kΩ		
			Min	Max	Min	Max	
f_{MAX} f_{MAX}	Input count frequency, $\overline{CP}_0$ to Q_0 Input count frequency, $\overline{CP}_1$ to Q_1	Waveform 1	10 10		32 16		MHz
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}_0$ input to Q_0 output	Waveform 1				16 18	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}_1$ input to Q_1 output	Waveform 1				16 21	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}_1$ input to Q_2 output	Waveform 1				32 35	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}_1$ input to Q_3 output	Waveform 1				32 35	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}_0$ input to Q_3 output	Waveform 1		100 100		48 50	ns
t_{PHL}	MR input to any output	Waveform 2				40	ns
t_{PLH}	MS input to Q_0 and Q_3 outputs	Waveform 3				30	ns
t_{PHL}	MS input to Q_1 and Q_2 outputs	Waveform 2				40	ns

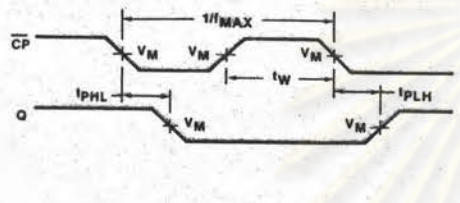
NOTE
Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

AC SETUP REQUIREMENTS $T_A = 25°C$, $V_{CC} = 5.0V$

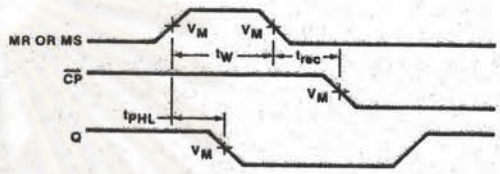
PARAMETER		TEST CONDITIONS	54/74		54/74LS		UNIT
			Min	Max	Min	Max	
t_W	$\overline{CP}_0$ pulse width	Waveform 1	50		15		ns
t_W	$\overline{CP}_1$ pulse width	Waveform 1	50		30		ns
t_W	MS, MR pulse width	Waveform 2	50		15		ns
t_{rec}	Recovery time, MR to $\overline{CP}$	Waveform 2			25		ns
t_{rec}	Recover time, MS to $\overline{CP}$	Waveforms 2 & 3			25		ns

3

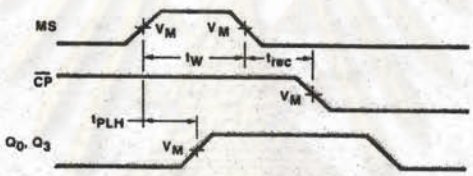
AC WAVEFORMS



Waveform 1



Waveform 2

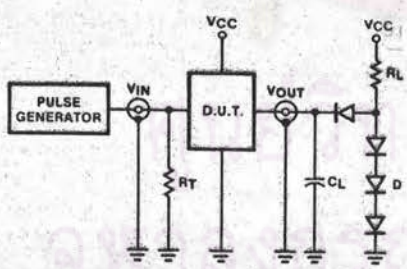


Waveform 3

$V_M = 1.5V$ for 54/74 and 54S/74S; $V_M = 1.3V$ for 54LS/74LS.
The number of Clock Pulses required between the t_{PLH} and t_{PHL} measurements can be determined from the appropriate Function Table.

TEST CIRCUITS AND WAVEFORMS

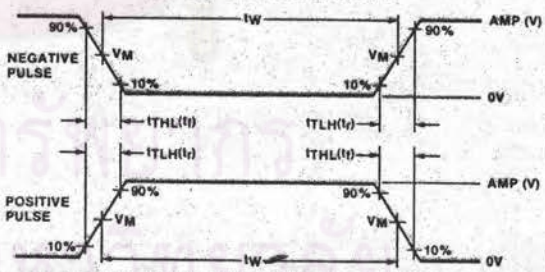
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



$V_M = 1.3V$ for 54LS/74LS; $V_M = 1.5V$ for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

DECODERS/DEMULTIPLEXERS

54/74LS138, S138

1-Of-8 Decoder/Demultiplexer

- **Demultiplexing capability**
- **Multiple input enable for easy expansion**
- **Ideal for memory chip select decoding**
- **Direct replacement for Intel 3205**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74LS138	20ns	6.3mA
74S138	7ns	49mA

DESCRIPTION

The '138 decoder accepts three binary weighted inputs (A_0, A_1, A_2) and when enabled, provides eight mutually exclusive, active LOW outputs ($\overline{0}$–$\overline{7}$). The device features three Enable inputs: two active LOW ($\overline{E}_1$, $\overline{E}_2$) and one active HIGH (E_3). Every output will be HIGH unless $\overline{E}_1$ and $\overline{E}_2$ are LOW and E_3 is HIGH. This multiple enable function allows easy parallel expansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four '138s and one inverter.

The device can be used as an eight output demultiplexer by using one of the active LOW Enable inputs as the Data input and the remaining Enable inputs as strobes. Enable inputs not used must be permanently tied to their appropriate active HIGH or active LOW state.

ORDERING CODE

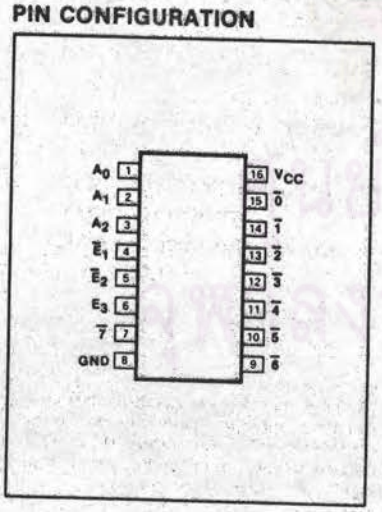
PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74S138N • N74LS138N	
Ceramic DIP	N74S138F • N74LS138F	S54S138F • S54LS138F
Flatpack		S54S138W • S54LS138W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

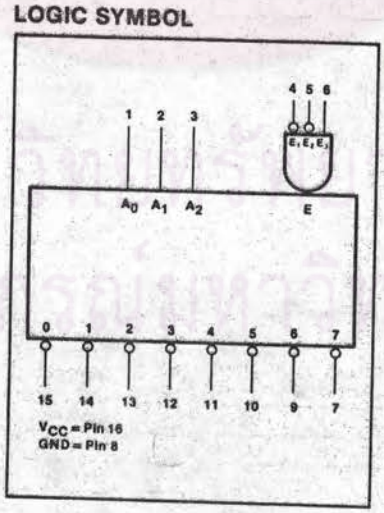
PINS	DESCRIPTION	54/74S	54/74LS
All	Inputs	1Sul	1LSul
All	Outputs	10Sul	10LSul

NOTE
Where a 54/74S unit load (Sul) is 50μA I_{IH} and −2.0mA I_{IL}, and a 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

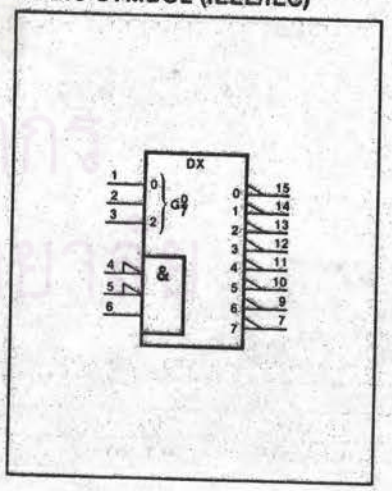
PIN CONFIGURATION



LOGIC SYMBOL

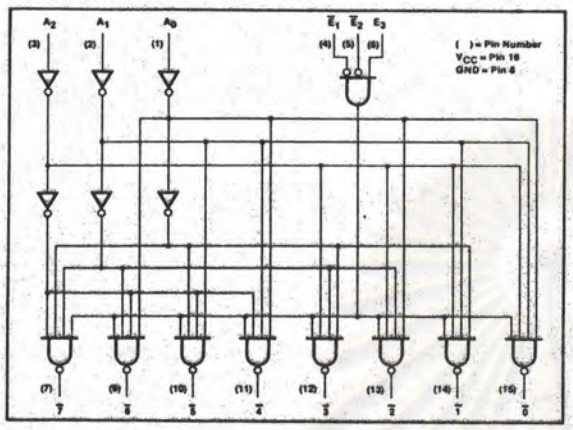


LOGIC SYMBOL (IEEE/IEC)



DECODERS/DEMULTIPLEXERS 54/74LS138, S138

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS						OUTPUTS							
$\overline{E}_1$	$\overline{E}_2$	E_3	A_0	A_1	A_2	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$	$\overline{4}$	$\overline{5}$	$\overline{6}$	$\overline{7}$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

NOTES
H = HIGH voltage level
L = LOW voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54LS	54S	74LS	74S	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +1	−30 to +5	−30 to +1	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125		0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74LS			54/74S			UNIT
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.7			+0.8	V
		Com'l			+0.8			+0.8	V
I_{IK}	Input clamp current				−18			−18	mA
I_{OH}	HIGH-level output current				−400			−1000	μA
I_{OL}	LOW-level output current	Mil			4			20	mA
		Com'l			8			20	mA
T_A	Operating free-air temperature	Mil	−55		+125	−55		+125	°C
		Com'l	0		70	0		70	°C

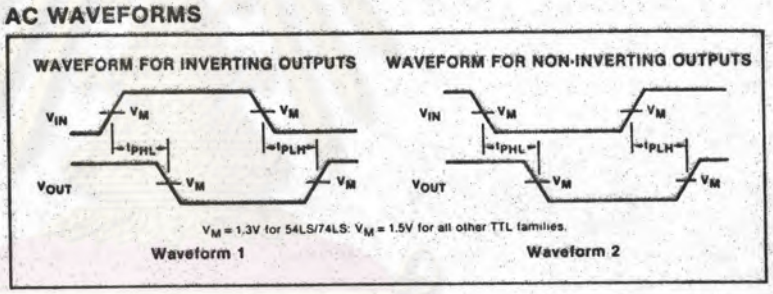
NOTE
V_{IL} = +0.7V MAX for 54S at T_A = +125°C only.

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74LS138			54/74S138			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	2.5	3.4		2.5	3.4		V
				Com'l	2.7	3.4		2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil		0.25	0.4			0.5[5]	V
				Com'l		0.35	0.5			0.5	V
			I_{OL} = 4mA	74LS		0.25	0.4				V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					– 1.5			– 1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V							1.0	mA
			V_I = 7.0V				0.1				mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V					20			50	μA
I_{IL}	LOW-level input current	V_{CC} = MAX	V_I = 0.4V				– 0.4				mA
			V_I = 0.5V							– 2	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			– 20		– 100	– 40		– 100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX				6.3	10		49	74	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. To measure I_{CC}, outputs must be enabled and open.
5. V_{OL} = +0.45V MAX for 54S at T_A = +125°C only.

AC WAVEFORMS

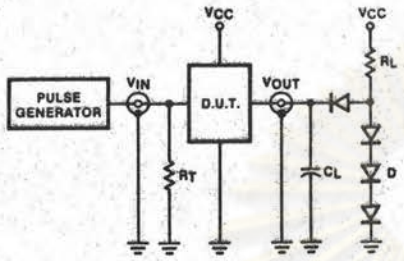


AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54/74LS		54/74S		UNIT
			C_L = 15pF, R_L = 2kΩ		C_L = 15pF, R_L = 280Ω		
			Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay Address to output	Waveform 2 2 logic levels		20 41		7 10.5	ns
t_{PLH} t_{PHL}	Propagation delay Address to output	Waveform 1 3 logic levels		27 39		12 12	ns
t_{PLH} t_{PHL}	Propagation delay Enable to output	Waveform 2 2 logic levels		18 32		8 11	ns
t_{PLH} t_{PHL}	Propagation delay Enable to output	Waveform 1 3 logic levels		26 38		11 11	ns

TEST CIRCUITS AND WAVEFORMS

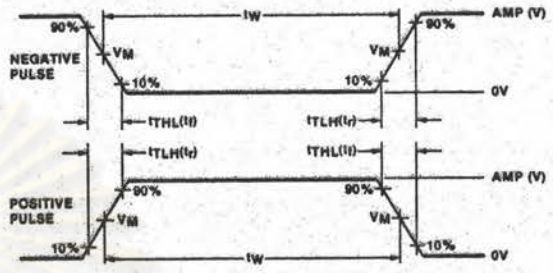
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

COUNTERS

54/74192, 54/74193, LS192, LS193

'192 Presettable BCD Decade Up/Down Counter
'193 Presettable 4-Bit Binary Up/Down Counter

- **Synchronous reversible 4-bit binary counting**
- **Asynchronous parallel load**
- **Asynchronous reset (clear)**
- **Expandable without external logic**

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT
74192	32MHz	65mA
74LS192	32MHz	19mA
74193	32MHz	65mA
74LS193	32MHz	19mA

3

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ± 5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ± 10%; T_A = −55°C to +125°C
Plastic DIP	N74192N • N74LS192N N74193N • N74LS193N	
Ceramic DIP	N74192F • N74LS192F N74193F • N74LS193F	S54LS192F S54193F • S54LS193F
Flatpack		S54LS192W S54193W • S54LS193W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74	54/74LS
All	Inputs	1ul	1LSul
All	Outputs	10ul	10LSul

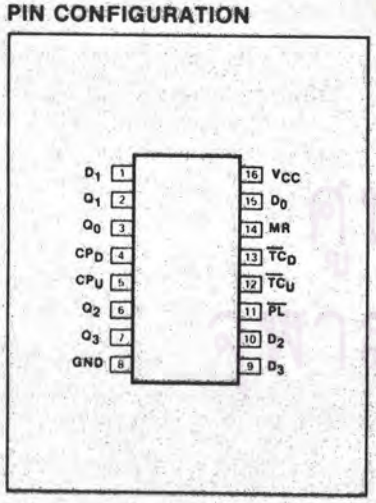
NOTE
Where a 54/74 unit load (ul) is understood to be 40μA I_{IH} and − 1.6mA I_{IL}, and a 54/74LS unit load (LSul) is 20μA I_{IH} and − 0.4mA I_{IL}.

Inside the device are four master-slave JK flip-flops with the necessary steering logic to provide the asynchronous reset, load, and synchronous count up and count down functions.

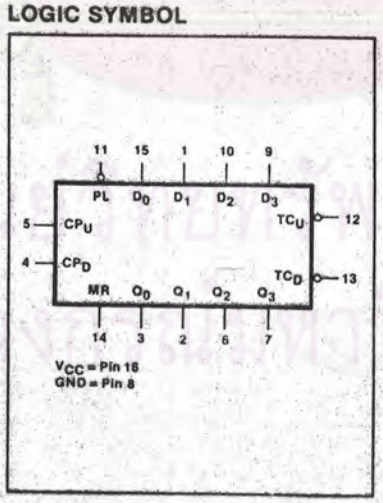
Each flip-flop contains JK feedback from slave to master, such that a LOW-to-HIGH transition on the CP_D input will decrease the count by one, while a similar transition on the CP_U input will advance the count by one.

One clock should be held HIGH while counting with the other, because the circuit will either count by two's or not at all, depending on the state of the first flip-flop, which cannot toggle as long as either Clock input is LOW. Applications requiring reversible operation must make the reversing decision while the activating clock is HIGH to avoid erroneous counts.

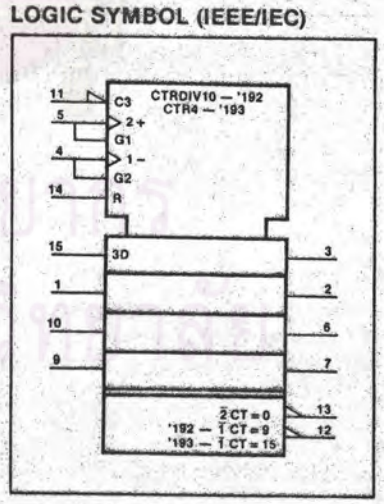
PIN CONFIGURATION



LOGIC SYMBOL

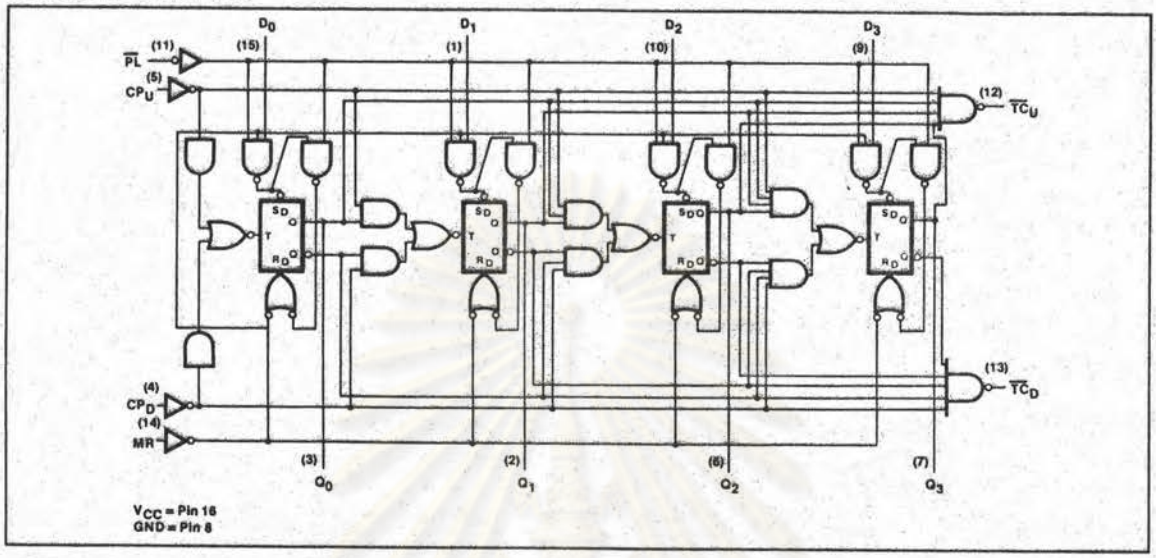


LOGIC SYMBOL (IEEE/IEC)

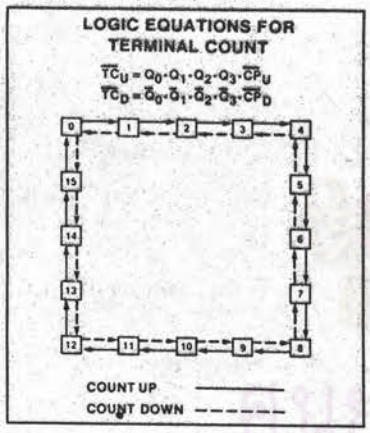


Signetics

LOGIC DIAGRAM, '193



STATE DIAGRAM, '193



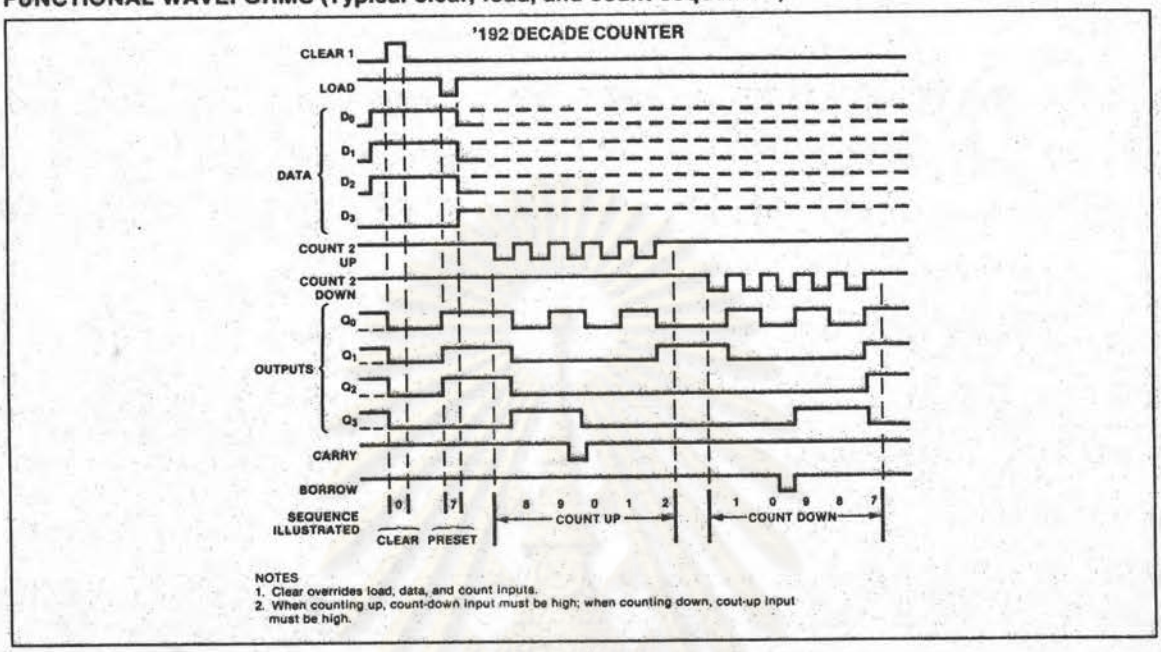
MODE SELECT—FUNCTION TABLE, '193

OPERATING MODE	INPUTS								OUTPUTS					
	MR	PL	CP_U	CP_D	D_0	D_1	D_2	D_3	Q_0	Q_1	Q_2	Q_3	$\overline{TC}_U$	$\overline{TC}_D$
Reset clear)	H	X	X	L	X	X	X	X	L	L	L	L	H	L
	H	X	X	H	X	X	X	X	L	L	L	L	H	H
Parallel load	L	L	X	L	L	L	L	L	L	L	L	L	H	L
	L	L	X	H	L	L	L	L	L	L	L	L	H	H
	L	L	L	X	H	H	H	H	H	H	H	H	L	H
	L	L	H	X	H	H	H	H	H	H	H	H	H	H
Count up	L	H	↑	H	X	X	X	X	Count up				H[c]	H
Count down	L	H	H	↓	X	X	X	X	Count down				H	H[d]

H = HIGH voltage level
L = LOW voltage level
X = Dont' care
↓ = LOW-to-HIGH clock transition

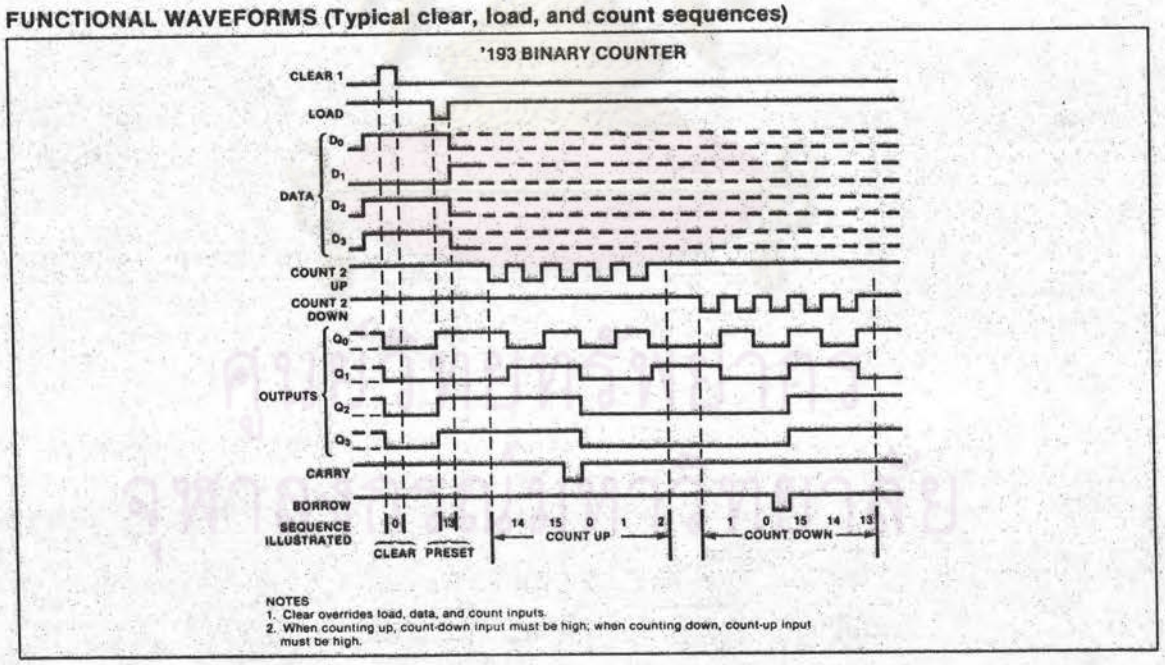
NOTES
c. $TC_U = CP_U$ at terminal count up (HHHH).
d. $TC_D = CP_D$ at terminal count down (LLLL).

FUNCTIONAL WAVEFORMS (Typical clear, load, and count sequences)



NOTES
1. Clear overrides load, data, and count inputs.
2. When counting up, count-down input must be high; when counting down, cout-up input must be high.

FUNCTIONAL WAVEFORMS (Typical clear, load, and count sequences)



NOTES
1. Clear overrides load, data, and count inputs.
2. When counting up, count-down input must be high; when counting down, count-up input must be high.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54	54LS	74	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +1	−30 to +5	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125		0 to 70		°C

3

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74			54/74LS			UNIT
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.8			+0.7	V
		Com'l			+0.8			+0.8	V
I_{IK}	Input clamp current				−12			−18	mA
I_{OH}	HIGH-level output current				−800			−400	mA
I_{OL}	LOW-level output current	Mil			16			4	mA
		Com'l			16			8	mA
T_A	Operating free-air temperature	Mil	−55		+125	−55		+125	°C
		Com'l	0		70	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74192, '193			54/74LS192, '193			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	2.4	3.4		2.5	3.4		V
				Com'l	2.4	3.4		2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil		0.2	0.4		0.25	0.4	V
				Com'l		0.2	0.4		0.35	0.5	V
			I_{OL} = 4mA	74LS					0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					−1.5			−1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V				1.0				mA
			V_I = 7.0V							0.1	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX	V_I = 2.4V				40				μA
			V_I = 2.7V							20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V					−1.6			−0.4	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		Mil	−20		−65	−20		−100	mA
				Com'l	−18		−65	−20		−100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX		Mil		65	89		19	34	mA
				Com'l		65	102		19	34	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure I_{CC} with Parallel Load and Master Reset inputs grounded, all other outputs at 4.5V and all outputs open.

AC CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER		TEST CONDITIONS	54/74 $C_L = 15pF$, $R_L = 400\Omega$		54LS/74LS $C_L = 15pF$, $R_L = 2k\Omega$		UNIT
			Min	Max	Min	Max	
f_{MAX}	Maximum input count frequency	Waveform 1	25		25		MHz
t_{PLH} t_{PHL}	Propagation delay CP_U input to $\overline{TC}_U$ output	Waveform 2		26 24		26 24	ns
t_{PLH} t_{PHL}	Propagation delay CP_D input to $\overline{TC}_D$ output	Waveform 2		24 24		24 24	ns
t_{PLH} t_{PHL}	Propagation delay CP_U or CP_D to Q_n outputs	Waveform 1		38 47		38 47	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ input to Q_n output	Waveform 3		40 40		40 40	ns
t_{PHL}	Propagation delay, MR to output	Waveform 4		35		35	ns

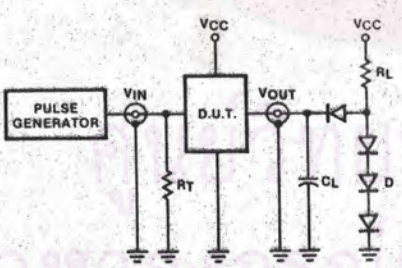
NOTE
Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

AC SETUP REQUIREMENTS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER		TEST CONDITIONS	54/74		54LS/74LS		UNIT
			Min	Max	Min	Max	
t_W	CP_U pulse width	Waveform 1	20		20		ns
t_W	CP_D pulse width	Waveform 1	20		20		ns
t_W	$\overline{PL}$ pulse width	Waveform 3	20		20		ns
t_W	MR pulse width	Waveform 4	20		20		ns
t_s	Setup time, Data to $\overline{PL}$	Waveform 5	20		20		ns
t_h	Hold time, Data to $\overline{PL}$	Waveform 5	0		5		ns
t_{rec}	Recovery time, $\overline{PL}$ to CP	Waveform 3	40		40		ns
t_{rec}	Recovery time, MR to CP	Waveform 4	40		40		ns

TEST CIRCUITS AND WAVEFORMS

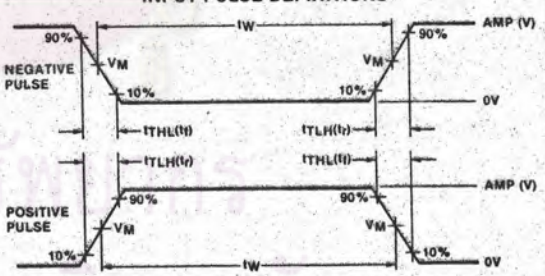
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS

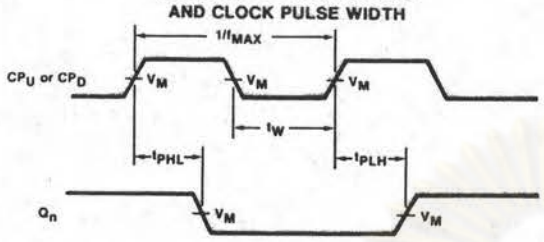


V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

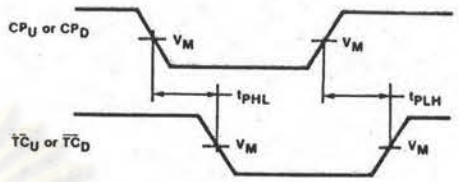
AC WAVEFORMS

CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



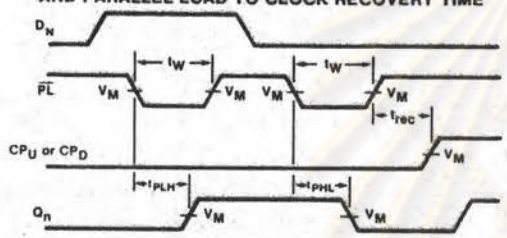
Waveform 1

CLOCK TO TERMINAL COUNT DELAYS



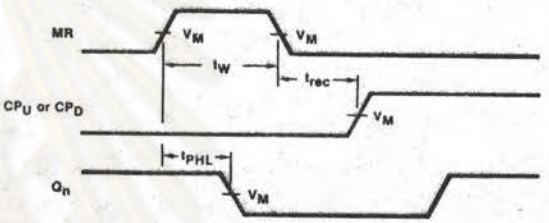
Waveform 2

PARALLEL LOAD PULSE WIDTH, PARALLEL LOAD TO OUTPUT DELAYS, AND PARALLEL LOAD TO CLOCK RECOVERY TIME



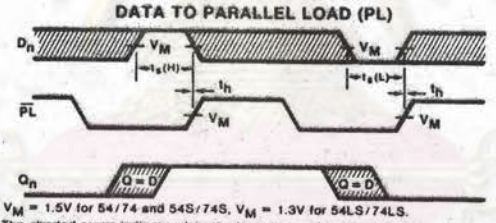
Waveform 3

MASTER RESET PULSE WIDTH, MASTER RESET TO OUTPUT DELAY & MASTER RESET TO CLOCK RECOVERY TIME



Waveform 4

SETUP AND HOLD TIMES DATA TO PARALLEL LOAD (PL)

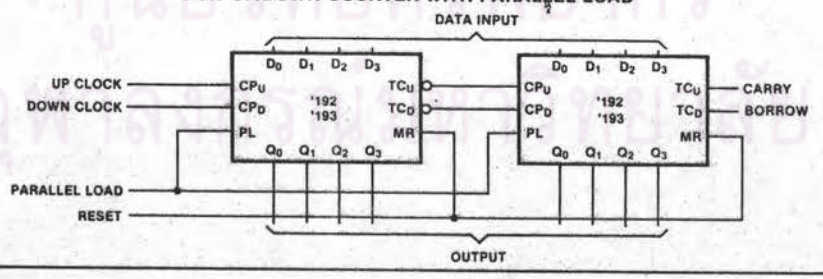


V_M = 1.5V for 54/74 and 54S/74S, V_M = 1.3V for 54LS/74LS.
The shaded areas indicate when the input is permitted to change for predictable output performance.

Waveform 5

APPLICATION

8-BIT UP/DOWN COUNTER WITH PARALLEL LOAD



BUFFERS

54/74LS244, S244

Octal Buffers (3-State)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74LS244	12ns	25mA
74S244	6ns	112mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74LS244N • N74S244N	
Ceramic DIP	74LS244F • N74S244F	S54LS244F • S54S244F

FUNCTION TABLE

INPUTS				OUTPUTS	
$\overline{OE}_a$	I_a	$\overline{OE}_b$	I_b	Y_a	Y_b
L	L	L	L	L	L
L	H	L	H	H	H
H	X	H	X	(Z)	(Z)

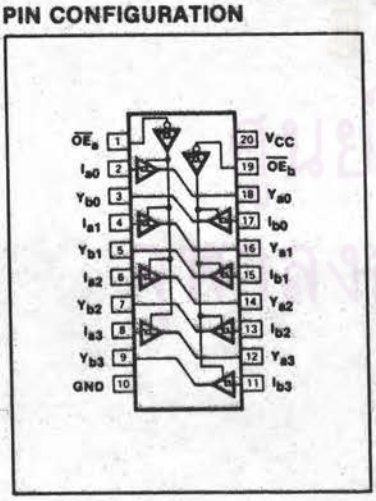
H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = HIGH impedance (off) state

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

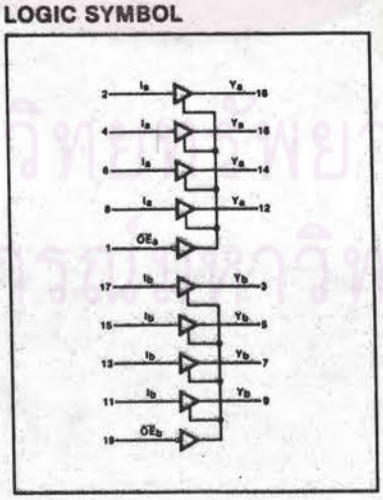
PINS	DESCRIPTION	54/74S	54/74LS
All	Inputs	1Sul	1LSul
All	Outputs	24Sul	30LSul

NOTE
A 54/74S unit load (Sul) is 50μA I_{IH} and −2.0mA I_{IL}, and a 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

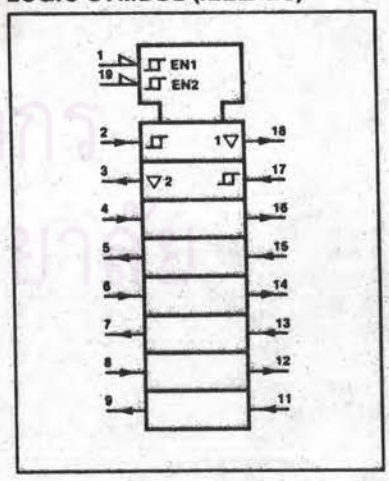
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54LS	54S	74LS	74S	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +1	−30 to +5	−30 to +1	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125		0 to 70		°C

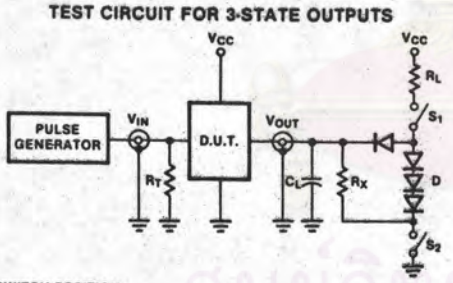
RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74LS			54/74S			UNIT
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.7			+0.8	V
		Com'l			+0.8			+0.8	V
I_{IK}	Input clamp current				−18			−18	mA
I_{OH}	HIGH-level output current	Mil			−12			−12	mA
		Com'l			−15			−15	mA
I_{OL}	LOW-level output current	Mil			12			48	mA
		Com'l			24			64	mA
T_A	Operating free-air temperature	Mil	−55		+125	−55		+125	°C
		Com'l	0		70	0		70	°C

NOTE
V_{IL} = +0.7V MAX for 54S at T_A = +125°C only.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS

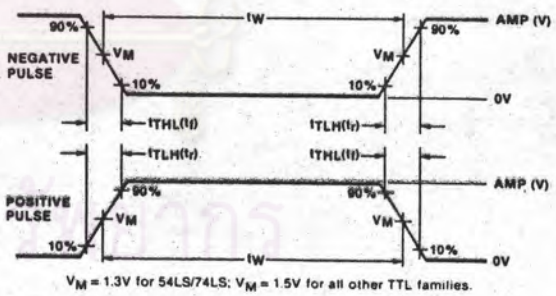


SWITCH POSITION

Test	Switch 1	Switch 2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed

DEFINITIONS
R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
R_X = 1kΩ for 54/74, 54S/74S. R_X = 5kΩ for 54LS/74LS.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS[1]			54/74LS244			54/74S244			UNIT
				Min	Typ[2]	Max	Min	Typ[2]	Max	
ΔV_T Hysteresis ($V_{T+}-V_{T-}$)	V_{CC} = MIN			0.2	0.4		0.2	0.4		V
V_{OH} HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = 0.5V, I_{OH} = MAX			2.0			2.0			V
	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = −3mA			2.4	3.4		2.4			V
V_{OL} LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil			0.4			0.55	V
			Com'l			0.5			0.55	V
		I_{OL} = 12mA	74LS			0.4				V
V_{IK} Input clamp voltage	V_{CC} = MIN, $I_I = I_{IK}$					−1.5			−1.2	V
I_{OZH} Off-state output current, HIGH-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_{IL} = MAX	V_O = 2.7V				20				μA
		V_O = 2.4V							50	μA
I_{OZL} Off-state output current, LOW-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_{IL} = MAX	V_O = 0.4V				−20				μA
		V_O = 0.5V							−50	μA
I_I Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V							1.0	mA
		V_I = 7.0V				0.1				mA
I_{IH} HIGH-level input current	V_{CC} = MAX, V_I = 2.7V					20			50	μA
I_{IL} LOW-level input current	V_{CC} = MAX	V_I = 0.4V				−0.2				mA
		V_I = 0.5V	$\overline{OE}$ inputs						−2.0	mA
			Other inputs						−0.4	mA
I_{OS} Short-circuit output current[3]	V_{CC} = MAX			−40		−130	−50		−130	mA
I_{CC} Supply current[4] (total)	V_{CC} = MAX	I_{CCH} Outputs HIGH	Mil		17	27		95	147	mA
			Com'l		17	27		95	160	mA
		I_{CCL} Outputs LOW	Mil		27	46		120	170	mA
			Com'l		27	46		120	180	mA
		I_{CCZ} Outputs OFF	Mil		32	54		120	170	mA
			Com'l		32	54		120	180	mA

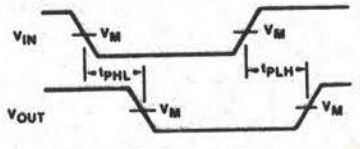
NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and $V_{CC} = V_{CC}$ MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. I_{CC} is measured with outputs open.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	54LS/74LS		54S/74S		UNIT
		C_L = 45pF, R_L = 667Ω		C_L = 50pF, R_L = 90Ω		
		Min	Max	Min	Max	
t_{PLH} Propagation delay	Waveform 1		18		9	ns
t_{PHL} Propagation delay	Waveform 1		18		9	ns
t_{PZH} Enable to HIGH	Waveform 2		23		12	ns
t_{PZL} Enable to LOW	Waveform 3		30		15	ns
t_{PHZ} Disable from HIGH	Waveform 2, C_L = 5pF		18		9	ns
t_{PLZ} Disable from LOW	Waveform 3, C_L = 5pF		25		15	ns

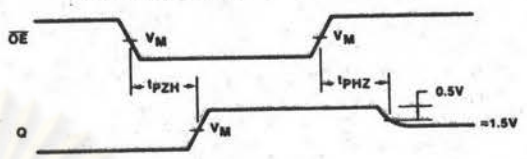
AC WAVEFORMS

WAVEFORM FOR NON-INVERTING OUTPUTS



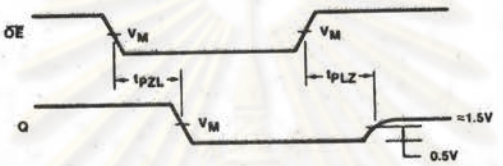
Waveform 1

3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL



Waveform 2

3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL



Waveform 3

V_M = 1.3V for 54LS/74LS, V_M = 1.5V for all other TTL families.

TRANSCEIVER

54/74LS245

Octal Transceiver (3-State)

- **Octal bidirectional bus interface**
- **3-State buffer outputs**
- **PNP inputs for reduced loading**
- **Hysteresis on all Data inputs**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74LS245	8ns	58mA

DESCRIPTION

The 'LS245 is an octal transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. The outputs are all capable of sinking 24mA and sourcing up to 15mA, producing very good capacitive drive characteristics. The device features a Chip Enable (CE) input for easy cascading and a Send/Receive (S/R) input for direction control. All Data inputs have hysteresis built in to minimize ac noise effects.

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74LS245N	
Ceramic DIP	N74LS245F	S54LS245F

FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
$\overline{CE}$	S/$\overline{R}$	A_n	B_n
L	L	A = B	INPUTS
L	H	INPUT	B = A
H	X	(Z)	(Z)

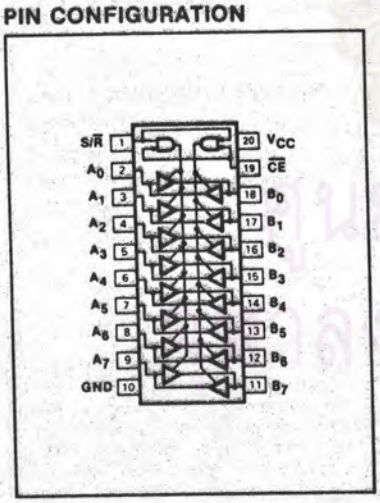
H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = HIGH impedance "off" state

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

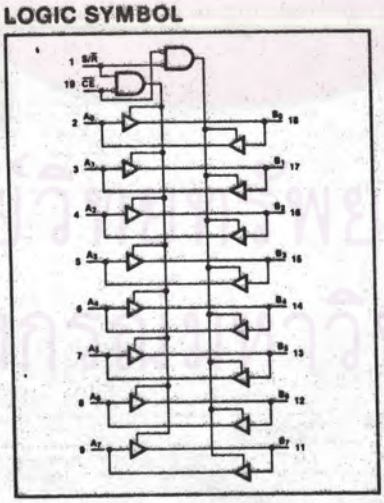
PINS	DESCRIPTION	54/74LS
All	Inputs	1LSul
All	Outputs	30LSul

NOTE
A 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

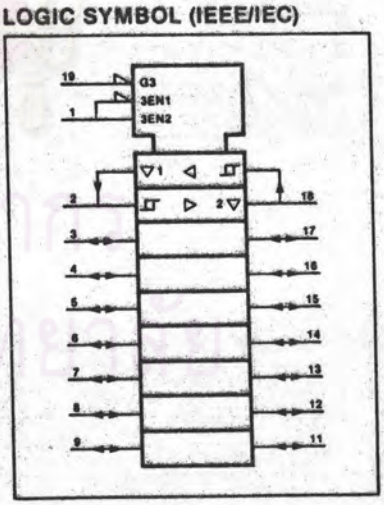
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



TRANSCEIVER 54/74LS245

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54LS	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +1	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

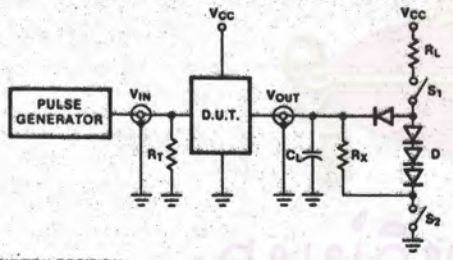
NOTE
V_{IN} limited to 5.5V on A and B inputs only.

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74LS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.7	V
		Com'l			+0.8	V
I_{IH}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current	Mil			−12	mA
		Com'l			−15	mA
I_{OL}	LOW-level output current	Mil			12	mA
		Com'l			24	mA
T_A	Operating free-air temperature	Mil	−55		+125	°C
		Com'l	0		70	°C

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS

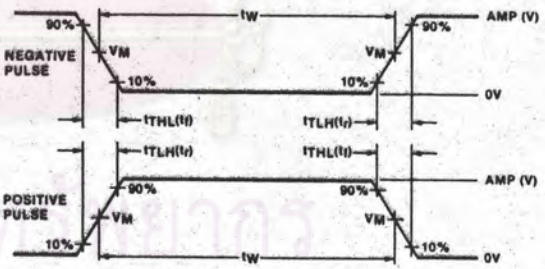


SWITCH POSITION

Test	Switch 1	Switch 2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed

DEFINITIONS
R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
R_X = 1kΩ for 54/74, 54S/74S, R_X = 5kΩ for 54LS/74LS.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

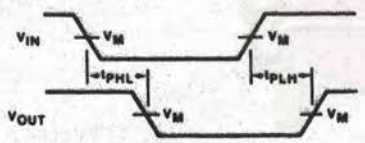
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74LS245 Min	54/74LS245 Typ[2]	54/74LS245 Max	UNIT
ΔV_T	Hysteresis (V_{T+}-V_{T-})	V_{CC} = MIN			0.2	0.4		V
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OH} = MAX		2.0			V
			I_{OH} = −3mA		2.4	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil			0.4	V
				Com'l			0.5	V
			I_{OL} = 12mA	74LS			0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					−1.5	V
I_{OZH}	Off-state output current, HIGH-level voltage applied	V_{CC} = MAX, V_O = 2.7V, $\overline{CE}$ = 2.0V					20	μA
I_{OZL}	Off-state output current, LOW-level voltage applied	V_{CC} = MAX, V_O = 0.4V, $\overline{CE}$ = 2.0V					−200	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V	A, B inputs			0.1	mA
			V_I = 7.0V	S/$\overline{R}$, $\overline{CE}$ inputs			0.1	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V					−0.2	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			−40		−130	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX	I_{CCH}	Outputs HIGH		48	70	mA
			I_{CCL}	Outputs LOW		62	90	mA
			I_{CCZ}	Outputs OFF		64	95	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure I_{CC} with outputs open.

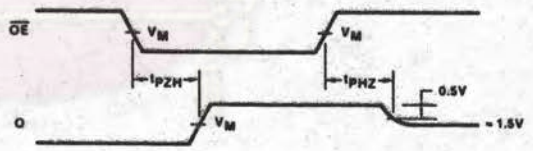
AC WAVEFORMS

WAVEFORM FOR NON-INVERTING OUTPUTS



Waveform 1

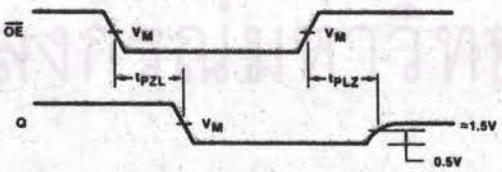
3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL



Waveform 2

V_M = 1.3V for 54LS/74LS. V_M = 1.5V for all other TTL families

3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL



Waveform 3

AC CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER		TEST CONDITIONS	54LS/74LS $C_L = 45pF$, $R_L = 667\Omega$		UNIT
			Min	Max	
t_{PLH}	Propagation delay	Waveform 1		12	ns
t_{PHL}	Propagation delay	Waveform 1		12	ns
t_{PZH}	Enable to HIGH	Waveform 2		40	ns
t_{PZL}	Enable to LOW	Waveform 3		40	ns
t_{PHZ}	Disable from HIGH	Waveform 2, $C_L = 5pF$		25	ns
t_{PLZ}	Disable from LOW	Waveform 3, $C_L = 5pF$		25	ns

LATCHES/FLIP-FLOPS

54/74LS373, 54/74LS374, S373, S374

'373 Octal Transparent Latch With 3-State Outputs
'374 Octal D Flip-Flop With 3-State Outputs

- 8-bit transparent latch — '373
- 8-bit positive, edge-triggered register — '374
- 3-State output buffers
- Common 3-State Output Enable
- Independent register and 3-State buffer operation

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74LS373	19ns	24mA
74S373	10ns	105mA
74LS374	19ns	27mA
74S374	8ns	116mA

3

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic	N74LS373N • N74S373N N74LS374N • N74S374N	
Ceramic DIP	N74LS373F • N74S373F N74LS374F • N74S374F	S54LS373F • S54S373F S54LS374F • S54S374F

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74S	54/74LS
All	Inputs	1Sul	1LSul
All	Outputs	10Sul	30LSul

NOTE
Where a 54/74S unit load (Sul) is 50μA I_{IH} and −2.0mA I_{IL}, and a 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

DESCRIPTION

The '373 is an octal transparent latch coupled to eight 3-State output buffers. The two sections of the device are controlled independently by Latch Enable (E) and Output Enable ($\overline{OE}$) control gates.

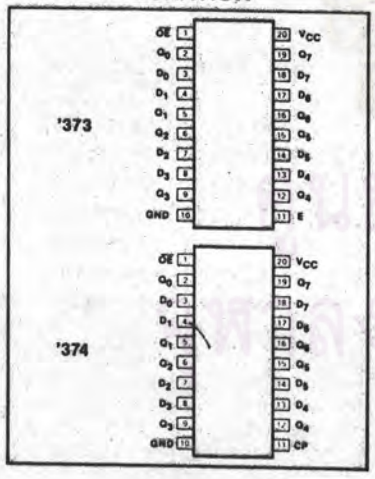
The data on the D inputs are transferred to the latch outputs when the Latch Enable (E) input is HIGH. The latch remains transparent to the data inputs while E is HIGH, and stores the data present one setup time before the HIGH-to-LOW enable transition. The enable gate has about 400mV of hysteresis built in to help minimize problems that signal and ground noise can cause on the latching operation.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active LOW Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the latch operation. When $\overline{OE}$ is LOW, the latched or transparent data appears at the outputs. When $\overline{OE}$ is HIGH, the outputs are in the HIGH impedance "off" state, which means they will neither drive nor load the bus.

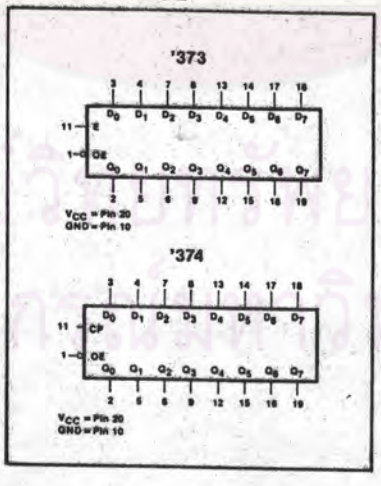
The '374 is an 8-bit, edge-triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by the Clock (CP) and Output Enable ($\overline{OE}$) control gates.

The register is fully edge triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output. The clock buffer has about 400mV of hysteresis built in to help minimize problems that signal and ground noise can cause on the clocking operation.

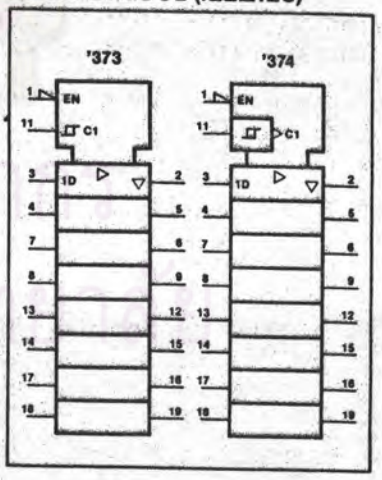
PIN CONFIGURATION



LOGIC SYMBOL



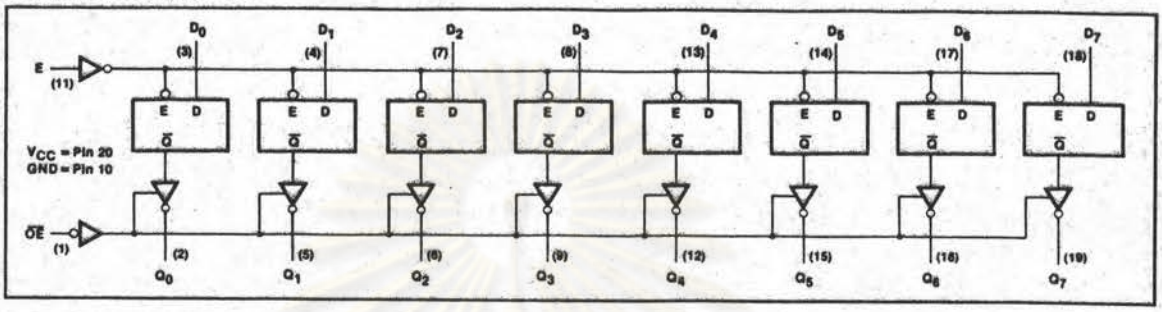
LOGIC SYMBOL (IEEE/IEC)



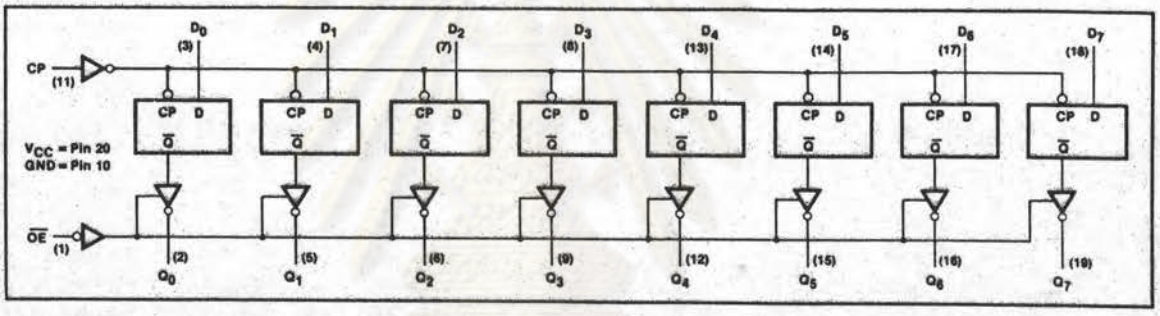
Signetics

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active LOW Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the register operation. When $\overline{OE}$ is LOW, the data in the register appears at the outputs. When $\overline{OE}$ is HIGH, the outputs are in the HIGH impedance "off" state, which means they will neither drive nor load the bus.

LOGIC DIAGRAM, '373



LOGIC DIAGRAM, '374



MODE SELECT—FUNCTION TABLE, '373

OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS
	$\overline{OE}$	E	D_n		Q_0–Q_7
Enable and read register	L	H	L	L	L
	L	H	H	H	H
Latch and read register	L	L	l	L	L
	L	L	h	H	H
Latch register and disable outputs	H	L	l	L	(Z)
	H	L	h	H	(Z)

MODE SELECT—FUNCTION TABLE, '374

OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS
	$\overline{OE}$	CP	D_n		Q_0–Q_7
Load and read register	L	↑	l	L	L
	L	↑	h	H	H
Load register and disable outputs	H	↑	l	L	(Z)
	H	↑	h	H	(Z)

H = HIGH voltage level
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition or HIGH-to-LOW $\overline{OE}$ transition
L = LOW voltage level
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition or HIGH-to-LOW $\overline{OE}$ transition
(Z) = HIGH impedance "off" state
↑ = LOW-to-HIGH clock transition

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54LS	54S	74LS	74S	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +1	−30 to +5	−30 to +1	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state.	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125		0 to 70		°C

3

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74LS			54/74S			UNIT
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.7			+0.8	V
		Com'l			+0.8			+0.8	V
I_{IK}	Input clamp current				−18			−18	mA
I_{OH}	HIGH-level output current	Mil			−1.0			−2.0	mA
		Com'l			−2.6			−6.5	mA
I_{OL}	LOW-level output current	Mil			12			20	mA
		Com'l			24			20	mA
T_A	Operating free-air temperature	Mil	−55		+125	−55		+125	°C
		Com'l	0		70	0		70	°C

NOTE
V_{IL} = +0.7V MAX for 54S at T_A = +125°C only.

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74LS373, 374			54/74S373, 374			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	2.4	3.4		2.4	3.0		V
				Com'l	2.4	3.1		2.4	3.1		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil		0.25	0.4			0.5[4]	V
				Com'l		0.35	0.5			0.5	V
			I_{OL} = 12mA	74LS		0.25	0.4				V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					– 1.5			– 1.2	V
I_{OZH}	Off-state output current, HIGH-level voltage applied	V_{CC} = MAX, V_{IH} = MIN	V_O = 2.7V				20				μA
			V_O = 2.4V							50	μA
I_{OZL}	Off-state output current, LOW-level voltage applied	V_{CC} = MAX, V_{IH} = MIN	V_O = 0.4V				– 20				μA
			V_O = 0.5V							– 50	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 7.0V				0.1				mA
			V_I = 5.5V							1.0	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V					20			50	μA
I_{IL}	LOW-level input current	V_{CC} = MAX	V_I = 0.4V				– 0.4				mA
			V_I = 0.5V							– 0.25	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			– 30		– 130	– 40		– 100	mA
I_{CC}	Supply current (total)	V_{CC} = MAX	I_{CCZ}	$\overline{OE}$ = 4.5V 'LS373		24	40				mA
			I_{CCL}	$\overline{OE}$ = 0V 'S373					105	160	mA
			I_{CCZ}	$\overline{OE}$ = 4.5V 'LS374		27	40				mA
			I_{CCL}	All inputs grounded 'S374					102	140	mA
			I_{CCZ}	CP, $\overline{OE}$ = 4.5V, D inputs = GND 'S374					131	180	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. V_{OL} = + 0.45V MAX for 54S at T_A = + 125°C only.

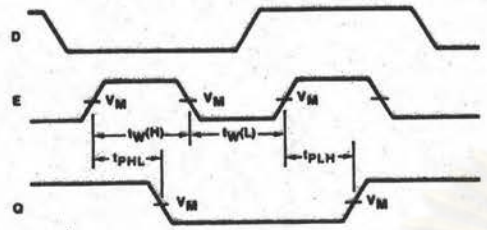
AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54/74LS		54/74S		UNIT
			C_L = 45pF, R_L = 667Ω		C_L = 15pF, R_L = 280Ω		
			Min	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 6, '374	35		75		MHz
t_{PLH} t_{PHL}	Propagation delay Latch Enable to output	Waveform 1, '373		30 30		14 18	ns
t_{PLH} t_{PHL}	Propagation delay Data to output	Waveform 4, '373		18 18		12 12	ns
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 6, '374		28 28		15 17	ns
t_{PZH}	Enable time to HIGH level	Waveform 2		28		15	ns
t_{PZL}	Enable time to LOW level	Waveform 3, '373 '374		36 28		18 18	ns
t_{PHZ}	Disable time from HIGH level	Waveform 2, C_L = 5pF		20		9	ns
t_{PLZ}	Disable time from LOW level	Waveform 3, C_L = 5pF		25		12	ns

NOTE
Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

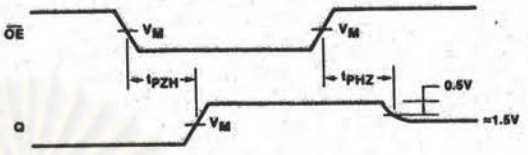
AC WAVEFORMS

LATCH ENABLE TO OUTPUT DELAYS AND LATCH ENABLE PULSE WIDTH



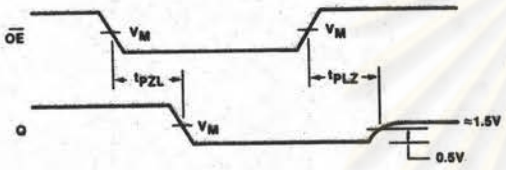
Waveform 1

3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL



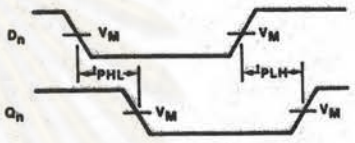
Waveform 2

3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL



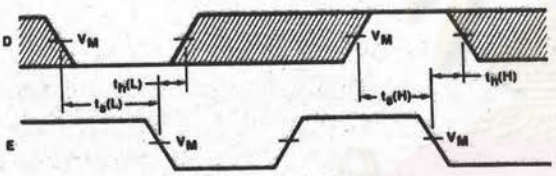
Waveform 3

PROPAGATION DELAY DATA TO Q OUTPUTS



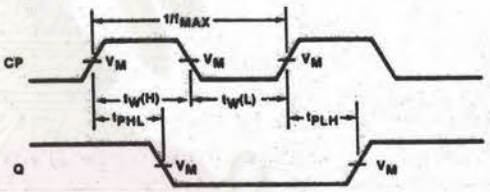
Waveform 4

DATA SETUP AND HOLD TIMES



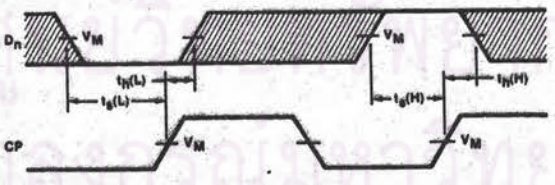
Waveform 5

CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



Waveform 6

DATA SETUP AND HOLD TIMES



Waveform 7

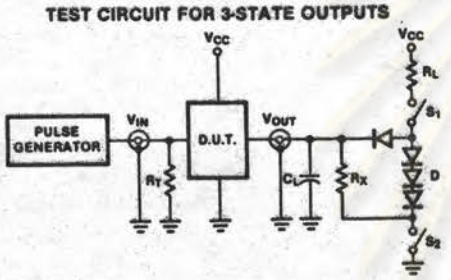
V_M = 1.5V for 54/74 and 54S/74S, V_M = 1.3V for 54LS/74LS.
The shaded areas indicate when the input is permitted to change for predictable output performance.

AC SETUP REQUIREMENTS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER		TEST CONDITIONS	54/74LS		54/74S		UNIT
			Min	Max	Min	Max	
$t_{W(H)}$ $t_{W(L)}$	Latch Enable pulse width	Waveform 1, '373	15 15		6 7.3		ns
t_s	Setup time, Data to Latch Enable	Waveform 5, '373	5		0		ns
t_h	Hold time, Data to Latch Enable	Waveform 5, '373	20		10		ns
$t_{W(H)}$ $t_{W(L)}$	Clock pulse width	Waveform 6, '374	15 15		6 7.3		ns
t_s	Setup time, Data to Clock	Waveform 7, '374	20		5		ns
t_h	Hold time, Data to Clock	Waveform 7, '374	0		2		ns

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS



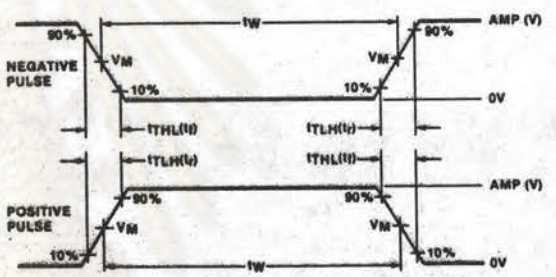
SWITCH POSITION

Test	Switch 1	Switch 2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
R_X = 1kΩ for 54/74, 54S/74S; R_X = 5kΩ for 54LS/74LS.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

ประวัติผู้เขียน

นาย พรยุทธ ชินมหาวงศ์ เกิดเมื่อวันที่ 16 เมษายน พ.ศ. 2501 ที่อำเภอบัวใหญ่ จังหวัดนครราชสีมา สำเร็จการศึกษาระดับปริญญาบัณฑิต จากภาควิชา ฟิสิกส์ คณะวิทยาศาสตร์ มหาวิทยาลัยเชียงใหม่ เมื่อ ปี พ.ศ. 2523 แล้วเข้าศึกษาต่อในระดับปริญญามหาบัณฑิต สาขา นิวเคลียร์เทคโนโลยี คณะวิศวกรรมศาสตร์ จุฬาลงกรณ์มหาวิทยาลัย ขณะที่ศึกษาอยู่ได้ทำงานอยู่ที่ บริษัท ซิกเนติกส์ ไทยแลนด์จำกัด ตำแหน่ง วิศวกรควบคุมคุณภาพ