CHAPTER 3

DESIGN CRITERIONS

The first step in the design of a converter is to specify the input-output voltage and the output power. Only the input current must be calculated. This can be found by assuming a value of efficiency and applying it to the output power. In general, an efficiency of 80% is assumed, which turn out to be quite close to that actually obtained for a well designed converter.

$$P_{in} = \frac{P_{out}}{\eta}$$

$$I_C = \frac{P_{in}}{V_{in}}$$

where η is the assumed overall efficiency.

3.1 Transistor Selection

The transistor type selected must be capable of carrying maximum collector current (I_C). The transistor must have collector- emitter breakdown in excess of the OFF voltage, which is approximately twice supply voltage. Additionally there should be some allowance for transients of input voltage. Consequently, collector- emitter breakdown voltage three times supply voltage is recommended. Emitter- base breakdown voltage must be higher than feedback voltage. The transistor must have sufficient safe operating area that operating load lines are well within device capabilities.

Transistor power losses limit overall efficiency. Factors influencing these losses should be a transistor selection criterion. Transistor losses normally consist of collector dissipation ON dissipation and OFF dissipation are usually low, and switching losses predominate, especially at high frequency. Transistor efficiency is maximized by high h_{FE}, low $V_{CE}(sat)$, fast switching response, and low leakage in the OFF condition.

The choice between silicon or germanium transistor is covered by the criterion above. In general, silicon transistors are more temperature stable and can be operated at higher temperature, but they are more expensive and have higher $V_{CE}(sat)$.

After transistor is selected, base current could be determined. A minimum I_B required is I_c/h_{FE}. If gain of transistor changes with temperature or aging, the transistor might operate in active region at the required value of I_c. Then a large amount of power is dissipated in the transistor. Furthermore, when the transistor is ON in the active region, V_{CE} is high. So voltage across the primary of the transformer is reduced. This reduces output voltage and the required output power may not be attained. As a result, additional base current is desirable to drive the transistor well into saturation. Practically the author use

$$\frac{I_C}{I_B} = \frac{h_{FE}\,(min)}{2} \qquad \text{..... (3-3)}$$

Note also that I_B should not be higher than that obtained from eq. (3-3) or loss in R_1 will be high.

3.2 Transformer Consideration

3.2.1 Core The core size selection is somewhat arbitrary, but it should be selected so that the calculated operating frequency (eq. 3-6) lies between 1-15 kHz. The core selected by this criterion yields high efficiency while its size is small.

The core material selection should provide high saturated flux density to decrease core size, square loop hysteresis curve to minimize spikes on the output of the square wave, and low loss for high efficiency of operation. Tape wound toroids of 50-50 nickel-iron are suitable for converter applications but the usefulness is reduced through the need of special winding machine. Owing to simplicity of manipulation ferrite cores in EE, EI and pot forms are widely used.

3.2.2 Flux Density : For self-oscillating converter, maximum flux density, B_{max} , is to be equal to saturated flux density, B_{sat} , so that the converter will oscillate properly. For driven converter, maximum flux density is to be lower than saturated flux density because if B_{max} is designed to be greater than B_{sat} then the converter tends to oscillate with higher frequency than the driver's frequency. As a result, the waveforms are shown in Fig. 7-D and Fig. 7-E. A large portion of operation is in active region and power dissipation loss in transistors arises. To ensure that this will not happen, B_{max} should be 10-20 percent lower than B_{sat}, i.e., the transformer should be designed

to operate as a linear transformer rather than a saturated one.

3.2.3 Frequency : From section 6.1, eq.(6-4), the maximum power handling by a core is

$$P_{max} = 2K_w B_{max} f J W A_{core} \times 10^{-8} \quad \ldots\ldots (3\text{-}4)$$

The losses in ferrite core are predominately due to hysteresis loss which is

$$P_h = f W_h V \times 10^{-7} \quad \ldots\ldots\ldots\ldots\ldots\ldots (3\text{-}5)$$

where $W_h = \frac{1}{4\pi} \oint HdB$

$\oint HdB$ = loop area of B-H curve in gauss-oersted

V = volume of the core in cubic centimeters.

Because for a given value of frequency, losses in a given core are fixed. Thus, efficiency will be maximized when the core handles power equal to P_{max}. At this condition efficiency is independent of frequency because both P_{max} and P_h vary linearly as frequency.

Now we can conclude that the optimum frequency of operation for a given core is: from eq. (3-4)

$$f = \frac{P_{max} \times 10^8}{2K_w B_{max} J W A_{core}} \quad \ldots\ldots\ldots\ldots (3\text{-}6)$$

For ferrite core it is suggested that the core size be selected so that the calculated frequency is found to be in the range of a few kilohertz to about ten kilohertz. If calculated frequency is too low, the selected core size will be big. In this case a smaller core can be replaced without any significant loss of efficiency. On the other hand, if

calculated frequency is higher than 30 kHz, problems of winding might arises because wire size is too big for the core. Additionally, although the efficiency of a converter using ferrite core is independent of frequency (if eq. 3-4 is satisfied), over-all efficiency will decrease at higher frequency due to transistor switching loss. So calculated frequency should be between 1-15 kHz. However, if the core size is to be minimized the frequency can be as high as 50 kHz or more but the core material and transistors must be selected carefully to minimize losses.

3.2.4 Windings : When the core and operating frequency are selected the number of turns can be calculated. Consider the equation for the square-wave voltage:

$$V = 4 f B_{max} A_{core} N \times 10^{-8} \quad \text{.....(3-7)}$$

$$\text{Thus} \quad N_1 = \frac{V_{in} \times 10^8}{4f B_{max} A_{core}} \quad \text{.....(3-8)}$$

The transformer equations

$$N_2 = \frac{K_1 V_{out} N_1}{V_{in}} \quad \text{.....(3-9)}$$

$$N_{FB} = \frac{K_1 V_{FB} N_1}{V_{in}} \quad \text{.....(3-10)}$$

where K_1 is a multiplier to compensate for transformer voltage drop and losses. $K_1 = 1.05$ is used in practice.

In selecting the value of current dendity of conductor wire there are some factors to be considered. For a given core, if it is used to handle high power the frequency must be high. Thus, from eqs. (3-8), (3-9), (3-10) a small number

of turns is required. In this condition a high value of curfent density, J, can be selected without significant power loss or voltage drop in wire. On the other hand, if the core is used for lower power handling the frequency is decreased and the number of turns is increased. Now, J must be small or significant power loss and voltage drop in wire will result. The optimum value of J is derived in section 6.3. The result is:

$$J = \left[\frac{2 P_{max} n}{\rho K_w l_w W}\right]^{\frac{1}{2}} \qquad \text{.....(3-11)}$$

For purposes of wire size calculation, duty cycle should be applied to peak winding current to obtain the average current. The duty cycle of N_1 and N_{FB} are 50%, of N_2 is 100%. Bifilar winding is recommended for close magnetic coupling.

3.3 Starting Circuits

R_1 and R_2 form simple voltage divider that properly biases the transistors to initiate oscillation. Without the starting circuit the converter may not oscillate. This is especially true at full load. The base starting bias developed by this circuit should be 0.3 volt for germanium transistors and 0.7 volt for silicon. This voltage is:

$$V_B = \frac{R_1 V_{in}}{R_1 + R_2} \qquad \text{.....(3-12)}$$

R_1 and R_2 can be found from:

$$R_1 = \frac{V_{FB} - V_{BE(sat)}}{I_B} \qquad \text{..... (3-13)}$$

from eq. (3-12)

$$R_2 = R_1\left[\frac{V_{in}}{V_B} - 1\right] \qquad \text{..... (3-14 A)}$$

$$\cong R_1\left[\frac{V_{in}}{V_{BE(sat)}} - 1\right] \qquad \text{..... (3-14 B)}$$

The feedback voltage must be chosen properly. If V_{FB} is too high a large amount of power will dissipate in R_1. If V_{FB} is too low, a large amount of power will dissipate in R_2. The optimum value of V_{FB} is derived in section 6.2. The result is tabulated in the Feedback Voltage Table. If $I_B R_1$ is much smaller than V_{in}, V_{FB} can be found from

$$V_{FB} = \sqrt{V_{in} V_{BE(sat)}} + V_{BE(sat)} \quad \text{.....(3-15)}$$

3.4 Speed-Up Circuit

A capacitor may be used to speed up the switching time of the transistor by connected parallel to R_1. It is especially important at higher frequencies. In the range of 1-15 kHz it contributes only a bit greater efficiency over the case where no capacitor is used. However, at 50 kHz approximately 10% greater efficiency may be obtained through the addition of the capacitor.

3.5 Diode Selection

The diode type selected must capable of maximum output current. It must have inverse breakdown voltage in excess of the output voltage and allowance for transients. The forward voltage drop in each diode should be low. It should have fast switching and low leakage in the OFF condition.