CHAPTER 5

DESIGN AND CONSTRUCTION

5.1 Introduction

A circuit design of a switching regulator dc power supply will be described in the following sections. The required specifications of this regulator are summarized below:

Input

AC input voltage	:	30	Volts
frequency		50	Hz

Output

DC output voltage		5	Volts
DC output rated current		10	Amperes

Regulation

Load regulation	$\leq$	1.5 %	(half load to full load)
line regulation	$\leq$	1.5 %	

Ripple and Noise

output ripple	$\leq$	60	mV_{pp}
noise attenuation	$\leq$	-40	dB at 10 MHz
Recovery time	<	10	microsecond
Ambient Temperature		0-70	°C
Efficiency	>	70%	

5.2 Radio Noise Filter Circuit

In general, most designers select the values of

the cutoff frequency, f_o 10 KHz,

the damping ratio d 0.01.

When the input current is about 1.5 amperes, the load resistance can be calculated as : R = 30 ohms

From eqns(3.6) and (3.8), the value of L and C can be determined as

$$C = \frac{1}{R\omega d^{1/3}} \quad \text{farad} \qquad (5.1)$$

$$L = \frac{2Rd^{2/3}}{\omega} \quad \text{henry} \qquad (5.2)$$

In this design, we choose

L = 600 micro-henry

C = 1 micro-farad

A typical RF noise filter based on these two values L and C has been constructed. The result of the frequency response of this RF noise filter campared with the theoritical form appendix A is shown in Fig.5.1

It can be seen that the frequency response of the RF noise filter is very close to the theoretical response.

5.3 AC line rectifier

A typical well-known fullwave rectifier circuit shown in Fig.5.2 has been employed. In this circuit, the values of components are listed below:

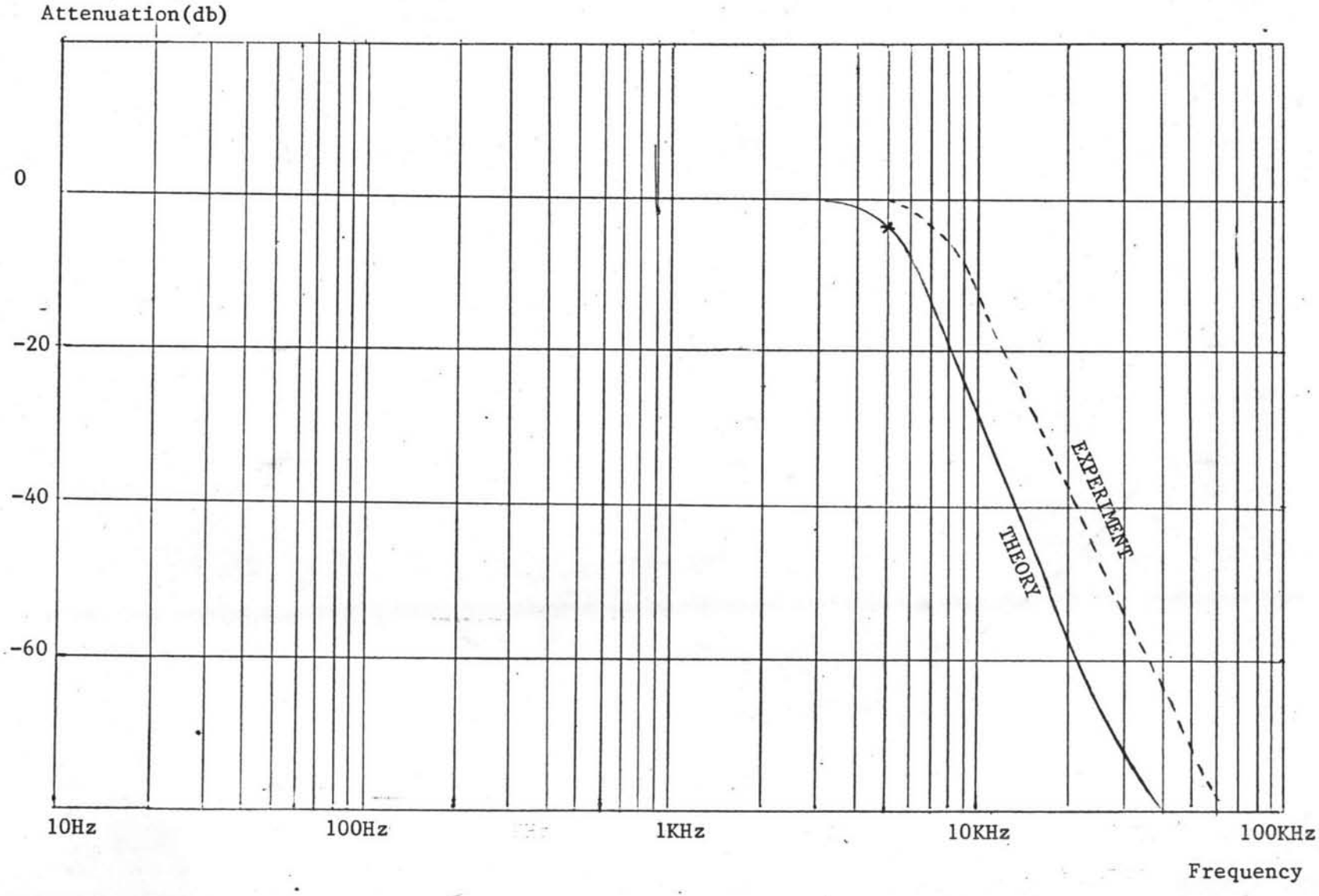

Fig. 5.1 Frequency response of RF noise filter

Diode type RAB 040,3A,400 Volts

Capacitor, C = 3300 micro-farads

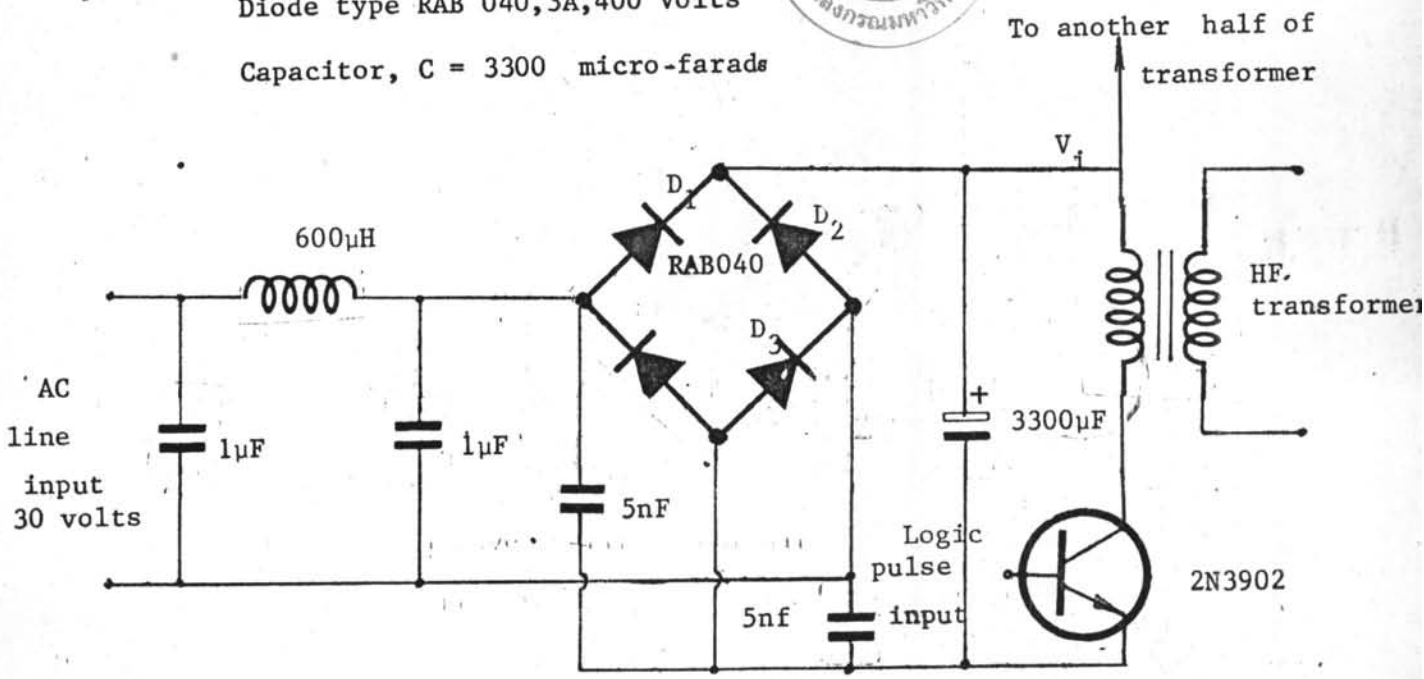

Fig 5.2 Full wave rectifier circuit.

Since the ac line input is 30 volts the output voltage V_i is a approximatly 40 volts and the current is about 2 amperes.

In this design, an additional simple filtering improvement has been combined into the rectifier circuit in order to reduce noise caused by the switching transistors mounted on the heat sink. Two capacitors which have small values 5nf nanofarads have been connected as shown in Fig.5.2

5.4 Power Stage

The power inverter stage is shown in Fig.

5.4.1 Output Filter

A ferrite toroid core has been introduced in the output filter the value of the inductance can be determined from Eqn.(3.19)

$$L = \frac{(E_r - E_o)E_o}{2f\,E_r(I_{max} - I_o)}$$

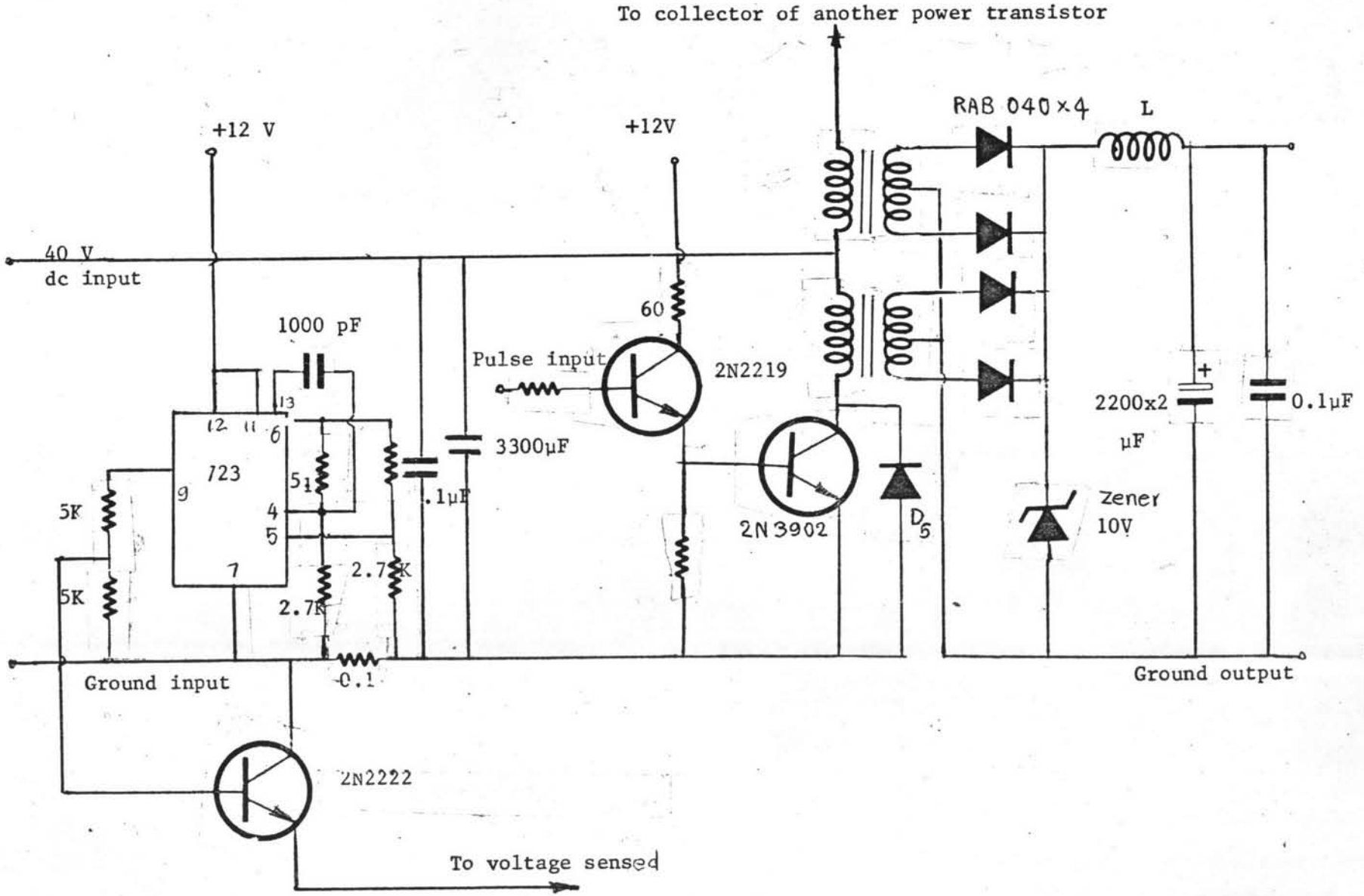

Fig.5.3 Power inverter stage

In this case the maximum current I_{max} is around to be 11 amperes I_o is 9 amperes, and E_r = 10 Volts the value of L will be

$$L \approx 31.25 \quad \text{micro-henry}$$

To avoid the saturation due to high current variations, it is recommended to choose the value of L = 50 micro-henry.

The minimum core size of this choke may be determined from the equation

$$A_F A_W \geq \frac{A_x L I_L \times 10^8}{0.8\, B_m}$$

Where I_L be the saturation current level

A_x be the wire size in unit of circul.

In this, the copper wire number 12 and 6500 circulamil is chosen.

Thus the core size will be

$$A_F A_W \geq \frac{6.5K \times 50\mu \times 10 \times 10^8}{0.8 \times 3700}$$

$$\geq 1.10 \times 10^5 \quad \text{CM } cm^2$$

In this design, a toroid core has the cross-sectional area cm^2 and the window area 4.5 cm^2 (7.0118×10^5 CM). Hence the value of $A_F A_W$ becomes 1.12 10^6 CM cm^2. This value is greater than the value of the calculation 1.10×10^5 CM cm^2. The required number of turns may be determined from the equation

$$N = \frac{L I_L}{A_F B_m} \times 10^8 \quad \text{turns}$$

Choose the cross-sectional area of core 1.6cm^2, thus the numbers of turns will be

$$N = \frac{50 \times 10^{-6} \times 10 \times 10^8}{1.6 \times 3700}$$

$$= 8.44594 \quad \text{turns}$$

It can be seen that the window of the ferrite core is sufficiently for this design.

5.4.2 Filter Capacitance

From eqn.(3.33), and assumed that ΔH is zero. The value of V_{pp} is 60 mV, the value of the filter capacitor can be determined as

$$C \geq \frac{LV_r(I_{max} - I_L)^2}{2V_o(V_r - V_o)(V_{pp} - \Delta H)}$$

$$\geq \frac{50\times10^{-6}\times10(11-10)^2}{2\times10(5)\times60\times10^{-3}}$$

$$C \geq 84 \quad \text{micro farad}$$

In this design, two capacitors which have the value 2200μF each are connected in parallel in the circuit.

5.4.3 Ripple voltage.

The ripple voltage of this power supply is tested on the load of 5 amperes and the result of the peak to peak ripple valtage is shown in Fig 5.4

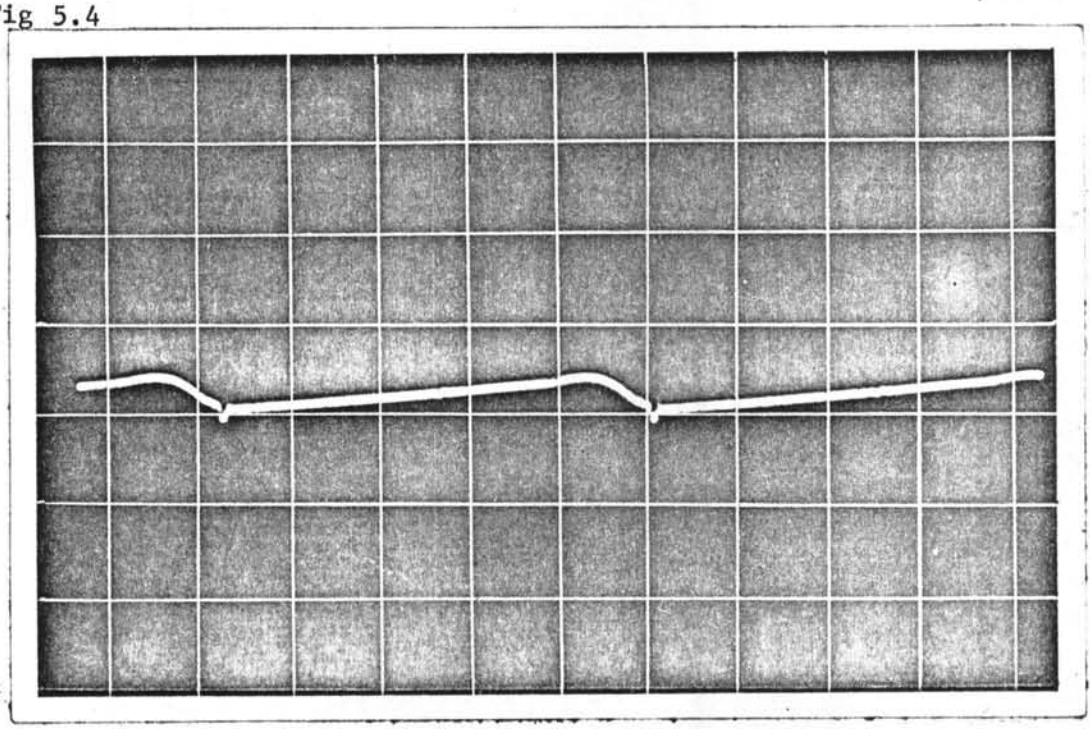

Fig 5.4 the ripple voltage [200mV/div., 5μs/div.]

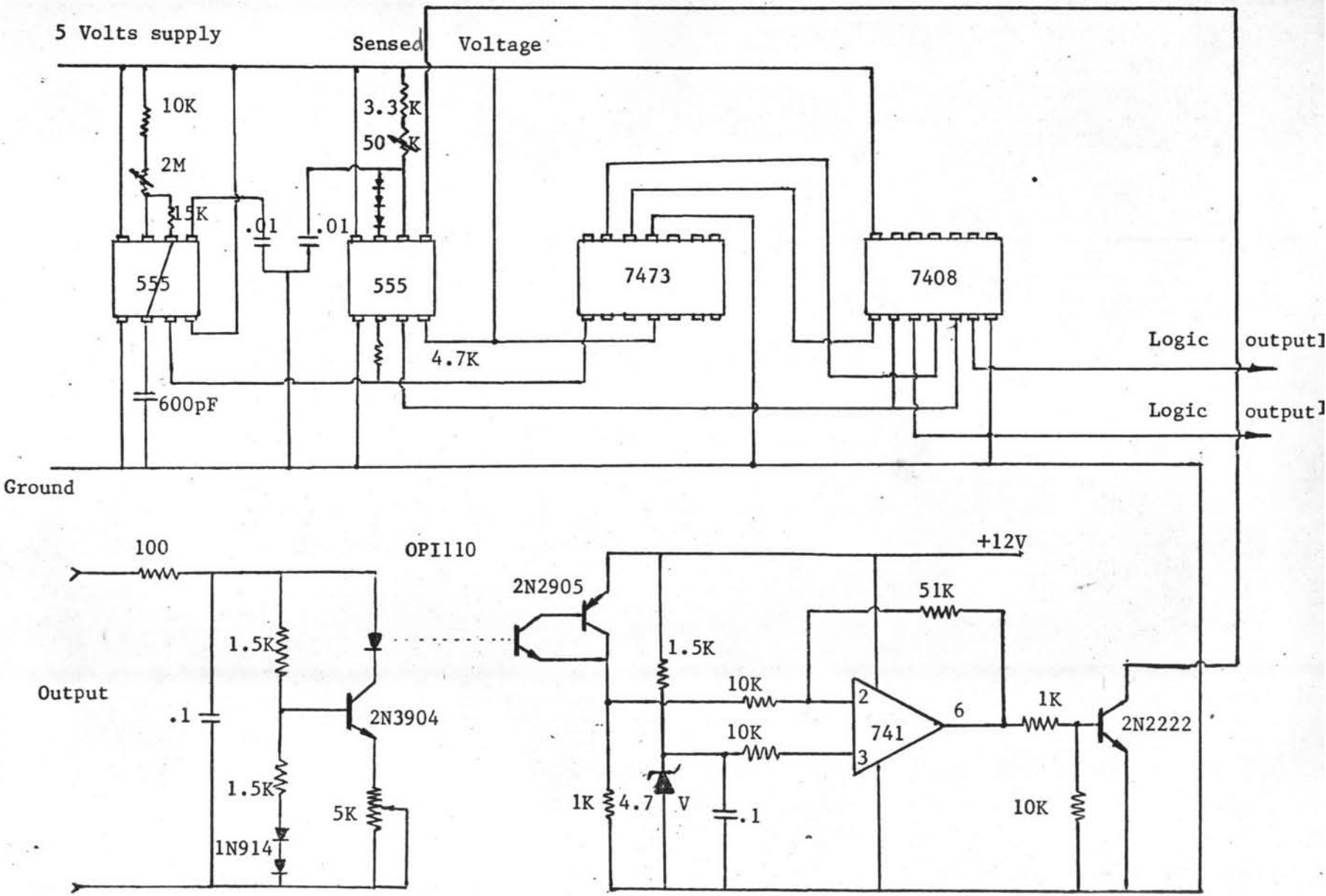

Fig. 5.5 The control circuit

This ripple voltage is a little bit higer form the expected calculation but it does not seriously influence the application.

5.5 Control unit.

The various circuits which are used in the control unit is illustrated in Fig 5.5 This control unit consists of the following circuits listed below

(a) an oscillator

(b) a phase splitter

(c) a pulse width control unit

(d) a comparator gate

(e) an opto isolation and feedback amplifier

(f) a limitting current

5.5.1 An oscillator

The 555 Ic's can be used for generating a clock pulse, and the circuit is shown in Fig 5.6

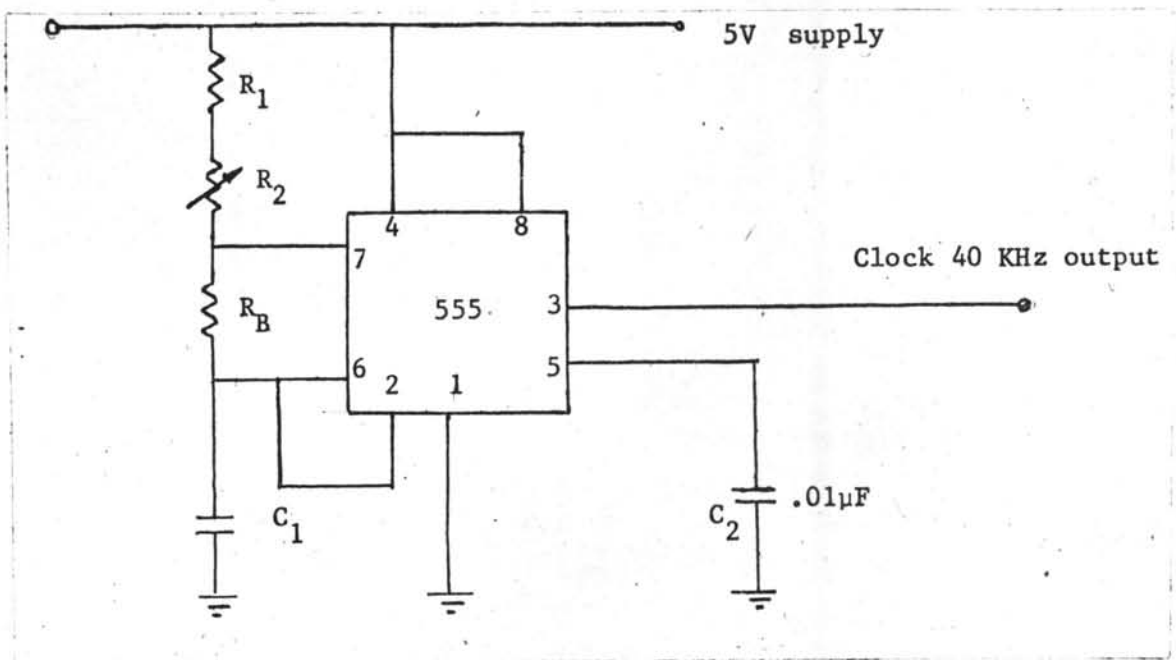

Fig 5,6 the circuit of an oscillator

The frequency of clock pulse is given by

$$f = \frac{1}{T} = \frac{1.44}{(R_1 + R_2 + 2R_B)C_1}$$

Since the desired frequency of the clock pulse is 40 KHz, then the values of R_1, R_2 and R_B are chosen as

R_B (fixed) = 15 KΩ

R_1 (fixed) = 2 MΩ

R_2 (variable resistor) = 10 KΩ

and the value of C_1 is 600 PF

The waveform of the clock pulse at 40 KHz is illustrated in Fig 5.7

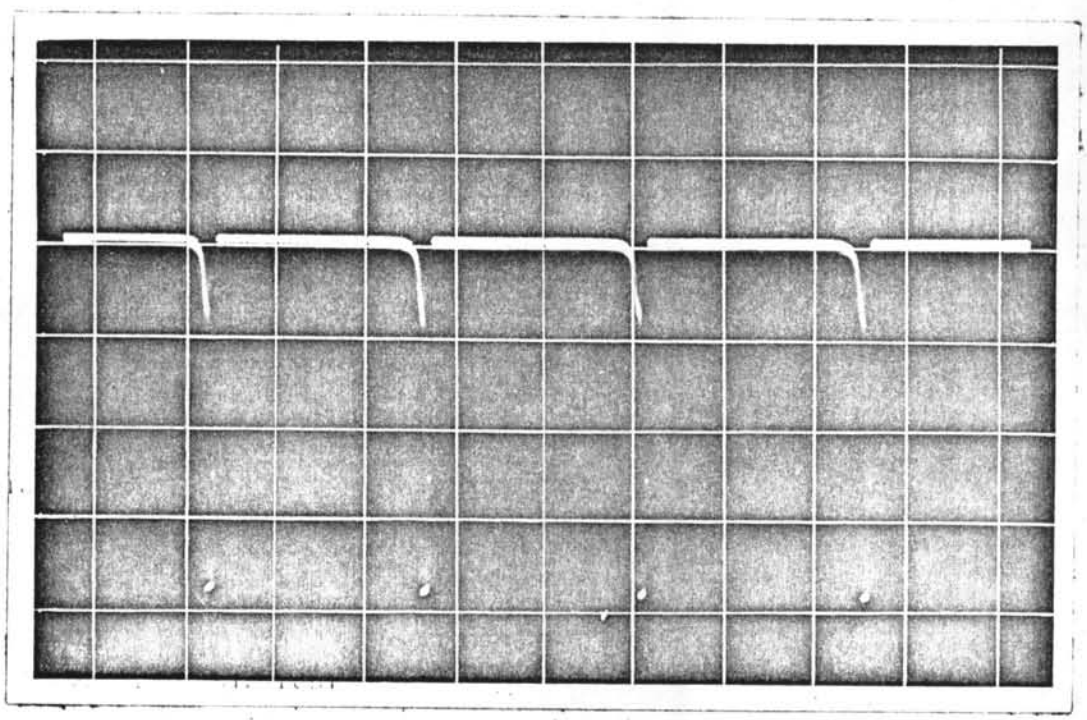

Fig 5.7 40KHz clock pulse (scale 1V/div., 10 μsec/div.)

5.5.2 A Phase Splitter

An IC flip-flop type SN7473 is used as a phase splitter shown in Fig 5.8

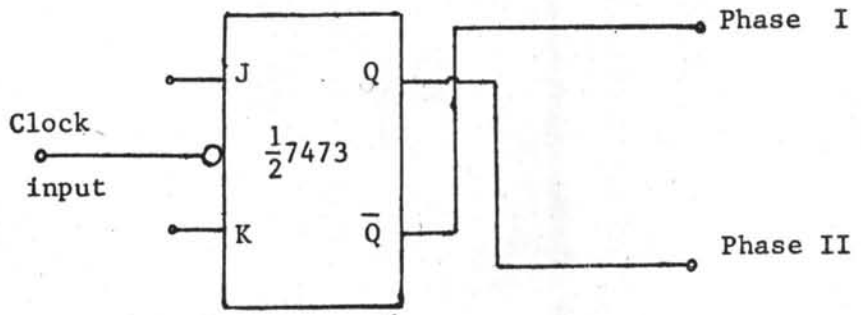

Fig 5.8 A Phase Splitter Circuit

The result of the phase splitter is illustrated in Fig 5.9

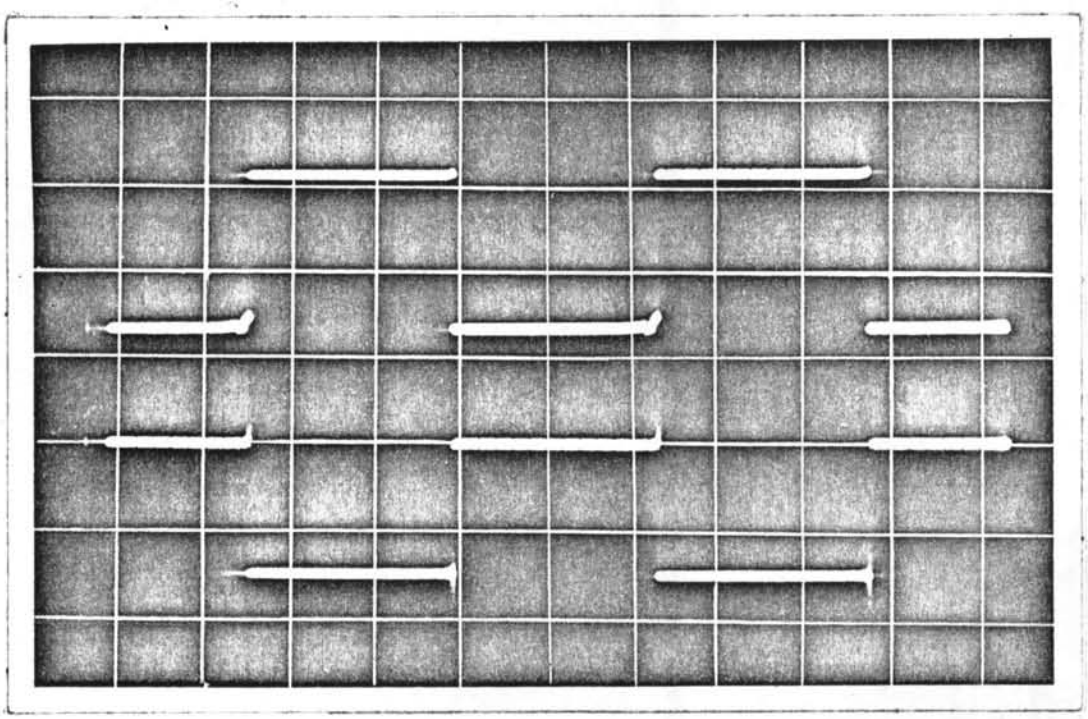

Fig 5.9 The waveform of the output of phase splitter circuit.

(Scale 2V/div., 10μs/div)

5.5.3 A Pulse width control unit

The regulated output voltage is determined by the pulse width of the control circuit shown in Fig 5.10

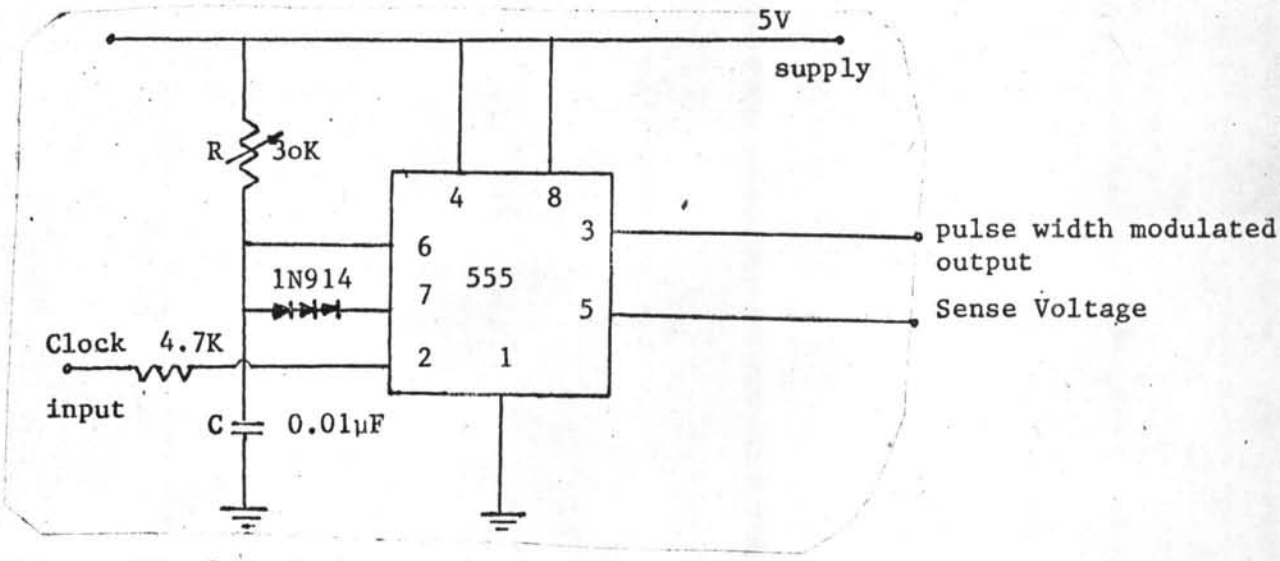

Fig 5.10 Pulse width control circuit.

This pulse-width control circuit consists of a well-known IC Type NE 555 arranged in the monostable mode. The circuit is triggered with a continuouse pulse train and the threshold voltage is modulated by the signal applied to the control voltage terminal. This has the effect of modulating the pulse width as the control voltage varies. Three diodes clamp the voltage to 1.8 Volt at pin 6 for the pulse width to decrease to zero . The width of the pulse must not be spread more than 40% of the period time controlled by the resistor R.

A typical result of this circuit is illustrated in Fig 5.11 and Fig 5.12

5.5.4 A comparator gate

A logic AND-gate is used as a simple comparator gate shown in Fig 5.13

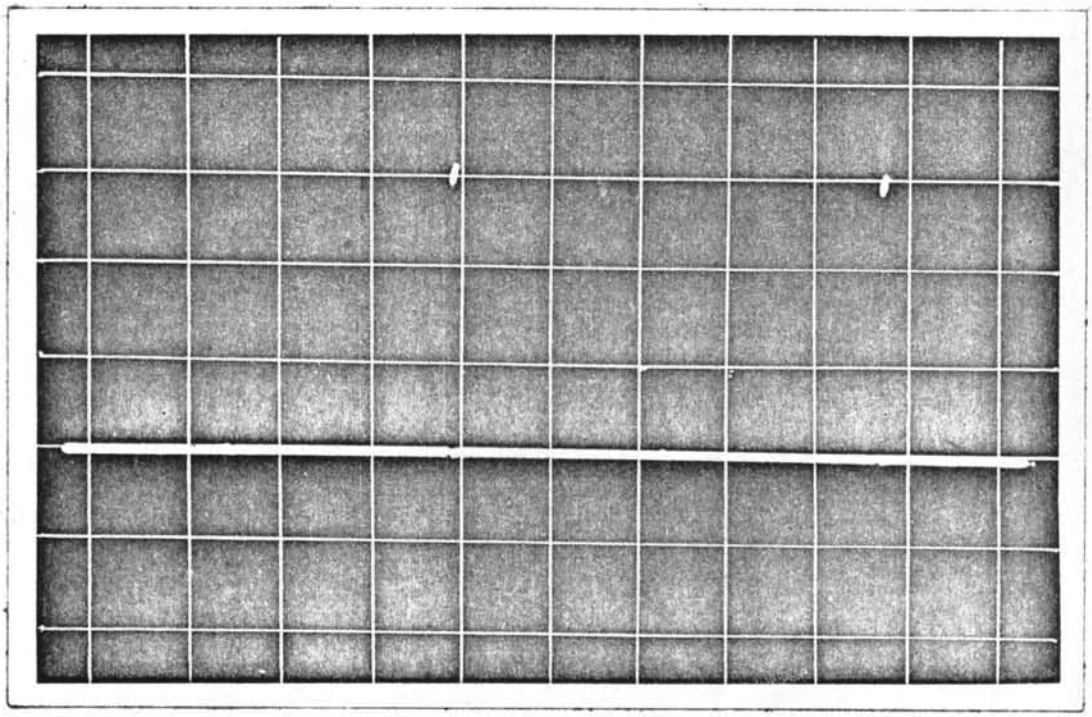

Fig.5.11 Logic pulse at no load

(scale 1V/div.,10μsec/div.)

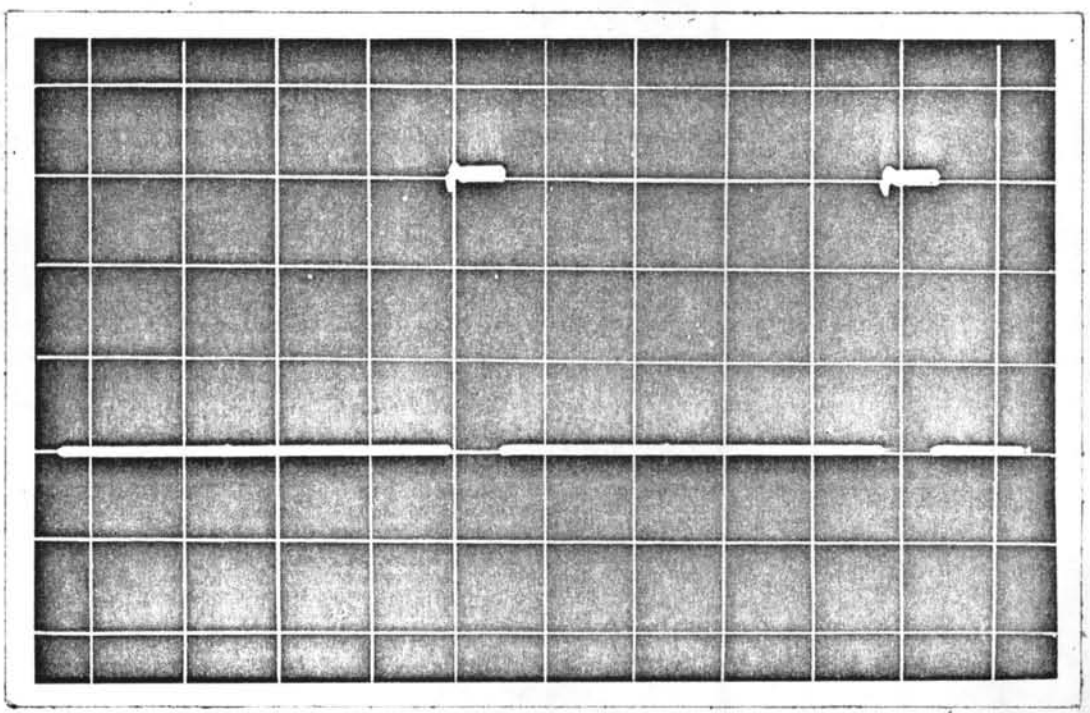

Fig.5.12 Logic pulse at load 5 A.

(scale 1 V/div.,10μsec/div.)

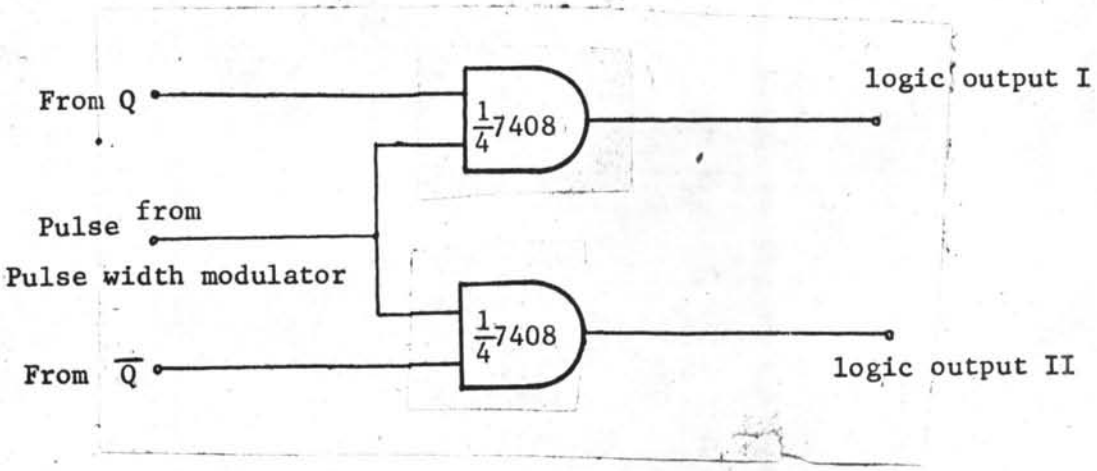

Fig 5.13 AND-gate Circuit

The results of the waveforms of a comparator gate are illustrated in Fig 5.14

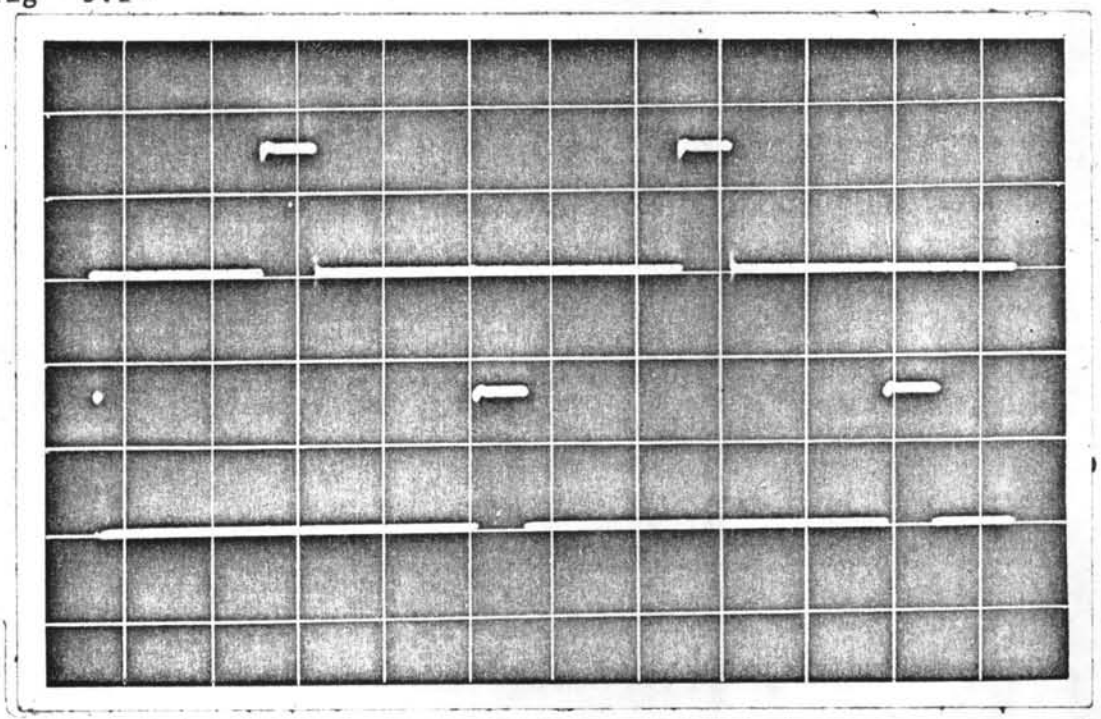

Fig 5.14 logic output I and logic output II

(Seale 2V/div., 10μs/div)

5.5.5 An Opto-coupler and a Feedback Amplifier

An opto-coupler and a feedback amplifier circuit is shown in Fig. 5.15

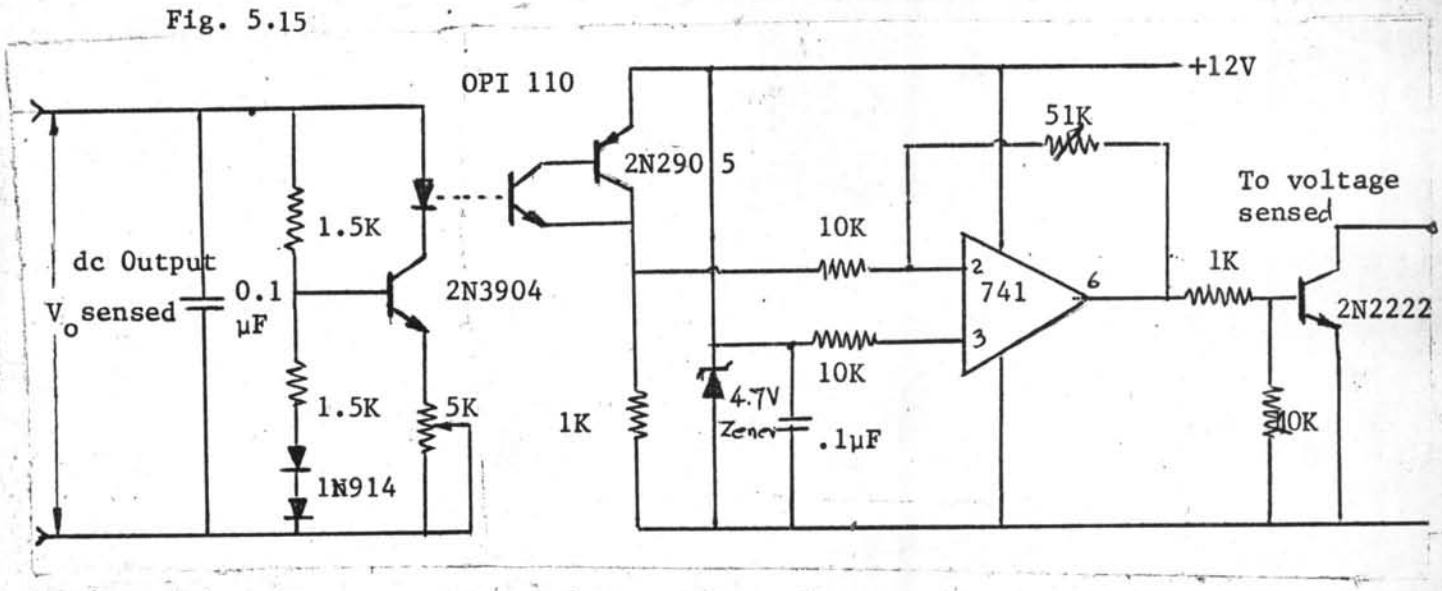

Fig 5. 15 An opto coupler and a feedback amplifier circuit.

In this circuit the comparater output voltage is determined by the pulse width of the control circuit and it in turn is controlled by the feedback elements in this close loop system. The optical electronic coupler consists of a LED to sense the change in output voltage, V_o and then this signal is transferred to the photo transistor. The result voltage from the photo transist r is amplified by an operational amplifier. The operational amplifier gain will show how good the comparing with the reference voltage.

It is seen that the variable resistor, R_3 as shown in Fig 5.15 can be adjusted to obtain any designed output voltage (0-9 Volts)

5.5.6 A limiting Current

A typical limiting circuit shown in Fig 5.16 is used to limit the output current for a good safety in the design.

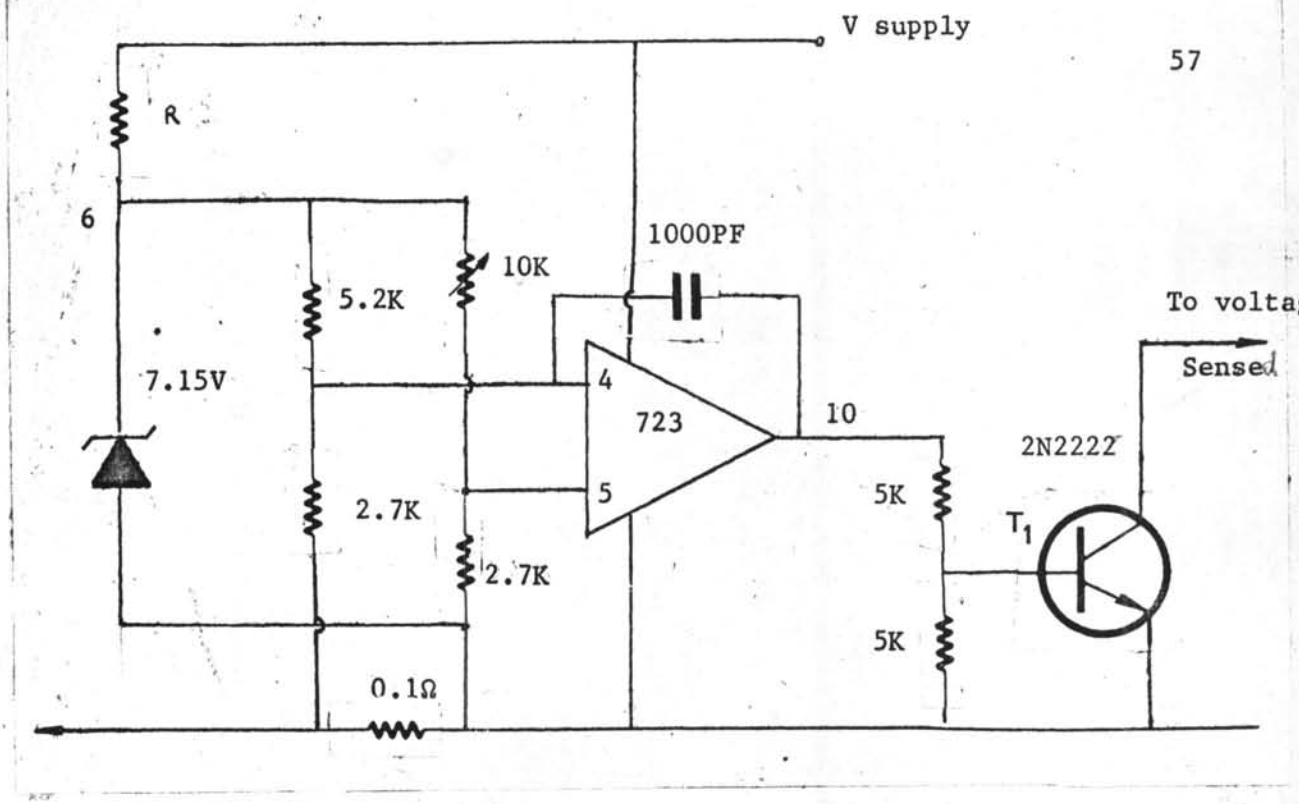

Fig. 5.16 The circuit of the limiting current.

The output transistor T_1 will operate at the boundary between active region and saturation region to control the pulse in the pulse width control unit.

5.6 A Driver Circuit

Normally, the output current obtained from any logic gate is about 2-5 milliampere, it is necessary to raise this current up to 100 milliampere in order to drive the switching transistor. A typical driver circuit shown in Fig 5.17 is used for this purpose. All the parameters in the circuit can be easily determined from this circuit

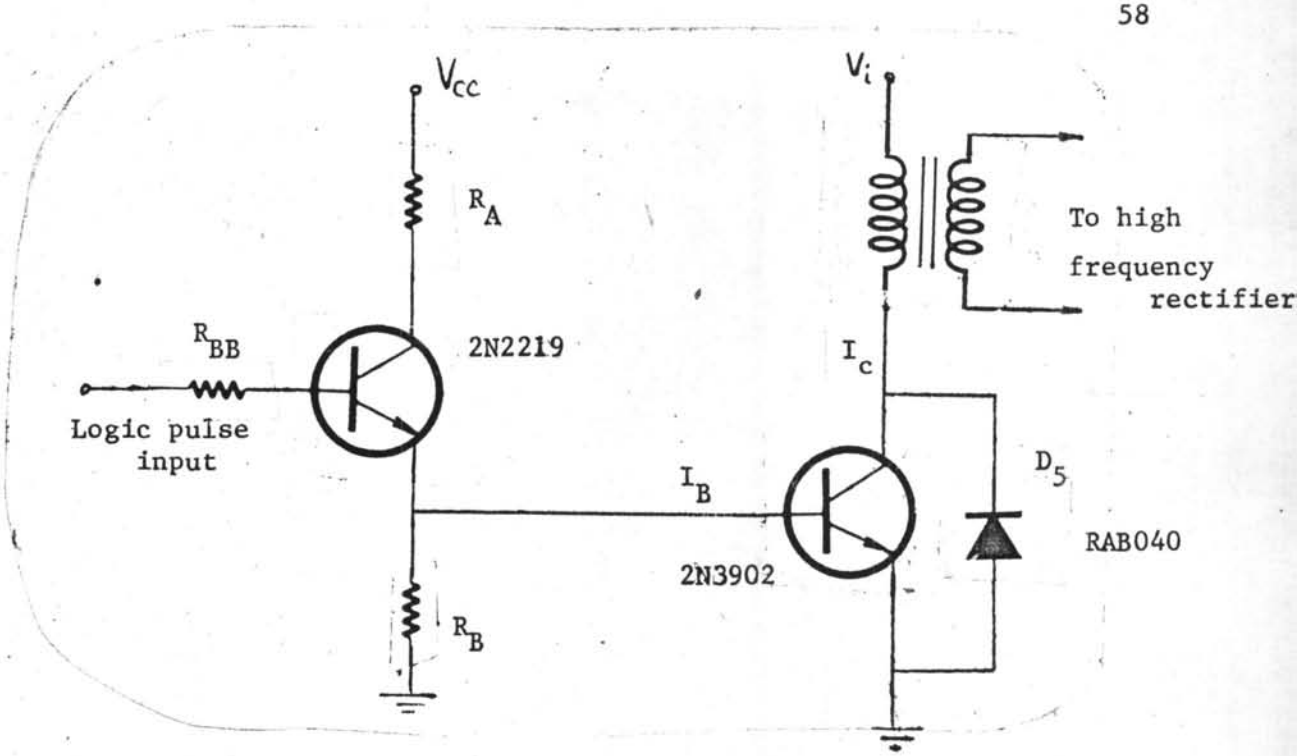

Fig 5.17 A driver circuit

Since the transistor used is the type 2N3902 with $h_{FEmin} = 10$

In this design, the value of I_c is 2 ampere

Thus

$$I_B \simeq \frac{I_c}{h_{FE(min)}} \quad \text{amperes}$$

The resistor R_A can be determined as

$$R_A = \frac{V_{cc}}{I_B}$$

$$= \frac{12}{0.02}$$

$$= 60 \quad \Omega$$

When the input logic is about 5 Volts, chosen $R_B = 50\ \Omega$

and $R_{BB} = 1000\ \Omega$

The diode D_5 is used to protect the transist r from the reverse current due to the store energy in the inductance of transformers.

5.7 Power switching transistors

The 2N3902 power transistors are selected in this design because they have high speed operation and also easily obtained. In addition, these devices have been selected for match betas and tested in the circuit to have equal collector current pulses in order to minimize potential transformer saturation problems.

5.8 Regulator Loss

There are normally four sources of loss in a nondissipative regulator. These losses can be summarized as follows:

(a) Conduction Losses

(b) Switching Losses

(c) Drive Losses

(d) Transformer Losses

Conduction Loss in the choke

The DC choke loss is easily determined by

$$P_{LL} = I_L^2 R_{ch}$$

In this case, the wire type number 12 is used and from the data sheet of the manufacturer given in Appendix-E the value of the resistance per kilometer is 1.62 Ω/KM

Thus $R_{ch} = \frac{1.62}{1000}$

From eqn(3.38),

$P_{LL} = 10^2$ 0.0016 Ohm

$= 0.16$ Watt

In this design, the choke loss due to ac voltage is neglected.

Therefore the dc loss is represented the choke loss.

Transistor conduction loss

From the data sheet of the transistor given in Appendix D :-

From eqn(3.36), the transistor conduction loss can be determined,

$$P_{TL} = V_{CES} I_C \frac{t_1}{T} \quad \text{watts}$$

Where V_{CES} is a saturation voltage 0.8 Volt

I_C is approximate maximum collector current of transistor 2 Amp

$\frac{t_1}{T}$ be a percent duty cycle = 0.4

Hench

$$P_{TL} = 0.8 \times 2 \times 0.4 \quad \text{Watts}$$

$$= 0.64 \quad \text{Watts}$$

Since two transistors are used,thus total loss in transistors is

$$P_{TL}\ \text{total} = 1.28 \quad \text{Watts}$$

Diode conduction loss

From equation (3.37), the conduction loss in diode can be determined as

$$P_{DL} = V_d I_d \frac{t_1}{T}$$

Where V_d be the forward voltage drop = 0.6 volt

I_d be the forward current in diode = 1.5 Amp.

Hench $P_{DL} = 0.6 \times 1.5 \times 0.4$

$$= 0.36 \quad \text{Watt}$$

Since,eight diodes are used, thus the total loss in diodes is

$$P_{DL} = 0.36 \times 8$$

$$= 2.88 \quad \text{Watts}$$

Switching loss in diodes and transistors

From eqn (3.40), the switching loss can be determined as

$$P_{ST} = f E_i I_{cmax} t_{off}$$

$$= 20 \times 10^3 \times 40 \times 2 \times 1.7 \times 10^{-6} \quad \text{Watts}$$

$$= 2.72 \quad \text{Watts}$$

Since two transistors are used in the circuit, the total switching loss is

$$P_{ST} = 5.44 \quad \text{Watts}$$

From eqn (3.41), the diode switching loss can be determined as

$$P_{SD} = 40 \times 10^3 \times 1.5 \times 5V \times 0.15 \times 10^{-6}$$

$$= 45 \quad \text{mW}$$

Since eight diodes are used in this circuit. Therefore the total diode switching loss is

$$P_{SD} = 360 \quad \text{mW}$$

Driver loss

When the collecter current is about 2 amperes the base current will be 0.2 amps.

From eqn (3.42), the driver loss can be determined as.

$$P_{DR} = 0.2 \times 12$$

$$= 2.4 \quad \text{Watts}$$

Transformer loss

From section 4.7, the loss in the transformer can be obtained from the core loss and copper loss as

$$P_{Tran} = 1.5+0.01$$

$$= 1.5 \quad \text{Watt}$$

The total loss in this tranformer is

$$P_{TT} = P_{LL}+P_{TL}+P_{DL}+P_{ST}+P_{SD}+P_{DR}+P_{Tran}+P_{CON}$$

Assume that the control circuit loss, P_{CON} be 0.2 Watt

Hence $P_{TT} = 0.16+1.28+2.88+5.44+.36+2.4+1.5+0.2$

$$= 14.22 \quad \text{Watts}$$

The total output power 10V×5A = 50 Watts

Therefore, the effeciency is $= \frac{50}{50+14.22}$

$$= 77.86 \ \%$$

5.9 The auxilary Power supply

A typical auxilary power supply circuit shown in Fig . been designed to supply the voltage and current to the control unit and driver circuits.

5.10 Testing Results

The regulation performance , the transient recovery time of the switching regulator power supply has been tested. The transient recovery time testing is also presented in Fig 5.19

The circuit used for this performance testing is shown in Fig 5.19

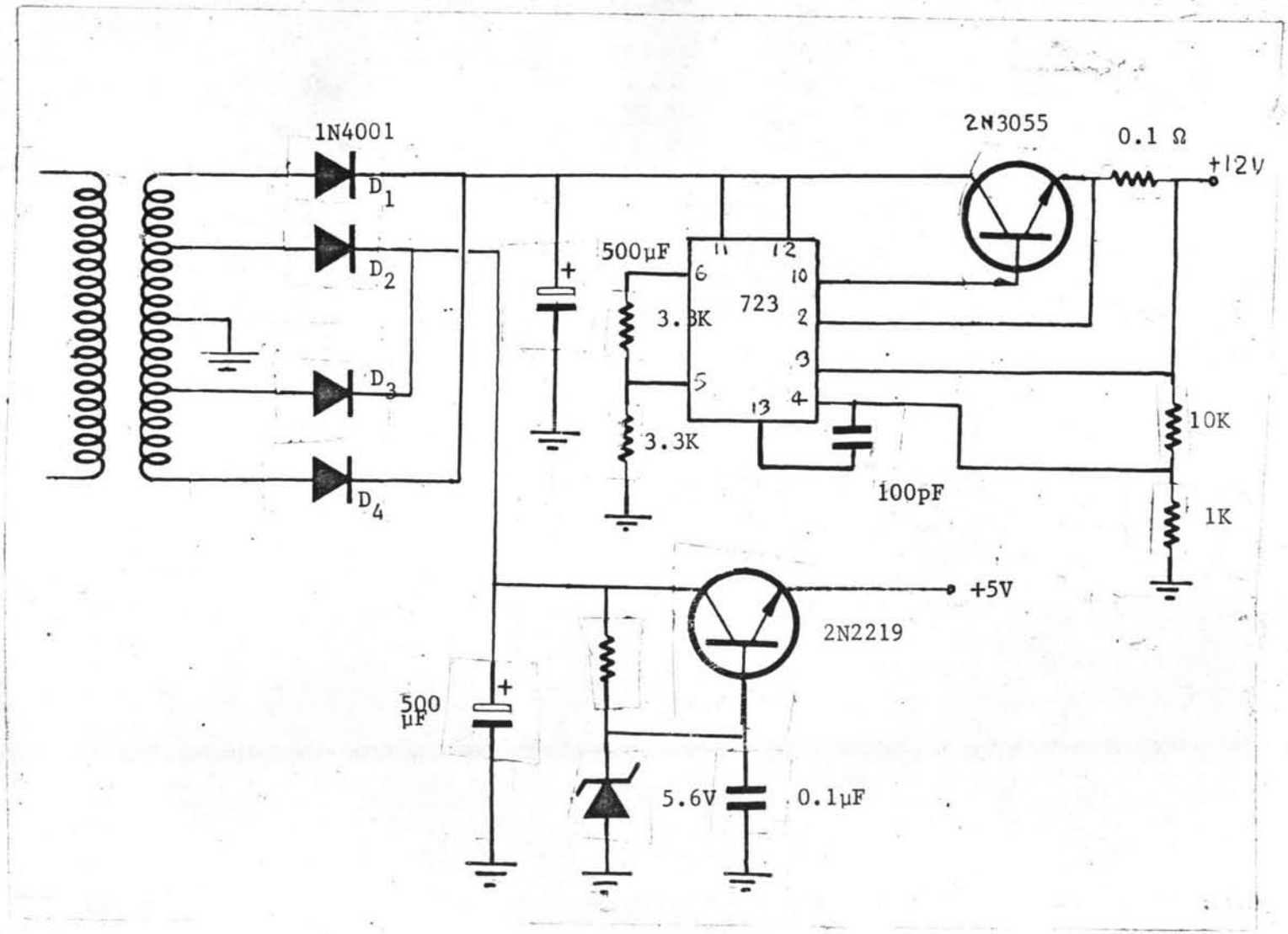

Fig 5.18 Auxillary Power supply

It can be seen that the transient recovery time can be found from Fig 5.20

The recovery risetime is 10 μsec

The regulation results have been summarized in Table 5.1

Table 5.1 The output voltage VS. the V_{in} when I_L = 9.2,5and 2 amperes, respectively

Table 5.1

V_{in}			
25 Volt	30 Volt	35 Volt	I_o
5.081	5.105	5.135	No load
5.038	5.072	5.102	2 A
5.003	5.036	5.073	5 A
4.946	4.974	5.026	9.2 A

The results show

the line regulation at 5 Amp is 1.3%

The load regulation at 30 Volts is 1.41%

The power supply has been tested for efficiency determination, the result is summarized in Fig.5.22

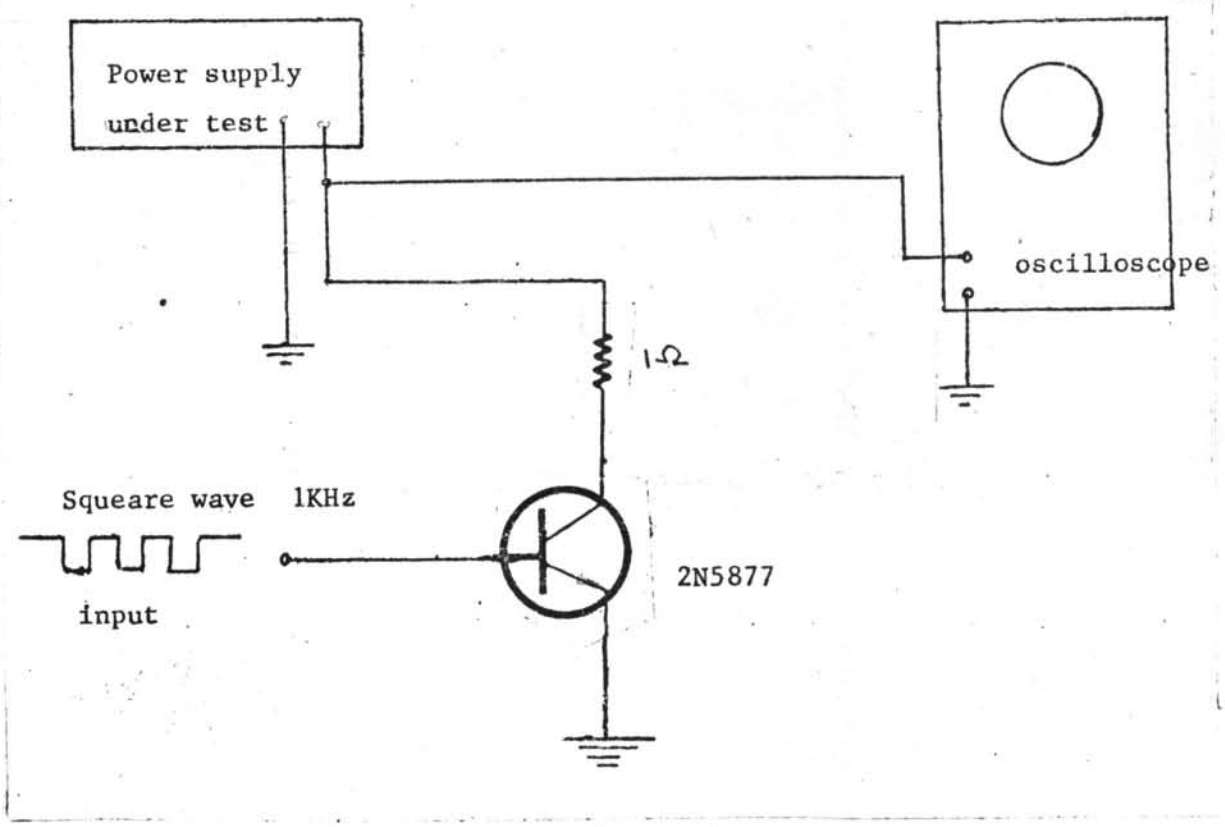

Fig 5.19 the recovery time test.

The results of the transient recovery time are shown in Fig 5.20

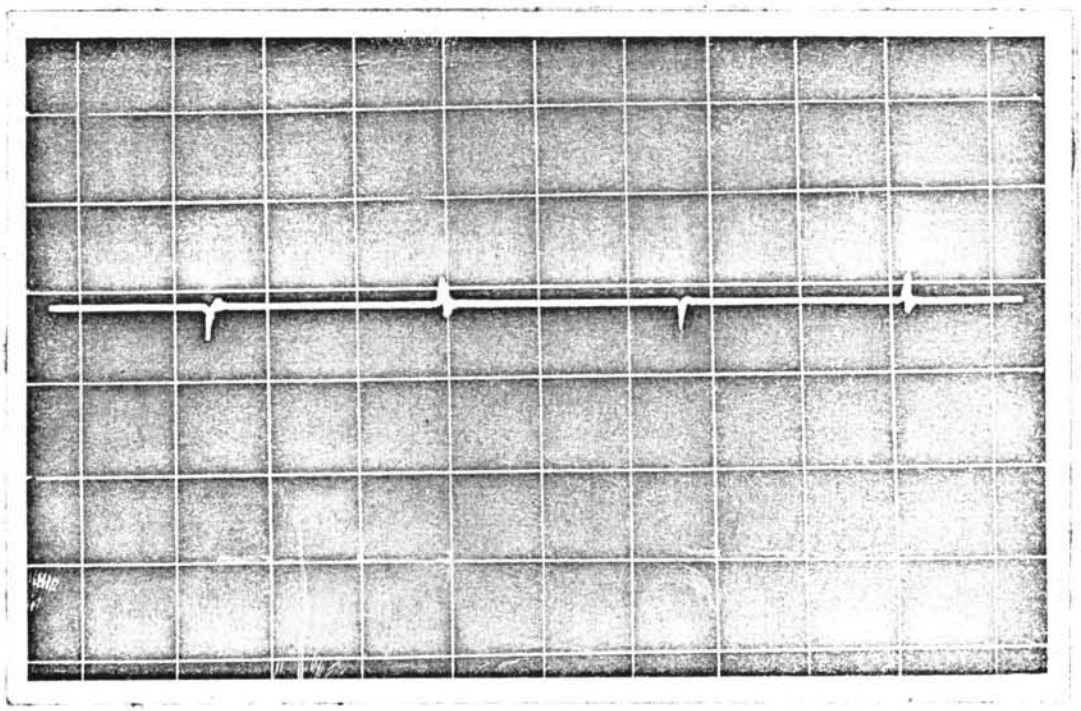

Fig 5.20 The result of the recovery of the switching power supply (Scale 200μsec/Div.20mV/Div.)

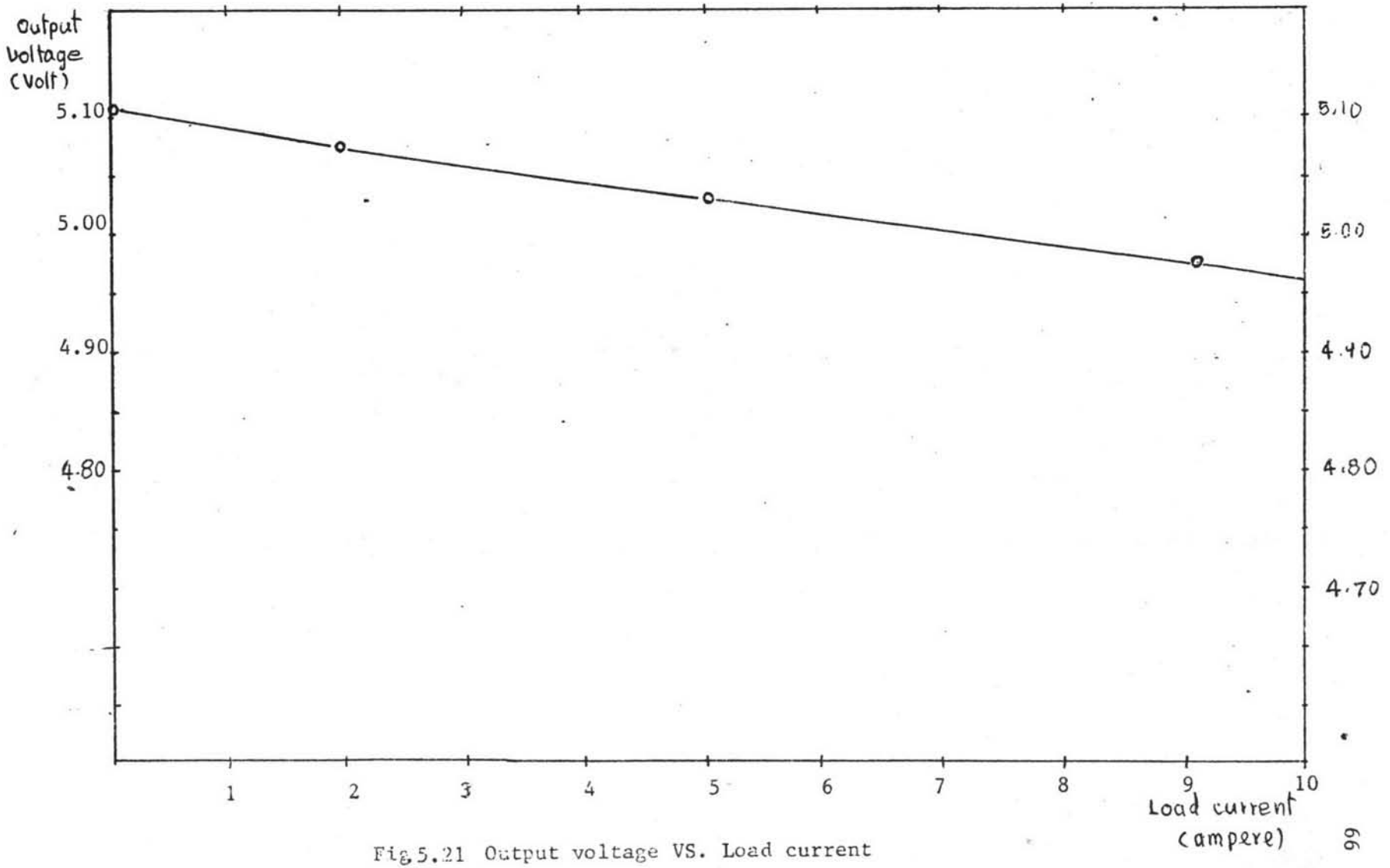

Fig.5.21 Output voltage VS. Load current

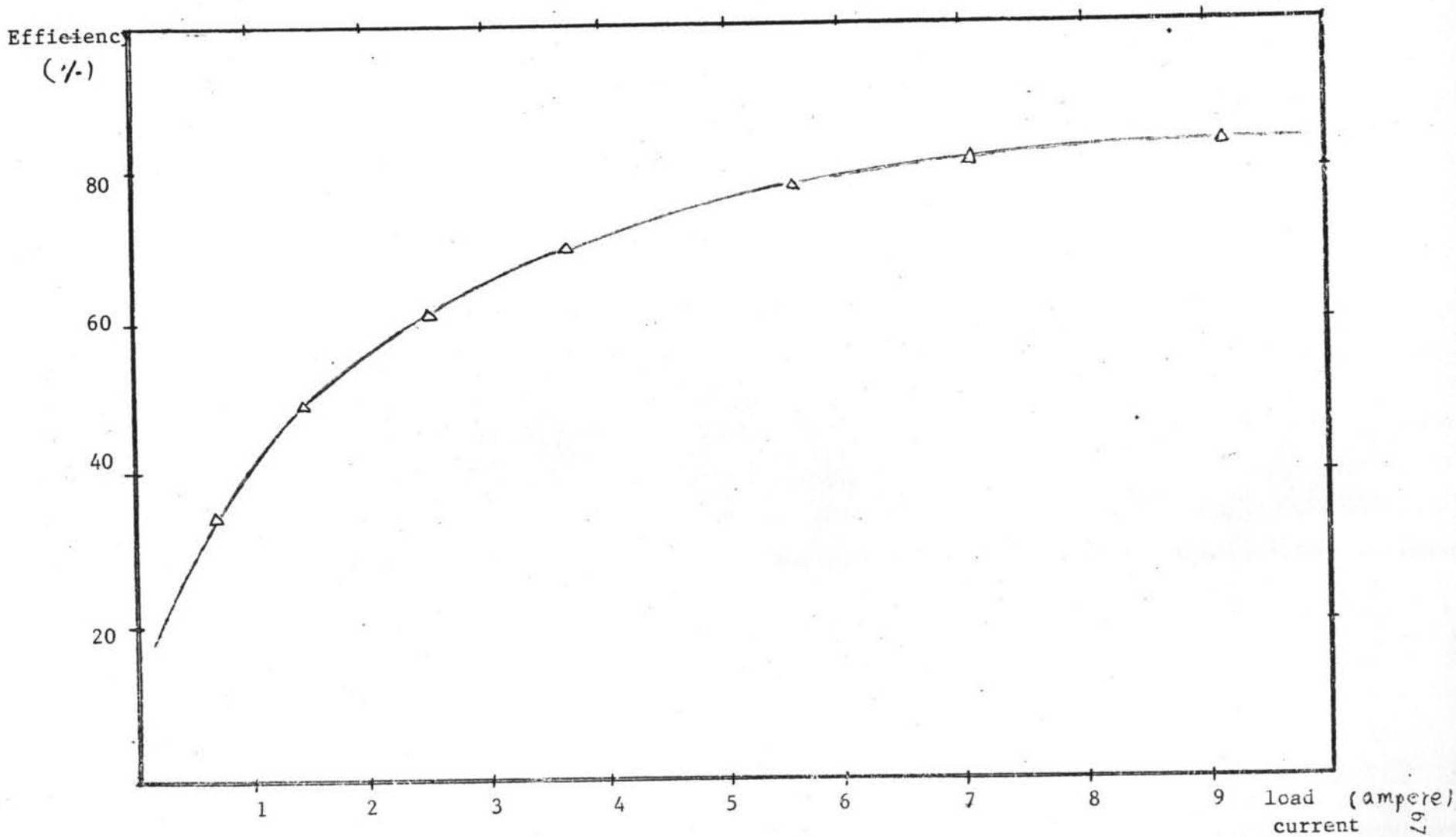

Fig. 5.2 2 the efficiency V.S. the load current