CHAPTER III

CIRCUIT DESIGN

3.1 COMPARATOR DESIGN [5]

The design is divided into three parts :

- Biasing.
- Reference Level.
- Hysteresis Level.

3.1.1 Biasing Design

Given : Positive supply + 12 volts, negative supply - 12 volts.

Design Procedure :

Choose μA 710c as the comparator which has the following characteristics :

Max. positive supply voltage + 14.0 volts.

Max. negative supply voltage - 7.0 volts.

Differential input voltage $\pm$ 5.0 volts.

Input bias current 40.0 μA

	Min.	Typ.	Max.
Positive output level	2.5 V	3.2 V	4.0 V
Negative output level	-1.0 V	-0.5 V	0.0 V
Positive supply current		5.2 mA	
Negative supply current		4.6 mA	

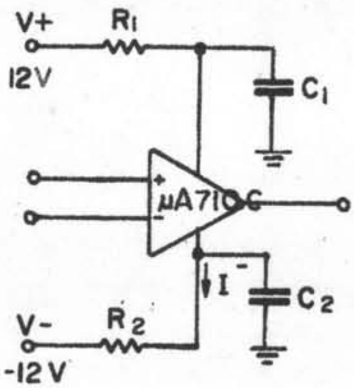


FIG.3.1 Circuit for Determination of R_1 and R_2.

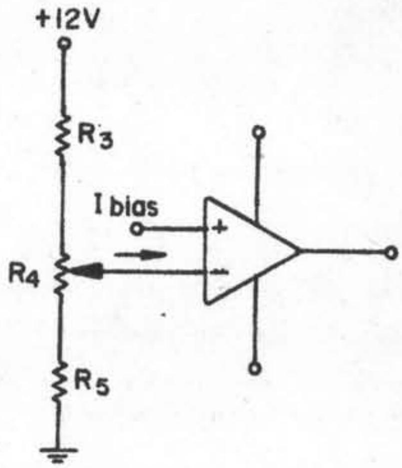
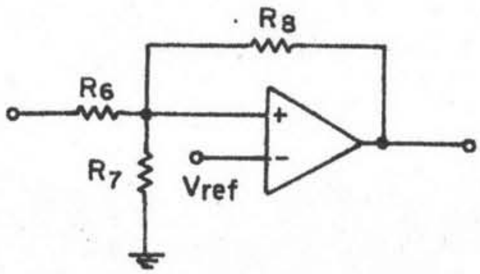


FIG.3.3 Equivalent Circuit for Reference Level Design.



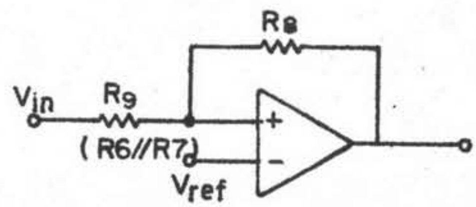


FIG. 3.2 Equivalent Circuit for Hysteresis Design.

Due to the limitation in negative supply requirement i.e. -7 V(Max.)at the negative input of the comparator, R_2 must be chosen to drop the excess voltage that is available from the NIM Bin. The value of R_2 can be calculated as follows :

$$I^- \times R_2(\text{Max.}) \geqslant V^- - 7$$

$$R_2(\text{Max.}) \geqslant \frac{V^- - 7}{I^-}$$

$$\geqslant \frac{12 - 7}{4.6} \geqslant 1.1\ K\Omega$$

Allow $\pm 5\%$ tolerence, the conventional value of R_2 should be 1.3 K Ω.

When the comparator is switching from high to low or vice versa a sharp spike may be introduced into the supply line. This can be eliminated using RC filter. To obtain low impedance path for the spike C_1 and C_2 should be in the order of .01 μF and be of ceramic type. In order not to lower voltage at the positive supply of the comparator the value of R_1 should be around 100 Ω.

3.1.2 Hysteresis Level Design

Given Max. input voltage +10 volts.

Input impedance 1.0 K Ω.

Peak noise voltage impcses on the input signal

<15 mV.

Design Procedure :

Requirements in input signal and input impedance imply that the max. voltage drop across R_7 should be equal to or less than 5 volts and R_6 plus R_7 should be in the vicinity of 1 KΩ.

Hence for $R_6 = R_7 = 511\,\Omega \pm 1\%$ the above condition will be satisfied.

R_8 can now be calculated under the restriction that the hysteresis level under maximum and minimum output voltage be less than 50 mV and greater than 15 mV respectively.

$$V_o \text{ High (Min.) } \left(\frac{R_9}{R_8}\right) > 15 \text{ mV and } V_o \text{ High (Max.) } \left(\frac{R_9}{R_8}\right) < 50 \text{ mV}$$

Hence $$\frac{V_o \text{ High (Max.)}}{50 \text{ mV}} R_9 < R_8 < \frac{V_o \text{ High (Min.)}}{15 \text{ mV}} R_9$$

$$\frac{2500 \times 505}{50} < R_8 < \frac{4000}{15} \times 505$$

$$40 \text{ K} < R_8 < 83.3 \text{ K}$$

Choose $R_8 = 75.5 \text{ K}\Omega \pm 5\%$

$$V_{in\ 1} = V_{ref.} \frac{(R_9 + R_8)}{R_8}$$

$$\simeq V_{ref.} \qquad (R_8 >> R_9)$$

3.1.3 Reference Level Design

Given : Lowest reference level = 50 mV

Highest reference level = 5 volts

Design Procedure :

The design should begin with the standard value of R_4. The value is chosen such that current in R_4 is much greater than I_{bias} of the comparator. With the wiper sets at its highest and lowest extremes the voltage should be 5.0 volts and 50 mV respectively. Therefore, the current in R_4 is :

$$i_{R4} = \frac{5-0.05}{R_4} = \frac{5-0.05}{1K} = 4.95 \text{ mA} > 100\ I_{bias}$$

And also 4.95 mA flows through R_3 and R_5, hence :

$$R_3 = \frac{12-5}{4.95} = 1.42 \quad K\Omega$$

and $$R_5 = \frac{0.05}{4.95} = 10.1 \ \Omega$$

Let R_3 be 1.42 $K\Omega \pm 1\%$ and R_5 be $10\Omega \pm 1\%$

3.2 DESIGN OF TTL DRIVER [6], [7]

The emitter follower stage acts as an impedance transformers from output to input terminals and is often used as a buffer element between an input and output stage. The driver for the TTL is shown in Fig. 3.4, and the values of R_1, R_2 and R_3 must be determined to meet the following specification :

1. For $V_{in} \leq 1.5$ V, V_{out} should be equal to or less than the logical 0 input voltage of TTL (i.e. ≤ 0.8 V).

2. For $V_{in} \geq 3$ V, V_{out} should be equal to or greater than the logical 1 input voltage of TTL (i.e ≥ 2.0 V).

3. Open circuit input causes Vout to approach V_{cc}.

4. $V_{bb} = 12$ V, $V_{cc} = 5$ V., $V_{ee} = -12$ V.

3.2.1 Determination of R_3

In determining R_3 the worst case occurs when R_3 has to sink the maximum load current, i.e. when Vin is at its lowest maximum voltage and in this case V_{in}(Mix.) ≈ 0 volt. Hence R_3 must be small enough to pass at least the current from the input of TTL. The equivalent circuit for calculating R_3 can be drawn as shown in Fig. 3.5.

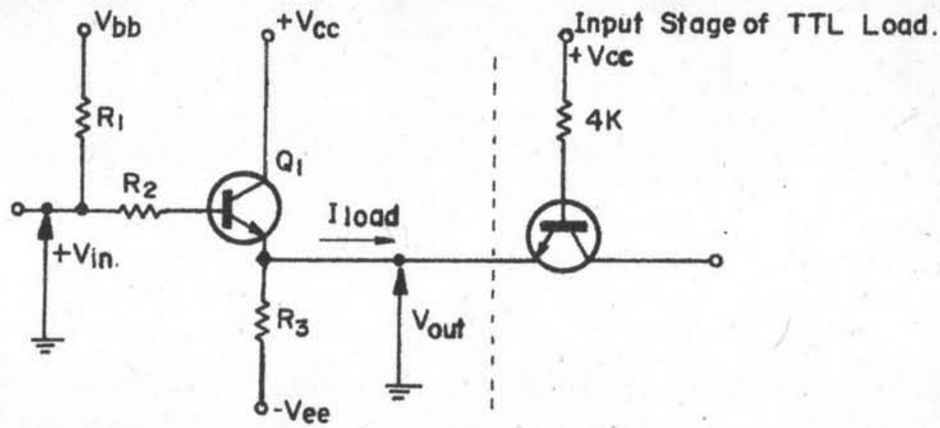


FIG. 3.4 Emitter-Follower Driving one TTL Load.

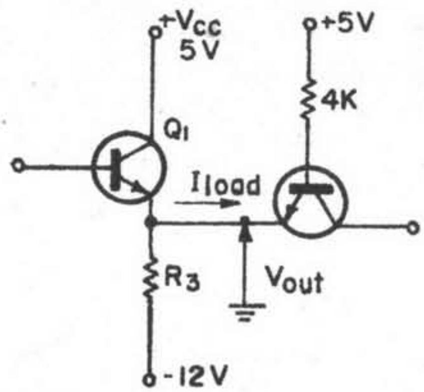


FIG. 3.5 Equivalent Circuit for Determining R_3.

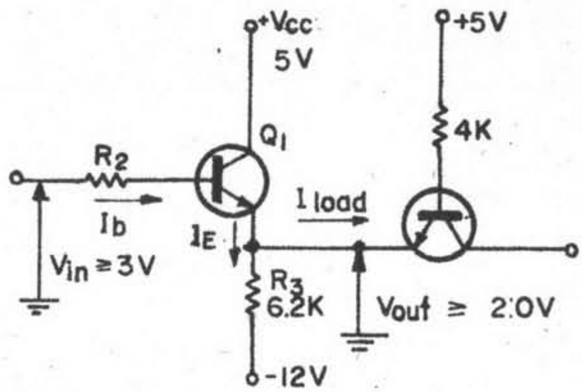


FIG. 3.6 Equivalent Circuit for Determining R_2.

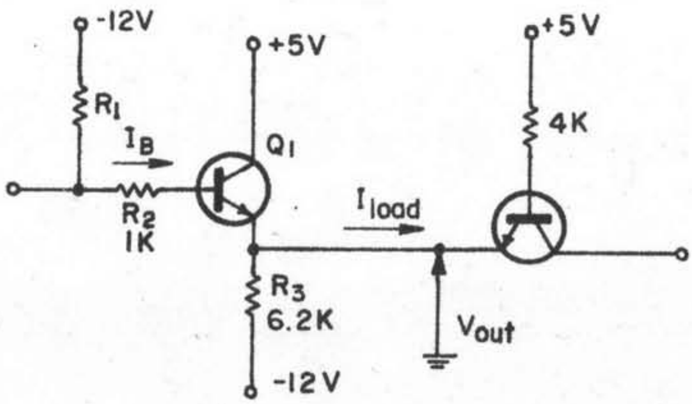


FIG. 3.7 Equivalent Circuit for Determining R_1.

Assume Q_1 be a silicon transistor with $V_{BE}(ON) = 0.7$ V, at this instant V_{out} should be approximately 0 volt with respect to ground. I_{load} is found to be 1.6 mA inward and the value of R_3 is found to be:

$$R_3 < \frac{V_{ee}}{I_{load}}$$

$$< \frac{1.2}{1.6 \text{ mA}}$$

$$< 7.5 \text{ K}$$

Let R_3 be 6.2 KΩ ± 5%

Under worst case design one can realized that for $V_{in} \leq 1.5$ V, $V_{out} \leq 0.8$ V and hence satisfies the first criterion.

3.2.2. Determination of R_2

With the aid of Fig. 3.6 and the second restriction ($V_{out} \geq 2.0$ V for $V_{in} \geq 3$ V), R_2 must be designed to supply enough base current to drive the required emitter current. For $2 < V_{out} < 5$ V, I_{out} varies from 40 μA to 1mA outwards. Max. emitter current is then found to be

$$I_E(\text{Max.}) = \frac{V_{out} + V_{ee}}{R_3} + I_{load}$$

$$= \frac{12 + 2}{6.2\text{K}} + 1 \text{ mA}$$

$$= 3.36 \text{ mA}$$

$$I_B(\text{Max.}) = \frac{3.36}{h_{FE}(\text{Min.})} \text{ mA}$$

Apply Kirchoff's voltage law at the input of the emitter follower

$$V_{in} - I_B R_2 - V_{BE}(ON) - V_{out} = 0$$

$$R_2 = \frac{V_{in} - V_{BE}(ON) - V_{out}}{I_C} \cdot h_{FE}(Min)$$

Assume $h_{FE}(Min) > 50$, R_2 is found to be

$$R_2 < \frac{(3 - 0.7 - 2)}{3.36} \times 50$$

$$< \frac{0.3 \times 50}{3.36} \quad < 1.5\ K$$

choose $\quad R_2 < 1\ K\Omega \pm 5\%$

3.2.3 Determination of R_1

R_1 is to be designed such that when the input is held open, the emitter-follower then saturates. The equivalent circuit for calculating R_1 is shown in Fig. 3.7. Under this condition R_1 and R_2 must be small enough to pass excess base current to drive both the sink currents in R_3 and load. Hence R_1 can be calculated from the following expressions:

$$V_{bb} - I_B (R_1 + R_2) - V_{BE}(Sat.) - V_{out} = 0$$

$$(R_1 + R_2) = h_{FE}(Sat.) \left[V_{bb} - V_{BE}(Sat.) - V_{out} \right] / I_C$$

Where I_C is given by $I_C = \dfrac{V_{out} + V_{ee}}{R_3} + I_{load}$

$$= \frac{5 + 12}{6.2\ K} + 1.6\ mA = 4.34\ mA$$

I_{load} is found to be 1.6 mA outward for $V_{out} = 5V$ and under saturation $h_{FE}(Sat.)$ usually be much smaller than $h_{FE}(Min.)$ when the transitor operates in active region in; assume $h_{FE}(Sat.) = 30$

Then $\quad R_1 - R_2 \approx \dfrac{30.}{4.34} \quad (12 - 0.7 - 5) \approx 43\ K\Omega$

Let $\quad R_1$ be $33\ K\Omega \pm 5\%$

3.2.4 Determination of the Transistor

Since max. dissipation on transistor never exceeds 25 mW Any type of switching transistor that can withstand the following requirements :

1. Power dissipation of 25 mW.
2. Collector emitter breakdown exceed 5 V.
3. Supply base current $> 150\ \mu A$ and emitter current > 5 mA.
4. Having min. h_{FE} in active region ≈ 50 and min. h_{FE} under saturation ≈ 30.

can be used and the transitor is found to be 2N6531.

3.3 DESIGN OF MULTIPLEXER TO MECHANIZE LOGIC FUNCTIONS USING MSI [8]

Digital Multiplexer is sometimes called a selector switch. Its function is to select one of the inputs to appear at the output. Knowing standard MSI circuit well one can implement some logic equations with much more intelligently at the system level.

Requirements : A portion of a present time unit is to be required with the followings specification.

1. The portion is to be designed to receive 6 inputs $I_0 \ldots I_5$ which represent the time intervals of 0.1 to 10^5 sec.(min.)

2. The output of the portion can be selected from only one of the inputs at a time by a group of command in binary code.

Design : Using positive level logic as command. Since 6 inputs are to be transferred to the output one at a time at least 3 bits of binary command must be employed. Let it be designated as X, Y and Z. Fig. 3.8 lists the inputs and outputs correspondences.

XY \ A	0	1
00	I_0	I_1
01	I_2	I_3
11	X	X
10	I_4	I_5

Inputs				Output
Command			Data	Output
X	Y	Z		Ii
0	0	0	I_0	I_0
0	0	1	I_1	I_1
0	1	0	I_2	I_2
0	1	1	I_3	I_3
1	0	0	I_4	I_4
1	0	1	I_5	I_5

FIG. 3.8 Input Output Behavior of Function Under Designed.

CB \ AS	00	01	11	10
00	D_0	L	L	D_1
01	D_2	L	L	D_3
11	D_6	L	L	D_7
10	D_4	L	L	D_5

Inputs				Output
Select			Strobe	
C	B	A	S	Y
X	X	X	H	L
L	L	L	L	D_0
L	L	H	L	D_1
L	H	L	L	D_2
L	H	H	L	D_3
H	L	L	L	D_4
H	L	H	L	D_5
H	H	L	L	D_6
H	H	H	L	D_7

FIG. 3.9 Truth Table and Karnaugh Map for a 74151 Data Selector.

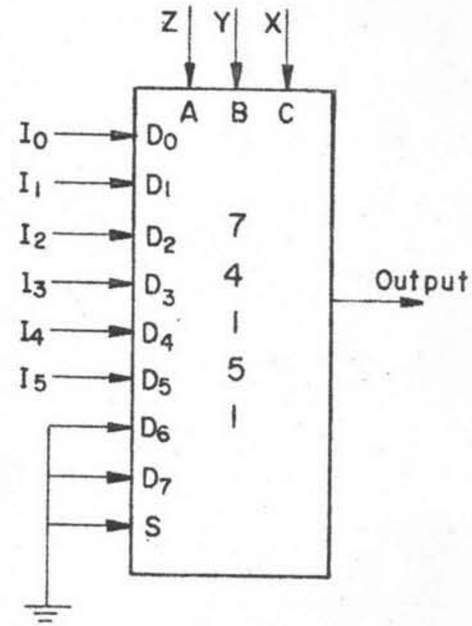


FIG. 3.10 The Complete Schematic Diagram of The Data Selection Under Design.

Fig. 3.8 shows that the function of this portion is simply a data selector or multiplexer. Select a conventional data selector at hand having at least 3 input commands and 6 data inputs. The device is found to be SN74151 with the following characteristics as shown in Fig 3.9. Compare Fig. 3.8 with Fig. 3.9 with strobe input shorted to ground one can conclude that:

1. $X = C$, $Y = B$, $Z = A$
2. $I_0 = D_0$, $I_1 = D_1$, $I_2 = D_2$, $I_3 = D_3$, $I_4 = D_4$, $I_5 = D_5$
3. Unuse data D_6 and D_7 can be either connected to ground or supply since it cannot occur.
4. The input command can be implemented with any thumb wheel switch operated in BCD code with a lock at position 6.

Fig. 3.10 concludes all the above results.

3.4 DESIGN OF ASTABLE MULTIVIBRATOR [9]

The circuit diagram for a free-running multivibrator using two inverter gates is shown in Fig. 3.11. Since capacitive coupling is used between stages, neither gate can remain permanently OFF. Instead, the circuit has two quasi-stable states, and it makes periodic transitions between these states

The waveforms at the inputs and outputs of the multivibrator are also shown in Fig. 3.12. Consider that immediately before $t = t_0$ gate G_1 is in saturation while gate G_2 is OFF. Hence for $t < t_0$ the output of the gate G_1 V_{out} (Low), G_2 is off. Capacitor C_1 charges through R_3 and R_4 towards V_{cc} causing an exponential rise at point B, waveforms of which is shown by Fig. 3.12a, and when the rise at B

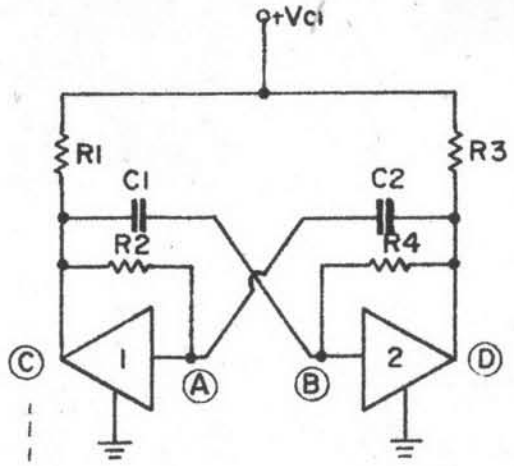


FIG. 3.11 Circuit of An Astable Multivibrator.

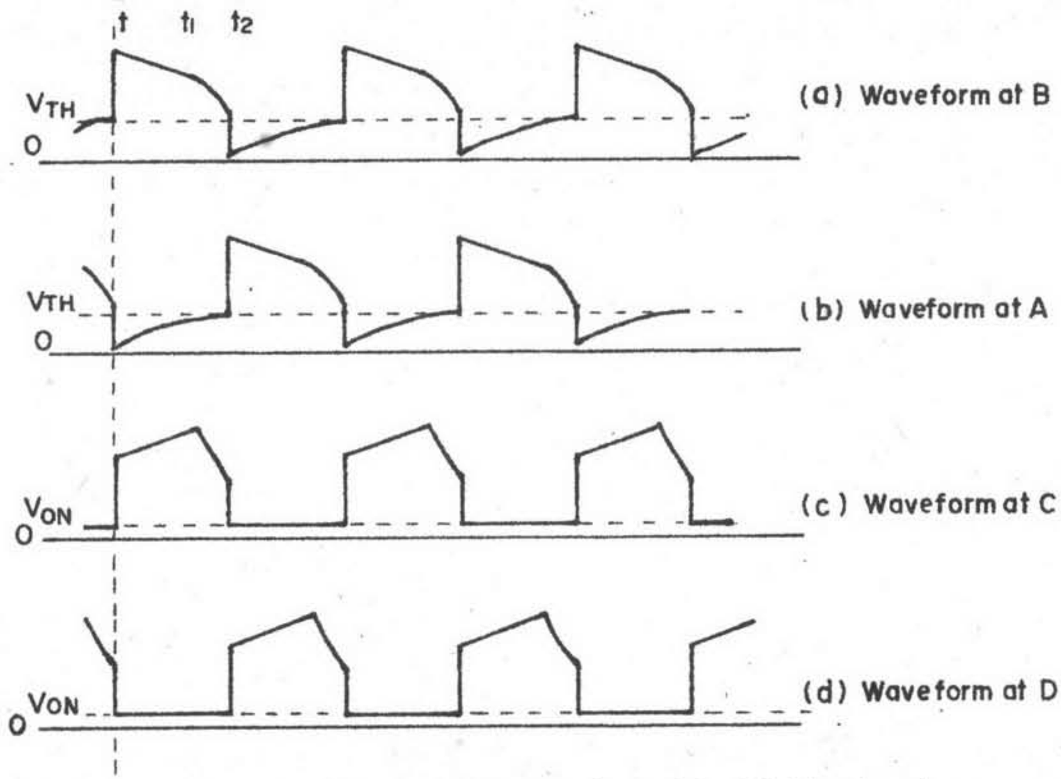


FIG. 3.12 Waveforms of The Astable Multivibrator.

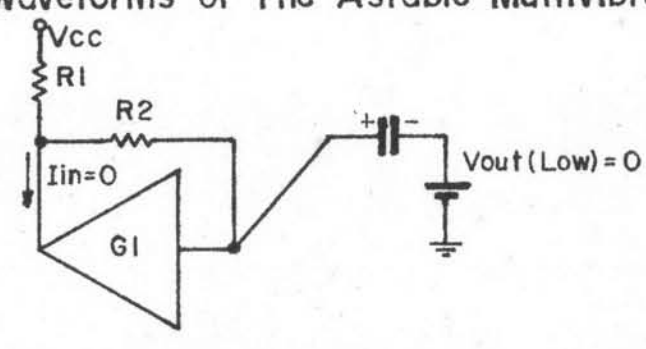


FIG. 3.13 Equivalent Circuit for Calculating The Period of Oscillation.

nearly V_{TH} (the threshold level of the gate G_2), gate G_2 starts to conduct. Capacitor C_2 then discharges through the output of gate G_2, hence an exponential decay is observed at the gate G_2 output (shown by Fig. 3.11d). At $t = t_0$, the voltage at B just rises beyond V_{TH}, immediately the gate G_2 is switched ON. Sudden transition to the ON state of the gate G_2 causes a sharp drop at A, turning the gate G_1 OFF (Fig. 3.11b). The step rise at the output of the gate G_1 depends on R_1, R_2, C_2 and C_1 R_4, and after the step rise (t_0) C_1 still gains furthen charges and voltage at C rises towards Vcc. At the instant after the step rise C_2 also charges through R_1 and R_2 until $t = t_1$ the voltage at A reaches V_{TH} of the gate C_1 (Fig. 3.11a) gate G_1 starts to conducts and after it passes through the threshold level of the gate G_1, gate G_1 is switched OFF (Fig. 3.11c). And after that the cycle repeats itself.

3.4.1 Timing Considerations

The time for each gate to make transition depends on the time required by C_1 and C_2 to charge to the threshold level of the gates and is approximately given by:

$$v_c = v_f + (v_i - v_f)\, e^{-t/RC}$$

where v_c = the voltages on C_1 and C_2 at any instant.

v_i = initial voltage on C_1 and C_2 at time $t = t_0$

v_f = final voltage on C_1 and C_2 if it is allowed to charge for infinite time.

R = resistance in the charging path for C_1 or C_2.

Considering either gate when is in the OFF state suppose gate 1 OFF one can draw an equivalent circuit as shown in Fig. 3.12

Hence $R = R_1 + R_2$

$$C = C_2$$

$$v_i \approx 0$$

$$v_f = V_{cc}$$

For $t = T_1, v_c = V_{TH}$, hence

$$V_{TH} = V_{cc} + (0 - V_{cc})\, e^{-T_1/(R_1 + R_2)C_2}$$

$$T_1 = (R_1 + R_2)C_2 \ln \left(\frac{1}{1 - V_{TH}/V_{cc}}\right)$$

For symmetrical circuit $(R_1 + R_2) = (R_3 + R_4)$ and $C_1 = C_2$

$$T = \text{period} = 2(R_1 + R_2)C_1 \ln \left(\frac{1}{1 - V_{TH}/V_{cc}}\right)$$

3.5 DESIGN OF PULSE NARROWING CIRCUIT [9], [10]

Often, the controlling input signals received by a sequential system are not in pulse form. In this case, they must be converted into pulse form, usually by a special pulse-narrowing circuit called a pulse generator. The pulse generator circuit responds to changes in its input signal rather than to the logical value of its input. This type of input is said to be transition sensitive, or edge-coupled, indicating its sensitivity to changes in logical value.

The pulse-narrowing action of the pulse generater can be achieved in a variety of ways. In TTL and DTL digital circuits, a resistance-capacitance (R-C) differentiative circuit is often used to generate such a pulse. The diagram and characteristics of such a circuit are shown in Fig. 3.14 and 3.15.

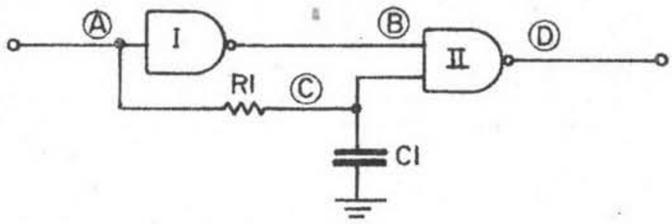


FIG. 3.14 Pulse Narrowing-Circuit.

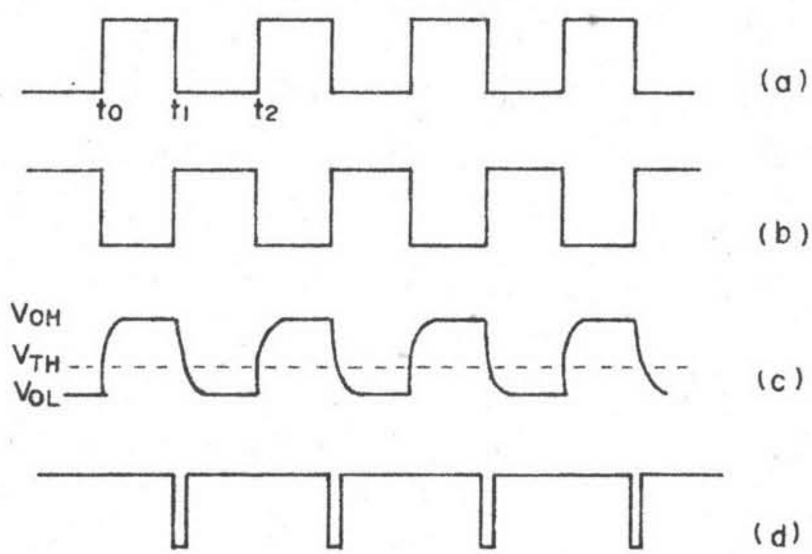


FIG. 3.15 a) Waveform at The Input of The Pulse Narrowing Circuit
b) Waveform at B is The Invert of A.
c) Waveform at A is Delayed by an R-C Circuit at C.
d) Waveform at D the Differentiator Output.

The width of the output pulses can be found as follow :

Prior to $t = t_1$ voltage at the input of the circuit (at A) is High. Voltage at B is the inversion that of A, hence it must be Low. If the width of the input pulse is long enough for $R_1 C_1$ to charge to its final value which is usually be the case, then potential at C must be equal to V_{OH}, the high level of the input voltage. The output of the circuit is $\overline{B}C$, hence it must be High and approximately equal to V_{OH}. At $t = t_1$ the input makes an abrupt transition from High to Low causes the voltage at B to change to the High state, C then discharges from V_{OH} to V_{OL}. At this instant the output then jump from High to Low and remains Low until voltage at C decays passing the gate threshold level(V_{TH}), it then switch High again and remain in this state until the input make another transition to Low again.

The width of the output pulse can be found from the equation below :

$$v_c = v_f + (v_i - v_f)\, e^{-t/R_1C_1}$$

where v_c = voltage on capacitor C_1 at the discharge instant

v_f = the final voltage that C_1 must discharge to, and in this case = V_{OL}

v_i = initial voltage on capacitor C_1 before discharge begins and again in this case = V_{OH}

for $t = T$ = pulse width of the output and for small value of $R \approx 220\,\Omega$

$$V_{TH} \approx V_{OL} + (V_{OH} - V_{OL})\, e^{-T/R_1C_1}$$

$$T \approx R_1C_1 \ln \left(\frac{V_{OH} - V_{OL}}{V_{TH} - V_{OL}}\right)$$