CHAPTER 3

THE SOLID-STATE INVERSE TIME-LAG RELAY WITH DEFINITE MINIMUM TIME LAG

3.1 The System Block Diagram

The block diagram of the solid-state inverse time-lag relay with definite minimum time lag is shown in Fig.3.1-1. Block 1 is composed of a current transformer, a voltage or potential transformer, a fullwave bridge rectifier and a d.c. filter. An a.c. input current is converted into a fullwave rectified voltage and a d.c. voltage, proportional to the input current.

$$V_{dc} = K_{dc}(I_{ac}/I_p) \qquad (3.1\text{-}1)$$

$$V_{ac} = K_{ac}(I_{ac}/I_p) \qquad (3.1\text{-}2)$$

where V_{dc} = the d.c. output voltage

V_{ac} = the a.c. fullwave rectified peak voltage

K_{dc} = a proportionality constant

K_{ac} = a proportionality constant

I_{ac} = the a.c. input current

I_p = the pick-up current (the current at which the relay starts operating)

Block 2 consists of an amplifier and an integrator. The amplifier amplifies V_{dc} into the form of a d.c. current which is integrated by the integrator. The integrator produces the sweep voltage V_s, proportional to the time, whose sweep speed varies directly as the magnitude

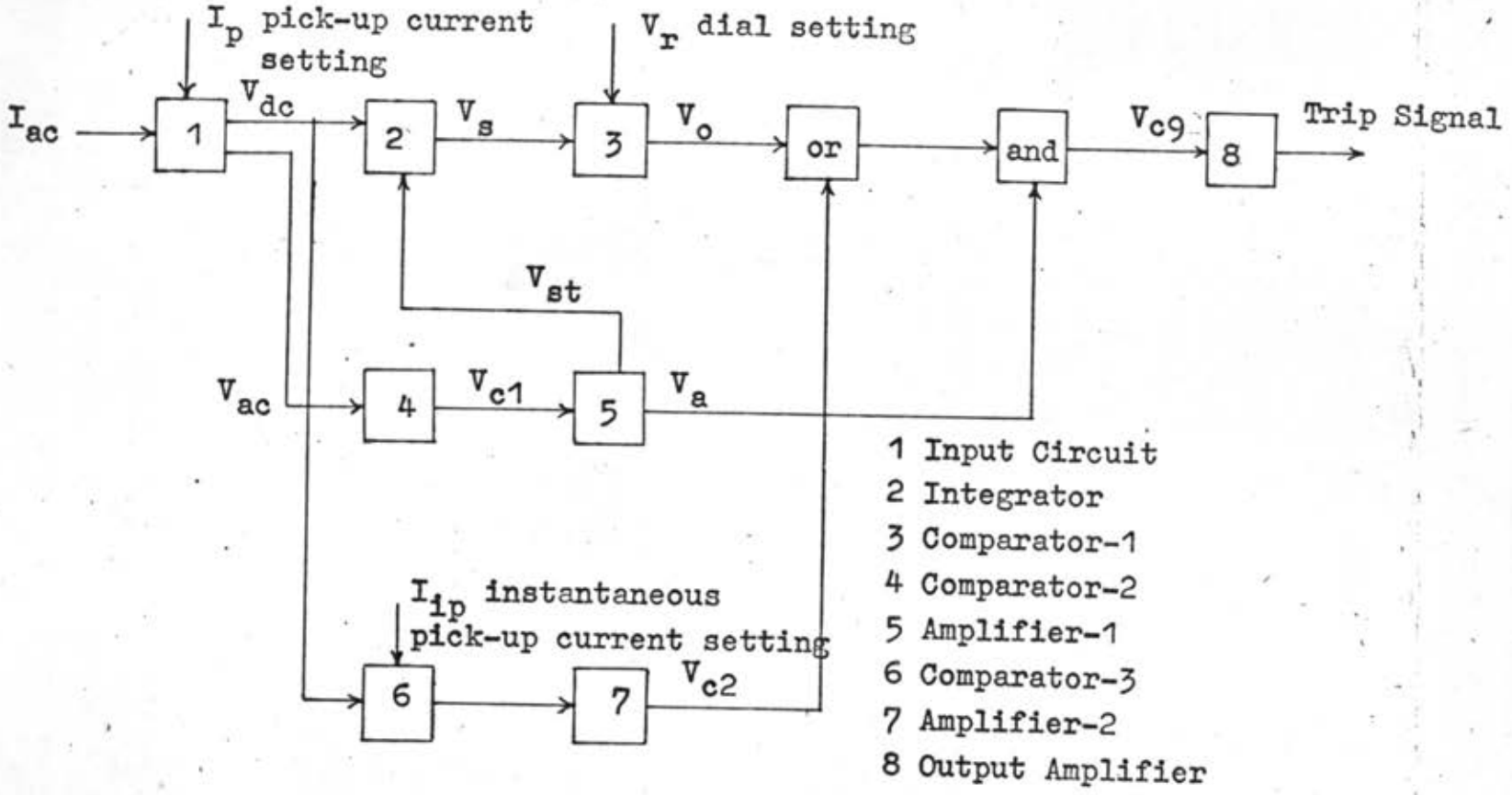

Fig.3.1-1 System Block Diagram of Solid-State Inverse Time-Lag Relay with Definite-Minimum-Time-Lag

of the d.c. current I_{dc}. The integrator will normally not operate unless a starting signal V_{st} from block 5 is received.

$$I_{dc} = K_2 \cdot V_{dc} \tag{3.1-3}$$

$$V_s = K_i \cdot I_{dc} \cdot t \tag{3.1-4}$$

where I_{dc} = the amplified d.c. current

V_s = the sweep voltage of the integrator

K_2 = an amplifier proportionality constant

K_i = an integrator proportionality constant

t = time

Substitute Eq.(3.1-1) into Eq.(3.1-3),

$$I_{dc} = K_{dc} \cdot K_2 \cdot (I_{ac}/I_p) \tag{3.1-5}$$

and substitute Eq.(3.1-5) into Eq.(3.1-4)

$$V_s = K_i \cdot K_{dc} \cdot K_2 \cdot (I_{ac}/I_p) \cdot t \tag{3.1-6}$$

Block 3 is a voltage comparator which produces a trip signal V_o when the sweep voltage V_s equals the reference voltage V_r. Therefore the trip signal V_o is delayed by a certain time which depends on the magnitude of the input current I_{ac}, after I_{ac} has exceeded I_p.

Let V_r = the reference voltage

T = the delay time of the trip signal, after I_{ac} having exceeded I_p

Substitute $V_s = V_r$ and $t = T$ into Eq.(3.1-6) and rearrange, the result is

$$T = V_r/(K_i \cdot K_{dc} \cdot K_2 \cdot (I_{ac}/I_p)) \tag{3.1-7}$$

Equation (3.1-7) is the operating characteristic of the designed relay. It is seen that the operating time T varies inversely proportional to the input current I_{ac}. The pick-up current can be varied by adjusting the variable resistor R_p in block 1. A set of the operating characteristics are obtained by varying the reference voltage V_r. K_1 can be varied by the value of the capacitor of the integrator. K_{dc} and K_2 are fixed by the values of the circuit components.

Block 4 is a comparator, with a hysteresis characteristic, which receives the fullwave rectified voltage V_{ac} from block 1 to determine whether I_{ac} exceeds I_p. If I_{ac} is larger than I_p it generates a pulse train voltage V_{c1}, to indicate an overcurrent condition, which is fed into block 5, the amplifier, the two outputs of which are V_{st} and V_a. These two output voltages are used to start the integrator and to allow the trip signal through the or-gate respectively. Block 6 is also a comparator similar to block 4 , it receives the d.c. voltage V_{dc} from block 1 to determine if the a.c. input current I_{ac} is larger than the instantaneous pick-up current I_{ip} (this block is the definite minimum time-lag or instantaneous unit), if so its output trip signal is amplified by block 7, the amplifier, V_{c2} the output of which initiates the or-gate to produce the final output trip signal. The purpose of using the or-gate is to share the same output amplifier between the delay trip signal V_o and the instantaneous trip signal V_{c2}. The output of the or-gate passes through the and-gate to block 8, the output amplifier, only when the overcurrent signal V_a from block 5

is present. The advantage of using the and-gate is to eliminate the overtravel of the integrator.

3.2 The Designed Circuit

The photograph of the designed solid-state relay is shown in Fig.3.2-1. The designed circuit is shown in Fig.3.2-2. The circuit components are as follows :-

CT. ratio	= 1 : 13
PT. ratio	= 1 : 128
R_p, variable resistor	= 2.5 k
D_1, D_2.....to D_{12}	= 1S121 diode
R_2, potentiometer	= 20 k
R_1	= 12 k
C	= 15 mf
T_1,T_7,T_{13},T_{14},T_{15},T_{17},T_{18}, T_{22},T_{23} and T_{24}	= 2N697 NPN transistor
T_{16}	= OC71 PNP transistor
The rest transistors	= 2S302 PNP transistor
R_{e1}	= 33 k
R_3	= 4.7 k
R_{e2}	= 28 k
C_1	= 200 mf
R_{c3}	= 1.5 k
R_{3a}	= 2.7 k
R_{3b}	= 39 k
D_{z1}	= Zener diode 15 volts

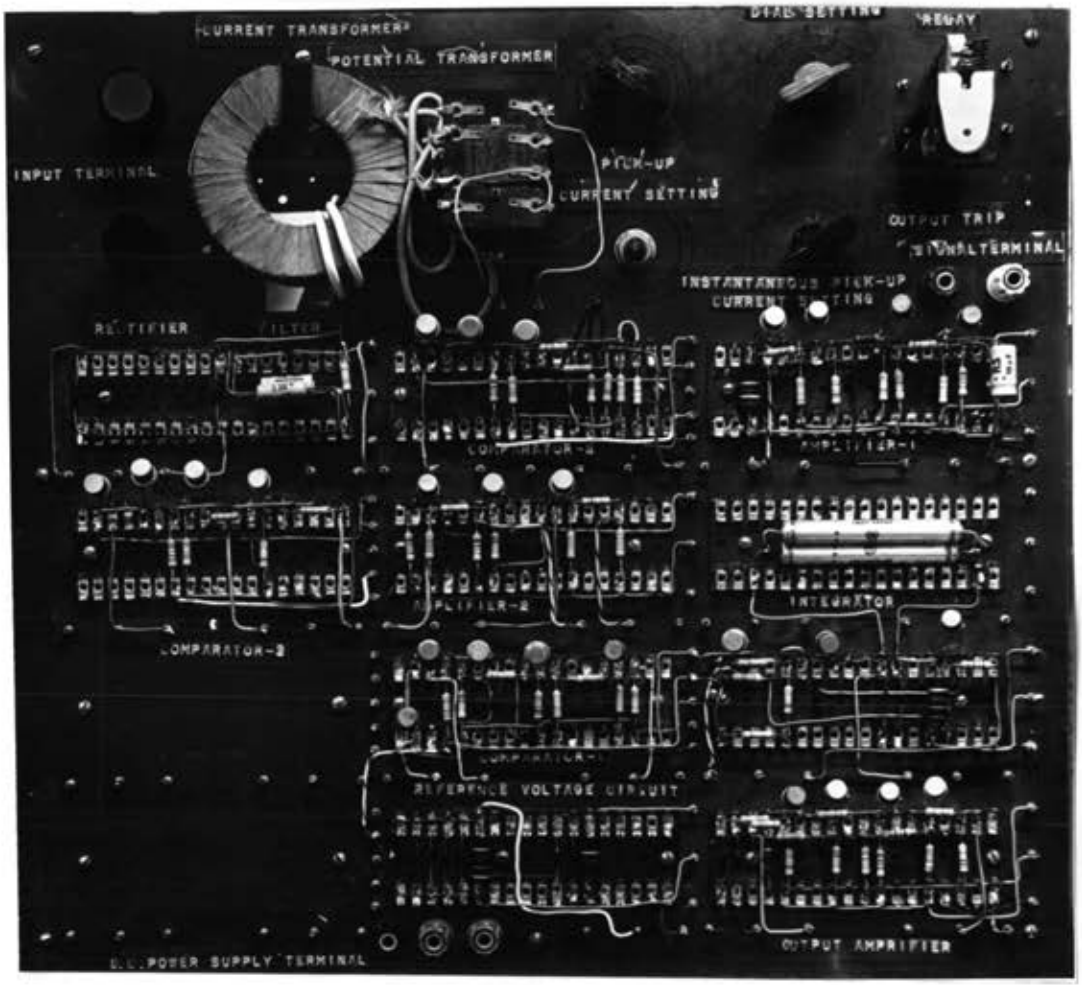

Fig.3.2-1 The Solid-State Inverse Time-Lag Relay with Definite Minimum Time Lag.

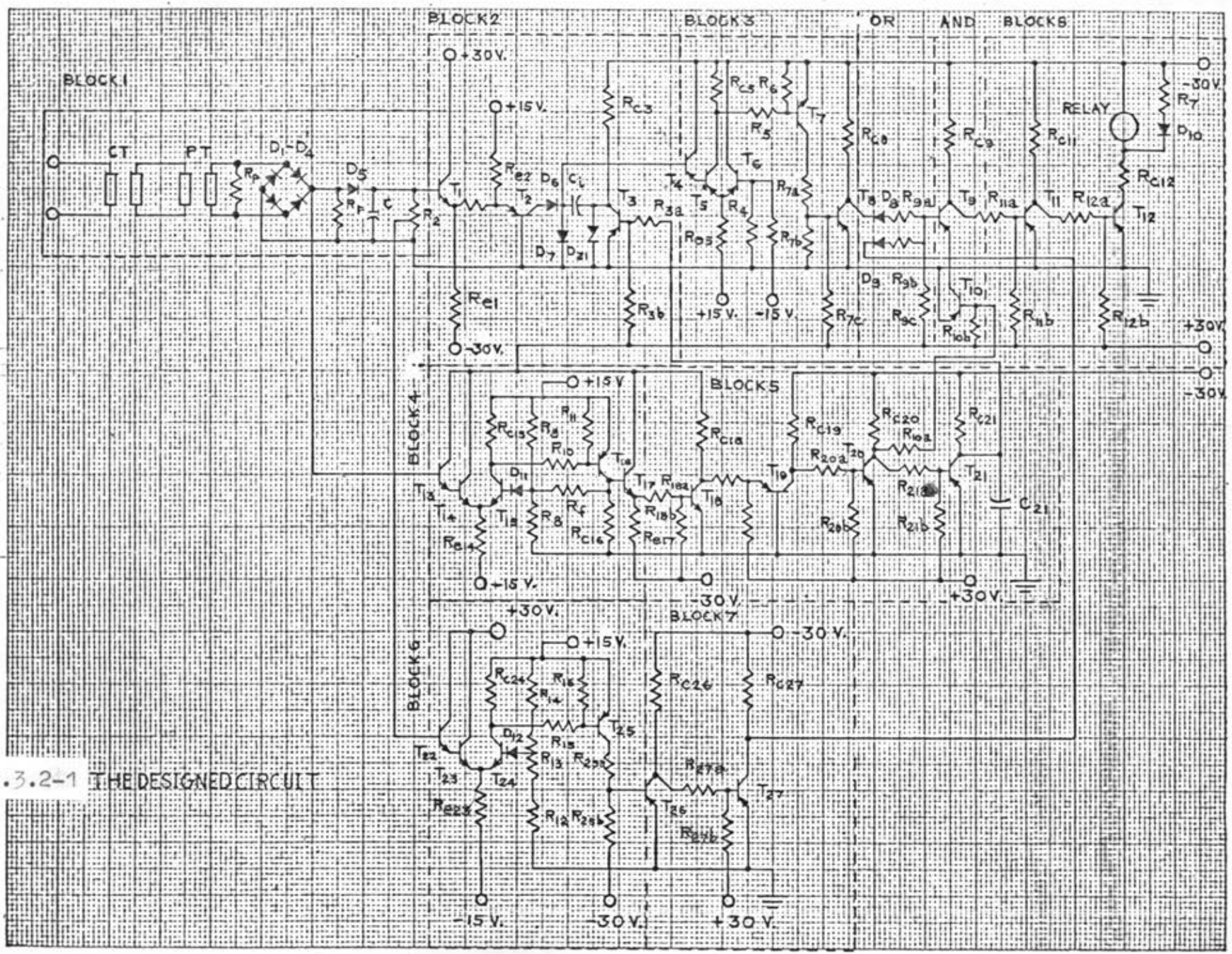

Fig.3.2-1 THE DESIGNED CIRCUIT

R_{e5}	= 5.6 k
R_{c5}	= 5.6 k
R_4, potentiometer	= 5 k
R_5	= 5.6 k
R_6	= 1 k
R_{7a}	= 12 k
R_{7b}	= 2.2 k
R_{7c}	= 33 k
R_{c8}	= 15 k
R_{9a}	= 12 k
R_{9b}	= 12 k
R_{9c}	= 100 k
R_{10a}	= 12 k
R_{10b}	= 100 k
R_{c9}	= 8.2 k
R_{11a}	= 5.6 k
R_{11b}	= 56 k
R_{c11}	= 3.9 k
R_{12a}	= 2.7 k
R_{12b}	= 39 k
R_{c12}	= 0.39 k
R, relay coil resistance	= 1 k

Remark : k = kilo-ohm, mf = micro-farad

R_7	= 0.1 k
R_{e14}	= 15 k
R_{e15}	= 12 k
R_8	= 0.39 k
R_9	= 39 k
R_{10}	= 6.8 k
R_{11}	= 1 k
R_f	= 33 k
R_{e16}	= 10 k
R_{e17}	= 33 k
R_{18a}	= 10 k
R_{18b}	= 68 k
R_{e18}	= 1.8 k
R_{19a}	= 1.5 k
R_{19b}	= 18 k
R_{e19}	= 10 k
R_{20a}	= 8.2 k
R_{20b}	= 82 k
R_{e20}	= 4.7 k
R_{21a}	= 5.6 k
R_{21b}	= 56 k
R_{e21}	= 3.9 k
C_{21}	= 50 mf
R_{e23}	= 15 k

R_{c24} = 12 k

R_{12} = 0.56 k

R_{13}, potentiometer = 5 k

R_{14} = 2.7 k

R_{15} = 6.8 k

R_{16} = 1 k

R_{25a} = 18 k

R_{25b} = 82 k

R_{c26} = 15 k

R_{27a} = 12 k

R_{27b} = 100 k

R_{c27} = 15 k

The operation of the circuit is explained in section 3.4.

3.3 The Design and Test of Each Block

This section is devided into 7 parts, as follows:-

1. the input circuit (block 1)
2. the integrator circuit (block 2)
3. the comparator-1 circuit (block 3)
4. the comparator-2 circuit (block 4)
5. the comparator-3 and amplifier-2 circuit (block 6 and 7)
6. the amplifier-1 circuit (block 5)
7. the output amplifier and and-or gate circuit (block 8)

3.3.1 The Input Circuit (block 1)

Function :

To produce a fullwave rectified voltage V_{ac} and a d.c. voltage V_{dc}, proportional to the input current I_{ac}.

Circuit and circuit operation :

The input circuit is shown in Fig.3.3.1-1. The current transformer and voltage transfermer produce an a.c. voltage across R_p, proportional to the input current I_{ac}. (One transformer can be used if it is specially designed.) D_1, D_2, D_3 and D_4 form a bridge rectifier which rectifies the a.c. voltage across R_p to be the fullwave rectified voltage across R_1. R_2 and C form a d.c. filter which is separated from R_1 by D_5 so that the voltage across R_1 is still a fullwave voltage. The waveforms of V_{ac} and V_{dc} are shown in Fig.3.3.1-2.

Circuit components :

the current transformer	: the turn ratio 1: 13; 2.5 volt-amp; max. secondary current 5 amp
the voltage transformer	: the turn ratio 1:128; 5 watts; max. secondary current 5 amp
R_p, variable resistor	: 2.5 k; 3 watts
R_2, potentiometer	: 20 k; 3 watts
R_1	: 12 k; 0.5 watts
C	: 10 mf and 5 mf; 50 volts
D_1 to D_5	: 1S121 diodes; 150 volt peak reverse voltage; 200 ma max. average forward current

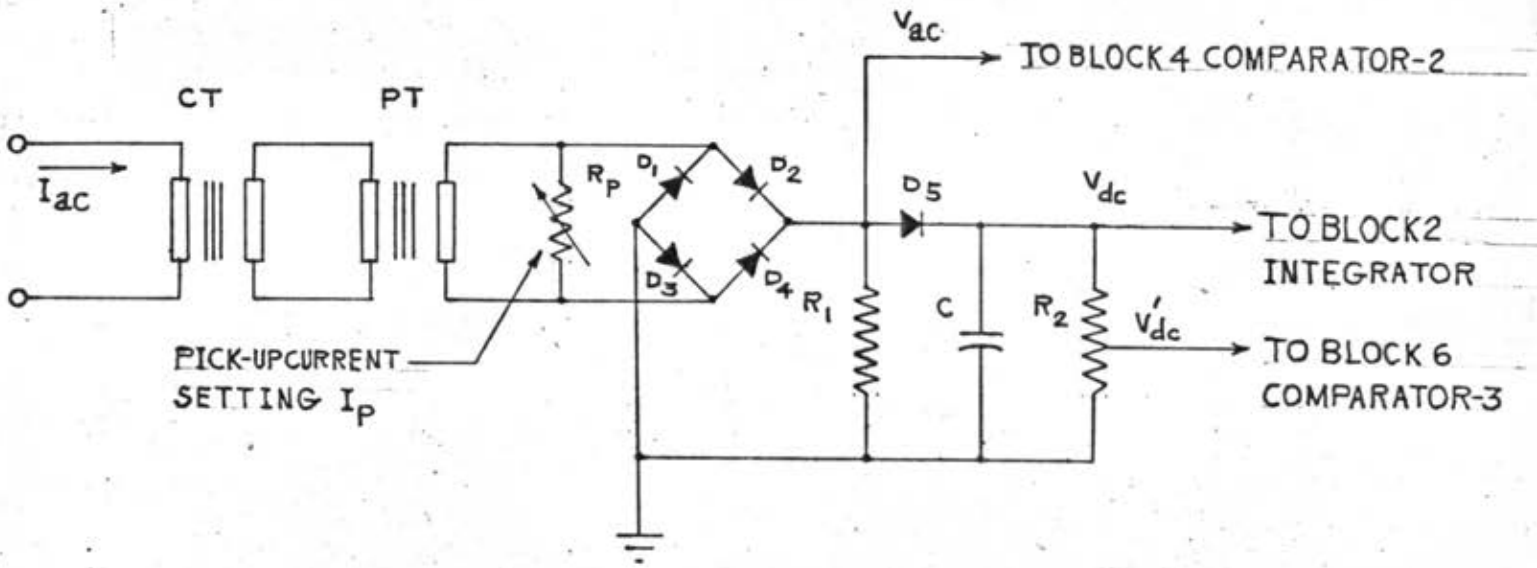

Fig.3.1.1-1 INPUTCIRCUIT (BLOCK 1)

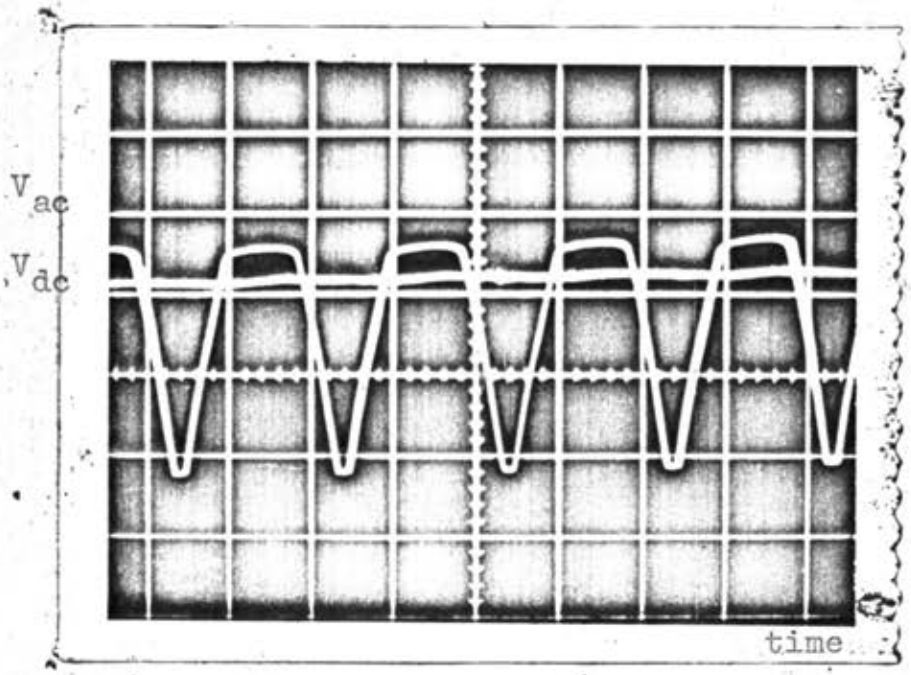

Fig.3.3.1-2 THE WAVEFORMS OF V_{ac} AND V_{dc}

Design :

In order to obtain a linear relation between the input current and the output voltage, the current transformer should not saturate. The saturation depends on the secondary load of the current transformer.

Max. secondary voltage of CT = 2.5/5 = 0.5 volts

Choose R_p = 2.5 k

This value of R_p will not saturate the current transformer for the variations of I_{ac} from 1 to 20 amp (1 amp is the pick-up current and 20 amp is 20 times of pick-up current).

For I_{ac} = 20 amp,

the secondary voltage of CT $= (20/13)*(2.5*10^3/128^2)$

$= 0.235$ volts

This voltage is less than 0.5 volts, therefore the current transformer does not saturate, and still some voltage is left for the resistance of the voltage transformer which is not considered.

For 1 amp input current, the output voltage across R_p, without the bridge rectifier load, is

$(1/(13*128))*2.5*10^3 = 1.5$ r.m.s. volts = 2.22 peak volts

This voltage is large enough to overcome the toe voltage of the bridge rectifier diodes, which is about 1.2 volts.[1]

Remark : * denotes multiplication.

[1] The toe voltage of the silicon diode is approximately 0.6 volts. Millman, Jacob and Taub, Herbert. 1965. Pulse,Digital and Switching Waveforms. New York: McGraw-Hill Book Co.Inc. Chapter 6 Sec.6.1 P 181.

R_1 is chosen so that it does not bypass too much current from R_p.

Let R_1 = 12 k

R_2 is chosen much larger than R_p so that a small capacitor can be used to filter out the d.c. voltage.

Choose R_2 = 20 k

Let wR_2C = 100

Ripple factor[1] = 0.01

$w = 2*3.1416f = 2*3.1416*50 = 314.16$ rad/sec

therefore,

$C = 100/(314.16*20*10^3) = 15.9$ mf

The capacitors of 10 mf and 5 mf are used.

Experiment :

To determine the relation of the current I_{ac} and the output voltage V_{ac} and V_{dc}.

Equipments :

2 Simpson voltmeters with 1 adapter

1 Oscilloscope

1 Variac-4.5 kva

1 Variac-1 kva

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[1] Ryder, J.D. Engineering Electronics. New York : McGraw-Hill Book Co. Inc. Chapter 10 section 4 Page 339.

Procedure :

The experiment circuit is shown in Fig.3.3.1-3. The two variacs are used to adjust the desired input current which is measured by the simpson voltmeter with adapter. The corresponding output voltages V_{ac} and V_{dc} are measured by the oscilloscope and the simpson voltmeter respectively. The readings are tabulated in table 3.3.1-1.

Result :

The graph of V_{dc} against I_{ac} is shown in graph sheet 3.3.1-1. The voltage V_{dc} varies linearly with the input current I_{ac} but the graph does not pass through the origin. This is due to the toe voltage of the diodes. The offset current is about 1 amp. The obtained result does not satisfy Eq.(3.1-1), but a compensation for the offset will be performed to satisfy Eq.(3.1-5) in Sec.3.3.2. V_{ac} needs only one reading for I_{ac} of 1 amp. It is used to design the comparator-2. The ripple of V_{dc} is very small and can not be measured. It can be seen by using the oscilloscope with enlarged scale but the waveform is not stable.

3.3.2 The Integrator Circuit (block 2)

Function :

To produce the sweep voltage V_s whose sweep speed is proportional to the input current I_{dc}.

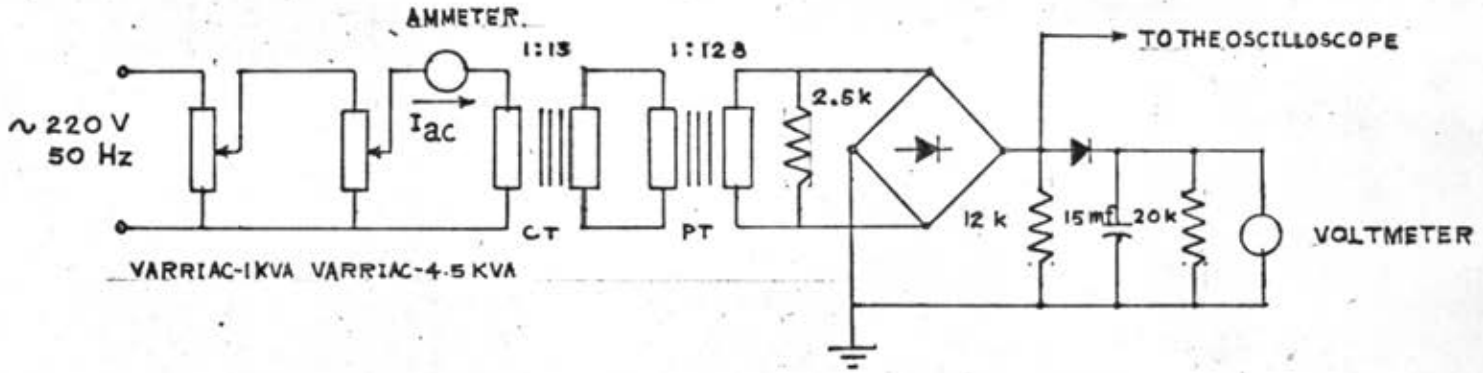
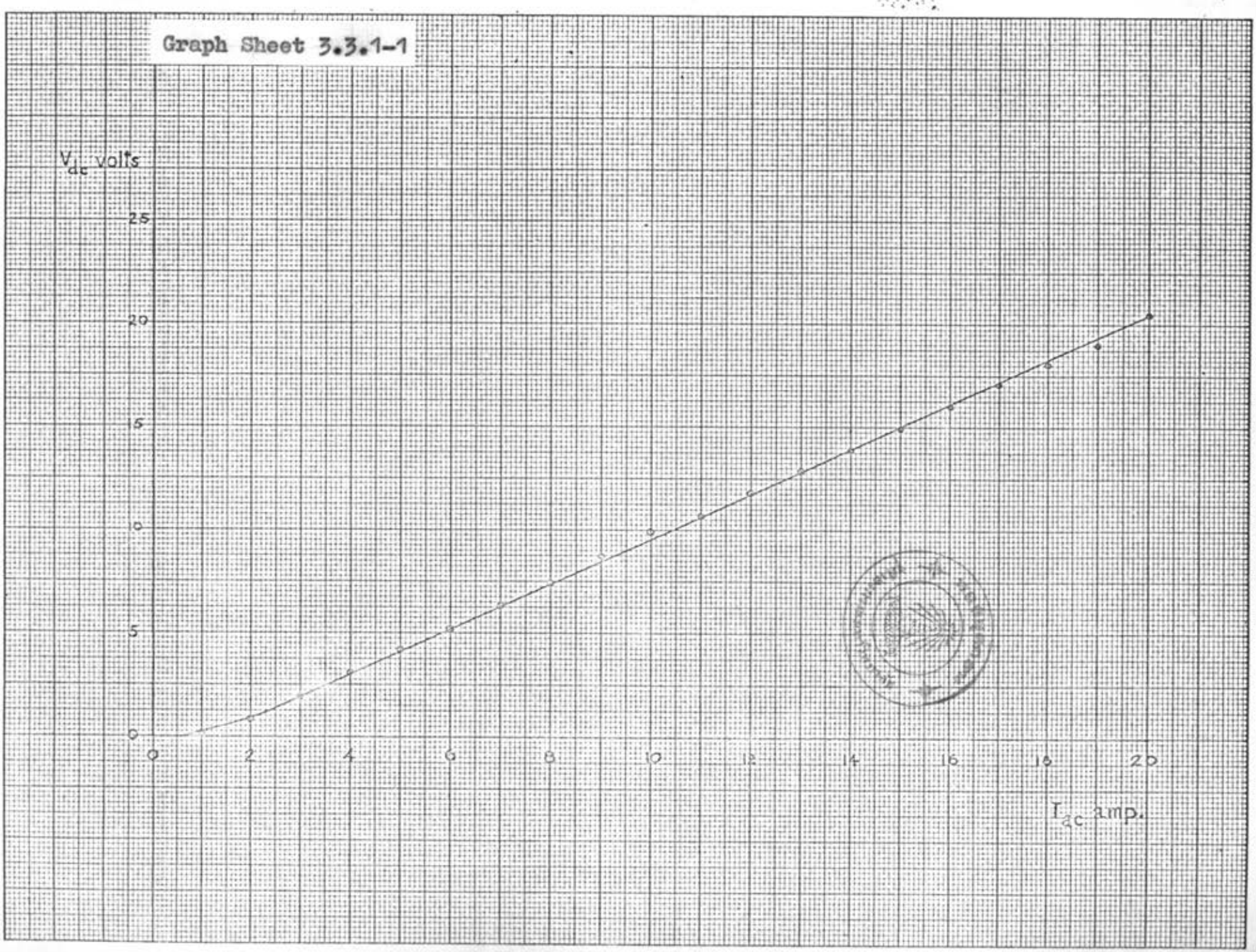


Fig.3.3.1-3 THE EXPERIMENT CIRCUIT

Table 3.3.1-1

I_{ac} r.m.s. amp	V_{dc} volts	V_{ac} peak volts
1	0.1	0.5
1.5	0.4	
2	0.84	
2.5	1.39	
3	1.97	
4	3.1	
5	4.2	
6	5.2	
7	6.3	
8	7.4	
9	8.7	
10	9.8	
11	10.7	
12	11.8	
13	12.8	
14	13.8	
15	14.9	
16	16.0	
17	17.1	
18	18.1	
19	19.0	
20	20.5	

Graph Sheet 3.3.1-1



Circuit and circuit operation :

The integrator circuit is shown in Fig.3.3.2-1. T_1 acts as an emitter follower amplifier which converts the input voltage V_{dc} into the d.c. current I_{dc}. R_{e1} and R_{e2} are biasing resistors. R_3 is the load resistor of T_1. T_2 is used as a constant current source to charge the capacitor C_i linearly. D_6 blocks the capacitor C_i from discharging through the collector of T_2 but through D_7. The zener diode D_{z1} serves as a constant voltage source. T_3 is included in the circuit as a switch to start or stop integration. Normally when an overcurrent does not occur (I_{ac} is less than I_p), V_{dc} is zero and V_{st} is -10 volts or higher. Thus there is a small biasing current flowing into T_2 emitter and T_3 is saturated. In this situation D_{z1} is shorted to ground and therefore no T_2 collector current can flow to charge the capacitor C_i, then the voltage V_s' stays at zero. When an overcurrent occurs V_{st} falls to zero and consequently cuts T_3 off. Now V_{dc}, which is larger than before, causes a certain larger current to flow into T_2 emitter and become T_2 collector current with the aid of D_{z1}, the constant voltage. The T_2 collector current will charge the capacitor C_i linearly until the voltage across it equals the D_{z1} voltage. The time function of the sweep voltage V_s' is given by Eq.(3.3.2-1).

$$V_s' = -15 + a.I_{dc}.t/C_i \qquad (3.3.2\text{-}1)^1$$

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[1] Millman, Jacob and Taub, Herbert. 1965. Pulse, Digital and Switching Waveforms. New York: McGraw-Hill Book Co. Inc. Chapter 14 Sec.7 Page 531.

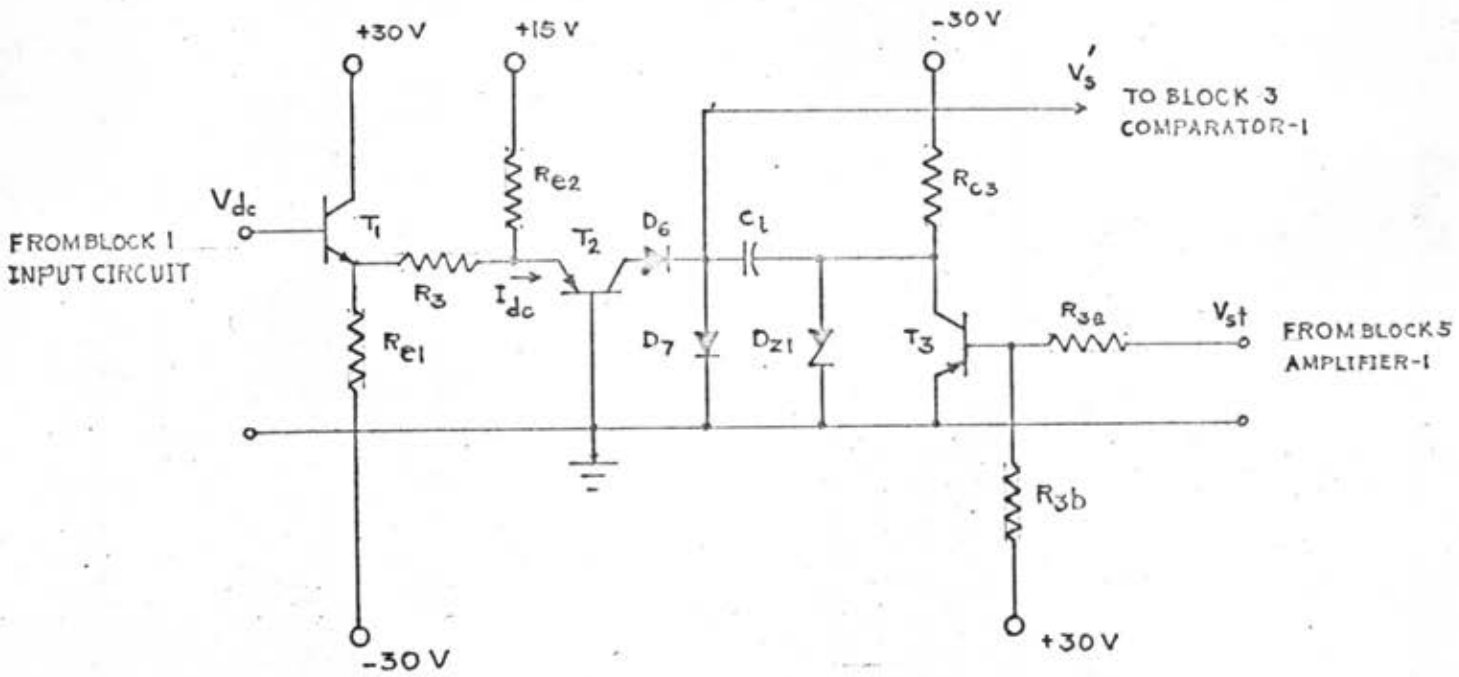

Fig.3.3.2-1 THE INTEGRATOR CIRCUIT (BLOCK 2)

where V_s' = the sweep voltage

-15 = the D_{z1} reference voltage in volts

I_{do} = T_2 emitter current

a = the common base current gain of T_2

C_i = the integrating capacitor

t = time

The charging equivalent circuit is shown in Fig.3.3.2-2 and the waveform of V_s' is shown in Fig.3.3.2-3 (I_{do}= 0.24 ma, C_i= 0.047 mf).

If T_3 is turned on after C_i having been completely charged the voltage across C_i will discharge through D_7 and T_3. V_s' is immediately clamped to the forward voltage drop of D_7 but the collector voltage V_{c3} can not change instantaneously because of the present voltage across C_i. The discharging time depends on the time constant $R_{c3}\cdot C_i$ and the base saturation current of T_3. The discharging equivalent circuit is shown in Fig.3.3.2-4. The variation of the T_3 collector voltage with time is given by Eq.(3.3.2-2).

$$V_{c3} = -15 + (b.I_{b3}.R_{c3} - 15).\left\{1 - \mathrm{Exp}.\left(\frac{t}{R_{c3}.C_i}\right)\right\} \qquad (3.3.2\text{-}2)^1$$

where V_{c3}= the T_3 collector voltage

b = the common emitter current gain of T_3

I_{b3}= the T_3 base saturation current

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[1] Ibid. Chapter 8 Section 12 Page 294.

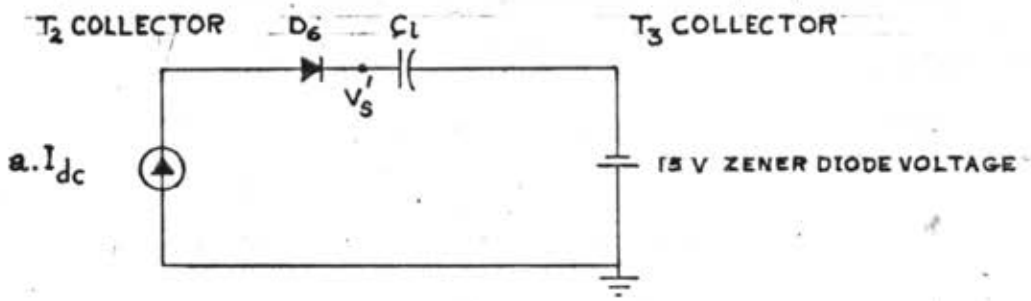

Fig.3.3.2-2 CHARGING EQUIVALENT CIRCUIT

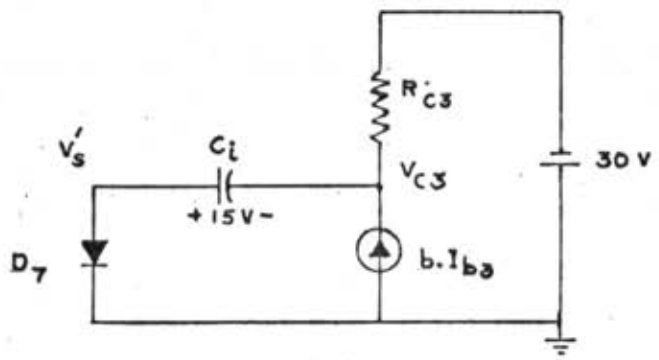

Fig.3.3.2-4 DISCHARGING EQUIVALENT CIRCUIT

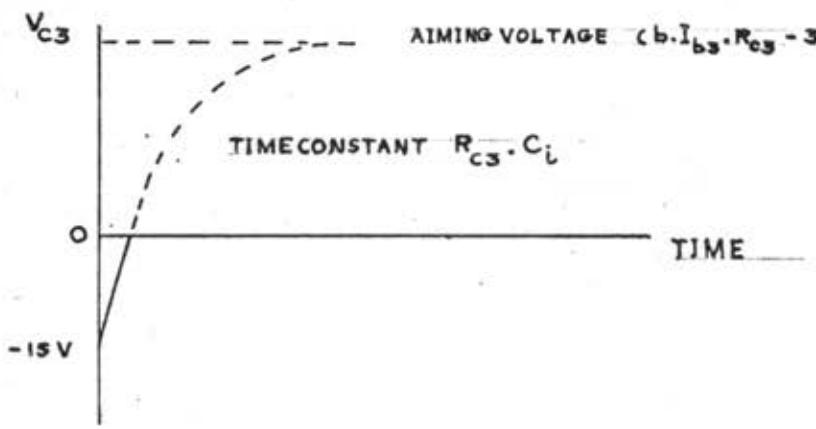

Fig.3.3.2-6 DISCHARGING WAVEFORM

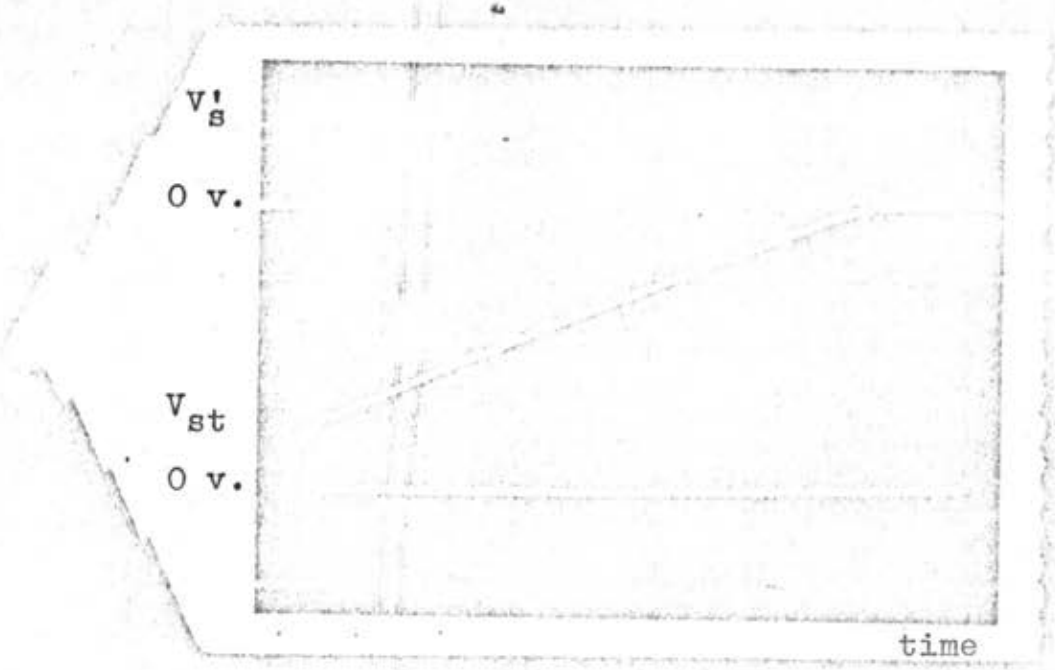

Fig.3.3.2-3 Charging waveform of V'_s .

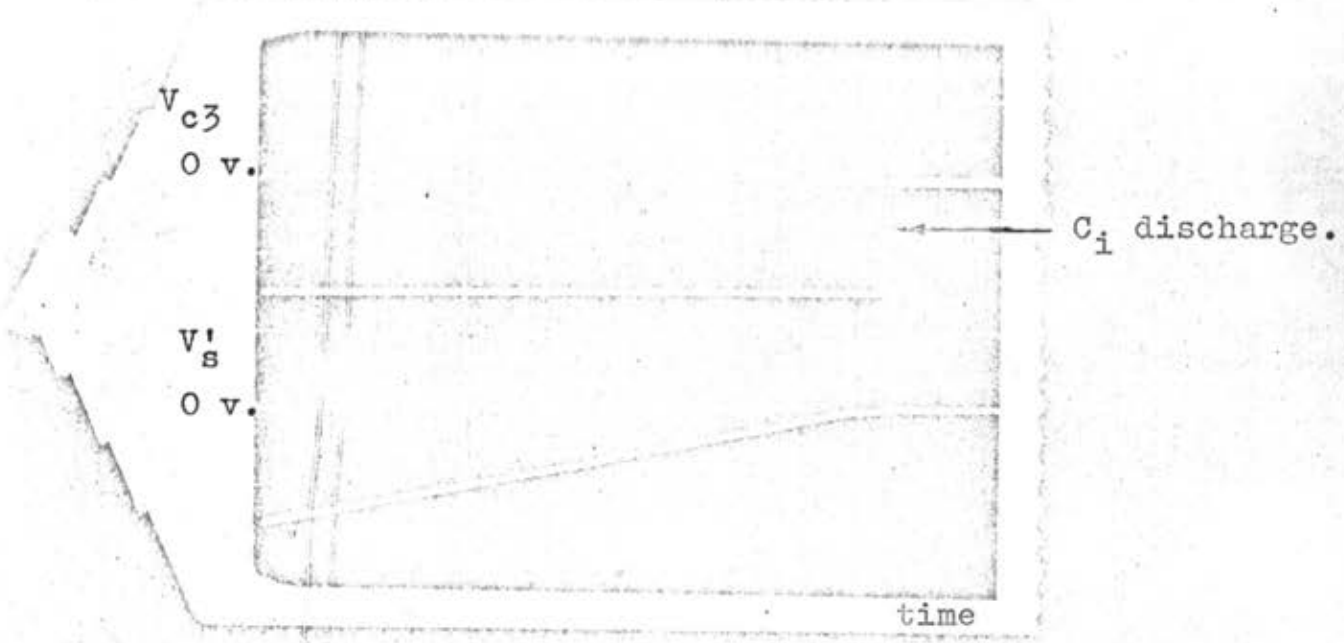

Fig. 3.3.2-5 Discharging waveform of V_{c3}.

The waveform of V_{c3} is shown in Fig.3.3.2-5 (C_i = 0.047 mf, I_{b3} = 3.8 ma). It is seen that V_{c3} changes from -15 volts to 0.3 volts (T_3 collector to emitter saturation voltage) linearly because of the imaginary aiming voltage ($b.I_{b3}.R_{c3}$- 30) is very large (please see Fig.3.3.2-6). The discharging process for C_i having been incompletely charged is the same as the previous discussion. The difference is only that the initial voltage of discharging is less than -15 volts.

Circuit components :

T_1	: 2N697 NPN (see the characteristics in Sec.3.3.7.1)
T_2 and T_3	: 2S302 PNP (see the characteristics in Sec.3.3.7.1)
D_6 and D_7	: 1S121 diode (see the characteristics in Sec.3.3.1)
D_{z1}	: Zener diode; 15 volts ± 5%; 250 mw
C_i	: two 100 mf capacitors; 25 volts
R_{e1}	: 33 k; 0.5 watts
R_3	: 4.7 k; 0.5 watts
R_{e2}	: 27 k and 1 k; 0.5 watts each
R_{c3}	: 1.5 k; 2 watts
R_{3a}	: 2.7 k; 0.5 watts
R_{3b}	: 39 k; 0.5 watts

Design :

Let the maximum power dissipation of D_{z1} is 150 watts.

I_z = 150/15 = 10 ma (see Fig.3.3.2-7a)

Therefore,

R_{c3} = (30 - 15)/10 = 1.5 k

R_3 is chosen so that max. I_{dc} does not exceed the minimum zener diode current I_z. This is because when I_{dc} flows into T_2 emitter and T_3 turns off, T_2 collector current I_{c2} is almost equal to I_{dc}. This collector current decreases the zener dipde current (see Fig.3.3.2-7b).

Let consider the worst situation that I_z is minimum.[1]

$\underline{I}_z = (\underline{30} - \overline{15})/\overline{1.5}$ = (30*0.9 - 15*1.05)/(1.5*1.1) = 6.8 ma (please see Fig.3.3.2-7a)

Therefore the maximum of I_{c2} is 6.8 ma which makes I_z equal zero (see Fig.3.3.2-7b). If at least 1 ma is allowed to flow through to flow through the zener diode so that it will not operate in the region of the knee of its characteristic. Therefore the maximum of I_{c2} is only 5.8 ma which is approximately equal to the maximum of I_{dc}. Since the maximum V_{dc} is 20.5 volts (from Sec.3.3.1),then

R_3 = 20.5/5.8 = 3.54 k

Choose R_3 = 4.7 k (to make sure that I_{dc} does not exceed 5.8 ma)

R_{e1} is the biasing resistor of T_1 and chosen so that about 1 ma flows through T_1 when V_{dc} is zero.

Let R_{e1} = 33 k

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[1] The bar under the symbol or number denotes the minimum value of that quantity. The bar over the symbol or number denotes the maximum value of that quantity.

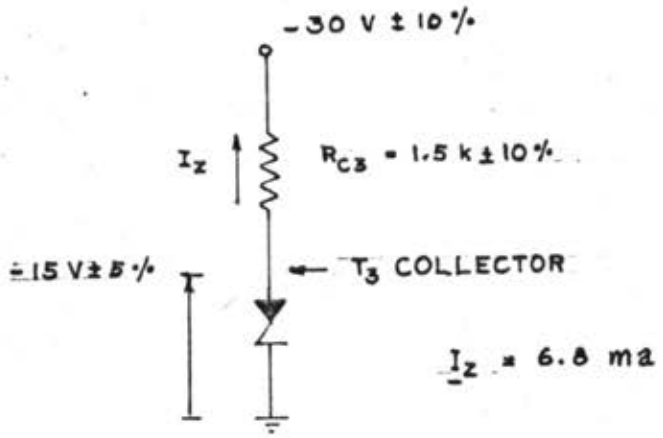

Fig.3.3.2-7 (a) circuit for choosing R_{C3}

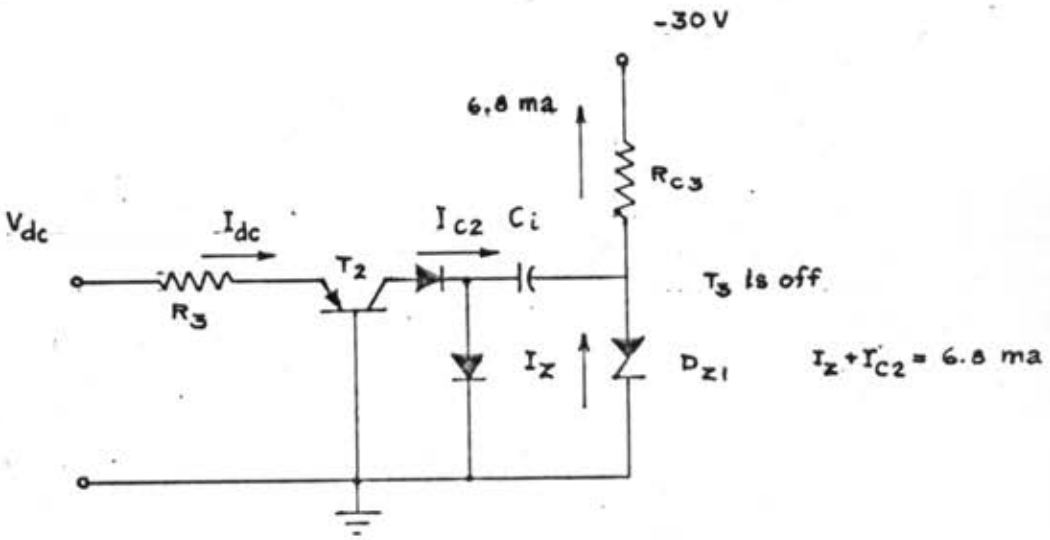

Fig.3.3.2-7 (b) circuit for choosing R_3

To choose the value of R_{e2} an experiment is performed to find the transfer chmracteristic between I_{ac} and I_{dc} (see experiment-1 of this section). The result is shown in graph sheet 3.3.2-1. The curve (a) is the transfer characteristic without R_{e2} in the circuit. The offset on the I_{ac} axis is 2.1 amp. The line (b) is drawn parallel to the line (a) and passes through the origin. On the line (b) I_{ac} equal to 1 amp corresponds to I_{dc} of 0.25 ma. Let bias T_2 to operate at the emitter current of 0.25 ma. When I_{dc} is zero, T_1 and T_2 emitter voltages are -0.6 and 0.6 volts respectively.[1] The current flowing from T_2 emitter to T_1 emitter through R_3 is

$(0.6 + 0.6)/4.7 = 0.26$ ma.

The required current flowing into T_2 emitter is 0.25 ma.

Therefore the current flowing through R_{e2} = 0.26+0.25 = 0.51 ma

$R_{e2} = (15 - 0.6)/0.51 = 28.2$ k

Use two resistors of 27 k and 1 k.

To select the values of R_{3a} and R_{3b} the procedures are followed as in the output amplifier design(in Sec.3.3.7.2).

The two inequalities are

$$R_{3a} \leq 1.15/(26/R_{3b} - 0.1) \qquad (3.3.2\text{-}3)$$

$$R_{3a} \geq 9.2/(33.8/R_{3b} + 2.04) \qquad (3.3.2\text{-}4)$$

The calculated data of the above inequalities are in table 3.3.2-1 and in table 3.3.2-2 respectively.

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[1] Millman, Jacob and Taub, Herbert. 1965. Pulse, Digital and Switching Waveforms. New York: McGraw-Hill Book Co. Inc. Chapter 6 Sec.18 Table 6-1 Page 219.

From graph sheet 3.3.2-2[1]

R_{3a} = 2.7 k ± 5%

R_{3b} = 39 k ± 5%

C_i is chosen corresponding to the desired maximum delay time. Let the maximum delay time is 12 seconds which occurs when the current I_{dc} is minimum which is 0.25 ma. Substitute t= 12 secconds, $V_s' = 0$ and a = 0.93 in Eq.(3.3.2-1), therefore

$C_i = 0.93 \cdot 0.25 \cdot 10^{-3} \cdot 12/15 = 186$ mf

Choose C_i to be 200 mf.

Experiment-1 :

To determine the transfer characteristics between I_{ac} and I_{dc} with and without R_{e2} in the circuit.

Equipments :

1 Current source; Relay Tester Model SR-51; Multiamp Devision Cranford N.J.

1 Sinpson d.c. ammeter

1 Oscilloscope

Procedure :

The experiment circuit is shown in Fig.3.3.2-8. The input

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[1] The rectangular area in graph sheet 3.3.2-2 denotes the possible resistance variation of the resistors.

circuit (block 1) is used to supply the d.c. voltage V_{dc} to the integrator amplifier, with the aid of the current source equipment. The d.c. current I_{dc} flowing into T_2 emitter is read from the simpson ammeter. The comparator-1 (block 4) is used to indicate that I_{ac} of 1 amp corresponds to the designed pick-up current (see comparator-2 in Sec.3.3.4). R_p of the input circuit (block 1) is adjusted in such a way that I_{ac} of 1 amp causes the comparator-1 to generate a pulse train voltage at its output terminal, which is observed by the oscilloscope. Table 3.3.2-3 is the set of readings of I_{ac} and I_{dc}, without R_{e2} in the circuit. Table 3.3.2-4 tabulates the readings of I_{ac} and I_{dc}, with R_{e2} in the circuit.

Result :

Graph sheet 3.3.2-1 shows the relation between I_{dc} and I_{ac}, which are curve (a) before compensation and curve (c) after compensation. It is seen that the extension of curve (c) passes through the origin an therefore Eq.(3.1-5) is satisfied. This will be clear in the next experiment.

Experiment-2 :

To determine the constant $K_{dc}.K_2$ of Eq.(3.1-5).

Equipments :

The same as those in the experiment-1.

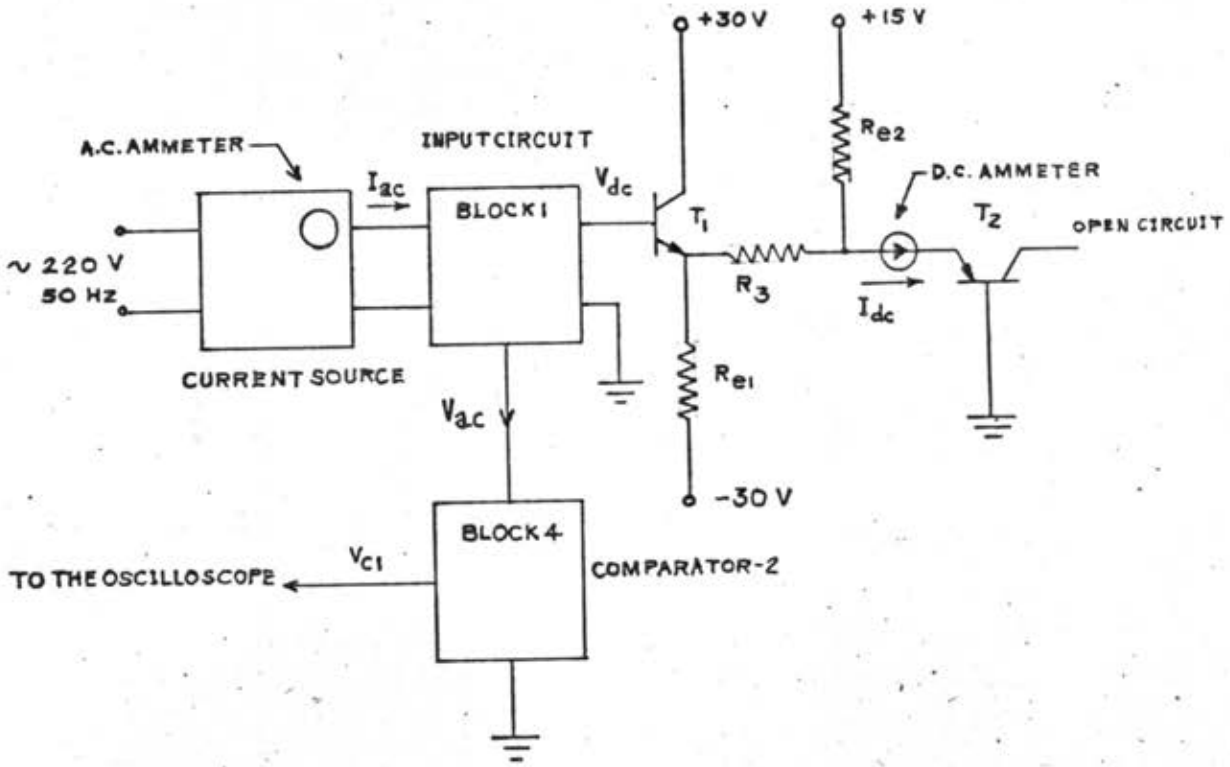


Fig.3.3.2-8 EXPERIMENT-1 CIRCUIT

Procedure :

The experiment circuit is the same as that in the experiment-1. R_p is adjusted for 1 amp pick-up current which is indicated by the pulse train output of the comparator-2 (block4). Readings of I_{dc} are recorded, as tabulated in table 3.3.2-5, for I_{ac} of 1 to 20 amp. The pick-up current setting of 3 amp is also performed and readings of I_{dc} are recorded for I_{ac} of 3 to 60 amp, as tabulated in table 3.3.2-6.

Result :

The curves of I_{dc} and I_{ac} in terms of multiple of pick-up current setting are shown in graph sheet 3.3.2-3 and graph sheet 3.3.2-4 for 1 amp and 3 amp pick-up current respectively.

From graph sheet 3.3.2-3 and 3.3.2-4,

$K_{dc}.K_2 = 4.4/20 = 0.22$ ma/multiple of setting (1 amp setting)

$K_{dc}.K_2 = 4.3/20 = 0.215$ ma/multiple of setting (3 amp setting)

The average value is

$K_{dc}.K_2 = 0.218$ ma/multiple of setting

Therefore $I_{dc} = 0.218\ (I_{ac}/I_p)$

Experiment-3 :

To determine the constant K_i of Eq.(3.1-4).

Equipments :

2 Varible d.c. power supplies, V_a and V_b

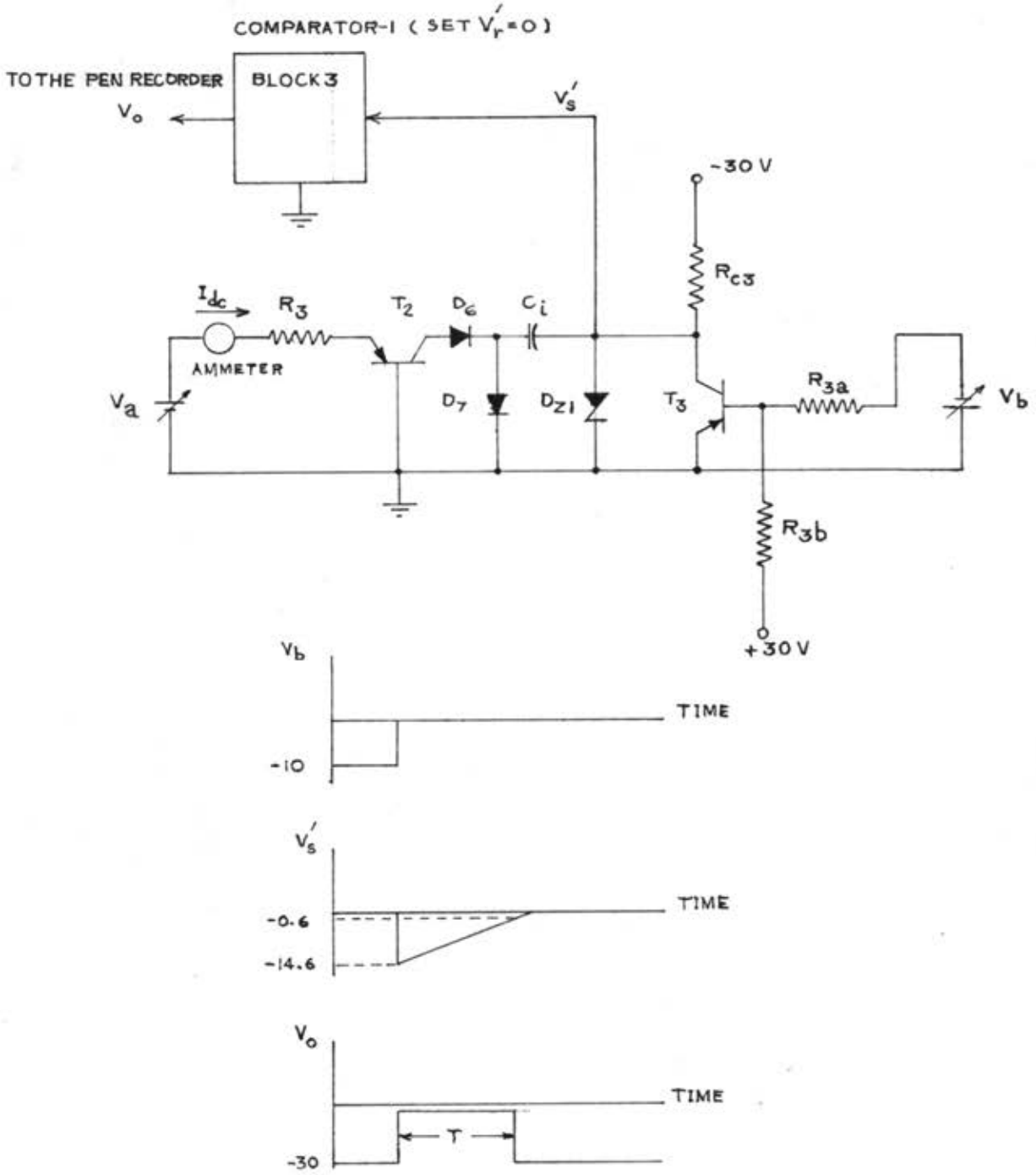


Fig.3.3.29 EXPERIMENT-3 CIRCUIT AND ASSOCIATED WAVEFORMS

1 Simpson d.c. ammeter

1 Set of the pen recorder

Procedure :

The expetiment circuit is shown in Fig.3.3.2-9. The integration of C_i is started by reducing the voltage source V_b from - 10 volts to 0. The desired value of I_{dc} is set by V_a. The sweep voltage V_s' is compared to the reference voltage V_r' of 0 volt. Starting integration causes the output voltage V_o of the comparator-1 (block 3) to change from - 30 volts to -0.1 volts (the saturation voltage of T_8). The sweep voltage V_s' will sweep linearly until it equals the reference voltage V_r' minus 0.6 volts, then the voltage V_o of the comparator-1 returns to - 30 volts again (see comparator-1 circuit and circuit operation and also experiment-1 in Sec.3.3.3). Because of the variations of the reference voltage of the zener diode D_{z1}, the sweep voltage V_s' starts from - 14.6 volts in stead of - 15 volts, therefore Eq.(3.3.2-1) is rewritten as :

$$V_s' = -14.6 + a.I_{dc}.t/C_i \qquad (3.3.2\text{-}5)$$

When V_s' equals $V_r' - 0.6$ volts t equals T, then

$$V_r'-0.6 = V_s' = -14.6 + a.I_{dc}.T/C_i$$

or

$$V_r' +14 = V_s' + 14.6 = a.I_{dc}.T/C_i \qquad (3.3.2\text{-}6)$$

As compared to Eq.(3.1-4),the effective sweep voltage V_s equals $V_s' + 14.6$ and K_i equal a/C_i. The effective reference voltage V_r is

therefore equal to $V_r' + 14$. The delay time T corresponding to each I_{dc} is tabulated in table 3.3.2-7.

Result :

The delay time or time lag T and the current I_{dc} are plotted on the log-log paper as shown in graph sheet 3.3.2-5. The curve is a straight line with the slope of -1.015 and at I_{dc} of 1 ma on the abcissa T ordinate is 3.1 seconds. Therefore the equation of this curve is

$T \cdot I_{dc} = 3.1$ sec-ma (approximate that the slope is 1)

From Eq.(3.1-5) and Eq.(3.1-7) and also $V_r = V_r' + 14 = 14$ volts,

$K_i = a/C_i = 14/3.1 = 4.52$ volt/sec-ma

This can be checked with the calculated value.

$a/C_i = 0.93/(200 \cdot 10^{-6})$ farad^{-1} = volt/sec-amp

$= 0.93 \cdot 10^{-3}/(200 \cdot 10^{-6})$ volt/sec-ma

$= 4.65$ volt/sec-ma

It is noted that the experiment value of K_i or a/C_i is slightly less than the calculated value because of some variations from the nominal values of a and C_i and also the presence of some finite input resistance of the comparator-1. However the conclusion is that

$$V_s = 4.52 \cdot I_{dc} \cdot t \qquad (3.3.2\text{-}7)$$

$$V_r = V_r' + 14 \qquad (3.3.2\text{-}8)$$

Table 3.3.2-1 Calculated data of inequality (3.3.2-3)

R_{3b} k_i	R_{3a} k_i
10	0.46
20	0.96
30	1.49
40	2.09
50	2.74
60	3.49

Table 3.3.2-2 Calculated data of inequality (3.3.2-4)

R_{3b} k_i	R_{3a} k_i
10	1.71
20	2.49
30	2.94
40	3.23
50	3.43
60	3.58

Table 3.3.2-3

I_{ac} amp.	I_{dc} ma.
0	0
1	0
2	0.05
2.5	0.1
3	0.24
3.5	0.35
4	0.49
4.5	0.61
5	0.76

Table 3.3.2-4

I_{ac} amp.	I_{dc} ma
0	0.22
1	0.24
1.5	0.32
2	0.39
2.5	0.49
3	0.6
3.5	0.72
4	0.84
4.5	0.92
5	1.05

Table 3.3.2-5 I_p = 1 amp. pick-up current.

I_{ac} amp.	I_{ac}/I_p multiple of pick-up current	I_{dc} ma.
0	0	0.22
1	1	0.24
2	2	0.39
4	4	0.84
6	6	1.3
8	8	1.7
10	10	2.2
12	12	2.6
14	14	3.1
16	16	3.5
18	18	4.0
20	20	4.4

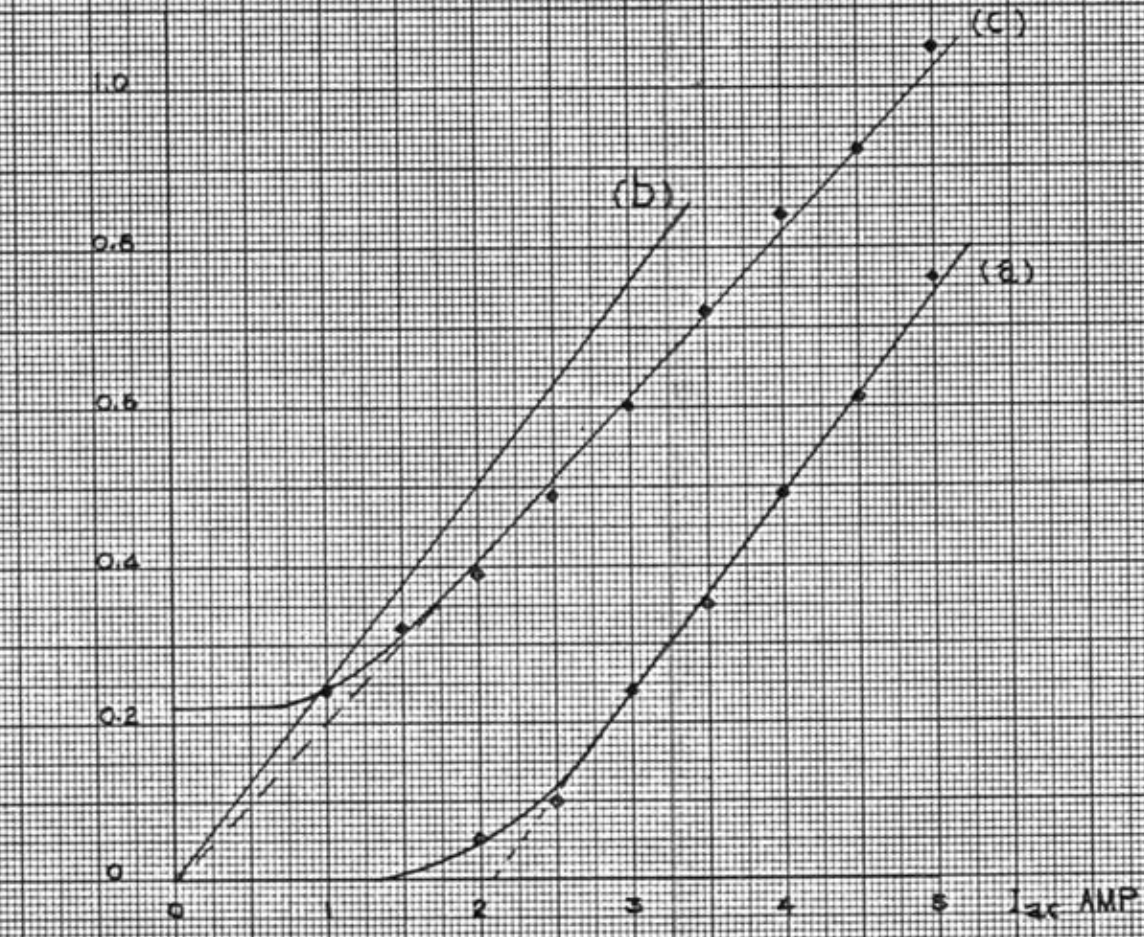
Table 3.3.2-6 I_p = 3 amp. pick-up current.

I_{ac} amp.	I_{ac}/I_p multiple of pick-up current	I_{dc} ma.
0	0	0.22
3	1	0.24
6	2	0.39
12	4	0.84
18	6	1.3
24	8	1.7
30	10	2.2
36	12	2.5
42	14	3
48	16	3.4
54	18	3.9
60	20	4.3

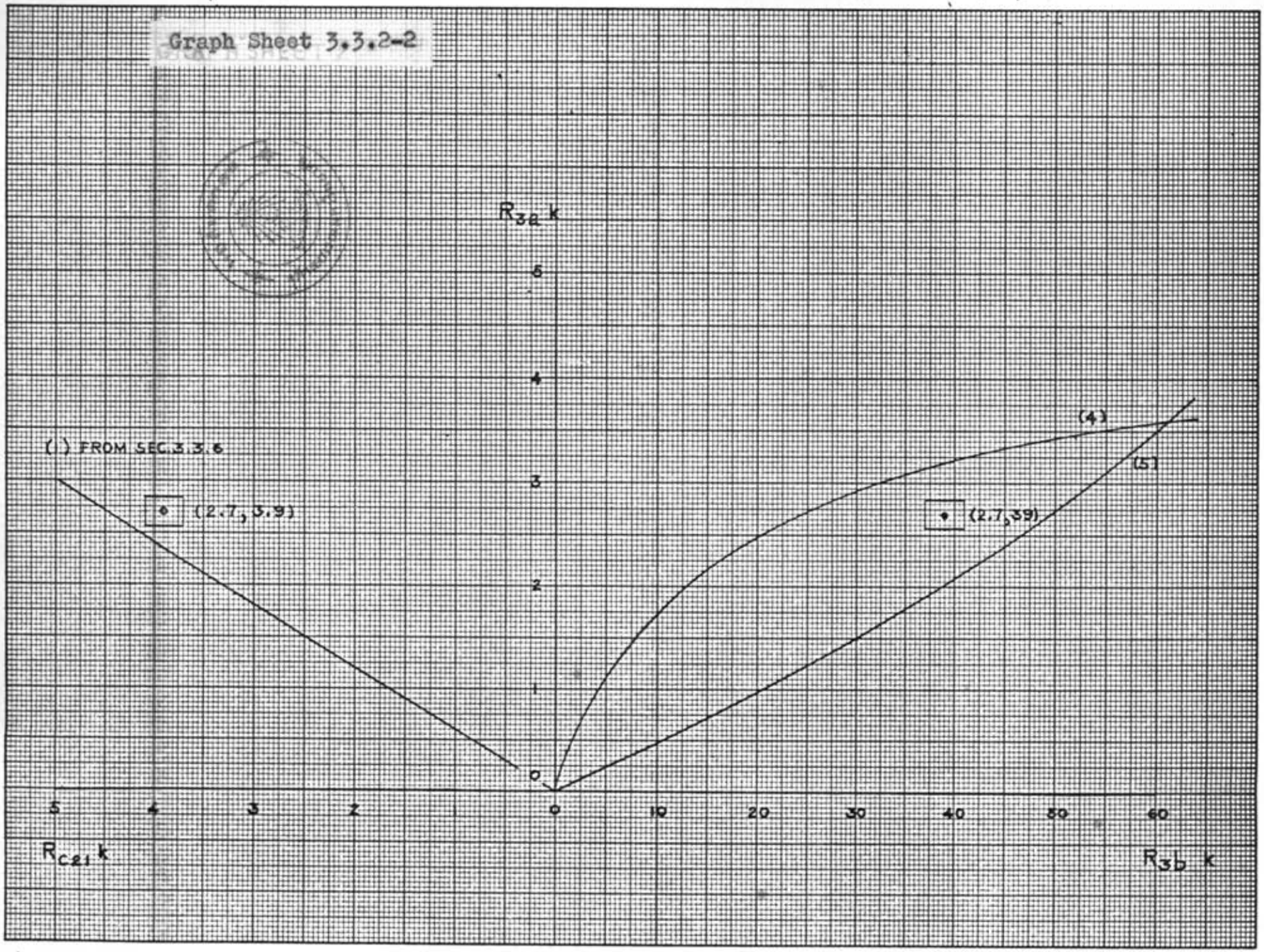
Table 3.3.2-7

I_{dc} ma.	T seconds
0.24	13.15
0.5	6.50
1.0	3.10
1.5	2.04
2.0	1.51
2.5	1.22
3.0	0.99
3.5	0.85
4.0	0.74
4.5	0.65
5.0	0.59

Graph Sheet 3.3.2-1

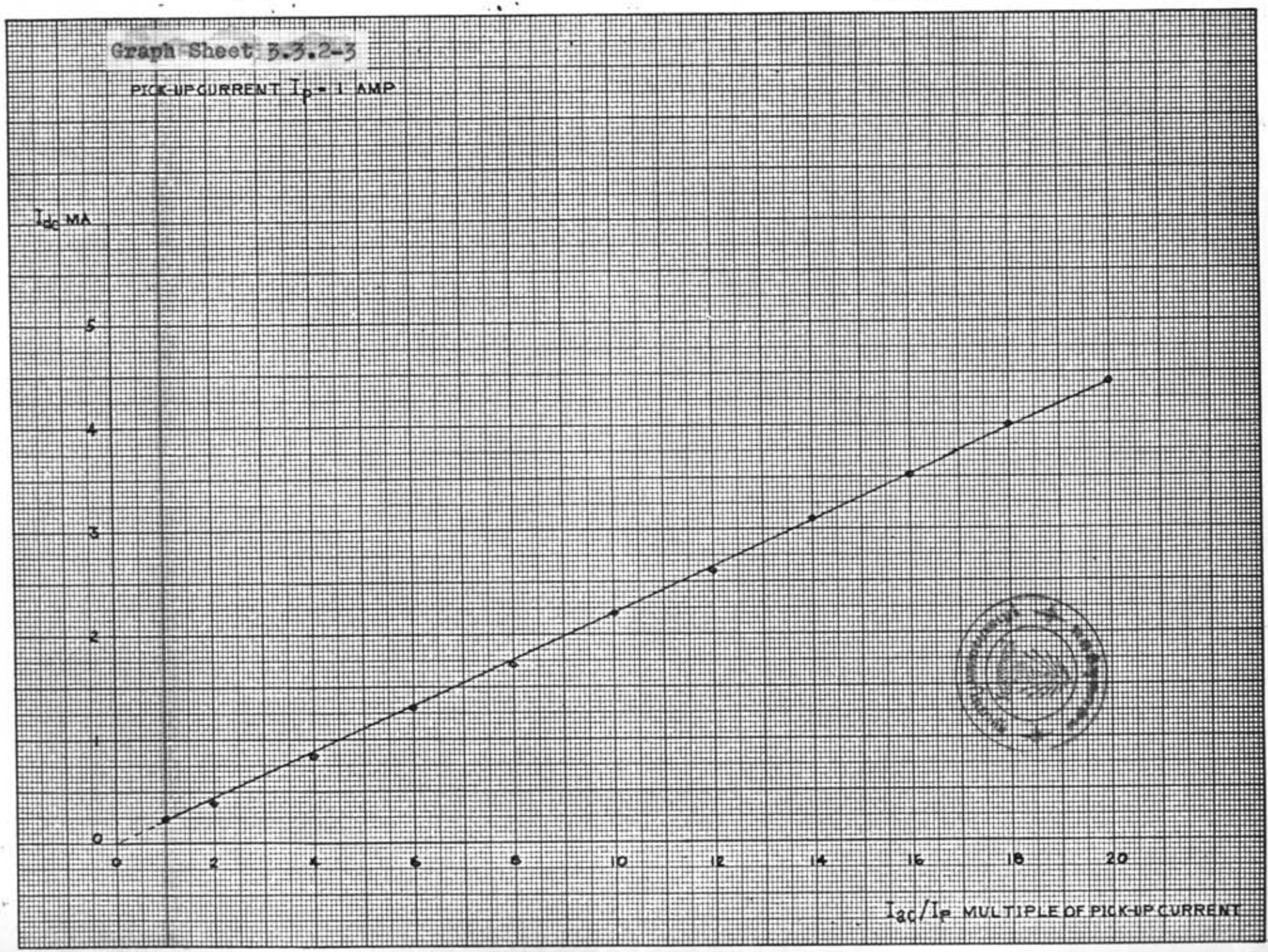


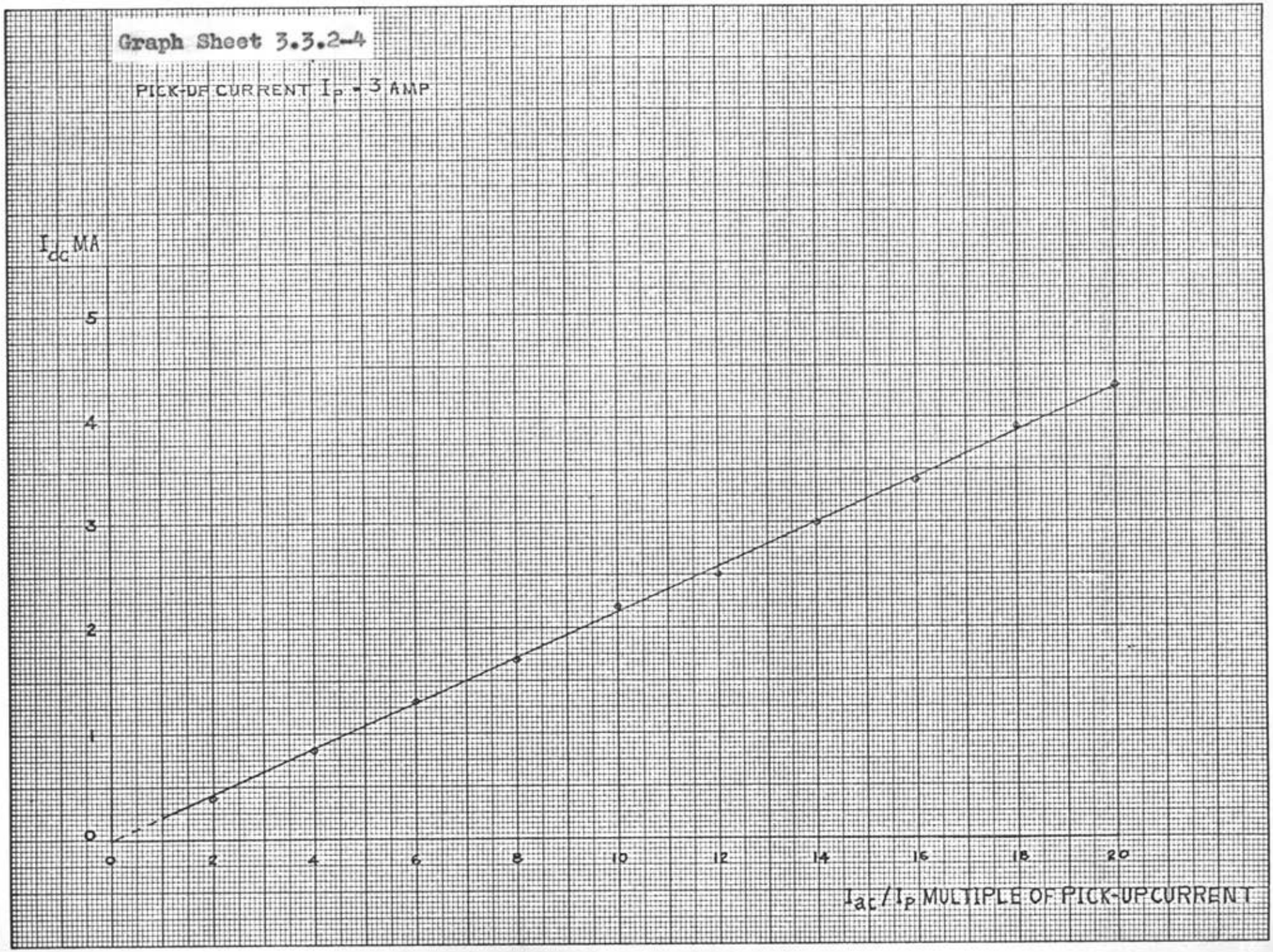
Graph Sheet 3.3.2-2



Graph Sheet 3.3.2-3

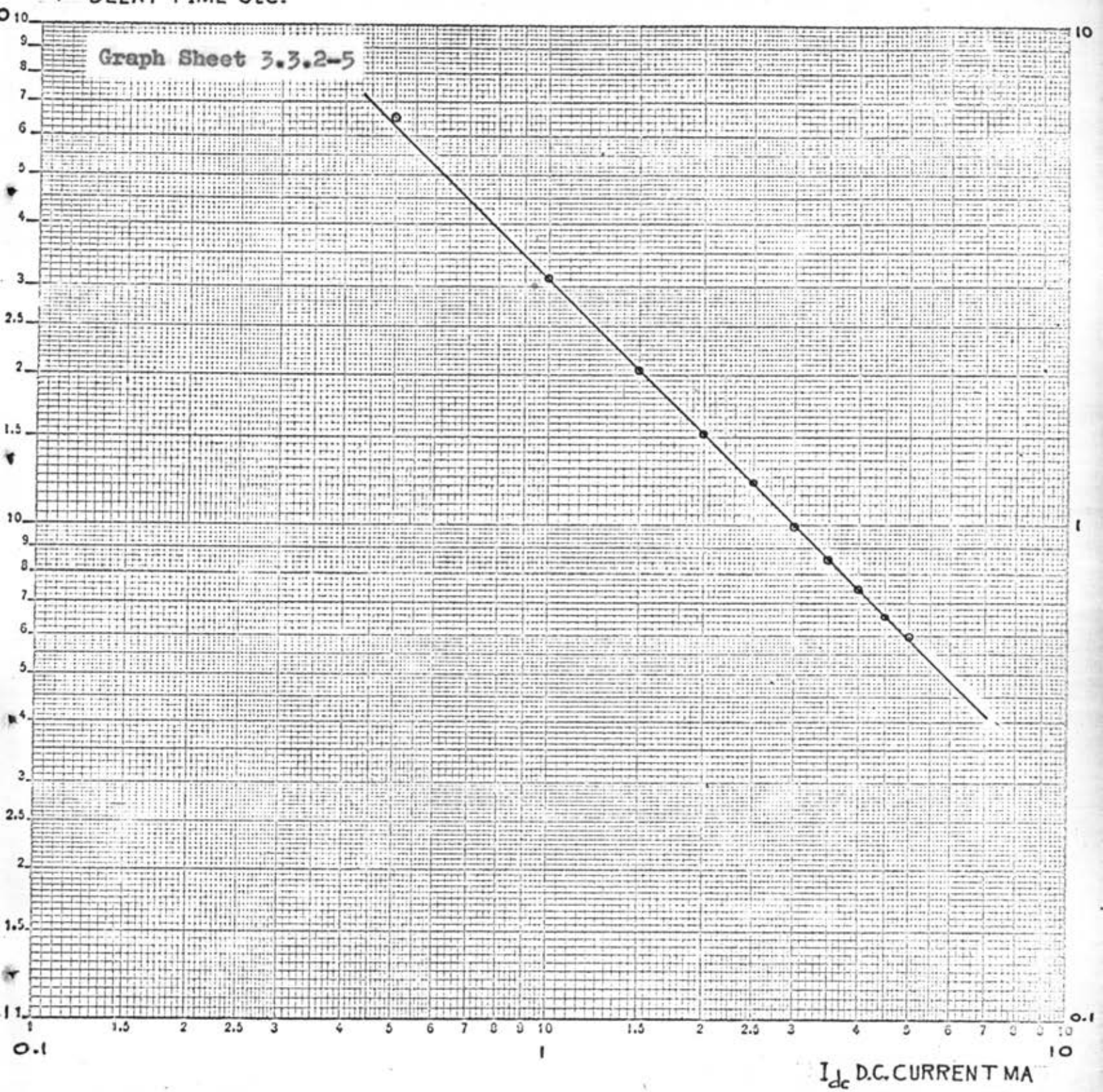
PICK-UP CURRENT I_p = 1 AMP





T DELAY TIME SEC.

T Delay Time Sec.



3.3.3 The Comparator-1 Circuit (block 3)

Function :

To compare the sweep voltage V_s' to the reference voltage V_r' and also to produce an output pulse whose pulse width T equals the sweep time of V_s' from -14.6 volts to V_r' -0.6 volts (see Fig.3.3.3-2).

Circuit and circuit operation :

The comparator-1 circuit is shown in Fig.3.3.3-1. (Note that the reference voltage V_r' is derived from -15 volt constant voltage which is derived from zener diodes, so that V_r' is not disturbed by the variation of -30 volt power supply). T_5 and T_6 form a back-to-back transistor comparator. T_4 increases the input impedance of the comparator. T_7 and T_8 are amplifiers to produce an appropriate signal to the next circuit. Normally T_4 and T_5 are off because V_s' is zero and V_r' stays at some negative level according to the desired dial setting (see experiment-2). T_7 and T_8 are also off because there is no base current flowing into T_7 and T_8 bases. Then V_o is at -30 volts. When the integrator starts operating V_s' changes immediately from 0 to -14.6 volts. Therefore T_4 and T_5 turn on, this makes T_7 and T_8 turn on with the result that V_o falls to the saturation voltage of T_8. Since V_s' does not stay permanently at -14.6 volts but sweeps in a positive-going manner to 0 volt. When V_s' reaches the voltage level of V_r' - 0.6 volts the circuit returns to the initial state,i.e., V_o returns to -30 volts again. The waveforms of V_s' and V_o are shown in Fig.3.3.3-2.

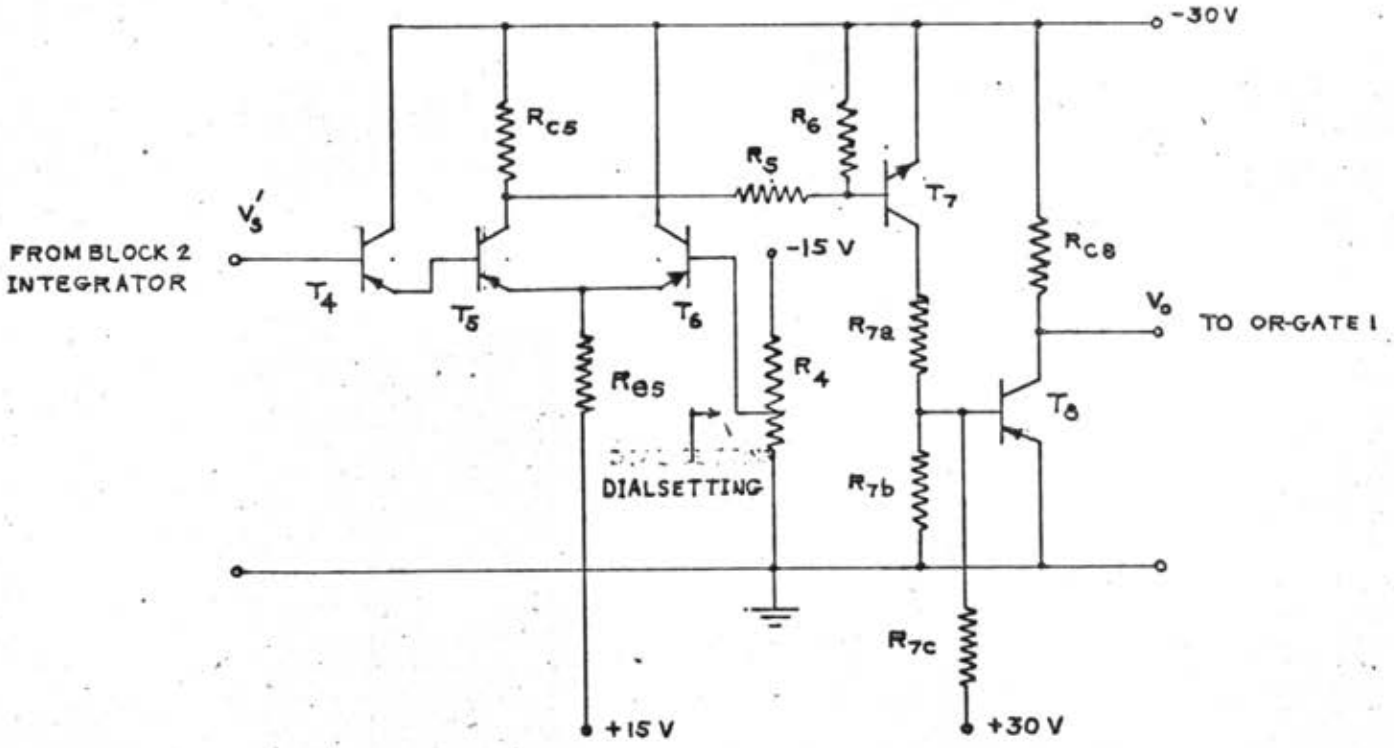


Fig.3.3.3-1 COMPARATOR-CICUIT (BLOCK 3)

3.3.3

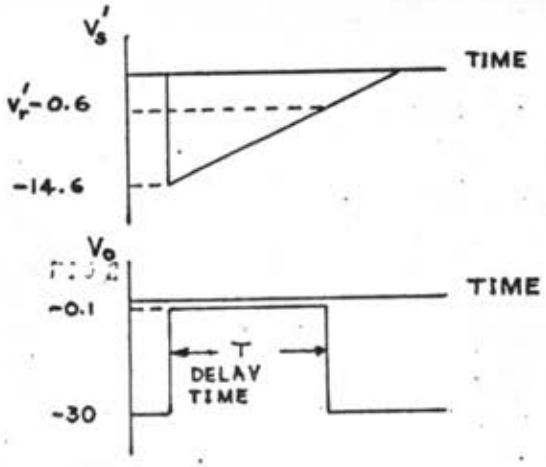


Fig.3.3.3-2 CIRCUIT OPERATION

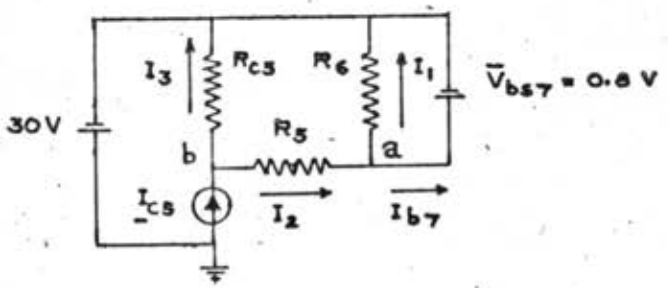


Fig.3.3.3-3 EQUIVALENT CIRCUIT TO DETERMINE R_5

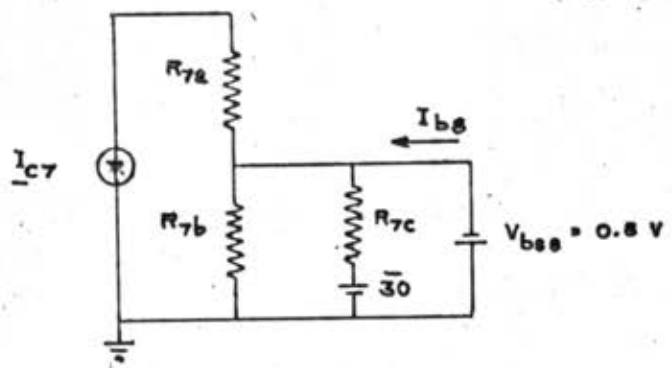


Fig.3.3.3-4 EQUIVALENT CIRCUIT TO CHECK I_{b8}

Circuit component :

T_4, T_5, T_6 and T_8	: 2S302 PNP (see the characteristics in Sec.3.3.7.1)
T_7	: 2N697 NPN (see the characteristics in Sec.3.3.7.1)
R_{e5}	: 5.6 k; 0.5 watts
R_{c5}	: 5.6 k; 0.5 watts
R_4, potentiometer	: 5 k; 3 watts
R_5	: 5.6 k; 0.5 watts
R_6	: 1 k ; 0.5 watts
R_{7a}	: 12 k; 0.5 watts
R_{7b}	: 2.2 k; 0.5 watts
R_{7c}	: 33 k; 0.5 watts
R_{c8}	: 15 k; 0.5 watts

Design :

Let choose R_{e5} = 5.6 k ± 5%

R_{c5} = 5.6 k ± 5%

R_6 = 1 k ± 5%

R_4 = 5 k (potentiometer)

To determine R_5 the equivalent circuit is drawn for the condition that T_5 is on and T_6 is off, as shown in Fig.3.3.3-3.

$I_{c5} = \underline{15}/5.6 = 15*095/(5.6*1.05) = 2.42$ ma

Let the required base current $I_{b7} = 1$ ma

$\bar{I}_1 = 0.8/(1*0.95) = 0.842$ ma

$I_2 = \bar{I}_1 + I_{b7} = 0.842 + 0.1 = 0.942$ ma

$I_3 = \underline{I}_{c5} - I_2 = 2.42 - 0.942 = 1.48$ ma

$\underline{V}_{ba} = I_3 \cdot \underline{R}_{c5} - 0.8 = 1.48*5.6*0.95 - 0.8$

$= 7.86 - 0.8 = 7.06$ volts

In order that I_{b7} be equal to or greater than 0.1 ma R_5 is chosen for the condition that

$R_5 \leq 7.06/0.942 = 7.5$ k

Choose $R_5 = 5.6$ k ±5%

To choose R_{7a}, let consider that when T_7 and T_8 are on R_{7a} can be regarded as the load of T_7 collector. In order that T_7 is saturated R_{7a} must be chosen in such a way that

$R_{7a} \geq (\overline{30}/(\underline{b}_7 \cdot I_{b7}) = 30*1.1/(32*0.1) = 10.31$ k

where $\underline{b}_7 = 32$ = the common emitter current gain of T_7

Choose $R_{7a} = 12$ k ± 5%

R_{7b} and R_{7c} are chosen according to the condition that when T_7 is off T_8 should be off. R_{7b} and R_{7c} form a voltage devider to provide a reverse-bias voltage to cut T_8 off.

Let the minimum cut-off voltage be 1 volt and choose R_{7c} to be 33.k.

Therefore $30*\underline{R}_{7b}/(\underline{R}_{7b} + \overline{33}) \geq 1$

$30*0.9*\underline{R}_{7b} \geq R_{7b} + 33*1.05$

i.e. $\underline{R}_{7b} \geq 34.6/26 = 1.33$ k

Choose $R_{7b} = 2.2$ k ± 5 %

Let check the saturated condition of T_8;

$\bar{I}_{c8} = 33/\underline{R}_{c8} = 33/(15*0.95) = 2.32$ ma

$I_{b8} = \bar{I}_{c8}/\underline{b}_8 = 2.32/12 = 0.194$ ma

The equivalent circuit when T_7 and T_8 are on is shown in Fig.3.3.3-4.

$\underline{I}_{c7} = (27-0.8)/(12*1.05) = 2.08$ ma

By the superposition theorem,

$\underline{I}_8 = 2.08-0.8/(2.2*0.95)-33/(33*0.95)-0.8/(33*0.95)$

$= 2.08 - 0.38 - 1.05 - 0.025 = 0.63$ ma

Therefore T_8 is well saturated.

Experiment-1 :

To check the operation of the circuit.

Equipments :

3 Simpson voltmetrs

1 D.C. power supply

Procedure :

The comparator in Fig.3.3.3-1 is biased with the power supplies as indicated in the circuit. The base of T_4 is connected to the d.c. power supply.V V_s' and V_r' are set at 0 volt. The measured voltage of T_8 collector, V_o is -29.2 volts. Then V_s' is set at -14.6 volts and the voltage V_o is observed to be -o.1 volts. Aftef this, V_s' is

varied slowly to 0 volt and the voltage at which V_o just falls to -29.2 volts again is recorded. The same procedure is repeated with V_r' setting of -1 to -14 volts. The readings are tabulated in table 3.3.3-1.

Result :

The graph of V_s' against V_r' is shown in graph sheet 3.3.3-1. It is seen that V_o makes transition from -0.1 volts to -29.2 volts when V_s' equals V_r' - 0.6 volts.

Experiment-2 :

To calibrate the time dial setting.

Equipments :

The same as those in the experiment-3 in Sec.3.3.2.

Procedure :

The experiment circuit is the same as in the experiment in Sec.3.3.2. From Eq.(3.3.2-8), it is seen that the maximum effective reference voltage V_r is 14 volts. If the effective reference is devided into 10 steps each step will be 1.4 volts. The number of dial setting and the corresponding reference voltage are tabulated in table 3.3.3-2. In order to check if the delay time is proportional to the number of the dial setting, the current I_{dc} is kept constant at 0.22 ma and the time lag or delay time T is measured for each dial

Table 3.3.3-1

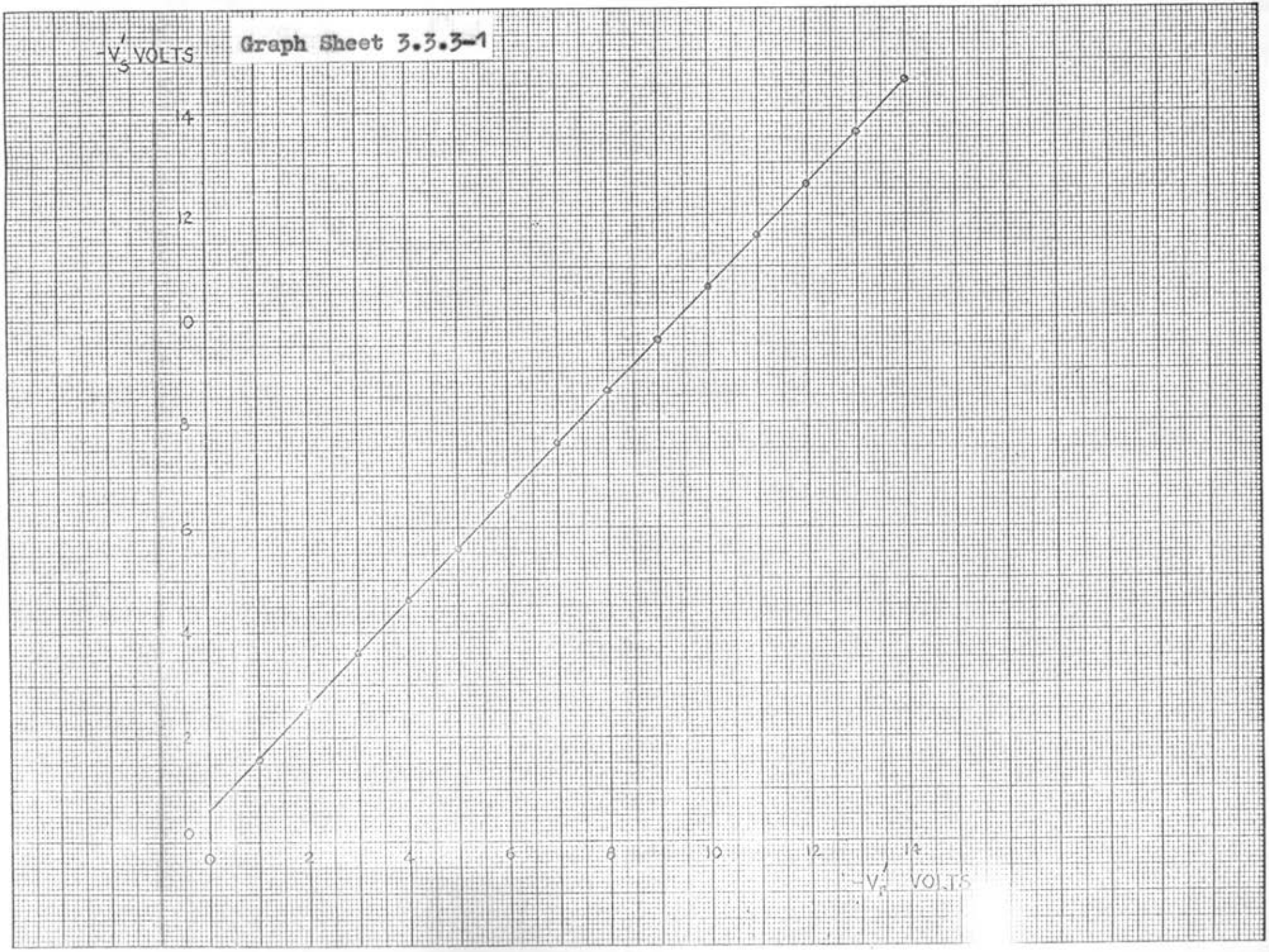
$-V_s'$ volts,	$-V_r'$ volts,
0.56	0
1.58	1
2.6	2
3.6	3
4.6	4
5.6	5
6.6	6
7.6	7
8.6	8
9.6	9
10.6	10
11.6	11
12.6	12
13.6	13
14.6	14

Table 3.3.3-2

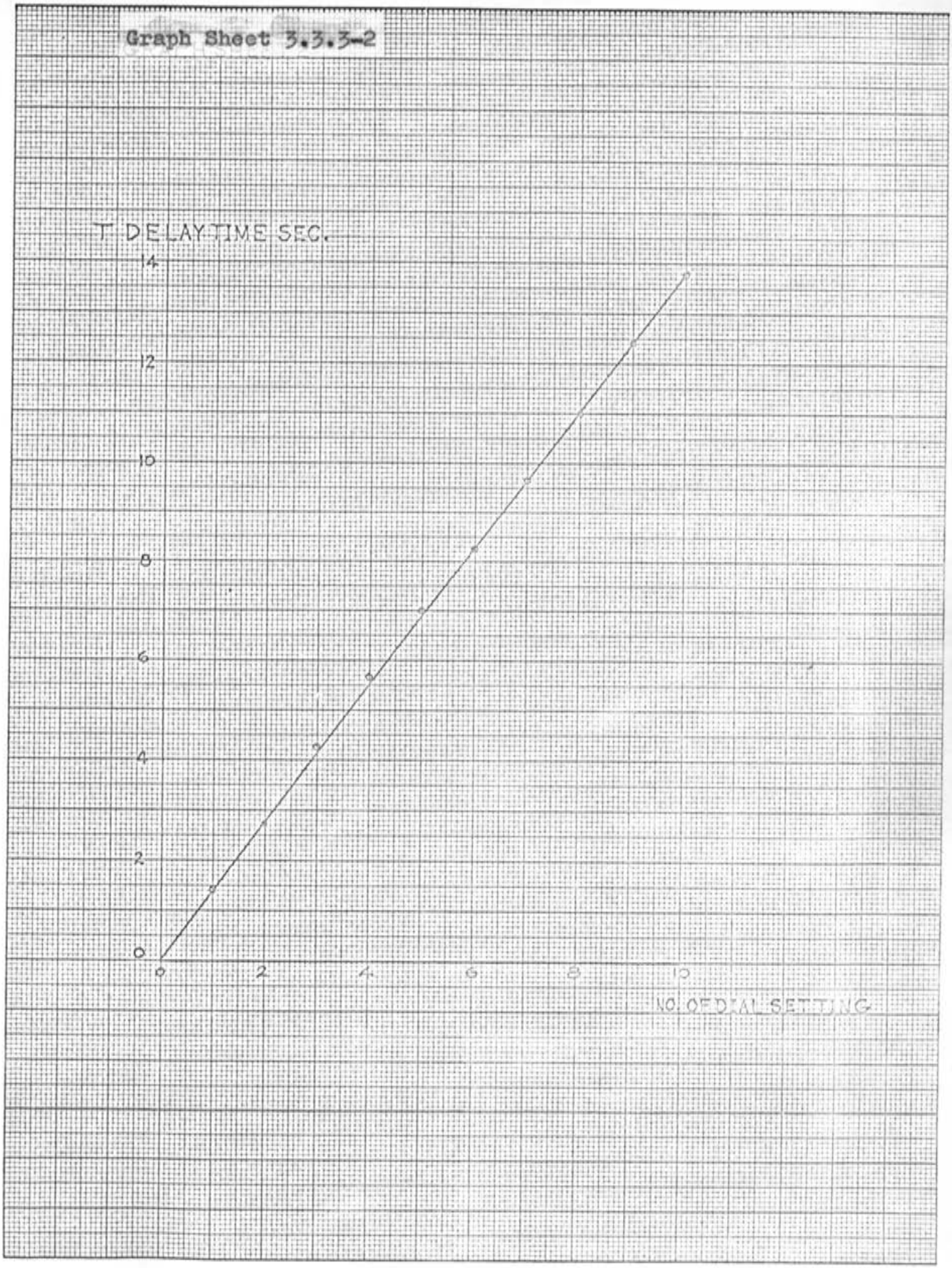
No. of Dial setting	V_r volts	$-V_r'$ volts
10	14.0	0
9	12.6	1.4
8	11.2	2.8
7	9.8	4.2
6	8.4	5.6
5	7.0	7.0
4	5.6	8.4
3	4.2	9.8
2	2.8	11.2
1	1.4	12.6

Table 3.3.3-3

T sec.	No. of Dial setting
13.78	10
12.40	9
10.94	8
9.62	7
8.25	6
7.0	5
5.66	4
4.25	3
2.72	2
1.4	1



Graph Sheet 3.3.3-2



setting (by adjusting the potentiometer R_4), as tabulated in table3.3.3-3.

Result :

The graph of the delay time T against the number of the dial setting is a straight line passing through the origin, as shown in Graph sheet 3.3.3-2.

3.3.4 The Comparator-2 Circuit (block 4)

Function :

To compare the amplitude of the fullwave rectified voltage V_{ac} with the reference voltage and also to generate a pulse train output voltage when the former is larger than the latter.

Cicuit and circuit operation :

The comparator-2 circuit is shown in Fig.3.3.4-1, T_{14} and T_{15} form a back-to-back transistor comparator. T_{13} increases the input resistance of the circuit. The diode D_{11} is used to protect T_{15} from excessively-reversed bias at the emitter-base junction when emitter voltage follows the voltage V_{ac}. The reference voltage is determined by the resistor R_8, R_9 and R_{10}. R_{11} decreases the collector leakage current of T_{16} when cut off.[1] T_{17} is an emitter follower amplifier

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[1] General Electric Company. Transistor Manual. Semiconductor Products Department Advertising and Sales Promotion, Syracuse,New York. Chapter 3 Page 81.

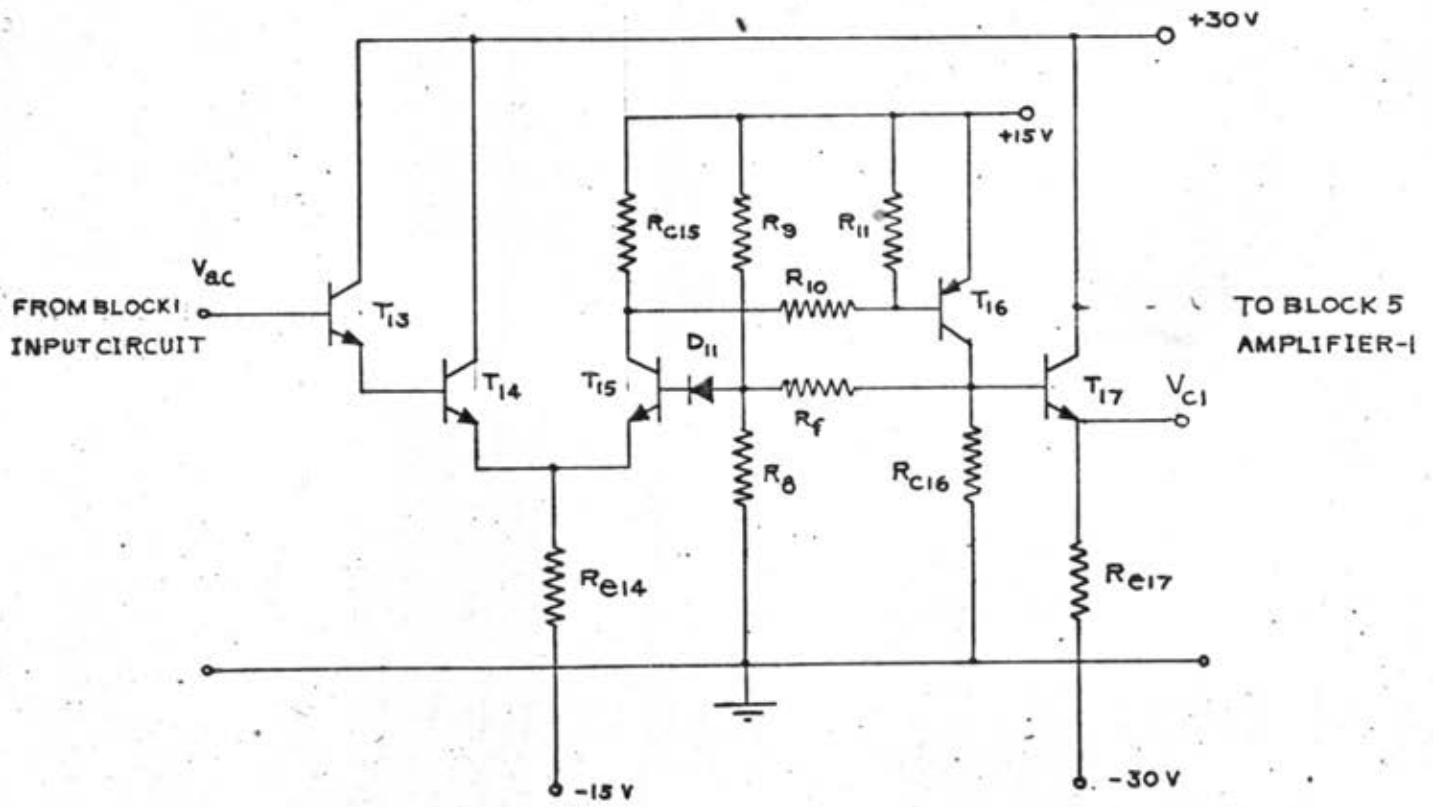


Fig.3.3.4-1 COMPARATOR-2 CIRCUIT (BLOCK 4)

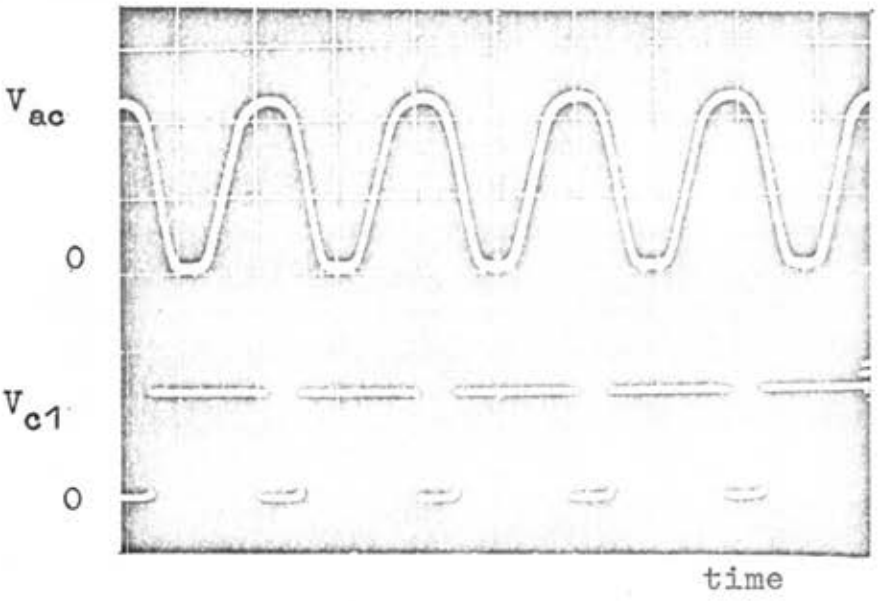


Fig.3.3.4-2 Waveforms of V_{ac} and V_{c1} for I_{ac} of 1 amp.

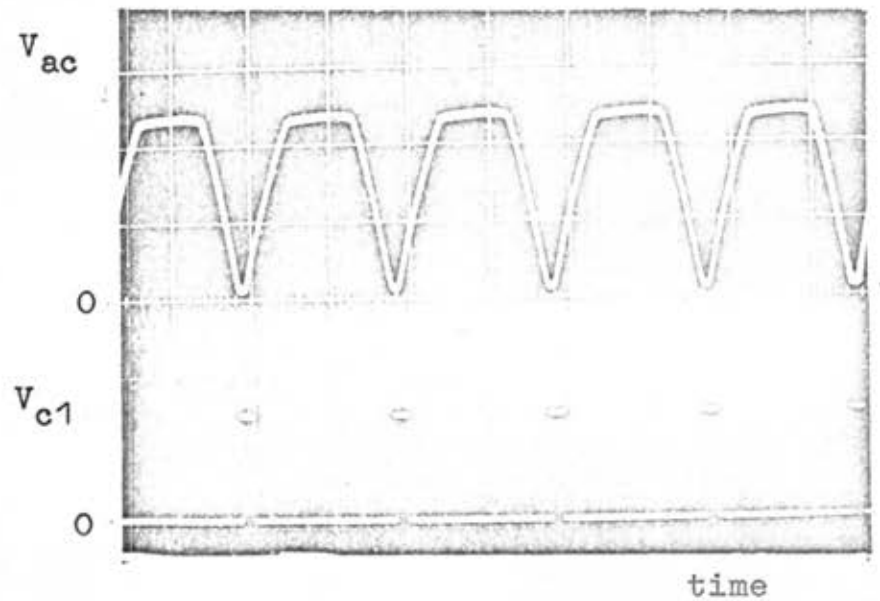


Fig.3.3.4-3 Waveforms of V_{ac} and V_{c1} for I_{ac} of 5 amp.

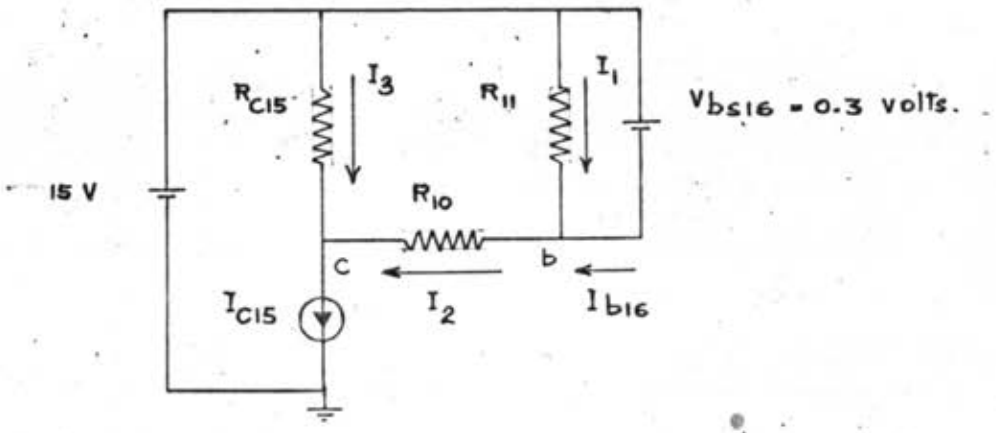


Fig.3.3.4 EQUIVALENT CIRCUIT TO DETERMINE R_{10}

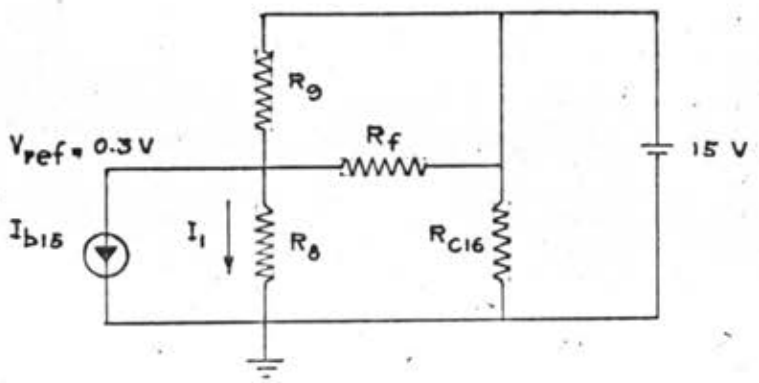


Fig. 3.3.5 EQUIVALENT CIRCUIT TO DETERMINE R_8

so that the loading effect of the next circuit is minimized. Normally when V_{ac} is less than the critical voltage, which is determined by the reference voltage, the voltage drop across D_{11}, the base-emitter voltage of T_{13}, T_{14} and T_{15}. T_{13} and T_{14} are off but T_{15} is on. A portion of T_{15} collector current flows through R_{10} to saturate T_{16}, then V_{c1} is about 15 volts. When V_{ac} is just equal to the critical voltage, T_{13} and T_{14} begin to conduct with the result that T_{15} collector current decreases and therefore less current flows through R_{10}. This makes T_{16} come out of saturation and its collector voltage decreses, which in turn decreases the base voltage of T_{15}. This results in further decreasing in magnitude of T_{15} collector current. The action of the circuit is regenerative, and if the loop gain is greater than one a quick transition of the circuit takes place, i.e.,T_{15} and T_{16} turn off and the voltage V_{c1} is almost zero (since R_9, R_f and R_{c16} are much greater than R_8). If V_{ac} is now decreased below the critical voltage the circuit will not return to the initial state since the reference voltage is decreased by the cut-off state of T_{16}. Transition to the initial state occurs when V_{ac} is decreased to another critical voltage which is less than the first one. F Fig.3.3.4-2 and Fig.3.3.4-3 show the waveforms of V_{ac} and V_{c1} for I_{ac} of 1 and 5 amp respectively (Fig.3.3.4-2 V_{ac} scale = 0.2 volts/cm, V_{c1} scale = 20 volts/cm, time base 5 ms/cm. Fig.3.3.4-3 V_{ac} scale = 2 volts/cm, V_{c1} scale = 20 volts/cm, time base 5 ms/cm). The upper level of V_{c1} indicates that the instantaneous value of V_{ac} is less than

the critical voltage and the lower level indicates on contrary.

Circuit components :

T_{13}, T_{14}, T_{15} and T_{17}	: 2N697 NPN transistor
T_{16}	: OC71 PNP transistor
D_{11}	: 1S121 diode
R_{e14}	: 15 k; 0.5 watts
R_{c15}	: 12 k; 0.5 watts
R_8	: 0.39 k; 0.5 watts
R_9	: 39 k; 0.5 watts
R_{10}	: 6.8 k; 0.5 watts
R_{11}	: 1 k; 0.5 watts
R_f	: 33 k; 0.5 watts
R_{c16}	: 10 k; 0.5 watts
R_{e17}	: 33 k; 0.5 watts

Design :

From table 3.3.1-1, V_{ac} of 0.5 volts corresponds to I_{ac} of 1 amp. Let the critical voltage of the comparator be 0.4 volts in order to allow some variation of the actual voltage which should be less than 0.5 volts. When V_{ac} is 0.5 volts T_{13} and T_{14} begin to conduct and their cut-in voltages are both 0.5 volts (typical value).

Hence $V_{e15} = 0.4 - 0.5 - 0.5 = -0.6$ volts

where $V_{e15} = T_{15}$ emitter voltage

Let choose $R_{e14} = 15\ k \pm 5\%$

Since T_{15} is conducting there exists T_{15} collector current which

is approximated as

$$\underline{I}_{c15} = (15*0.95 - 0.6)/(15*1.05) = 0.86 \text{ ma}$$

where $\underline{I}_{c15}$ = min. T_{15} collector current

(+ 15 and - 15 volts have a tolerance of ± 5%)

In order that T_{15} does not saturate when it is on, let choose R_{c15} to be 12 k ± 5%. To reduce T_{16} collector leakage current when T_{16} is off, choose R_{11} to be 1 k ± 5%.

The value of R_{10} should be small enough to provide T_{16} base saturation current when T_{15} collector current is minimum. The equivalent circuit when T_{15} is on and T_{16} is saturated is shown in Fig.3.3.4-4.

Let T_{16} base saturation current $I_{b16} = 0.1$ ma

$I_1 = 0.3/(1*0.95) = 0.316$ ma

$I_2 = 0.316 + 0.1 = 0.416$ ma

$I_3 = 0.86 - 0.416 = 0.444$ ma

$\underline{V}_{bc} = 0.444*12*0.95 - 0.3 = 5.06 - 0.3 = 4.76$ volts

If it is required that I_2 should larger than or equal to 0.416 ma, then R_{10} is chosen so that

$$\overline{R}_{10} = 4.76/0.416 = 11.4 \text{ k}$$

Let R_{10} = 6.8 k ± 5% (also to ensure that the loop gain is greater than 1)

When T_{13} and T_{14} start conducting T_{15} is assumed to be in the active region, therefore T_{15} base-emitter voltage is about 0.6 volts. The voltage drop across D_{11}, for small current through it, is 0.3 volts (by measurement). Thus the required reference voltage is

V_{ref} = 0.3 + 0.6 - 0.6 = 0.3 volts

where V_{ref} = the reference voltage across R_8

The equivalent circuit to determine the values of R_8, R_9, R_f and R_{c16} is shown in Fig.3.3.4-5. (T_{16} collector to emitter saturation voltage is negligible; the typical value is 0.1 volts). V_{ref} is determined by R_9, R_8 and R_f. The value of R_8 and R_9 should be not too small since they bypass the regenerative current from the base of T_{15}. R_f serves as the regenerative path of the circuit and also affects the reference voltage V_{ref}. R_f and R_{c16} combine in parallel to be the collector load of T_{16} (since V_{ref} is small as compared to 15 volts).

Let choose R_9 = 39 k ± 5%

R_f = 33 k ± 5%

R_{c16} = 10 k ± 5%

To calculate the value of R_8 the nominal values of the resistors are used (see Fig.3.3.4-5).

I_{e15} = (15-0.6)/15 = 0.96 ma

I_{b15} = 0.96/40 = 0.024 ma (current gain of T_{15} = 40)

$R_9//R_f$ = 39*33/(39+33) = 17.9 k

I_1 = (15-0.3)/17.9 - 0.024 = 0.82 - 0.024 = 0.796 ma

Therefore R_8 = 0.3/0.976 = 0.377 k

Choose R_8 = 0.39 k ± 5%

and choose R_{e17} = 33 k ± 5%

Experiment-1 :

To check the operation of the circuit.

Equipments :

2 Simpson voltmeters

1 Variable d.c. power supply

Procedure :

The experiment circuit is the same as in Fig.3.3.4-1. After the circuit has been biased as specified in Fig.3.3.4-1, the base voltage of T_{13} is varied from 0, positively, until V_{c1} changes the voltage level from the initial level. Then the base voltage of T_{13} is decreased until V_{c1} returns to the initial level. The associated voltages are measured and recorded.

Result :

The first critical voltage = 0.43 volts

V_{c1} changes from 13.6 volts to 0.45 volts

The second critical voltage = 0.36 volts

V_{c1} changes from 0.45 volts to 13.6 volts

The action of the circuit is regenerative since V_{c1} quickly changes from one level to the other. The hysteresis of the circuit is 0.07 volts.

Experiment-2 :

To calibrate the variable resistor R_p of the input circuit for the pick-up current of 1 to 3 amp.

Equipments :

1 Current source, Relay Tester

1 Oscilloscope

Procedure :

The output voltage V_{ac} from the input circuit (block 1), is put into the base of T_{13}. The oscilloscope is used to observe the voltage waveform of V_{c1}. The current source is set for I_{ac} of 1 amp, then R_p is increased from its minimum value until the pulse train voltage of V_{c1}, as in Fig.3.3.4-2, appears on the oscilloscope. The position of the knob of R_p is marked for 1 amp pick-up current. The same procedure is repeated for the pick-up current of 1.5, 2, 2.5 and 3 amp respectively.

Result :

The pick-up current can be varied continuously from 1 to 3 amp. The scale is not linear but is inversely proportional to the pick-up current.

3.3.5 The Comparator-3 and Amplifier-2 Circuit (Block 6 and 7)

Function:

To compare the d.c. voltage V'_{dc} to the reference voltage and also to produce an instantaneous trip signal when the former is larger than the latter.

Circuit and Circuit operation :

The circuit is shown in Fig. 3.3.5-1. The comparator is almost the same as comparator-2. The difference is that there is no regenerative feed back and that the critical voltage of the comparator can be adjusted by the potentiometer R_{13}. Normally when V'_{dc} is less than the critical voltage T_{24} and T_{25} are on with the result that T_{26} is off and T_{27} is on. (T_{26} and T_{27} are the amplifiers). Therefore T_{27} collector voltage V_{c2} is about 0 volt. When V'_{dc} is greater than the critical voltage T_{24} and T_{25} are off with the result that T_{26} is on and T_{27} is off. Then V_{c2} is about -30 volts.

Circuit Components :

T_{22}, T_{23} and T_{24}	:	2N697 NPN Transistor
T_{25}, T_{26} and T_{27}	:	2S302 PNP Transistor
D_{12}	:	1S121 Diode
R_{e23}	:	15 k;0.5 watts
R_{e24}	:	12 k;0.5 watts
R_{12}	:	0.56 k;0.5 watts
R_{13} potentiometer	:	5 k;3 watts
R_{14}	:	2.7 k;0.5 watts
R_{15}	:	6.8 k;0.5 watts

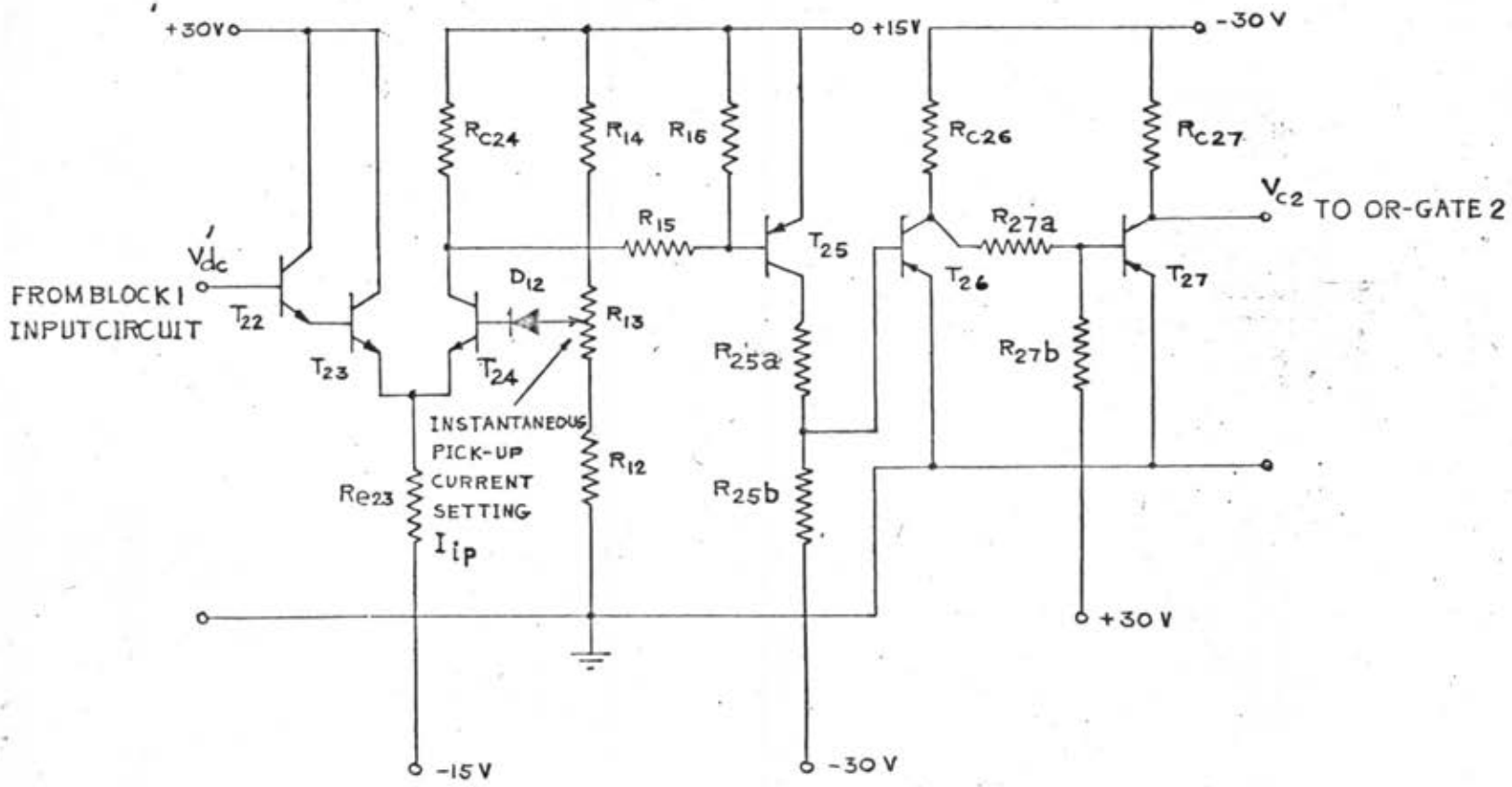


Fig.3.3.5-1 COMPARATOR-3 CIRCUIT AND AMPLIFIER-2 CIRCUIT (BLOCK 6 AND BLOCK 7)

3.3.5

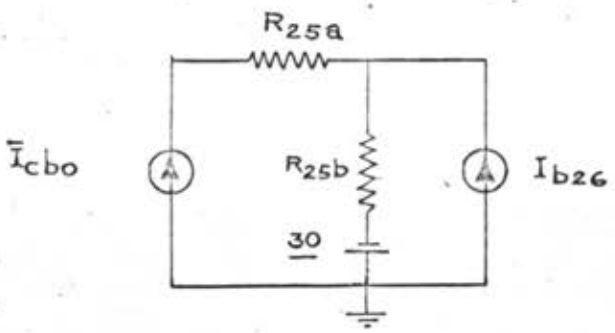


Fig.3.3.5-2 EQUIVALENT CIRCUIT WHEN T_{25} IS OFF AND T_{26} IS ON.

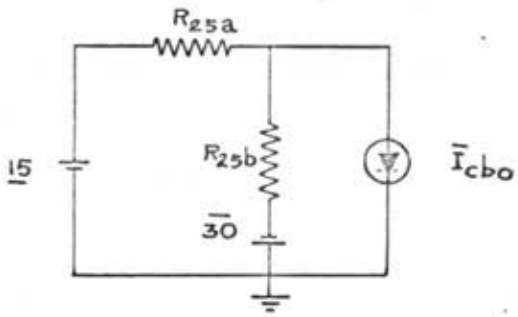


Fig.3.3.5-3 EQUIVALENT CIRCUIT WHEN T_{25} IS ON AND T_{26} IS OFF

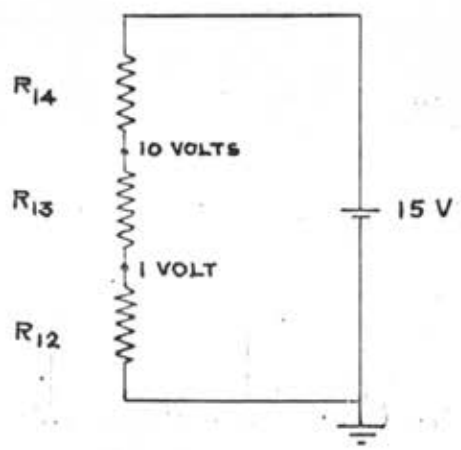


Fig.3.3.5-4 CIRCUIT TO DETERMINE R_{12} AND R_{14}.

R_{16} : 11k;0.5 watts

R_{25a} : 18 k;0.5 watts

R_{25b} : 82 k;0.5 watts

R_{c26} : 15 k;0.5 watts

R_{27a} : 12 k;0.5 watts

R_{27b} : 100 k;0.5 watts

R_{c27} : 15 k;0.5 watts

Design:

R_{e23}, R_{e24}, R_{15} and R_{16} are selected to be 15, 12, 6.8 and 1 k respectively (similar to the comparator-2 circuit).

R_{25a} and R_{25b} are chosen in such a way that when T_{25} is off T_{26} should be saturated and also that when T_{25} is saturated T_{26} should be off. The equivalent circuit when T_{25} is off and T_{26} is saturated is shown in Fig.3.3.5-2. The min. T_{26} base saturation current is

$$\underline{I}_{b26} = (\underline{30} + V_{bs26})/R_{25b} - \overline{I}_{cbo}$$

where V_{bs26} = base to emitter saturation of T_{26} = -0.8 volts

$\overline{I}_{cbo}$ = max. T_{25} collector leakage current

= 0.1 ma

(Remark: Please see transistor characteristics in Sec. 3.3.7.1)

The required base saturation current of T_{26}

$$= 33/(\underline{R}_{c26} * \underline{\beta}_{26})$$

$$= 33/(15*0.95*12)$$

$$= 0.193 \text{ ma}$$

where $\underline{R}_{c26}$ = min. T_{26} load

= 1.5*0.95 k

(The value of R_{c26} is obtained from the end of this design section.)

$\underline{b}_{26}$ = min. T_{26} common emitter current gain

= 12

It is required that base saturation current is equal to or greater than 0.193 ma.

Hence $(27 - 0.8)/R_{25b} - 0.1 \geq 0.193$

or $R_{25b} \leq 89.5$ k (3.3.5-1)

The equivalent circuit when T_{25} is saturated and T_{26} is off is in Fig.3.3.5-3 (collector to emitter saturation voltage of T_{25} may be considered to include in $\underline{15}$ volts which is 15*0.9 volts for this equivalent circuit).

T_{26} base to emitter cut-off voltage is

$\underline{V}_{bo26} = (\underline{15}*R_{25b} - \overline{30}*R_{25a} - \overline{I}_{cbo}*R_{25a}*R_{25b})/(R_{25a} + R_{25b})$

where $\overline{I}_{cbo}$ = max. T_{26} collector leakage current = 0.1 ma

$\underline{15}$ = 15*0.9 = 13.5 volts

If it is required that the min. base emitter cut-off voltage is equal to or greater than 1 volts, then

$(13.5*R_{25b} - 33*R_{25a} - 0.1*R_{25a}*R_{25b})/(R_{25a} + R_{25b}) \geq 1$

or $R_{25a} \leq 12.5/(34/R_{25b} + 0.1)$ (3.3.5-2)

Since T_{25} base saturation current is 0.1 ma (the same in the comparator-2 circuit). $R_{25a} + R_{25b}$ must satisfy the condition below.

$R_{25a} + R_{25b} \geq (\overline{15}+\overline{30})/(0.1*\underline{b}_{25}) = 49.5/(0.1*12) = 41.2$ k

(3.3.5-3)

The three inequalities are plotted in graph sheet 3.3.5-1 (the calculated data of Ineq.(3.3.5-2) is tabulated in tabe 3.3.5-1).

Select R_{25a} = 18 k ± 5%

R_{25b} = 82 k ± 5%

To select the values of R_{12}, R_{13} and R_{14}, let consider that when V'_{dc} is 0 T_{24} should be on but the output resistance of block is not large enough to obtain this condition, for a small forward bias voltage of T_{24}. Let this forward bias voltage be 1 volt to make T_{24} cut-off. The other condition is that if the forward bias voltage of T_{24} which can be varied by the potentiometer R_{13}, is maximum T_{24} should not saturate. Let this max. voltage is 10 volts (1 and 10 volts are determined by the experiment). The equivalent circuit to determine R_{12}, R_{13} and R_{14} is shown in Fig.3.3.5-4 (base current of T_{24} is negligible).

$5/R_{14} = 1/R_{12} = 9/R_{13}$

Since R_{13} is selected to be 5 k

therefore R_{14} = 25/9 = 2.78 k

R_{12} = 5/9 = 0.556 k

Choose R_{14} = 2.7 k ± 5%

R_{12} = 0.56 k ± 5%

Choose R_{c27} = 15 k ± 5% (see the output amplifier section)

Since R_{c27} is larger than R_{c9}, the collector load of T_9, which is 8.2 k. R_{27a}, R_{27b} and R_{c26} are chosen the same value as R_{10a}, R_{10b} and R_{c27} and it is sure that the saturated and cut-off conditions of T_{27} are obtained.

Therefore R_{27a} = 12 k ± 5%

R_{27b} = 100 k ± 5%

R_{c26} = 15 k ± 5%

Experiment :

To calebrate the potentiometer R_{13} and R_2 (block 1,the input circuit) for the instantaneous or definite minimum time-lag pick-up current (I_{ip}) of 5 to 25 multiple of the pick-up current (I_p).

Equipments :

1 Current source, Relay Tester

1 Simpson voltmeter

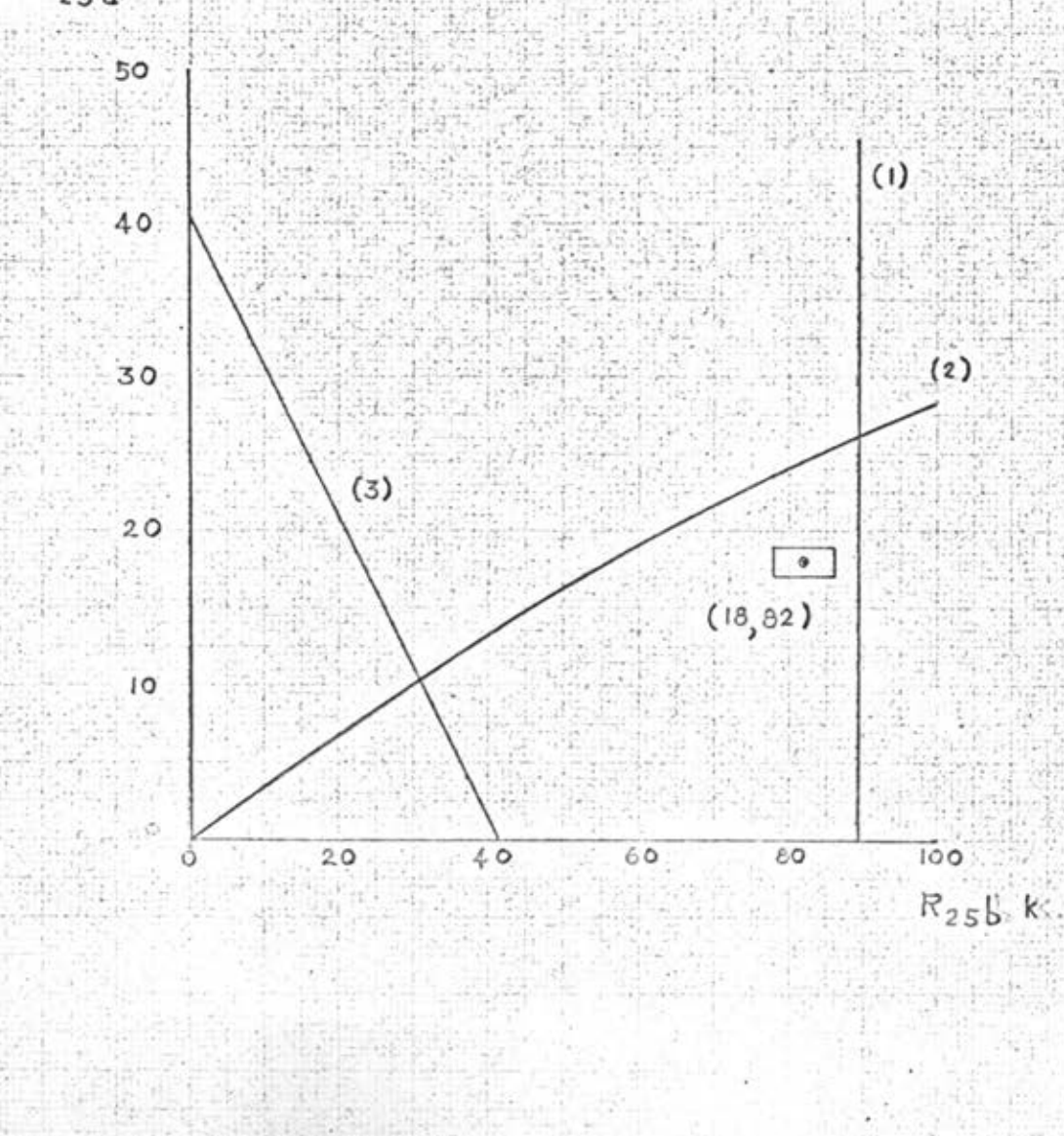
Procedure :

The middle terminal of the potentiometer R_2 of the input circuit is connected to the base of T_{22}. R_p of the input circuit is kept at 1 amp pick-up current. The potentiometer R_{13} is set for the min. T_{24} forward bias voltage. Now the potentiometer R_2 is set for zero output voltage, T_{27} collector voltage V_{c27} is measured and should be about 0 volt. Then the current source is set for I_{ac} of 5 amp and the potentiometer R_2 is adjusted to increase the output voltage V'_{dc} until V_{c27} swings to - 30 volts and the position of R_2 adjusting knob is marked and kept at this position. The adjusting knob of R_{13} is marked for the instantaneous pick-up current I_{ip} of 5 amp. Then I_{ac} is increased to 10 amp, V_{c27} is still -30 volts, the knob of R_{13} is adjusted to the position at which V_{c27} falls to 0 volt and this position is marked for I_{ip} of 10 amp. The same procedure is repeated for I_{ip} of 15, 20 and 25 amp.

Table 3.3.5-1 Calculated data of Ineq.(3.3.5-2)

R_{25b} k	R_{25a} k
10	3.58
20	6.95
30	10.2
40	13.2
50	16.7
60	18.7
70	21.2
80	23.6
90	26.1
100	28.4

Graph Sheet 3.3.5-1



Result :

V_{c27} = - 29.1 volts when T_{27} is off.

V_{c27} = - 0.1 volts when T_{27} is saturated.

The scale of I_{ip} pick-up current setting is linear. If I_p is set at 2 amp and I_{ip} is set at 5 amp I_{ac} must be 2*5 amp to make V_{c27} swing from - 0.1 volts to - 29.1 volts, therefore R_{13} potentiometer is calebrated for I_{ip} in terms of multiple of the pick-current I_p.

3.3.6 The Amplifier-1 Circuit (block 5)

Function :

To amplify the overcurrent signal V_{c1} from the comparator-2 circuit (block 4) in order to obtain the amplified voltages, V_a and V_{st}, which are used to initiate the and-gate and to start integration respectively.

Circuit and circuit operation :

The amplifier circuit is shown in Fig.3.3.6-1. Normally when an overcurrent does not occur V_{c1} is 13.6 volts and consequently makes T_{18} saturated, therefore T_{19} is cut off by the negative voltage which is provided by the negative bias and the voltage devider formed by R_{19a} and R_{19b}. This results in about -10 volts T_{19} collector voltage which in turn turns T_{20} on, then V_a is about -0.1 volts (collector to emitter saturation voltage of T_{20}) and no trip signal is allowed through the and-gate. The saturation of T_{20} causes the positive voltage, determined by R_{21a} and R_{21b} to cut T_{21} off with the result that V_{st} is about - 10

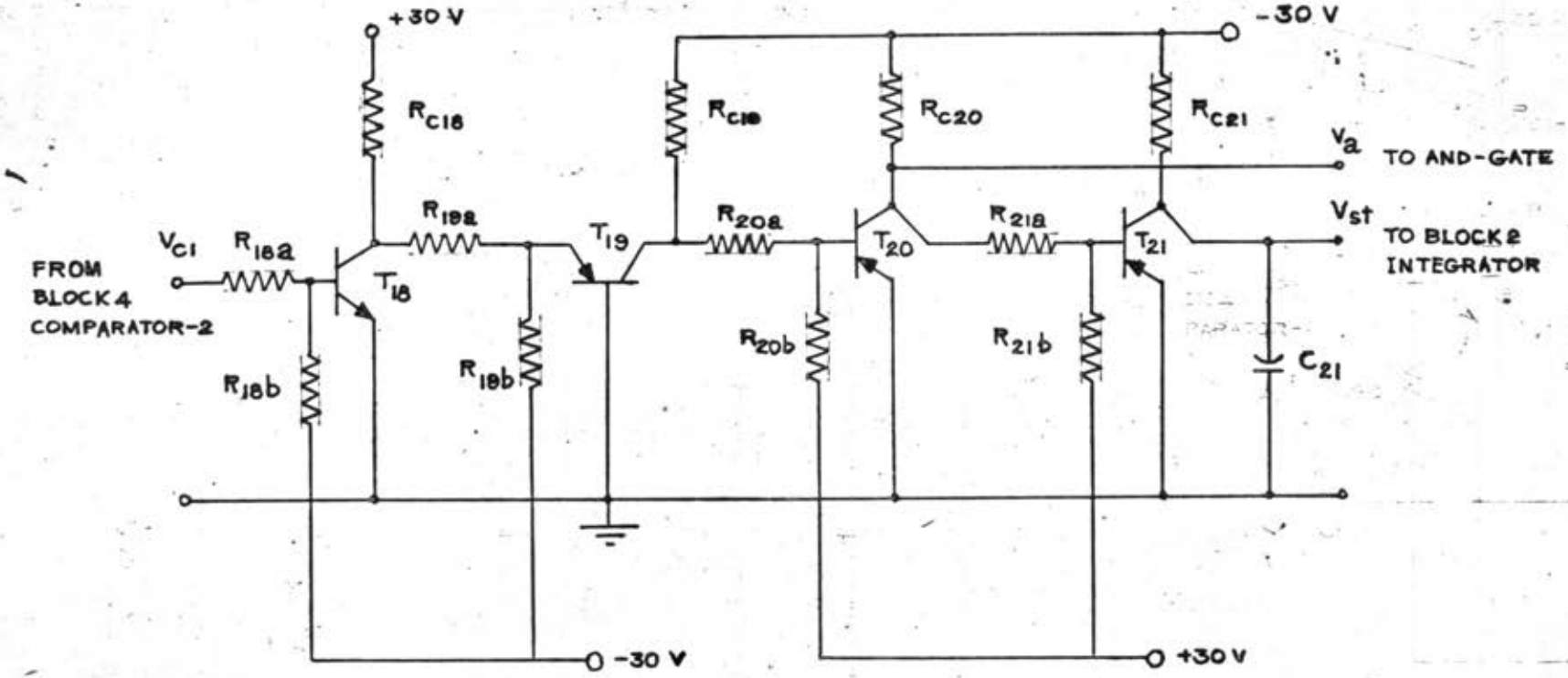


Fig.3.3.6-1 AMPLIFIER-ICIRCUIT (BLOCK 5)

2.3.6

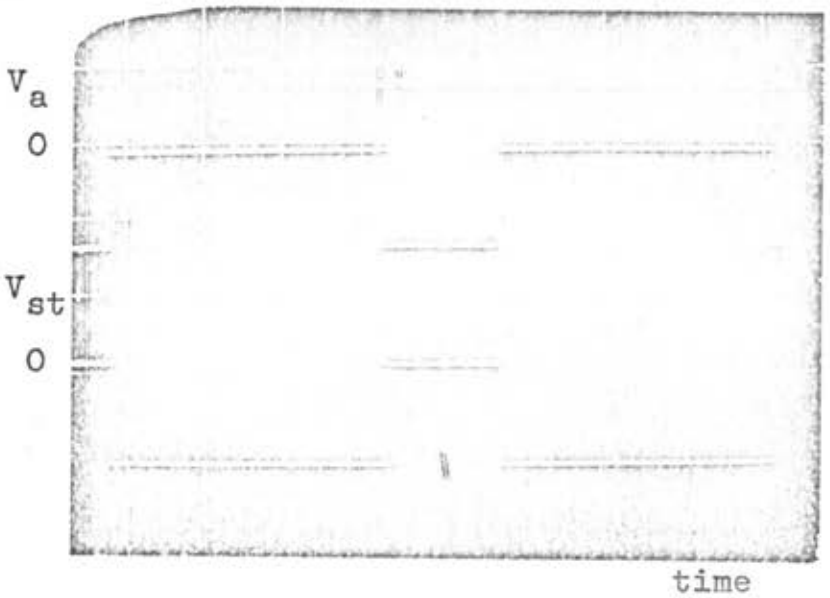


Fig.3.3.6-2 The waveforms of V_a and V_{st} (without C_{21})

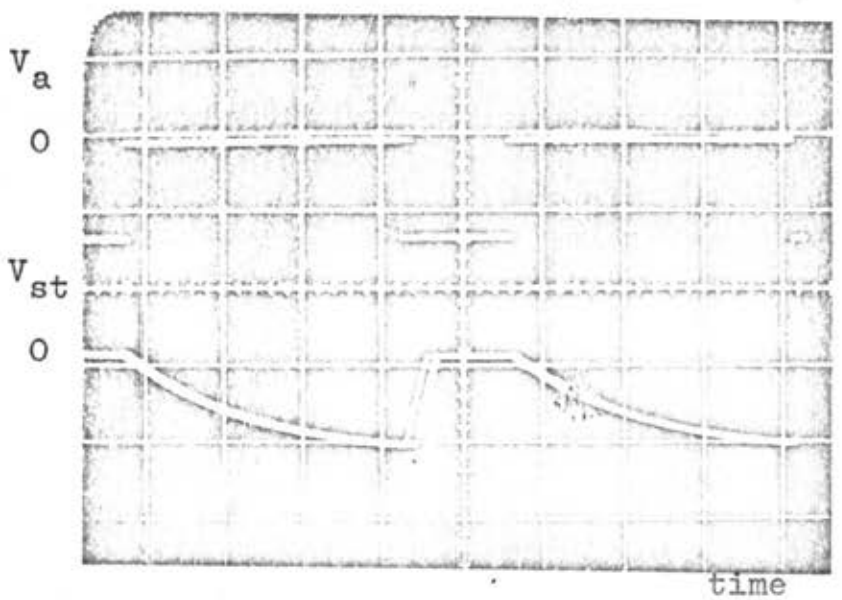


Fig.3.3.6-3 The waveforms of V_a and V_{st} (with C_{21}= 2 mf.)

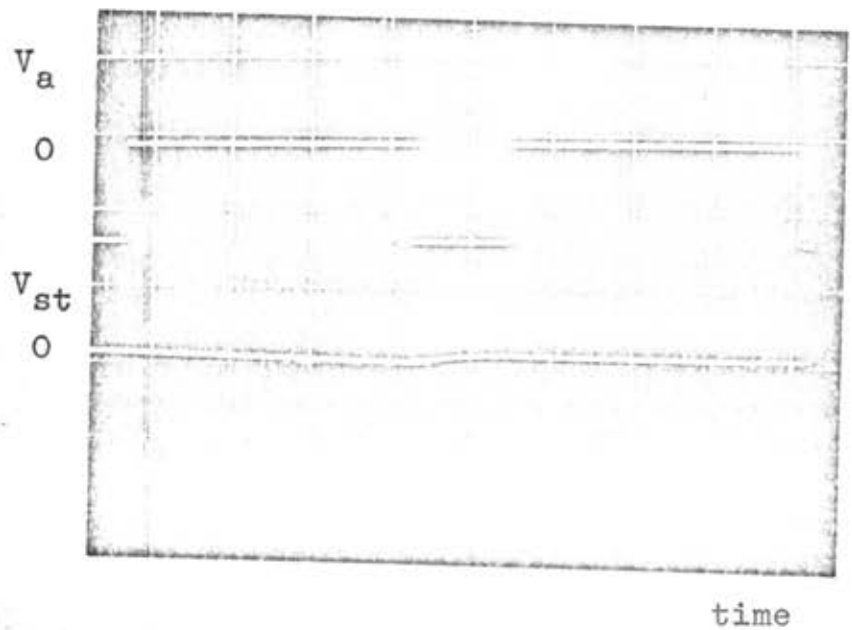


Fig.3.3.6-4 The waveforms of V_a and V_{st} (with C_{21} = 50 mf.)

volts (instead of -30 volts because of the input resistance of block 3, the integrator). Therefore integration is stopped (since T_3 is on, please refer to Sec.3.3.2).

When an overcurrent occurs V_{c1} falls to 0.45 volts and consequently cuts T_{18} off, then T_{19} turns on, T_{20} turns off and T_{21} turns on, successively. Now V_a is about -10 volts and allows the trip signal through the and-gate if a trip signal is received from one of the or-gate or both. V_{st} is now at the saturation voltage of T_{21}, which is about -0.1 volts, and therefore the integration is started. Since V_{c1} is a pulse train voltage when an overcurrent takes place (please refer to Fig.3.3.4-2 and Fig.3.3.4-3). V_a is a pulse train voltage and V_{st} is also a pulse train voltage in the absence of C_{21}. So the and-gate is closed an opened periodically. In the presence of C_{21}, V_{st} can not change instantaneously corresponding to V_{c1} but is controlled by the charge and discharge of C_{21}. Since the discharge rate is greater than the charge rate,[1] V_{st} is about -0.1 volts when an overcurrent occurs.

Circuit components :

T_{18}	: 2N697 NPN transistor
T_{19}, T_{20} and T_{21}	: 2S302 PNP transistor
R_{18a}	: 10 k;0.5 watts

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[1] Millman, Jacob and Taub, Herbert. 1965. Pulse, Digital and Switching Waveforms. New York: McGraw-Hill Book Co. Inc. Page 294.

R_{18b} : 68 k; 0.5 watts

R_{c18} : 1.8 k; 2 watts

R_{19a} : 1.5 k; 0.5 watts

R_{19b} : 18 k; 0.5 watts

R_{c19} : 10 k; 0.5 watts

R_{20a} : 8.2 k; 0.5 watts

R_{20b} : 82 k; 0.5 watts

R_{c20} : 4.7 k; 0.5 watts

R_{21a} : 5.6 k; 0.5 watts

R_{21b} : 56 k; 0.5 watts

R_{c21} : 3.9 k; 0.5 wattss

C_{21} : 50 mf; 15 volts

Design :

To choose the value of R_{c21}, the same procedure as in the output amplifier (Sec.3.3.7.2) is performed. The two inequalities to determine R_{3a} and R_{3b} are referred to in the design paragraph in Sec.3.3.2 (Ineq.(3.3.2-3) and Ineq.(3.3.2-4)). The third inequality is

$$R_{c21} \leq 17/(10/R_{3a} + 0.1) \qquad (3.3.6\text{-}1)$$

The calculated data of Ineq.(3.3.6-1) is tabulated in table 3.3.7.1-3 (R_{c21} and R_{3a} are equivalent to R_{c11} and R_{12a} respectively). This inequality is plotted in graph sheet 3.3.2-2.

Choose $R_{c21} = 3.9$ k ± 5%

The value of C_{21} is selected so that the time constant $R.C_{21}$ is

greater than the period of the pulse train V_{c1} (R is parallel combination of R_{c21} and R_{3a} plus R_{3b}).

$R = 3.9//(2.7 + 39) = 3.56$ k

From Fig.3.3.4-2, the period of the pulse train voltage V_{c1} is 10 ms.

Therefore C_{21} must have the value so that

$C_{21} >> 10/3.56 = 2.81$ mf

Choose $C_{21} = 50$ mf

Fig.3.3.6-2 shows the waveforms of V_a and V_{st} without C_{21} in the circuit. Fig.3.3.6-3 and Fig.3.3.6-4 show the same waveforms but with C_{21} of 2 and 50 mf, respectively, in the circuit.

R_{21a} and R_{21b} are the same as R_{11a} and R_{11b} since T_{21} collector load is the same as that of T_{11} in Sec.3.3.7.2.

Therefore

$R_{21a} = 5.6$ k ± 5%

$R_{21b} = 56$ k ± 5%

The determination of R_{c20} differs from that of R_{c9} since the collector load of T_{20} is the parallel combination of R_{21a} and R_{10a}:

$R'_{21a} = 5.6//12 = 3.82$ k

where R'_{21a} = the parallel combination of R_{21a} and R_{10a}

$R_{10a} = 12$ k (from Sec.3.3.7.2)

Then the inequality to determine R_{c20} is

$$R_{c20} \leq 17/(10/R'_{21a} + 0.1) \qquad (3.3.6\text{-}2)$$

The calculated data is the same as Ineq.(3.3.6-1), and from graph sheet 3.3..6-1

$R_{c20} = 4.7\ k \pm 5\%$

To calculated the values of R_{c19}, R_{20a}, and R_{20b}, the below inequalitiec are used (these three inequalities are referred to in Sec.3.3.7.1).

$$R_{20a} \geq 1/(26/R_{20b} - 0.1) \qquad (3.3.6\text{-}3)$$

$$R_{20a} \leq 9.2/(33.8/R_{20b} + 0.62) \qquad (3.3.6\text{-}4)$$

$$R_{c19} \leq 17/(10/R_{20a} + 0.1) \qquad (3.3.6\text{-}5)$$

The calculated data of Ineq.(3.3.6-3) and Ineq.(3.3.6-4) are tabulated in table 3.3.6-1 and table 3.3.6-2. The calculated data of Ineq.(3.3.6-5) is referred to in table 3.3.7.2-3. These three inequalities are plotted in graph sheet 3.3.6-2.

$R_{20a} = 8.2\ k \pm 5\%$

$R_{20b} = 82\ k \pm 5\%$

$R_{c19} = 10\ k \pm 5\%$

The three inequalities to determine R_{19a}, R_{19b} and R_{c18} are

$$R_{19a} \geq 1.15/(26/R_{19b} - 0.1) \qquad (3.3.6\text{-}6)$$

$$R_{19b} \leq 9.2/(33.8/R_{19b} + 3.2) \qquad (3.3.6\text{-}7)$$

$$R_{c18} \leq 17/(10/R_{19a} + 0.1) \qquad (3.3.6\text{-}8)$$

The calculated data of Ineq.(3.3.6-6) and Ineq.(3.3.6-8) are referred to in table 3.3.2-1 and table 3.3.7.2-3. The calculated data of Ineq.(3.3.6-7) is in table 3.3.6-7. The values of the three resistances are determined from graph sheet 3.3.6-3.

$R_{19a} = 1.5\ k \pm 5\%$

$R_{19b} = 18\ k \pm 5\%$

$R_{c18} = 1.8\ k \pm 5\%$

To determine R_{18a} and R_{18b}, Ineq.(3.3.7.1-1) and Ineq.(3.3.7.1-2) are used. It is known that V_{c1} is 13.6 volts or 0.45 volts (from experiment-1 in Sec.3.3.4).

Let $\overline{V}_{ico}$ = 1 volt (instead of 0.45 volts to ensure the performance of the circuit at high temperature)

$\underline{V}_{is}$ = 13.6 volts

V_{bo} = 1 volt

$\overline{I}_{cbo}$ = 0.1 ma

R_1 = R_{18a}

R_2 = R_{18b}

$\underline{V}_{bb}$ = 27 volts

$\overline{V}_{bb}$ = 33 volts

$\overline{V}_{bs}$ = 0.8 volts

I_b = 33/(1.8*0.9*32) = 0.63 ma (from Eq.(3.3.7.1-3))

These numerical values are substituted and the results are

$$R_{18a} \geq 2/(26/R_{18b} - 0.1) \qquad (3.3.6\text{-}9)$$

$$R_{18a} \leq 12.8/(33.8/R_{18b} + 0.63) \qquad (3.3.6\text{-}10)$$

The calculated data of these two inequalities are in table 3.3.6-4 and table 3.3.6-5 respectively, and from graph sheet 3.3.6-4

R_{18a} = 10 k ±5%

R_{18b} = 68 k ±5%

Experiment :

To check the operation of the circuit.

Equipments :

1 Current source

1 Oscilloscope

2 Simpson voltmeters

1 Variable d.c. power supply

Procedure :

The amplifier circuit is biased as indicated in Fig.3.3.6-1. The collector of T_{20} and T_{21} are connected to the input of the and-gate and the input of the integrator, to start or stop integration, respectively. (Please refer to Fig.3.3.7.2-1 and Fig.3.3.2-1). V_{c1} is set equal to 13.6 volts and V_a and V_{st} are measured. This procedure is repeated for V_{c1} of 1 volt. Then the output of the comparator-2 (block 4) is fed into the input of T_{18}. The current source, which provides the current to the input circuit (block 1), is set for 1 amp (I_{ac}) and the pick-up current (I_p) is also set at 1 amp. The waveforms of V_a and V_{st} are observed by the oscilloscope and T_3 collector voltage is measured.

Result :

For V_{c1} = 13.6 volts

V_a = -0.06 volts

V_{st} = -12.8 volts

For V_{c1} = 1 volt

V_a = -13.5 volts

V_{st} = -0.05 volts

Table 3.3.6-1 Calculated data of Ineq.(3.3.6-3)

R_{20b} [k]	R_{20a} [k]
10	0.4
25	1.06
50	2.38
75	4.0
100	6.25
125	9.1
150	14.3

Table 3.3.6-2 Calculated data of Ineq.(3.3.6-4)

R_{20b} [k]	R_{20a} [k]
10	2.3
25	4.66
50	7.1
75	8.6
100	9.6
125	10.3
150	10.9

Table 3.3.6-3 Calculated data of Ineq.(3.3.6-7)

R_{19b} k	R_{19a} k
10	1.4
20	1.88
30	2.12
40	2.28
50	2.37

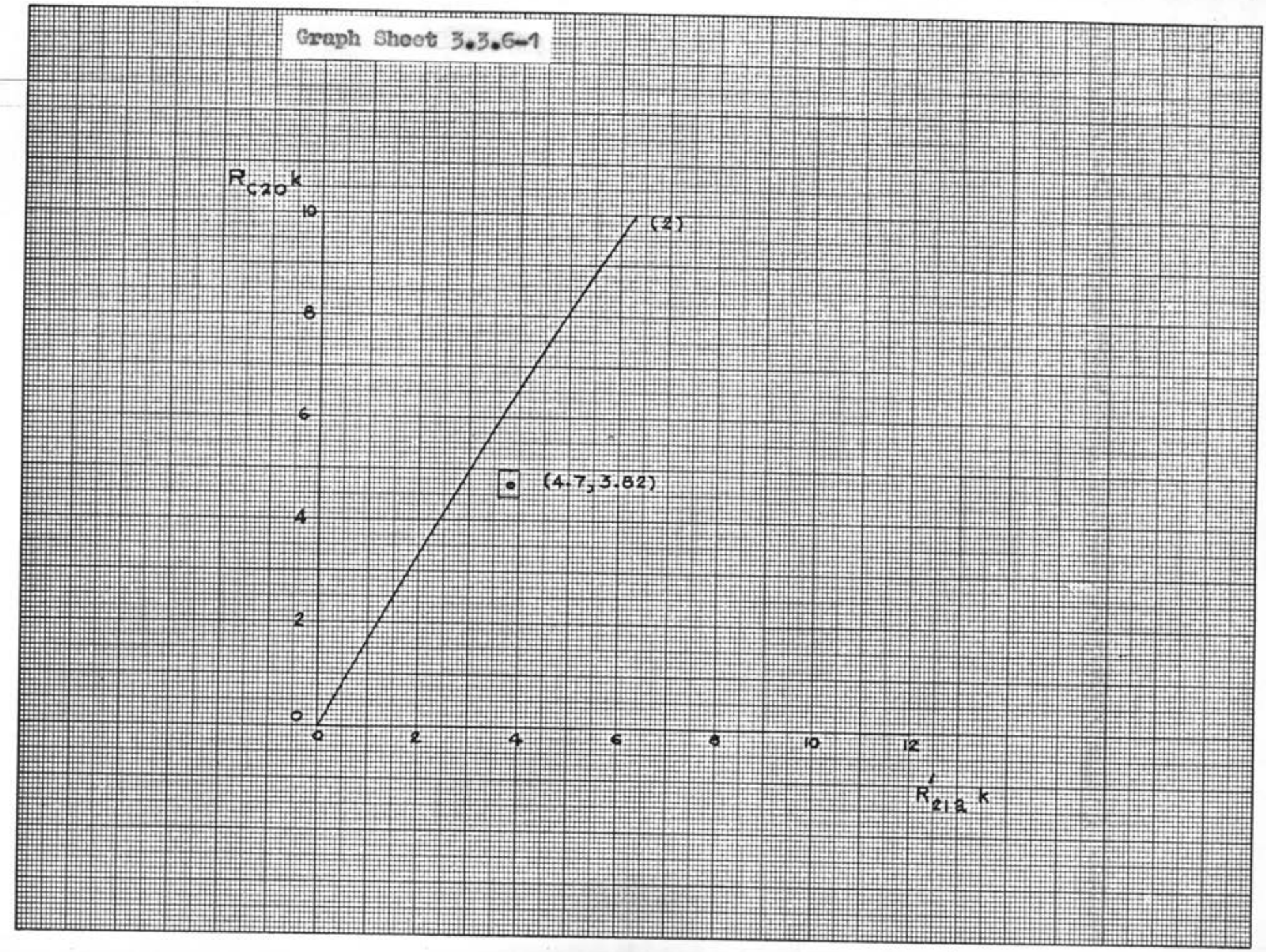
Table 3.3.6-4 Calculated data of Ineq.(3.3.6-9)

R_{18b} k	R_{18a} k
10	0.3
20	1.66
30	2.6
40	3.64
50	4.76
60	6.05
70	7.4
80	8.7
90	10.5
100	12.5

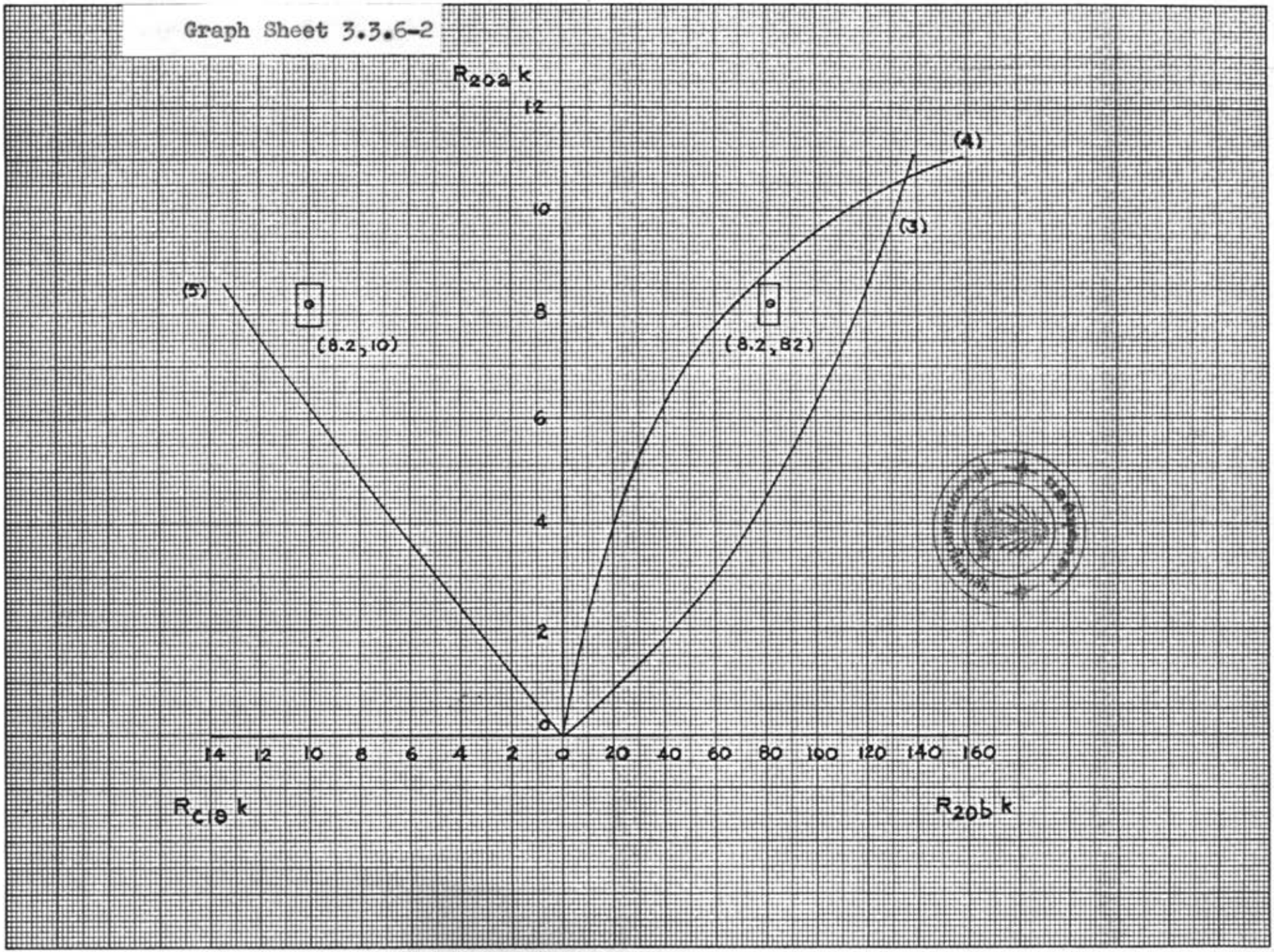
Table 3.3.6-5 Calculated data of Ineq.(3.3.6-10)

R_{18b} k	R_{18a} k
10	3.19
20	5.5
30	7.28
40	8.63
50	9.76
60	10.7
70	11.5
80	12.2
90	12.7
100	13.2

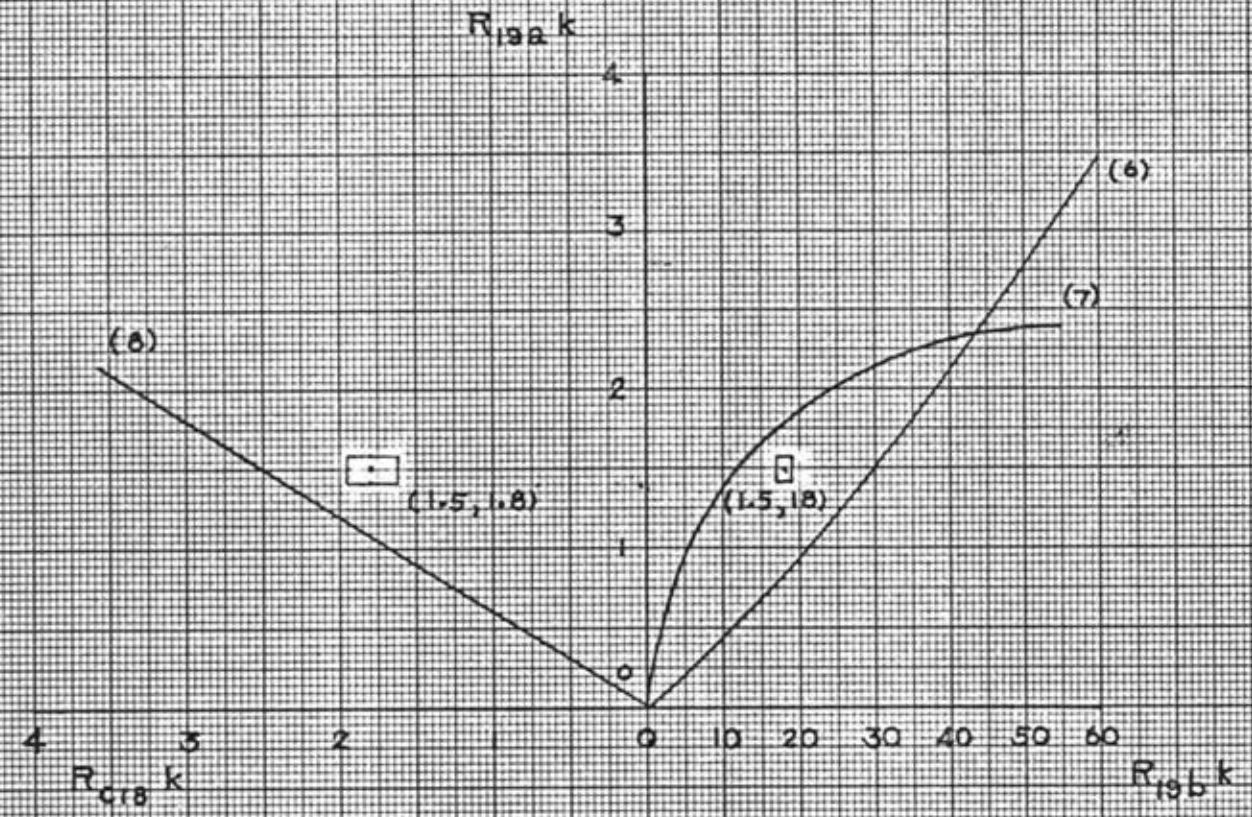
Graph Sheet 3.3.6-1

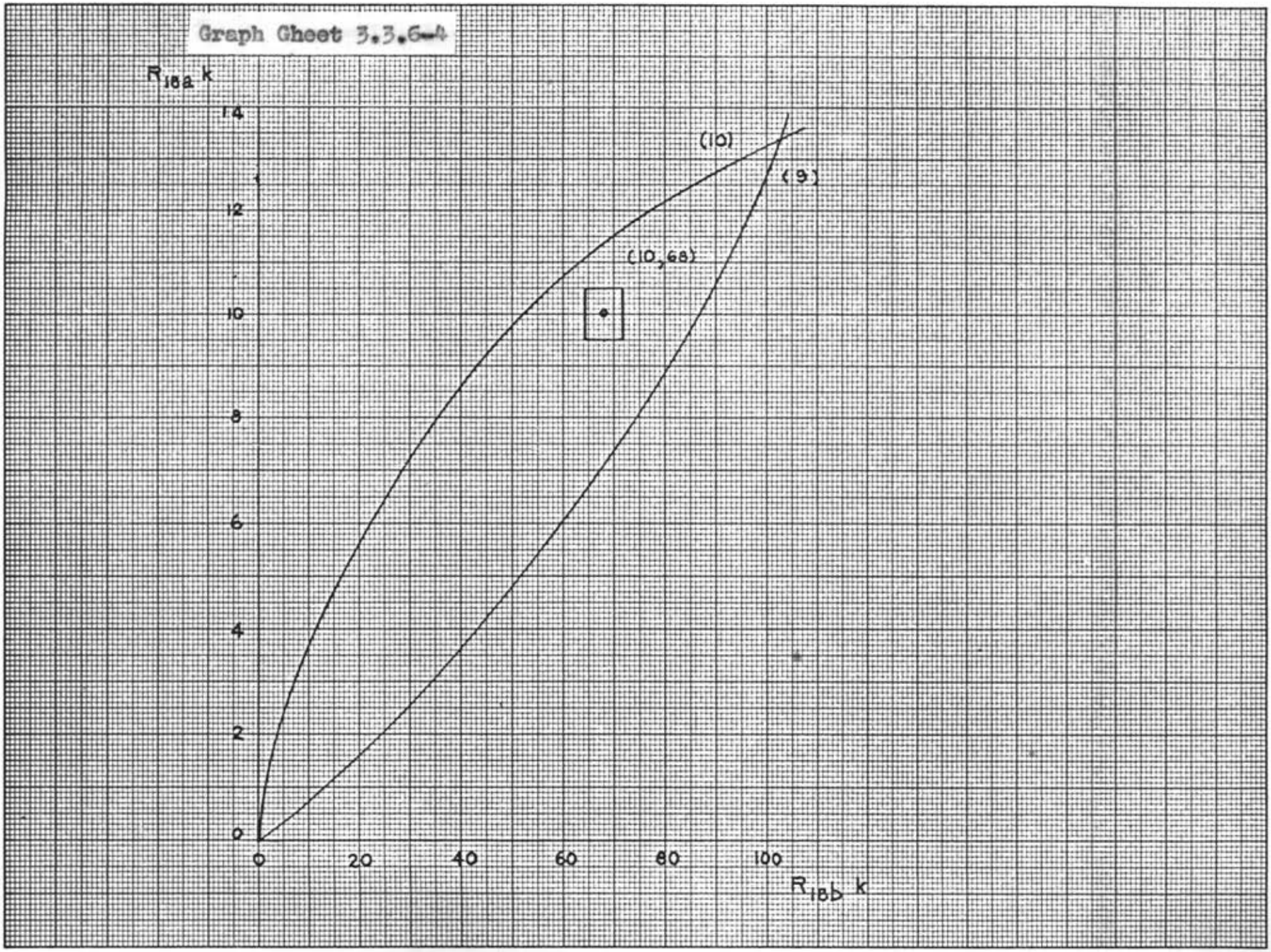


Graph Sheet 3.3.6-2



Graph Sheet 3.3.6-3





The waveforms of V_a and V_{st} when an overcurrent occurs are shown in Fig.3.3.6-4. T_3 collector voltage is measured to be -14.6 volts.

3.3.7.1 Design Technique of Transistor On-Off Circuit[1]

The amplifiers in this project are in forms of on-off circuit. The steps in designed are discussed below.

a) an inverter amplifier

Fig.3.3.7.1-1 (a), (b) and (c) show an inverter amplifier, the equivalent circuit for cut-off condition and the equivalent circuit for saturated condition respectively.

To ensure the cut-off condition, the base to emitter voltage should be greater than a certain value. This voltage is determined by the bias voltage, the input voltage and the circuit components. Therefore an inequality can be set up with the aid of the superposition theorem.

$$V_{bO} \leq (V_{bb}*R_1-V_{ico}*R_2-I_{cbo}*R_1*R_2)/(R_1+R_2)$$

where V_{bo} = the required cut-off voltage from base to emitter

V_{ico} = the input voltage for cut-off condition

I_{cbo} = the collector leakage current

To account for the variations of the above quantities, the worst condition inequality is written as

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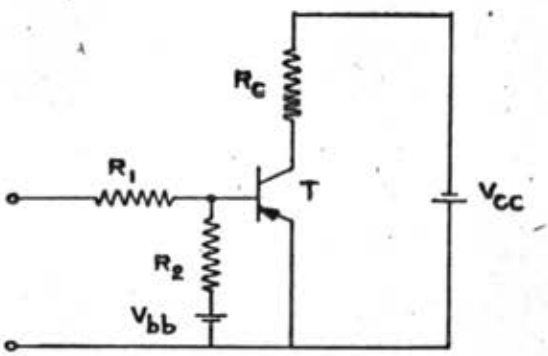
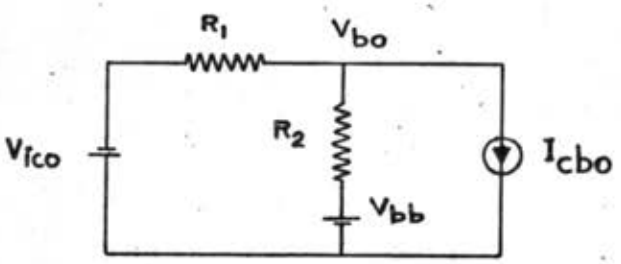
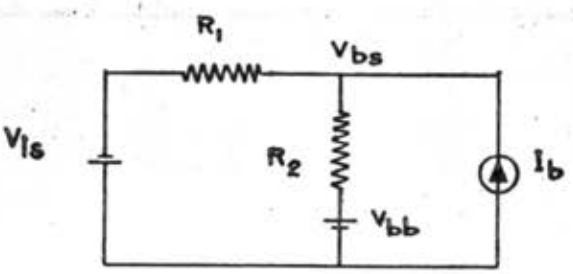
[1] abridged from "Novel Design Technique for Transistor Digital Circuits". R.W. Hockenberger. Electronics August 24,1962.



(a) an inverter amplifier circuit



(b) equivalent circuit for cut-off condition



(c) equivalent circuit for saturated condition

Fig.3.3.7.1-1 AN INVERTER AMPLIFIER

$$V_{bo} \leq (\underline{V}_{bb} \cdot R_1 - \overline{V}_{ico} \cdot R_2 - \overline{I}_{cbo} \cdot R_1 \cdot R_2)/(R_1 + R_2)$$

where $\overline{V}_{ico}$ = max. input voltage for cut-off condition

$\underline{V}_{bb}$ = min. base power supply voltage

$\overline{I}_{cbo}$ = max. collector leakage current

The above inequality is rearranged to be

$$R_1 \geq (V_{bo} + \overline{V}_{ico})/((\underline{V}_{bb} - V_{bo})/R_2 - \overline{I}_{cbo}) \qquad (3.3.7.1\text{-}1)$$

To ensure the saturated condition, the base current should be greater than a certain value. This current is determined by the bias voltage, the input voltage and the circuit components. Therefore an equality can be written, on accont for the variations of the voltages and the circuit components, as

$$I_b \leq \underline{V}_{is}/R_1 - \overline{V}_{bb}/R_2 - \overline{V}_{bs} \cdot (R_1 + R_2)/(R_1 \cdot R_2)$$

where $\underline{V}_{is}$ = min. input voltage for saturated condition

$\overline{V}_{bb}$ = max. base power supply voltage

$\overline{V}_{bs}$ = max. saturated voltage from base to emitter

I_b = the required base current

The above inequality is rearranged to be

$$R_1 \leq (\underline{V}_{is} - \overline{V}_{bs})/((\overline{V}_{bb} + \overline{V}_{bs})/R_2 + I_b) \qquad (3.3.7.1\text{-}2)$$

I_b is determined from Eq.(3.3.7.1-3)

$$I_b = \overline{V}_{cc}/(\underline{R}_c \cdot \underline{b}) \qquad (3.3.7.1\text{-}3)$$

where $\overline{V}_{cc}$ = max. collector power supply voltage

$\underline{R}_c$ = min. collector load

$\underline{b}$ = min. common emitter current gain

By using Ineq.(3.3.7.1-1) and Ineq.(3.3.7.1-2), R_1 and R_2 can be determined by a graphical method.

b) a noninverting amplifier

Fig.3.3.7.1-2 (a), (b) and (c) show a noninverting amplifier circuit, the equivalent circuit for T_1 off and T_2 on and the equivalent circuit for T_1 on and T_2 off respectively.

The design of the noninverting amplifier follows the same procedures as the inverter amplifier. Knowing the load in T_2 collector, R_{c2}, one can calculate the required base saturation current of T_2 by using Eq.(3.3.7.1-3). The value of T_1 collector voltage, when T_1 is off, which is the input voltage to saturate T_2 is assumed so that R_3 and R_4 can be determined by using Ineq.(3.3.7.1-1) and Ineq.(3.3.7.1-2). T_1 collector load R_{c1} is chosen in such a way that T_1 collector voltage , when cut-off, must be equal to or larger than the assumed value so that T_2 is surely saturated under the saturated condition. One more inequality is written, following the equivalent circuit in Fig,3.3.7.1-2 (b), as

$$V_{co1} \leq (\underline{V}_{bs2}*R_{c1}+\underline{V}_{cc}*R_3-\overline{I}_{cbo1}*R_{c1}*R_3)/(R_{c1}+R_3)$$

where V_{co1} = the assumed collector voltage of T_1 when cut-off

$\underline{V}_{bs2}$ = min. T_2 base to emitter saturated voltage which may be regarded to be zero

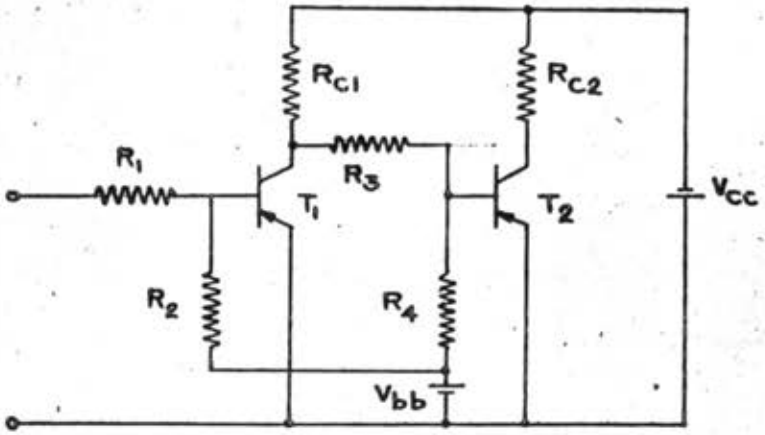
$\underline{V}_{cc}$ = min, collector power supply voltage

$\overline{I}_{cbo1}$ = max. T_1 collector leakage current

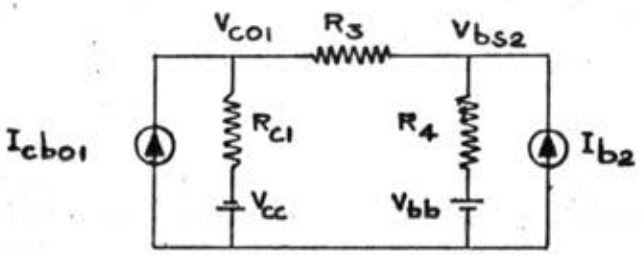
The above inequality is rearranged to be

$$R_{c1} \leq (\underline{V}_{cc}-V_{co1})/(V_{co1}/R_3+\overline{I}_{cbo1}) \qquad (3.3.7.1\text{-}4)$$

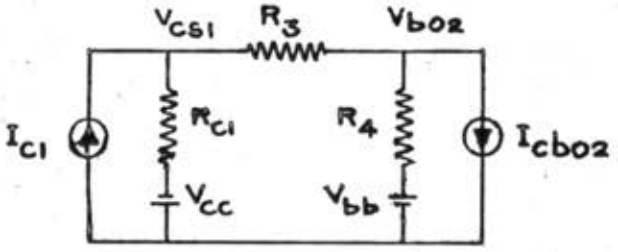
Hence R_{c1} can be determined after R_3 having been chosen and then R_1 and R_2 can be found out by Ineq.(3.3.7.1-1) and Ineq.(3.3.7.1-2)



(a) a noninverting amplifier



(b) equivalent circuit for T_1 off and T_2 on



(c) equivalent circuit for T_1 on and T_2 off

Fig.3.3.7.1-2 ANONINVERTING AMPLIFIER

(a) a noninverting amplifier

(Remark : All inequalities can be used for both PNP and NPN transistor. only the magnitudes of voltages and currents are substituted into the inequalities.)

c) a positive to negative logic amplifier

Fig.3.3.7.1-3 (a), (b) and (c) show a positive to negative logic amplifier, the equivalent circuit for T_1 off and T_2 on and the equivalent circuit for T_1 on and T_2 off respectively. From Fig.3.3.7.1-3 (b), the saturated condition of T_2, relating R_3 to R_4, results in a similar inequality to Ineq.(3.3.7.1-2). R_{c1} can be determined by using Ineq. (3.3.7.1-4). From Fig.3.3.7.1-3 (c), it is known that the saturated voltage from collector to base of T_1 is positive (for PNP transistor), so the cut-off inequality of T_2 should be

$$R_3 \geq (V_{bo2}-V_{-cs1})/((V_{-bb}-V_{bo2})/R_4-\bar{I}_{cbo2})$$

Since V_{-cs1}, min. collector saturated voltage of T_1 may regarded to be zero, the above inequality becomes

$$R_3 \geq V_{bo2}/((V_{-bb}-V_{bo2})/R_4-\bar{I}_{cbo2}) \qquad (3.3.7.1\text{-}5)$$

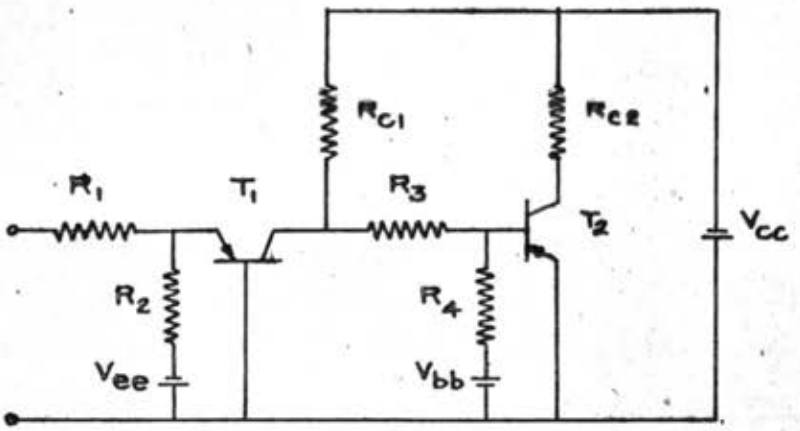
The inequalities 1 to 5 are applied in the designs of the amplifiers in Sec.3.3.6 and Sec.3.3.7.2.

Transistor Charateristics

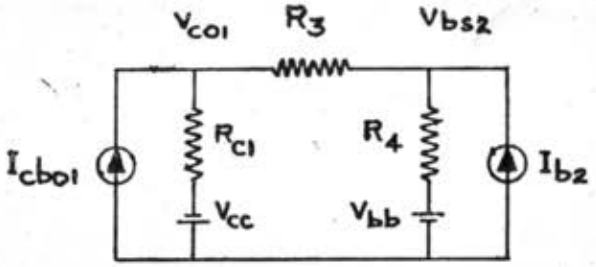
2N697 NPN Silicon transistor

Mâximum rating (T_{amb} = 25°C)

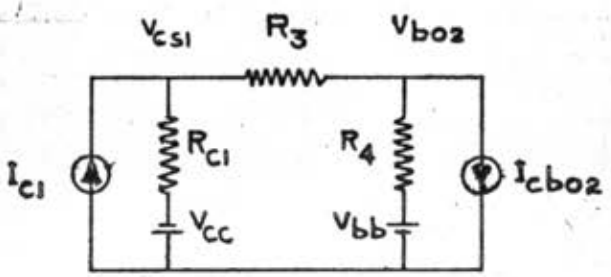
Collector base break down voltage	60	volts
Collector emiiter break down voltage	60	volts
Reverse emitter base voltage	-	
Collector current	-	



(a) a positive to negative logic amplifier



(b) equivalent circuit for T_1 off and T_2 on



(c) equivalent circuit for T_1 on and T_2 off

Fig.3.3.7.1-3 A POSITIVE TO NEGATIVE LOGIC AMPLIFIER

Total power dissipation	600		mw
Collector leakage current	100		microamp
(V_{cb}= 30 volts, T_j = 150°C)			
	min.	typ.	max.
d.c. current gain	40	-	120
collector emitter saturation voltage	-	-	1.5 volts
(I_c = 150 ma, I_b = 15 ma)			
base emitter voltage	-	-	1.3 volts

(From General Electric Transistor Manual.)

2S302 Silicon PNP transistor

Maximum rating (T_{amb}= 25°C)

Collector base break down voltage	-40		volts
Collector emitter break down voltage	-40		volts
Reverse emitter base break down voltage	-20		volts
Collector current	100		ma
Total power dissipation	300		mw
Collector leakage current (V_{cb}= -40 volts)	10		microamp
	min.	typ.	max.
d.c. current gain	15	25	60
collector emitter saturation voltage	-	-100	-150 mv
(I_c= 10 ma, I_b = 1.5 ma)			
base emitter voltage	-0.5	-0.65	-0.8 volts
(V_{ce}= -5 volts, I_c = 10 ma)			

(From Texas Instruments Specification Sheet).

OC71 PNP Germanium transistor

Maximum rating (T_{amb} = 25°C)

Collector base break down voltage	-20		volts
Collector emitter break down voltage	-20		volts
Reverse emitter base voltage	-		
Collector current	10		ma
Total power dissipation	125		mw
Collector leakage current	150		microamp
	min.	typ.	max.
d.c. current gain	30	47	75
(V_{ce} = -2 volts, I_c = 2 ma)			
collector emitter saturation voltage	-	-	-
base emitter voltage	-	-	-

The characteristics of the transistors, which are used in the design, are the d.c. current gain, the base emitter saturation voltage, the collector emitter saturation voltage, the base emitter voltage and the collector leakage current.

D.C. current gain :

Eighty percent of the min. value is used.

2N697 : min. d.c. current gain = 32

2S302 : min. d.c. current gain = 12

Base emitter saturation voltage :

Since 2N697 base emitter saturation voltage is too large and the collector current of the designed circuit never exceeds 30 ma which is

much less than 150 ma, it is preferable to assume that 2N697 base emitter saturation voltage is the same as that of 2S302 transistor.

2N697 : max. base emitter saturation voltage = 0.8 volts

2S302 : max. base emitter saturation voltage = -0.8 volts

Collector emitter saturation voltage :

2N697 saturation voltage is assumed to be equal to that of 2S302.

2N697 : max. collector emitter saturation voltage = 0.15 volts

2S302 : max. collector emitter saturation voltage = -0.15 volts

Base emitter cut-off voltage :

Both 2N697 and 2S302 transistors are silicon transistors and their cut-off voltage is 0 volt. To make sure the cut-off condition let use -1 and 1 volts respectively.

Collector leakage current :

Since the designed relay will be tested at 50°C, collector leakage current of 100 micro amp is used as the maximum value for both types.

3.3.7.2 The Output Amplifier and And-Or Gate Circuit (block8)

Function :

To produce the final trip signal.

Circuit and circuit operation :

The output amplifier circuit and the and-or gate circuit are shown in Fig.3.3.7.2-1. T_9 and T_{10} form the and-gate. No collector current can flow through T_9 unless both transistors are simultaneously on. The turn-on

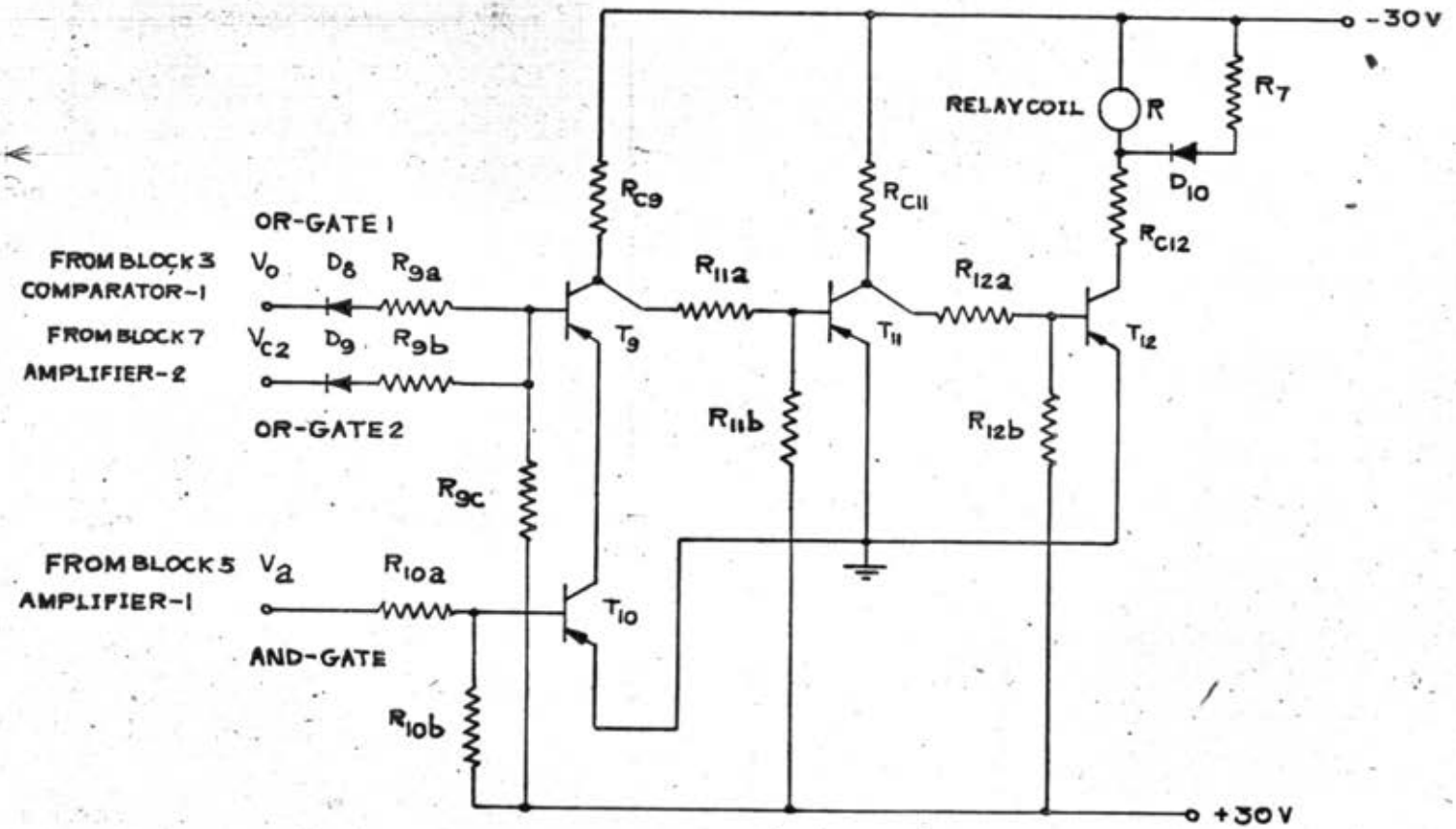


Fig.3.3.7.2-1 OUTPUT AMPLIFIER AND AND-OR CIRCUIT (BLOCK 8)

signals of T_9 are fed through the diodes D_8 and D_9 which form the or-gate. T_{10} is on and off periodically by the signal V_a of the amplifier-1 (block 5). T_{11} and T_{12} amplify the pulse train current through the resistor R_{09} to energize the relay coil in the collector of T_{12}. The diode D_{10} and the resistor R_7 are used to protect the collector of T_{12} from a voltage kick produced by the inductance of the coil. Normally when an overcurrent does not occur V_o from the comparator-1 is about -10 volts and V_{o2} from the amplifier-2 is -0.1 volts, therefore T_9 is forward biased by V_0 through the first or-gate. But there is still no current flowing through T_9 because T_{10} is cut off by the voltage V_a of - 0.05 volts. Thus T_{11} is saturated and T_{12} is cut off and no current flows to energize the relay coil. In this situation the relay contact remains opening. When an overcurrent occurs, V_0 changes from -10 volts to -0.1 volts and V_a becomes a pulse train voltage to turn T_{10} on and off periodically, but still no current flowing through T_9 until a certain delay time, which is determined by the integrator, has passed. After the delay time V_o returns to -10 volts and consequently turns T_9 on. V_a pulse train voltage is then transmitted to turn T_{12} on and off periodically. Because of the inductance of the relay coil, a d.c. pulsating current flows through the relay coil, hence the relay contact closes.

Circuit components :

T_9 to T_{12}	: 2S302 PNP transistor
D_8,D_9 and D_{10}	: 1S121 diode

R_{9a} : 12 k; 0.5 watts

R_{9b} : 12 k; 0.5 watts

R_{9c} : 100 k; 0.5 watts

R_{10a} : 12 k; 0.5 watts

R_{10b} : 100 k; 0.5 watts

R_{c9} : 8.2 k; 0.5 watts

R_{11a} : 5.6 k; 0.5 watts

R_{11b} : 56 k; 0.5 watts

R_{c11} : 3.9 k; 0.5 watts

R_{12a} : 2.7 k; 0.5 watts

R_{12b} : 39 k; 0.5 watts

R_{c12} : 0.39 k; 0.5 watts

R_7 : 0.1 k; 0.5 watts

R, coil resistance : 1 k; coil rating voltage 24 volts

Design :

R_{c12} is used to limit the voltage across the coil.

Hence $R/(R + R_{c12}) = 24/33$

or $R_{c12} = 9*R/24 = 9*1/24 = 0.375$ k

Choose $R_{c12} = 0.39$ k ± 5%

Therefore the total T_{12} collector load is 1.39 k.

When T_{12} is saturated, max. T_{12} collector current is

$\bar{I}_{c12} = 33/(1.39*0.95) = 25$ ma

The required base saturation current is

$I_{b12} = 25/12 = 2.1$ ma

Let $\overline{V}_{bs12}$ = max. base emitter saturation voltage of T_{12} = -0.8 volts

V_{co11} = the asummed input voltage to saturate T_{12} = -10 volts

$\overline{I}_{cbo12}$ = max. T_{12} collector leakage current = 0.1 ma

V_{bo12} = the required base emitter cut-off voltage of T_{12} = 1 volt

$\overline{V}_{cs11}$ = max. collector emitter saturation of T_{11}

= max. input voltage to cut T_{12} off = -0.15 volts

$\overline{I}_{cbo11}$ = max. T_{11} collector leakage current = 0.1 ma

From Ineq.(3.3.7.1-1), the cut-off inequality is

$$R_{12a} \geq (V_{bo12}+\overline{V}_{cs11})/((V_{-bb}-V_{bo12})/R_{12b}-\overline{I}_{cbo12})$$

Substitute the above inequality with the numerical values (only the magnitudes, and V_{-bb} = 27 volts), therefore

$$R_{12a} \geq (1+0.15)/((27-1)/R_{12b}-0.1)$$

or $$R_{12a} \geq 1.15/(26/R_{12b}-0.1) \qquad (3.3.7.2\text{-}1)$$

From Ineq.(3.3.7.1-2), the saturated inequality is

$$R_{12a} \leq (V_{co11}-\overline{V}_{bs12})/((\overline{V}_{bb}+\overline{V}_{bs12})/R_{12b}+I_{b12})$$

Substitute the above inequality with the numerical values (only the magnitudes, and $\overline{V}_{bb}$ = 33 volts), therefore

$$R_{12a} \leq (10-0.8)/((33+0.8)/R_{12b}+2.1)$$

or $$R_{12a} \leq 9.2/(33.8/R_{12b}+2.1) \qquad (3.3.7.2\text{-}2)$$

From Ineq.(3.3.7.1-4), the inequality to determine R_{c11} is

$$R_{c11} \leq (V_{-cc}-V_{co11})/(V_{co11}/R_{12a}+\overline{I}_{cbo11})$$

Substitute the above inequality with the numerical values (only the magnitudes, and V_{-cc} = (-) 27 volts), therefore

$$R_{c11} \leq (27-10)/(10/R_{12a}+0.1)$$

or $$R_{c11} \leq 17/(10/R_{12a}+0.1) \qquad (3.3.7.2\text{-}3)$$

The calculated data of the above three inequalities are tabulated in table 3.3.7.2-1, table 3.3.7.2-2 and table 3.3.7.2-3) respectively and also plotted on graph sheet 3.3.7.2-1. The selected values of the three resistors are

R_{12a} = 2.7 k ± 5%

R_{12b} = 39 k ± 5%

R_{c11} = 3.9 k ± 5%

When T_{12} is saturated, its collector current increases exponentially to the steady state value. Then T_{12} turns off, because the pulse train voltage V_a with the result that T_{12} collector current stops flowing but the relay coil current continues flowing through D_{10} and R_7. Therefore R_7 must be small enough to hold the relay coil current until the next saturation of T_{12} takes place.

Let R_7 = 0.1 k ± 5%

Fig.3.3.7.2-2 shows the waveforms of V_{Rc12}, the voltage across R_{c12}, and V_{R7} the voltage across R_7, when the and-gate allows the trip signal to energize the relay coil. V_{Rc12} represents the coil current when T_{12} is saturated and V_{R7} represents the coil current when T_{12} is cut-off.

After R_{c11} having been selected, the required base saturation current of T_{11} is calculated.

I_{b11} = 33/(3.9*0.95*12) = 0.74 ma

To choose the values of R_{c9}, R_{11a} and R_{11b}, three inequalities are

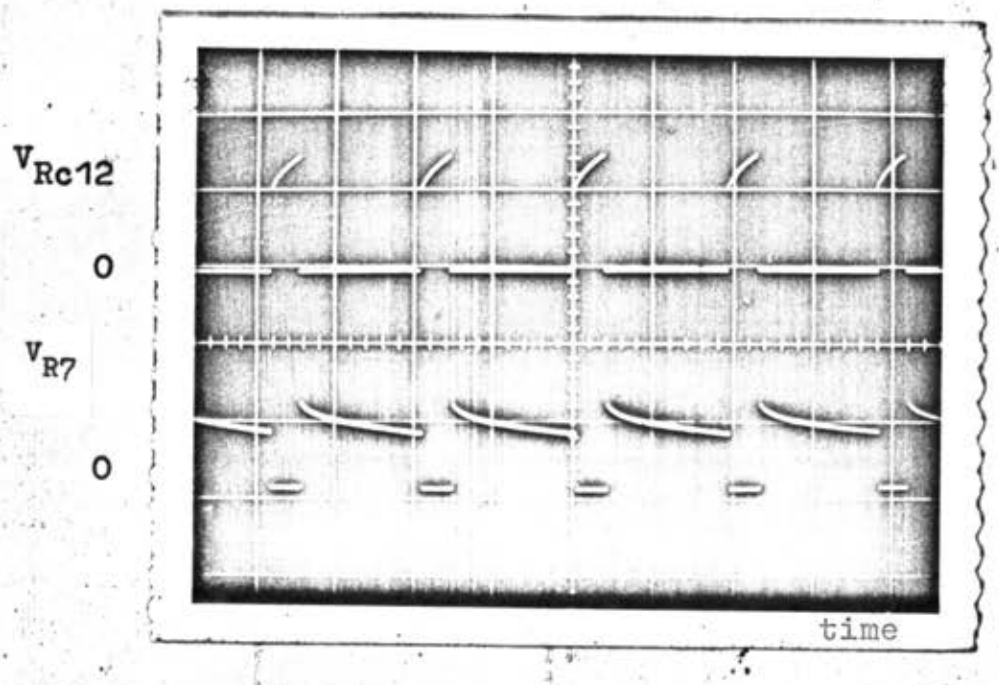


Fig.3.3.7.1-2 **The Waveforms of V_{RC12} and V_{R7}**

written following the same procedures as before.

The cut-off inequality is similar to Ineq.(3.3.7.2-1).

$$R_{11a} \geq 1.3/(26/R_{11b}-0.1) \qquad (3.3.7.2\text{-}4)$$

(Remark : $\overline{V}_{ces9}$, max. collector saturation voltage of T_9 is doubled since the collector saturation voltage of T_{10} is included.)

The saturated inequality is similar to Ineq.(3.3.7.2-2).

$$R_{11a} \leq 9.2/(33.8/R_{11a}+ 0.74) \qquad (3.3.7.2\text{-}5)$$

The inequality to determine R_{c9} is similar to Ineq.(3.3.7.2-3).

$$R_{c9} \leq 17/(10/R_{11a}+ 0.1) \qquad (3.3.7.2\text{-}6)$$

The calculated data of Ineq.(3.3.7.2-4) and Ineq.(3.3.7.2-5) are tabulated in table 3.3.7.2-4 and table 3.3.7.2-5 respectively. The caculated data of Ineq.(3.3.7.2-6) is referred to in table 3.3.7.2-3. From graph sheet 3.3.7.2-2,

R_{11a} = 5.6 k ± 5%

R_{11b} = 56 k ± 5%

R_{c9} = 8.2 k ± 5%

The two inequalities to determine R_{10a} and R_{10b} are

$$R_{10a} \geq 1.15/(26/R_{10b}-0.1) \qquad (3.3.7.2\text{-}7)$$

$$R_{10a} \leq 9.2/(33.8/R_{10b}+0.35) \qquad (3.3.7.2\text{-}8)$$

The calculated data of Ineq.(3.3.7.2-7) is referred to in table 3.3.7.2-1 and the calculated data of Ineq.(3.3.7.2-8) is in table 3.3.7.2-6. From graph sheet 3.3.7.2-3,

R_{10a} = 12 k ± 5%

R_{10b} = 100 k ± 5%

Similary,

$R_{9a} = R_{9b} = 12\ k \pm 5\%$

$R_{9c} = 100\ k \pm 5\%$

Since R_{9a} and R_{9b} is the load of T_8 and T_{27}, R_{c8} and R_{c27} can be determined from the below inequalities.

$$R_{c8} \leq 17/(10/R_{9a}+0.1) \qquad (3.3.7.2\text{-}9)$$

$$R_{c27} \leq 17/(10/R_{9b}+0.1) \qquad (3.3.7.2\text{-}10)$$

The calculated data of both above inequalities are referred to in table 3.3.7.2-3, and from graph sheet 3.3.7.2-4

$R_{c8} = R_{c27} = 15\ k \pm 5\%$

Experiment :

To check the operation of the circuit.

Equipments :

3 Variable d.c. power supplies

3 Simpson voltmeters

Procedure :

The circuit is biased as indicated in Fig.3.3.7.2-1. The three d.c. power supplies are connected to the three input terminals. The three input voltages are set for -0.15 volts and -10 volts as shown in the below table.

Result :

The results of the experiment are tabulated below.

V_a volts	V_o volts	V_{c2} volts	Relay contacts	V_{c12} volts
-0.15	-0.15	-0.15	open	-29.5
-0.15	-0.15	-10	open	-29.5
-0.15	-10	-0.15	open	-29.5
-0.15	-10	-10	open	-29.5
-10	-0.15	-0.15	open	-29.5
-10	-0.15	-10	close	-0.1
-10	-10	-0.15	close	-0.1
-10	-10	-10	close	-0.1

The operation of the circuit is satisfactory.

Table 3.3.7.2-3 Calculated data of Ineq.(3.3.7.2-3)

R_{12a} [k]	R_{c11} [k]
1	1.68
2	3.34
3	4.96
4	6.54
5	8.1
6	9.6
7	11.1
8	12.6
9	14.05
10	15.44
12	18.3
14	21.0

Table 3.3.7.2-4 Calculated data of Ineq.(3.3.7.2-4)

R_{11b} [k]	R_{11a} [k]
10	0.52
20	1.08
30	1.7
40	2.36
50	3.09
60	3.91
70	4.8
80	5.78
90	6.86
100	8.12

Table 3.3.7.2-1 Calculated data of Ineq.(3.3.7.2-1)

R_{12b} [k]	R_{12a} [k]
10	0.46
20	0.96
30	1.49
40	2.09
50	2.74
60	3.49
75	4.6
100	7.2
125	10.5
150	16.4
175	25.0
200	38.3

Table 3.3.7.2-2 Calculated data of Ineq.(3.3.7.2-2)

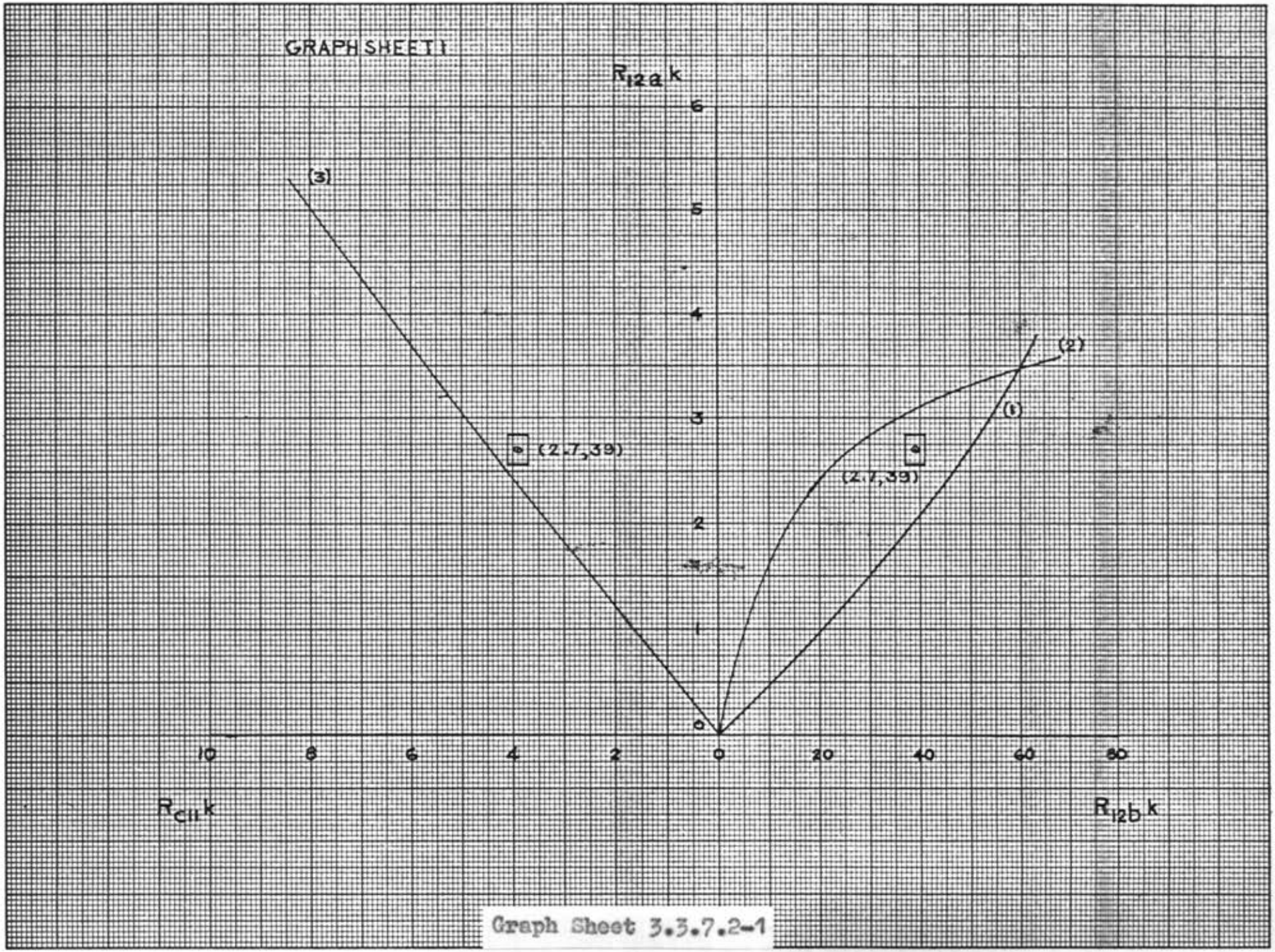
R_{12b} [k]	R_{12a} [k]
10	1.68
20	2.42
30	2.85
40	3.12
50	3.31
60	3.46

Table 3.3.7.2-5 Calculated data of Ineq.(3.3.7.2-5)

$R_{11b}{}^{k}$	$R_{11a}{}^{k}$
10	2.24
20	3.78
30	4.92
40	5.78
50	6.48
60	7.07
70	7.55
80	7.94
90	8.22
100	8.52

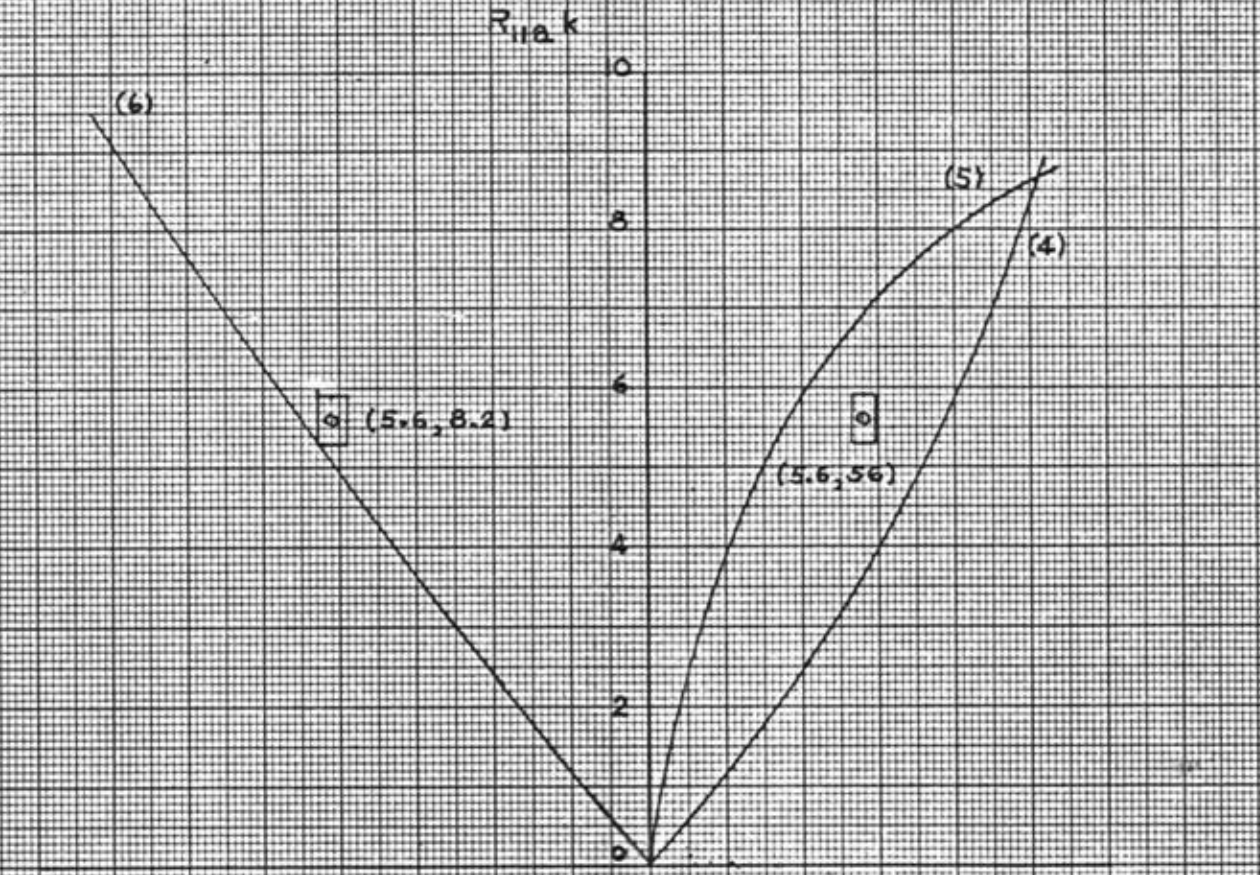
Table 3.3.7.2-6 Calculated data of Ineq.(3.3.7.2-8)

$R_{10b}{}^{k}$	$R_{10a}{}^{k}$
10	2.47
25	5.4
50	8.95
75	11.5
100	13.3
125	14.6
150	15.9
200	17.1
	17.7



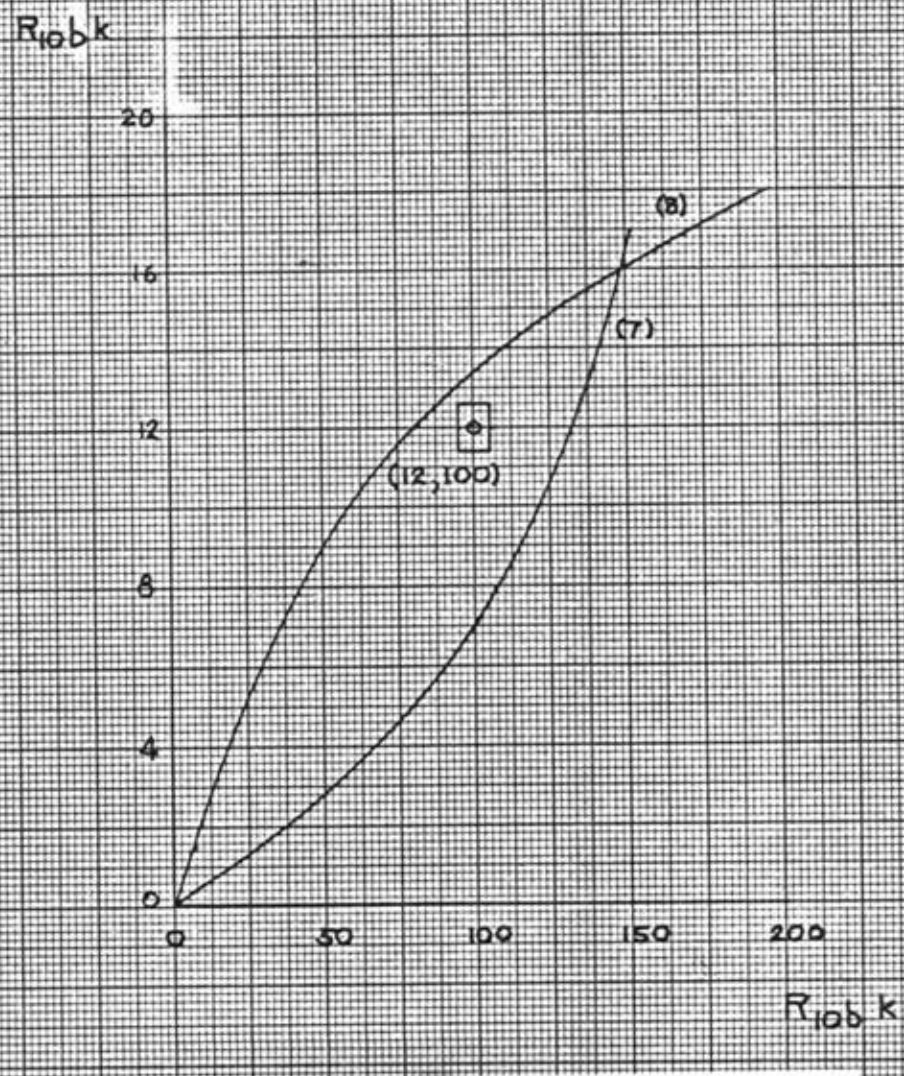
Graph Sheet 3.3.7.2-1

GRAPH SHEET 2



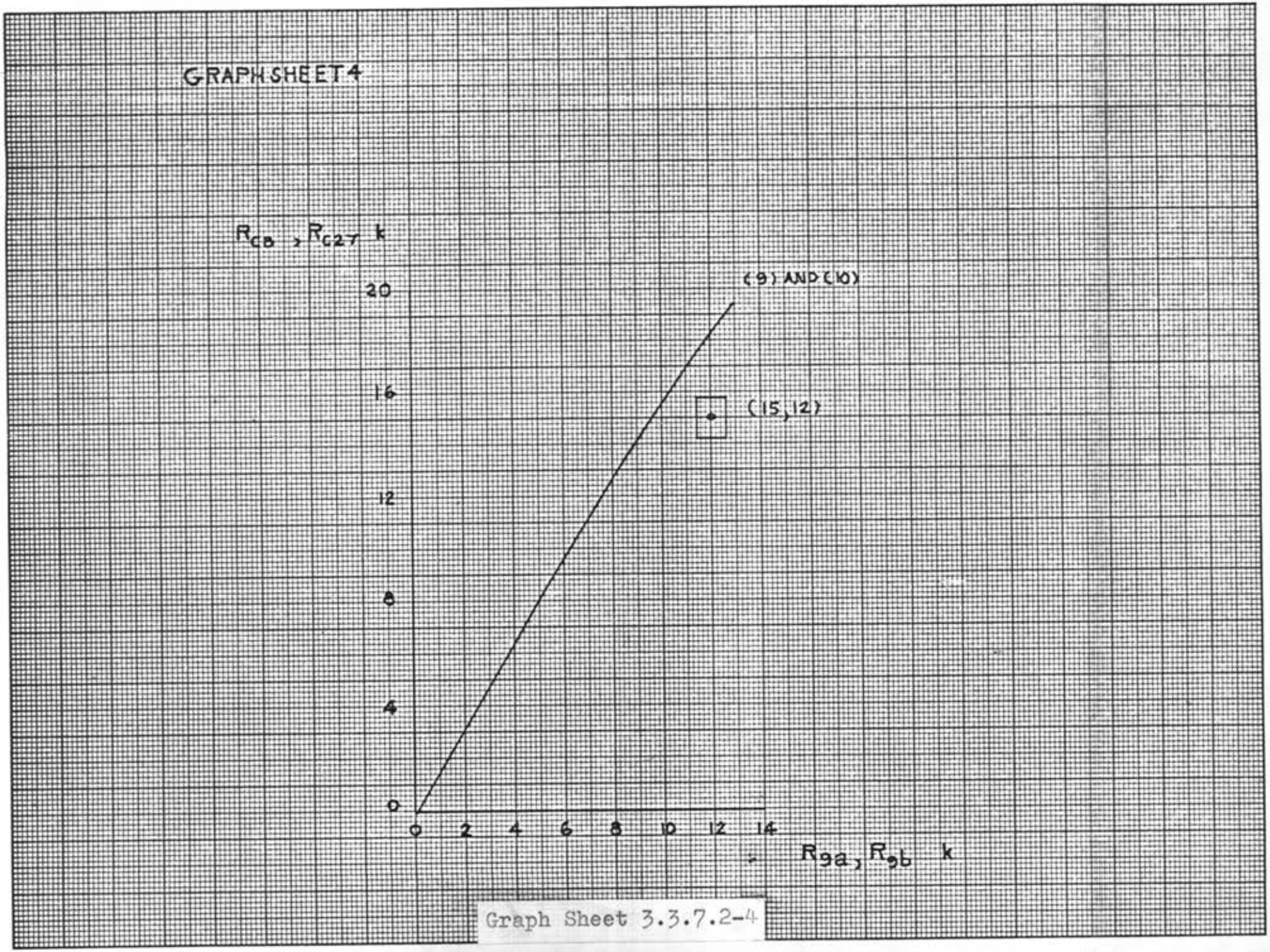
Graph Sheet 3.3.7.2-2

GRAPHSHEET 3



Graph Sheet 3.3.7.2-3

GRAPH SHEET 4



Graph Sheet 3.3.7.2-4

3.4 Operation of the Designed Relay

This section covers the operation and the operating characteristics of the inverse time-lag unit and that of the definite minimum time-lag (instantaneous)unit.

3.4.1 The Inverse Time-Lag Unit

Fig.3.4-1 shows the recorded waveforms of the relay operation. When an overcurrent occurs (the current magnitude I_{ac} is larger than the pick-up current setting I_p but not larger than the instantaneous pick-up current setting $I_p * I_{ip}$), the operating current I_{ac} is rectified to be a fullwave rectified voltage V_{ac} and the d.c. voltage V_{dc}. Let assume, for the explanation purpose, that the following signals have two states, namely 0 and 1.

V_{c1}, the comparator-2 output

= 0, nonovercurrent state

= 1, overcurrent state

V_a, the amplifier-1 output to initiate the and-gate

= 0, blocking the trip signal

= 1, allowing the trip signal

V_{st}, the amplifier-1 output to start or stop integration

= 0, start integration

= 1, stop integration

V_o, the comparator-1 output to initiate the first or-gate

= 0, no time-lag trip signal

= 1, time-lag trip signal

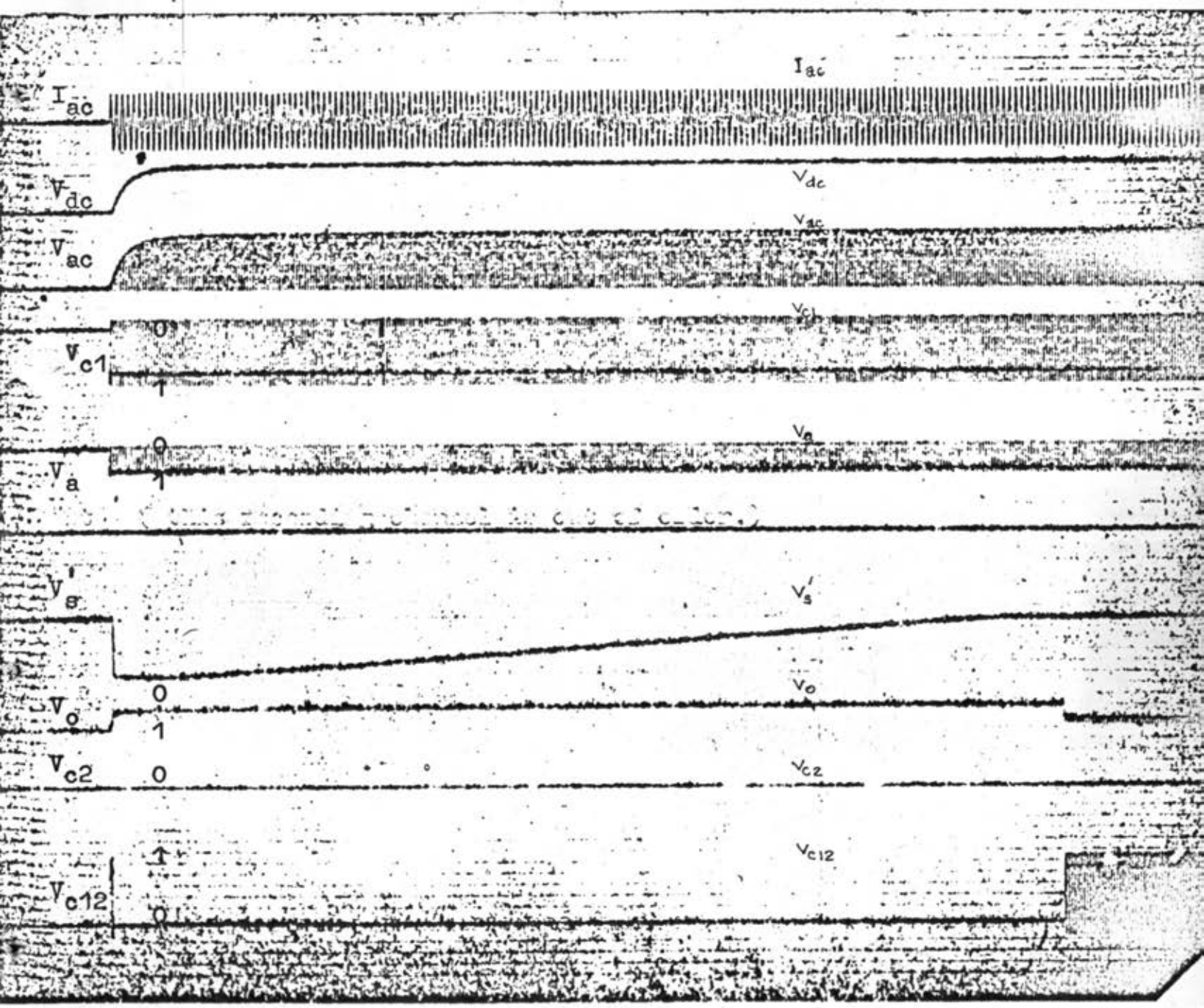


Fig.3.4-1 The recorded waveforms of the relay operation.

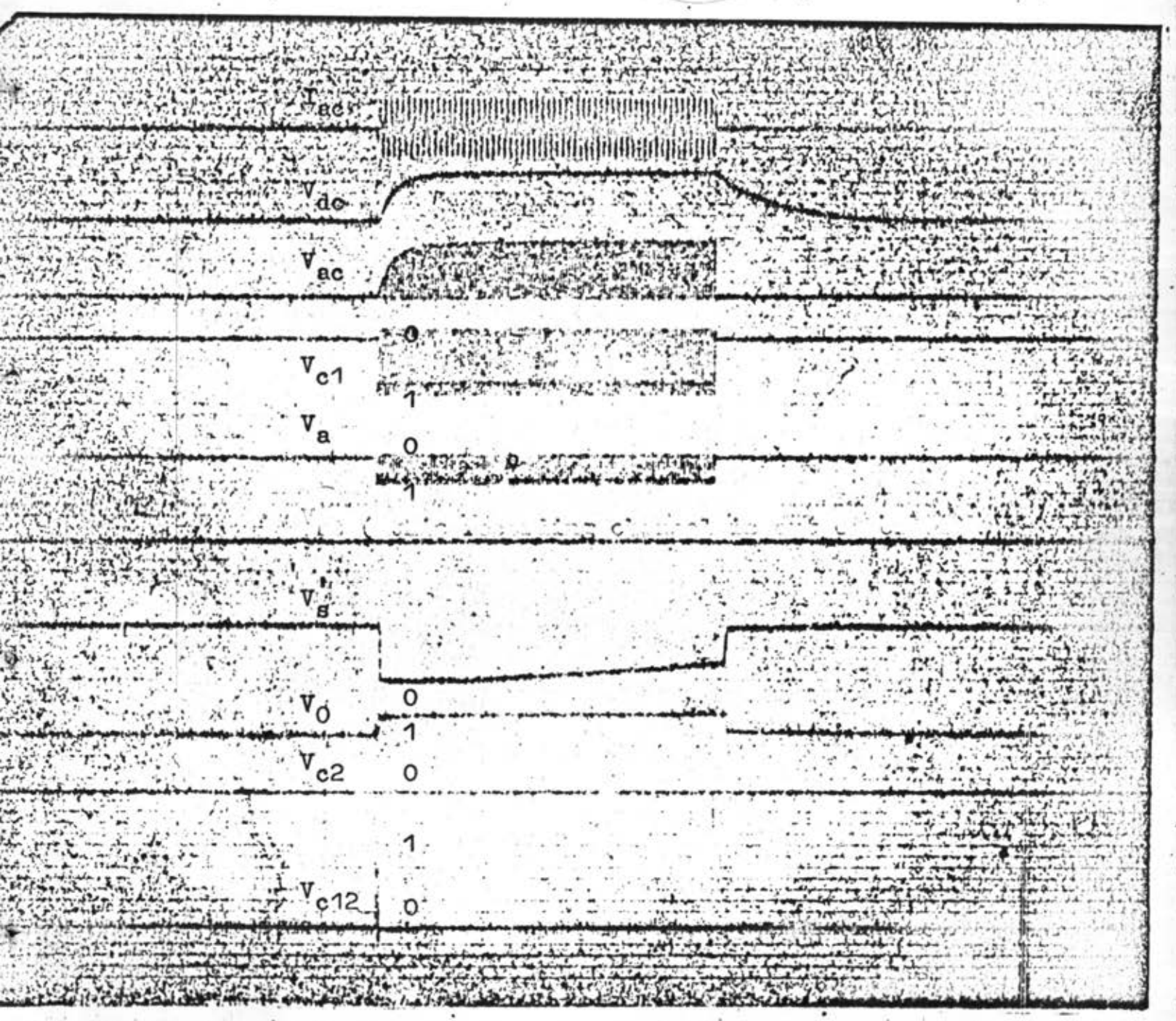


Fig.3.4-2 The waveforms of the relay reset operation.

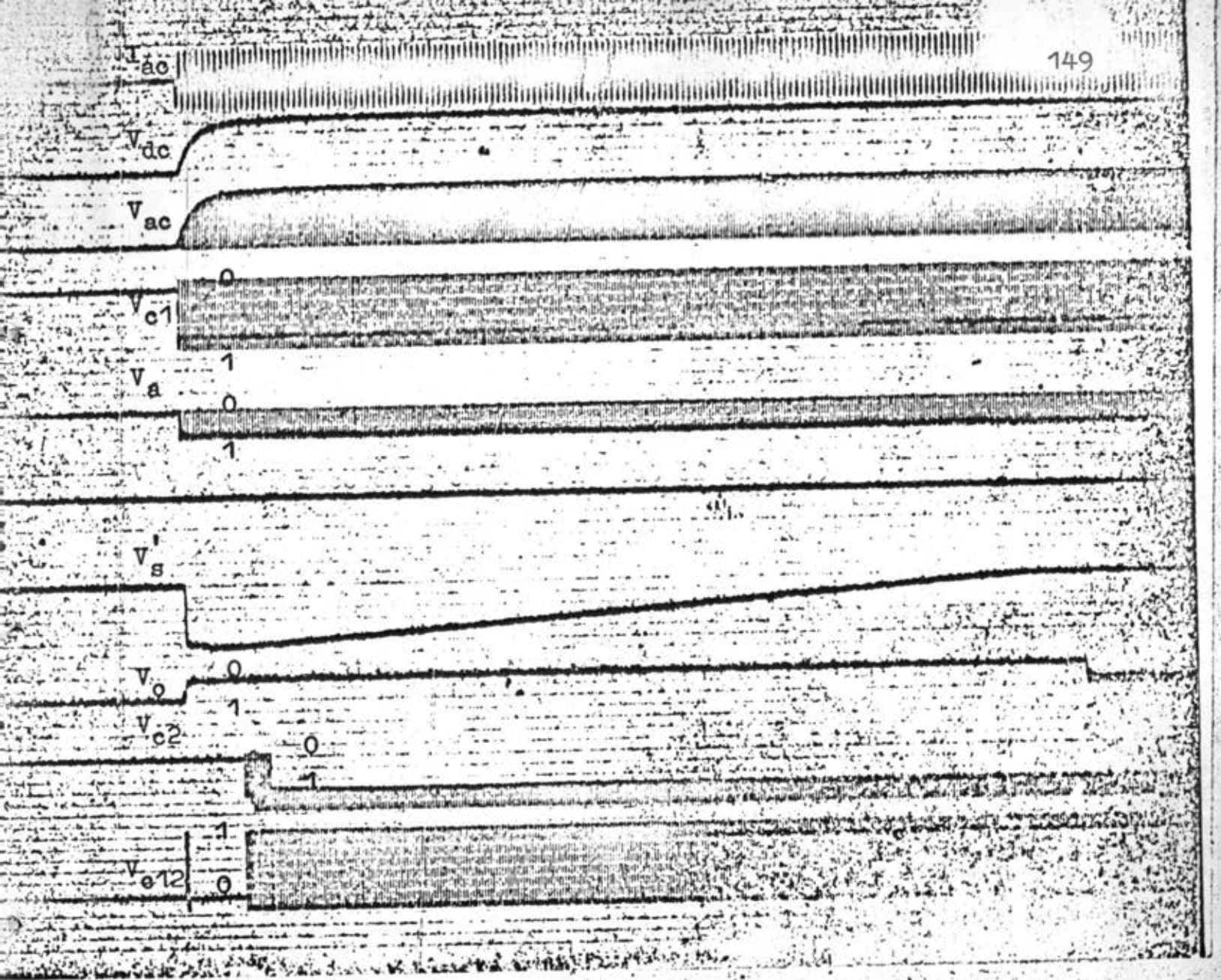


Fig.3.4-3 The waveforms of the instantaneous operation.

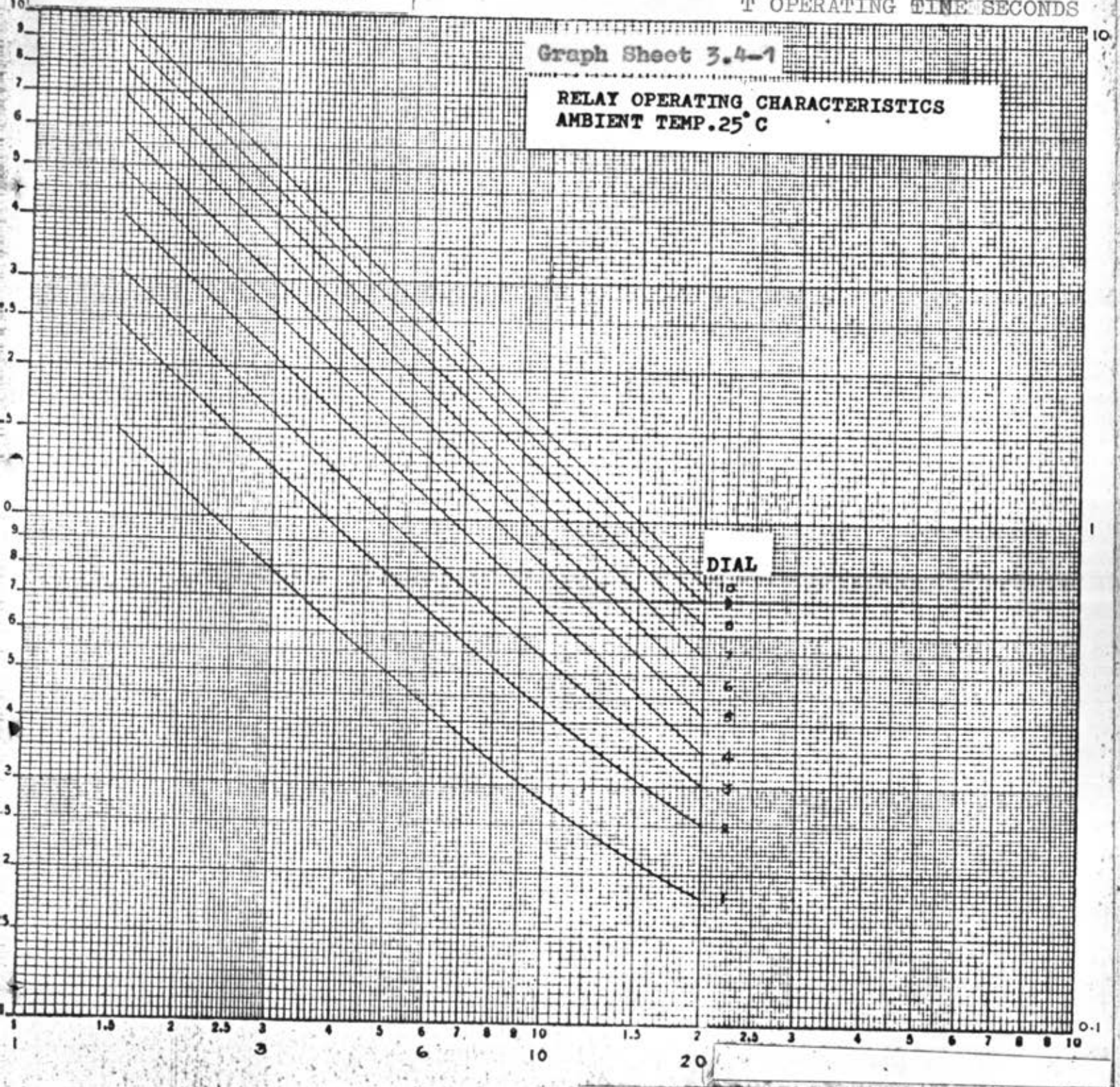
GRAPH SHEET 1

T OPERATING TIME SECONDS

T OPERATING TIME SECONDS

Graph Sheet 3.4-1

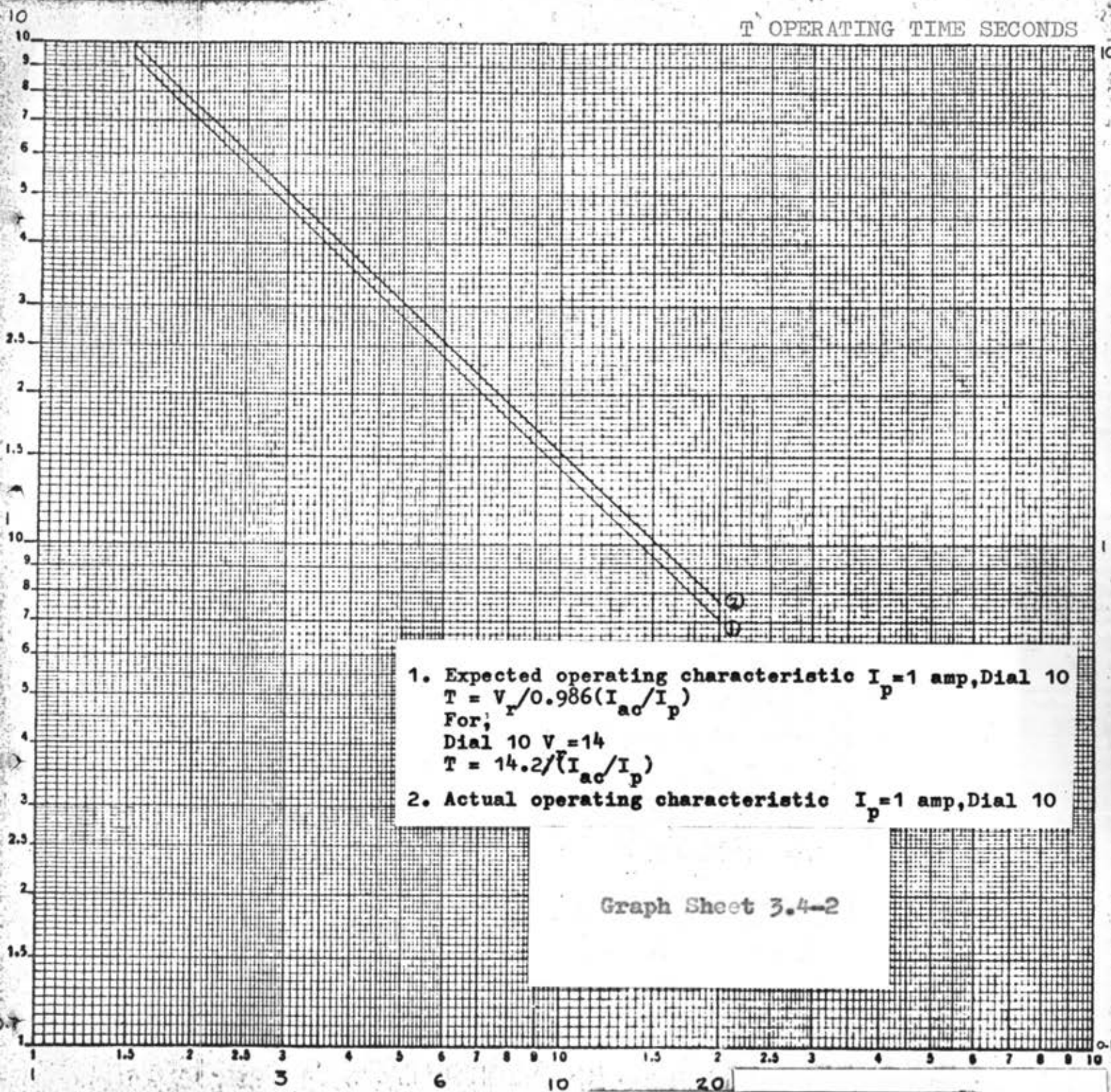
RELAY OPERATING CHARACTERISTICS
AMBIENT TEMP. 25° C



OPERATING CURRENT MULTIPLE OF SETTING
I_{ac}/I_p

GRAPH SHEET 2

T OPERATING TIME SECONDS

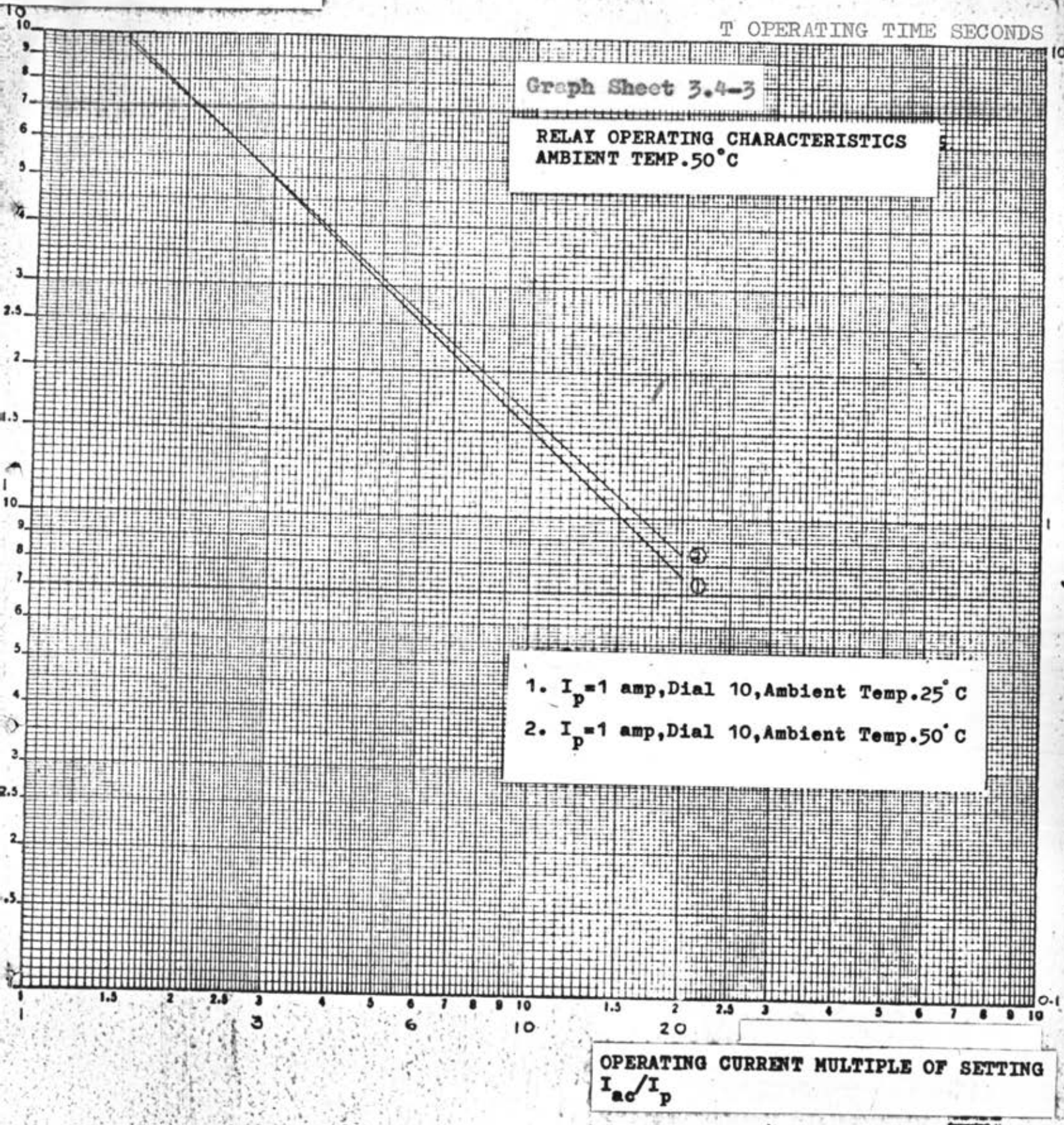


1. Expected operating characteristic I_p=1 amp, Dial 10
   $T = V_r/0.986(I_{ac}/I_p)$
   For,
   Dial 10 V_r=14
   $T = 14.2/(I_{ac}/I_p)$
2. Actual operating characteristic I_p=1 amp, Dial 10

Graph Sheet 3.4-2

GRAPH SHEET 3

T OPERATING TIME SECONDS



GRAPH SHEET 4

OPERATING TIME SECONDS

T OPERATING TIME SECONDS

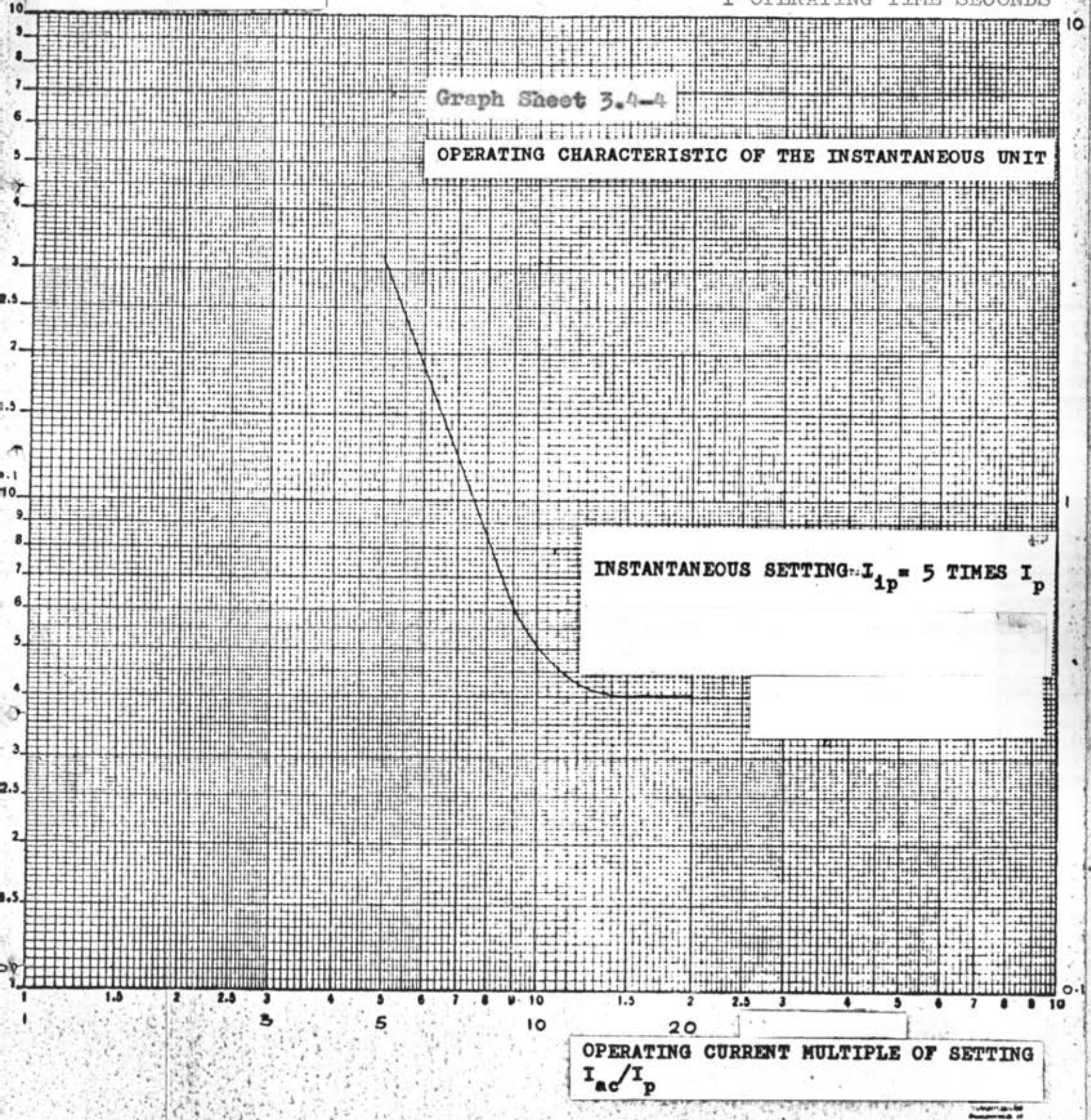


Table 3.4-1 Relay operating characteristics at 25°c

Dial	1	2	3	4	5	6	7	8	9	10
I_{ac}/I_p	operating time sec.									
1.5	1.47	2.41	3.10	4.03	4.95	5.80	6.91	7.82	8.82	9.82
3	0.8	1.26	1.62	2.10	2.58	2.98	3.56	4.03	4.51	5.01
6	0.43	0.66	0.84	1.10	1.34	1.53	1.80	2.05	2.30	2.53
10	0.28	0.42	0.54	0.68	0.82	0.93	1.08	1.25	1.38	1.52
20	0.18	0.25	0.30	0.35	0.42	0.48	0.55	0.63	0.70	0.76

I_{ac} = operating current amp.

I_p = pick-up current setting amp.

The relay setting, under test, is 1 amp.

Table 3.4-2 Relay operating characteristics at 50°c

I_{ac}/I_p	T sec.
1.5	9.6
3	5.1
6	2.6
10	1.53
20	0.85

The relay setting is I_p=1, dial=10.

T = operating time.

Table 3.4-3 The operating characteristics of the instantaneous unit.

I_{ac}/I_p	T sec.
5	0.32
10	0.05
15	0.04
20	0.04

The instantaneous pick-up setting=5 amp.
The pick-up current setting I_p =1 amp.

V_{c2}, the amplifier-2 output to initiate the second or-gate

= 0, no instantaneous trip signal

= 1, instantaneous trip signal

V_{c12}, T_{12} collector voltage

= 0, opening of the relay contact

= 1, closing of the relay contact

V_{ac} is fed into the comparator-2 (block 4) and causes its output V_{c1} to oscillate between 0 and 1. V_{c1} is then amplified by the amplifier-1 the output of which are V_a and V_{st}. V_a oscillates between 0 and 1 thus the and-gate, which is initiated by V_a, closes and opens periodically to allow and block the trip signal. V_{st} changes from 1 to 0 state and consequently starts integration of the integrator to establish a delay time (V_{st} is a d.c. signal, please refer to Sec. 3.3.6). This delay time is inversely proportional to the magnitude of the operating current (I_{ac}). While integration starts, V_o the output of the comparator-1 changes from 1 to 0 and V_{c2} the output of the amplifier-2 is at 0 state, therefore the relay contact remains open. A pulse signal of a short duration appears in the recored waveform of V_{12} i.e. V_{c12} changes from 0 to 1. This is because of the slow transition of V_o. however the relay contact remains open since the inductance of the relay coil prevents a sudden increase of the relay coil current. After the relay time, which is determined by the operating current I_{ac} and the number of dial setting, V_o returns to state 1 and therefore the pulsetrain voltage V_a is transmitted to T_{12} collector as seen in the record of V_{c12}. The oscillation of V_{c12} causes a d.c. fluctuating current to flow through

decreases at high operating current. This is beeause of the time needed by the sweep voltage V_s' to accelerated to the constant sweep speed, as seen in Fig.3.4-1, is large compared to the relay operating time. Table 3.4-1 is the relay operating time of the relay.

Graph sheet 3.4-2 shows the expected operating characteristic compared to the actual characteristic. The operating characteristic equation is obtained as follows.

From the result of the experiment-2 in Sec.3.3.2.

$$I_{dc} = 0.218*(I_{ac}/I_p)$$

and from the result of the experiment-3 in Sec.3.3.2

$$V_s = 4.52*I_{dc}*t$$

where I_{dc} = the d.c. input current into the integrator (ma)

I_{ac} = the operating current (amp)

I_p = the pick-up current setting (amp)

V_s = the effective sweep voltage (volt)

t = time (second)

The above equations combine to be

$$V_s = 4.52*0.218*(I_{ac}/I_p)*t$$

$$= 0.986*(I_{ac}/I_p)*t$$

The relay operating time T is corresponding to the time that V_s sweeps to V_r, the effective reference voltage, therefore

$$V_r = 0.986*(I_{ac}/I_p)*T$$

or $$T = V_r/(0.986*(I_{ac}/I_p))$$

for I_p = 1 amp

and the dial number = 10, V_r = 14 volts (from Table3.3.3-2)

the relay coil, hence the relay contact closes and the operation of the relay is complete.

Fig. 3.4-2 shows the waveforms of the relay reset operation. The waveforms of the associated voltage are similar to that in Fig.3.4-1 when an overcurrent occurs. The difference is that before completion of the relay operation the operating current I_{ac} has disappeared. In this situation, V_{ac} collapses as soon as I_{ac} collapses. But V_{dc} decays exponentially with the time constant of 160 ms (from the record in Fig. 3.4-2). V_{c1} which is controlled by V_{ac} suddenly returns to 0 state. Therefore no trip signal is allowed through the and-gate. V_{st} can not change instantaneously from 0 to 1 because of the presence of the capacitance C_{21}. Hence the integration continues about 40 ms (from V_s' wavefrom in Fig.3.4-2 after I_{ac} has collapsed. If the number of dial setting is such a low number that V_s' overcomes the reference voltage V_r' and causes V_o to change from 0 to 1 within this 40 ms, there is still no trip signal at T_{12} collector since V_a is in the blocking state during this time interval. Therefore no overtravel trip signal can occur, and the advantage of the and-gate is to eliminate the overtravel.

Operating Characteristics :

Graph sheet 3.4-1 shows the operating characteristics of the relay at the ambient temperature of 25° C. The curves between the delay operating time T and the operating current I_{ac}/I_p in terms of multiple of the pick-up current setting are straight line, on the log-log paper, for the dial setting of 4 to 10. For dial setting of 1 to 3, the slope of the curve

The operating equation becomes

$T = 14.2/I_{ac}$

The expected operating time is less than the actual operating time since the accelerating time of V_s', the time that V_s' requires to drive the comparator-1 and the operating time of the output relay is not taken into consideration.

Graph sheet 3.4-3 shows the operating characteristic of the relay at the ambient temperature of 50° C compared to that of 25° C. The actual pick-up current at 50° C for 1 amp pick-up current setting is 1.15 amp which is 15% more than the setting. The operating time at 50° C for I_{ac} of 1.5 amp and dial 10 is 2.2% less than that at 25° C for the same operating current and the same dial. The operating time at 50° C for I_{ac} of 20 amp and dial 10 is 11.3% more than that at 25° C for the same operating current and the same dial. The data of the operating characteristic at 50° C is in Table 3.4-2.

3.4.2 The Definite Minimum Time-Lag Unit

Fig.3.4-3 shows the waveforms of the operation of the definite minimum time-lag unit. The operating current I_{ac} is larger than the definite minimum time-lag unit pick-up current setting times the time delay pick-up current setting ($I_p * I_{ip}$). (Please refer to the experiment in Sec.3.3.5) Therefore V_{c2} changes from 0 to 1 and is supervised by the pulse train V_a to establish the final trip signal V_{c12} to energise the relay coil.

Operating Characteristics :

Graph sheet 3.4-4 shows the operating time of the instantaneous unit against the operating current for the instantaneous pick-up current setting of $5^{*}I_{p}$. The operating time at low operating current is not fast enough. This is because of the presence of the capacitor C in the input circuit and the operating time of the output relay. Table 3.4-3 is the operating data of the instantaneous unit.

Power Consumption :

The designed relay needs a continuous d.c. power drain of 2.98 watts (+30 volts and 46 ma, -30 volts and 950 ma). The input resistance seen by the operating current is 0.02 ohms. The predominent load resistance is the primary winding of the current transformer. Thus at 60 amp operating current the power consumption is 72 watts which is such lower than the power consumption of the conventional overcurrent relay operating at the same current.

3.5 Comparison Between the Designed Relay and a Typical Electro- Mechanical Relay

The designed solid-state inverse time-lag relay with definite minimum time-lag looks more complicate than an electro-mechanical one. However the design of this relay is based on the operation of a typical electro - mechanical relay. The operating characteristics of the inverse-time lag unit of a typical electromechanical relay is accomplished by converting the operating current into a torque exerting on a rotating disc. This torque must overcome the restraining torque of the control spring in order to cause the disc to rotate. The delay operating time is the time that

the moving contact uses to reach the stationary contacts. In the designed relay the operating current is converted into a voltage which must overcome the first reference voltage to start a sweep voltage. The delay operating time is the time that the sweep voltage uses to reach the second reference voltage.

The operation of the definite minimum time-lag unit of a typical electromechanical relay is that the operating current is converted into a force which must overcome the restraining force in order to close the output contact. In the designed relay, the operating current is converted into a voltage which must overcome the reference voltage in order to close the output contact.

The comparison between the designed relay and a typical electromechanical one is in the below table.

	Designed Relay	Electromechanical Relay
Power consumption	low	high
Continuous power drain	d.c. supply	-
Input impedance	resistive	resistive + inductive
Temperature effect	more effect	less effect
Overtravel	-	yes
Pick-up current setting	continuous	discrete
Dial setting	continuous	continuous
Reset time	fast	slow

Besides, the above consideration, there are some more topics to be considered, if the designed relay were put in service, such as cost, reliability, aging etc..