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ภาคผนวก

ภาคผนวก ก.

การคำนวณหม้อแปลงไฟฟ้าศักดาสูง [4]

หม้อแปลงไฟฟ้าศักดาสูงคำนวณได้จากพารามิเตอร์ดังนี้ แหล่งจ่ายไฟฟ้าศักดาต่ำ (V_{cc}) เท่ากับ 5 โวลต์ ความต้านทานขาอิมิตเตอร์ (R_E) เท่ากับ 200 โอห์ม ความถี่ที่ใช้ 60 กิโลเฮิรตซ์ ดิวตีไซเคิล เท่ากับ 0.5 (duty cycle = t_d/T_P) t_d (pulse duration) เท่ากับ 8.34 ไมโครวินาที T_P (pulse period) เท่ากับ 16.667 ไมโครวินาที

การคำนวณหม้อแปลงไฟฟ้าศักดาสูงมีขั้นตอนดังนี้

1. คำนวณค่าความเหนี่ยวนำขดปฐมภูมิ (primary inductance; L_P)

จากสมการ $$t_d = \frac{L_P}{nR_E}$$

ดังนั้น $$L_P = t_d \times n \times R_E$$

เมื่อ n = 1

$$L_P = 8.34 \times 10^{-6} \times 1 \times 200$$

$$= 1.668 \text{ mH}$$

$I_o = i_m$ (เมื่อ $t = t_d$) = peak magnetizing current

$$I_o = \frac{V_{cc}}{n+1} \cdot \frac{t_d}{L_p}$$

$$I_o = \frac{5}{1+1} \cdot \frac{8.34 \times 10^{-6}}{1.668 \times 10^{-3}}$$

$$= 12.5 \text{ mA}$$

2. เลือกชนิดและขนาดของแกนหม้อแปลงไฟฟ้า (จาก Data book TDK ferrite cores-2 for Telecommunication and industrial fields) จากความถี่ที่ใช้งาน 60 KHz เลือกใช้แกนเบอร์ H5B P14/8 Z-52H มีค่าพารามิเตอร์ดังนี้

A_L (Inductance coefficient) = 7400 nH/N^2

μ_e (Effective permeability) = 4646

$\Sigma l/A$ (Core factor) = 7.89 cm^{-1}

A_e (Effective area) = 0.251 cm^2

l_e (Effective length) = 1.98 cm

V_e (Effective volume) = 0.495 cm^3

3. คำนวณจำนวนรอบ

จากสมการ $N_p = \sqrt{\frac{L_p}{A_L}}$

ดังนั้น N_p = 15 รอบ

$N_{s1} = N_p$ = 15 รอบ

จาก V_o = 250 โวลต์

$$\frac{N_s}{N_p} = \frac{V_o}{V_p}$$

$$N_{s2} = \frac{N_p \times V_o}{V_p}$$

N_{s2} = 750 รอบ

4. ตรวจสอบจุดอิ่มตัวของแกนที่ออกแบบ

หาค่า maximum flux density ของแกนคำนวณจากสมการ

$$B_{max} = \frac{aVt_d}{N_p A_e}$$

สมมติให้ attenuation factor a = 1

B_{max} = 0.11T

= 100 mT

จากคู่มือ B_{sat} (Saturation flux density) เท่ากับ 420 mT

$B_{max} < B_{sat}$

แกนที่เลือกใช้ออกแบบใช้งานได้

5. เลือกขนาดของขดลวด จากกราฟใช้ขดลวดเบอร์ AWG 40

<u>สรุป</u> ชนิดของแกน H5B, P14/8 Z-52H (without air gap)

จำนวนรอบขดลวดปฐมภูมิ N_p = 15 รอบ

จำนวนรอบขดลวดทุติยภูมิ 1 N_{s1} = 15 รอบ

จำนวนรอบขดลวดทุติยภูมิ 2 N_{s2} = 750 รอบ (N_p / N_{s2} = 1 / 50)

ขนาดขดลวดเบอร์ AWG 40 (Enamelled copper wire)

ภาคผนวก ข.

ตารางแสดงการเลือกค่าหารความถี่ที่ตำแหน่งต่างๆ ของสวิตช์ SW_2 และ SW_3

ตารางที่ ข.1 ตารางเลือกค่าหารความถี่ที่ตำแหน่งต่างๆ ของ SW_2

จำนวนเลขฐาน 10	SW_{2-1}	SW_{2-2}	SW_{2-3}	SW_{2-4}	SW_{2-5}	SW_{2-6}	SW_{2-7}	SW_{2-8}
32	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF
64	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF
128	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF
256	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF
512	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF
1024	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF
2048	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF
4098	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON

ตารางที่ ข.2 ตารางเลือกค่าหารความถี่ที่ตำแหน่งต่างๆของSW_3

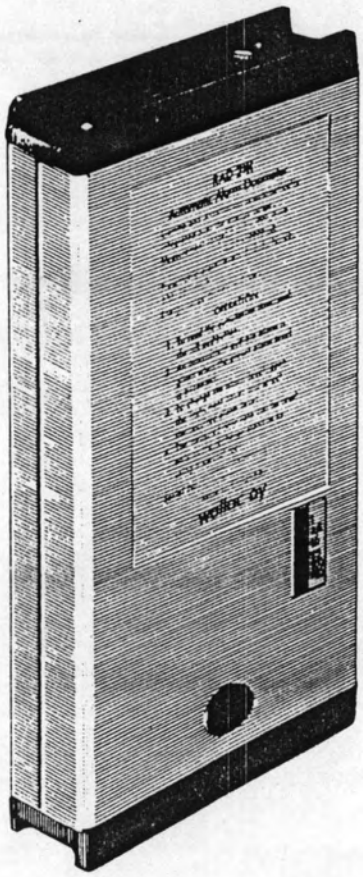
จำนวนหารเลขฐาน 10	SW_{3-1}	SW_{3-2}	SW_{3-3}	SW_{3-4}
0 (ไม่ใช้)	OFF	OFF	OFF	OFF
1	ON	OFF	OFF	OFF
2	OFF	ON	OFF	OFF
3	ON	ON	OFF	OFF
4	OFF	OFF	ON	OFF
5	ON	OFF	ON	OFF
6	OFF	ON	ON	OFF
7	ON	ON	ON	OFF
8	OFF	OFF	OFF	ON
9	ON	OFF	OFF	ON
10	OFF	ON	OFF	ON
11	ON	ON	OFF	ON
12	OFF	OFF	ON	ON
13	ON	OFF	ON	ON
14	OFF	ON	ON	ON
15	ON	ON	ON	ON

ภาคผนวก ค.

พิกัดของเครื่องวัดปริมาณรังสีประจำบุคคลจากต่างประเทศ

ALNOR

Radiation dosimeter and dose rate alarm monitor RAD-21 L



SPECIFICATIONS:

Radiation Detected:	X-ray and Gamma Radiation
Dose Measurement Range:	0,1 mR to 999,9 mR
Dose Rate Alarm Levels:	Selectable 1, 2, 5, 10, 25, 100, 250 mR/h
Accuracy of Dose Measurement:	±15% of indicated dose excluding energy dependence
Accuracy of Dose Rate Alarms:	±20% excluding energy dependence
Energy Dependence:	±20% from 50 KeV to 3 MeV gamma radiation.
Detector:	Halogen quenched GM-tube with filter
Display:	Four digit LED display
Switches:	Display "mR" push-button Alarm level select switch inside the instrument
Audible Signals:	Dose rate alarm: 2500 Hz, intermittent
Test Signal:	Same as the dose rate alarm signal above
Display overflow indication:	0.0.0.0.
Batteries:	3 x 1,5 V, size AA, IEC R6 or 3 x 1,25 V rechargeable batteries of the same size
Battery life:	Typically 500 h when rechargeable batteries (450 mAh) are used.
Operating temperature:	— 20 to + 50°C
Dimensions:	73 mm x 135 mm x 22 mm
Weight:	210 g
Accessories: Standard	Tool for resetting dose memory
Optional:	Battery charging equipment for either 3 or 10 RAD-21 monitors Dose reader

Data subject to change without notice

CALIBRATION

Alarm level calibration

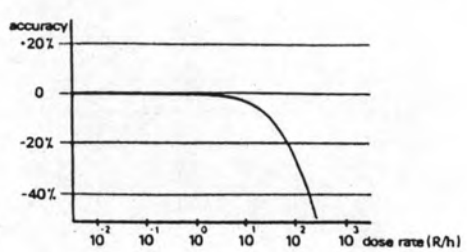
The calibration of each alarm levels is made by a pulse generator and at two levels by means of a radiation source.

Source: ^{137}Cs, activity abt. 50mCi

Calibration points: 25mR/h

The instrument shall give the alarm in the point $D_n + 10\%$ and shall not in the point $D_{n-10\%}$ where the D_n is the nominal dose rate.

Calibrated by: HA



ภาคผนวก ง.

ลักษณะพิกัดของอุปกรณ์ที่สำคัญ

ง.1 ลักษณะพิกัดของหัววัดรังสีไกเกอร์ที่ใช้ในเครื่องวัดปริมาณรังสีประจำบุคคล

ง.2 ลักษณะพิกัดของไอซีเบอร์ ICM 7217

ง.3 ตารางเทียบหัววัดรังสีไกเกอร์ของผู้ผลิตต่างๆ

LND 716

THIN WALL BETA GAMMA DETECTOR

The LND 716 is a halogen quenched Thin Wall Beta Gamma Detector.

GENERAL SPECIFICATIONS

Gas Filling:	Ne + Halogen Admixture
Cathode Material	446 Stainless Steel
Maximum Length: (inches/mm)	1.0/25.4
Effective Length: (inches/mm)	0.125/3.18
Maximum Diameter: (inches/mm)	0.200/5.08
Effective Diameter: (inches/mm)	0.190/4.82
Connector:	Pin
Operating Temperature Range: (°C)	-40 to +75

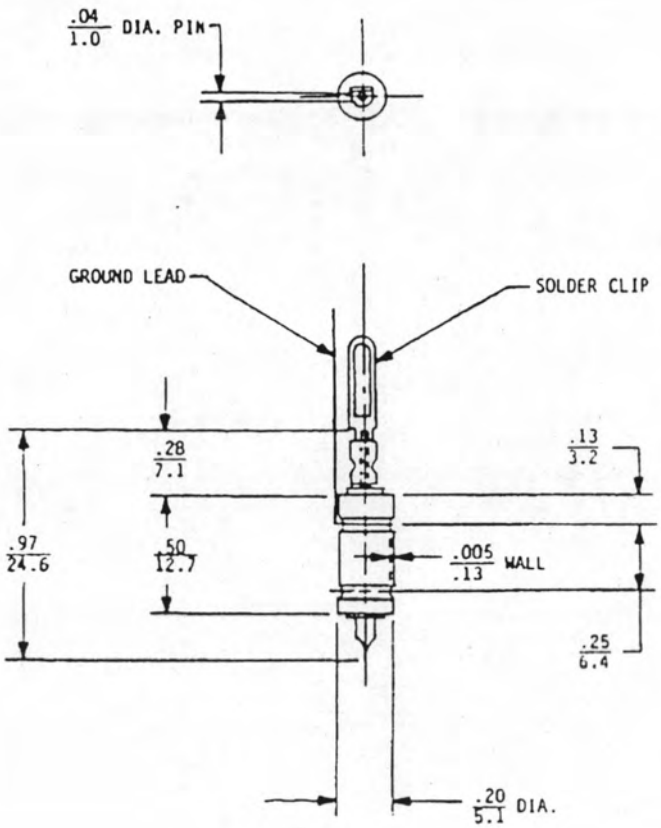
WALL SPECIFICATIONS

Areal Density: (mg/cm^2)	90
Thickness: (inches/mm)	0.01/0.25

ELECTRICAL SPECIFICATIONS

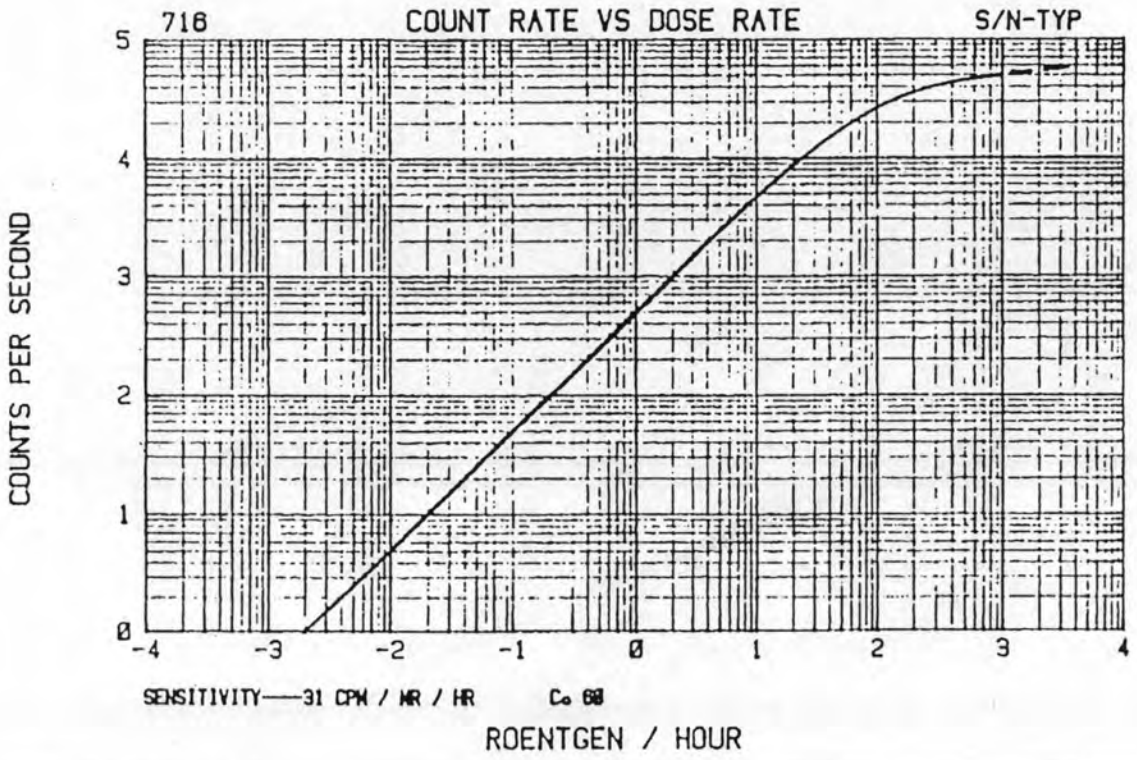
Recommended Anode Resistor: (mΩ)	10
Maximum Starting Voltage: (volts)	390
Recommended Operating Voltage: (volts)	500
Operating Voltage Range: (volts)	450-600
Maximum Plateau Slope: (%/100 volts)	20
Minimum Dead Time: (µs)	20

The LND 716 is available with a sensitivity of 60 C/M/MR/hr as the 71630.



Designers & Manufacturers of LND, INC. Nuclear Radiation Detectors

3230 Lawson Blvd., Oceanside, N.Y. 11572 (516) 678-6141 / Telex 14-4583



Designers & Manufacturers of LND, INC. Nuclear Radiation Detectors

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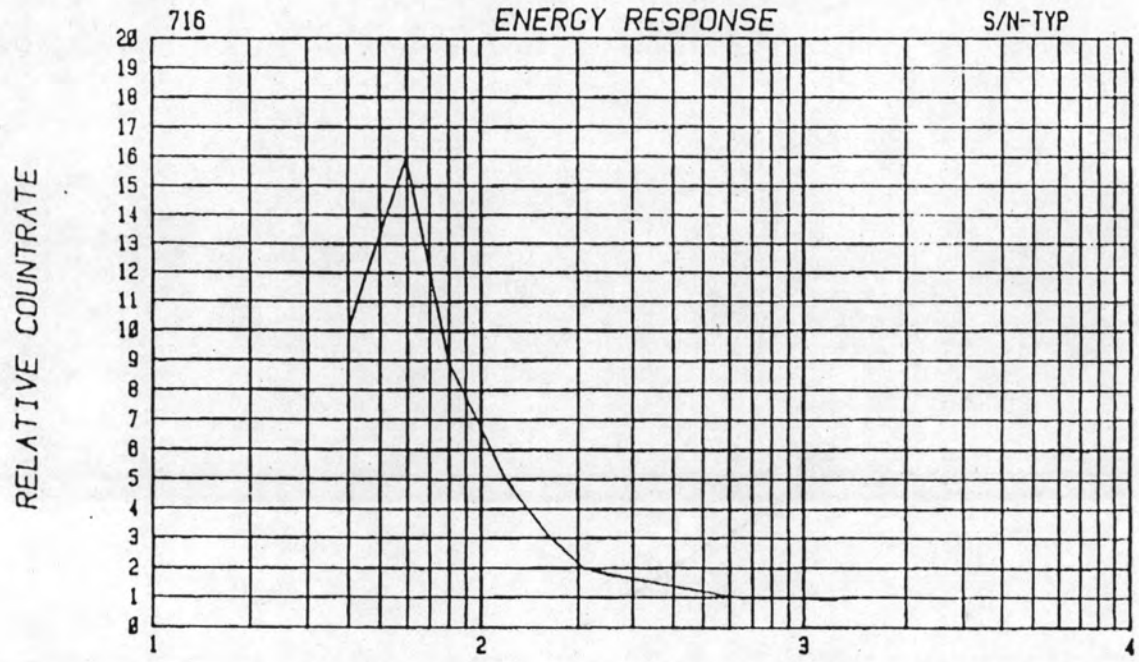


ICM7217/ICM7227
4-Digit LED Display Programmable Up/Down Counter

INTERSIL

GENERAL DESCRIPTION

The ICM7217 and ICM7227 are four digit, presettable up/down counters, each with an onboard presettable register continuously compared to the counter. The ICM7217 versions are intended for use in hardwired applications where thumbwheel switches are used for loading data, and simple SPDT switches are used for chip control. The ICM7227 versions are for use in processor-based systems, where presetting and control functions are performed under processor control.

These circuits provide multiplexed 7 segment LED display outputs, with common anode or common cathode configurations available. Digit and segment drivers are provided to directly drive displays of up to 0.8" character height (common anode) at a 25% duty cycle. The frequency of the onboard multiplex oscillator may be controlled with a single capacitor, or the oscillator may be allowed to free run. Leading zeros can be blanked. The data appearing at the 7 segment and BCD outputs is latched; the content of the counter is transferred into the latches under external control by means of the Store pin.

The ICM7217/7227 (common anode) and ICM7217A/7227A (common cathode) versions are decade counters, providing a maximum count of 9999, while the ICM7217B, 7227B (common anode) and ICM7217C/7227C (common cathode) are intended for timing purposes, providing a maximum count of 5959.

FEATURES

- **Four Decade, Presettable Up-Down Counter With Parallel Zero Detect**
- **Settable Register With Contents Continuously Compared to Counter**
- **Directly Drives Multiplexed 7 Segment Common Anode or Common Cathode LED Displays**
- **On-Board Multiplex Scan Oscillator**
- **Schmitt Trigger On Count Input**
- **TTL Compatible BCD I/O Port, Carry/Borrow, Equal, and Zero Outputs**
- **Display Blank Control for Lower Power Operation; Quiescent Power Dissipation <5mW**
- **All Terminals Fully Protected Against Static Discharge**
- **Single 5V Supply Operation**

These circuits provide 3 main outputs; a CARRY/BORROW output, which allows for direct cascading of counters, a $\overline{\text{ZERO}}$ output, which indicates when the count is zero, and an $\overline{\text{EQUAL}}$ output, which indicates when the count is equal to the value contained in the register. Data is multiplexed to and from the device by means of a three-state BCD I/O port. The CARRY/BORROW, $\overline{\text{EQUAL}}$, $\overline{\text{ZERO}}$ outputs, and the BCD port will each drive one standard TTL load.

To permit operation in noisy environments and to prevent multiple triggering with slowly changing inputs, the count input is provided with a Schmitt trigger.

Input frequency is guaranteed to 2MHz, although the device will typically run with f_{in} as high as 5MHz. Counting and comparing ($\overline{\text{EQUAL}}$ output) will typically run 750kHz maximum.

ORDERING INFORMATION

Part Number	Temperature Range	Package	Display Option	Count Option Max Count
ICM7217IJI	−25°C to +85°C	28 Lead CERDIP	Common Anode	Decade/9999
ICM7217AIPI	−25°C to +85°C	28 Lead PLASTIC	Common Cathode	Decade/9999
ICM7217BIJI	−25°C to +85°C	28 Lead CERDIP	Common Anode	Timer/5959
ICM7217CIPI	−25°C to +85°C	28 Lead PLASTIC	Common Cathode	Timer/5959
ICM7227IJI	−25°C to +85°C	28 Lead CERDIP	Common Anode	Decade/9999
ICM7227AIPI	−25°C to +85°C	28 Lead PLASTIC	Common Cathode	Decade/9999
ICM7227BIJI	−25°C to +85°C	28 Lead CERDIP	Common Anode	Timer/5959
ICM7227CIPI	−25°C to +85°C	28 Lead PLASTIC	Common Cathode	Timer/5959

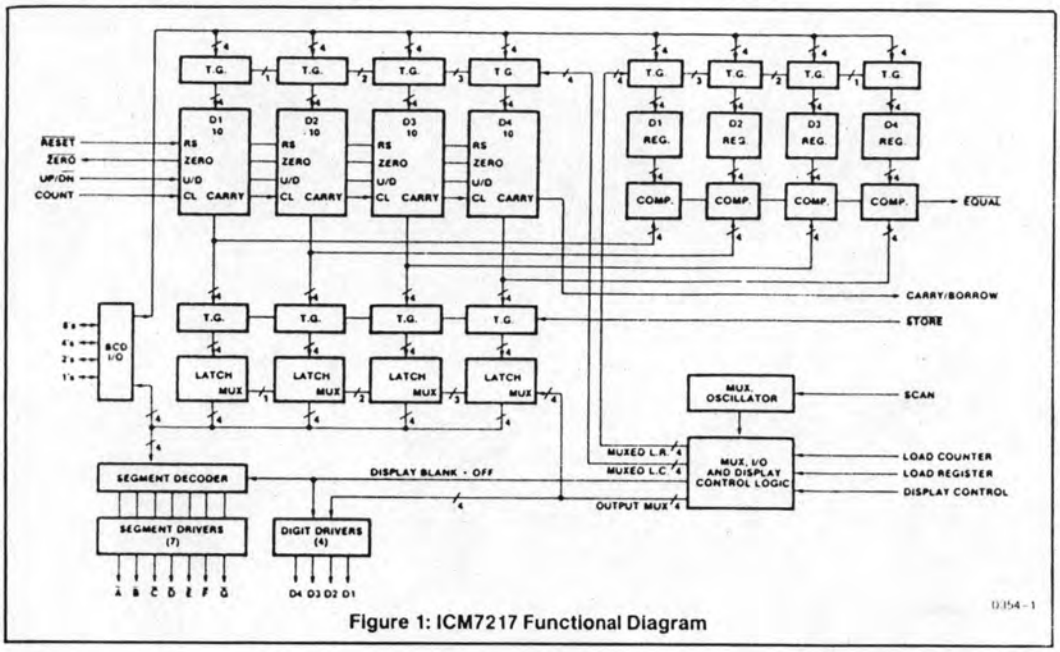


Figure 1: ICM7217 Functional Diagram

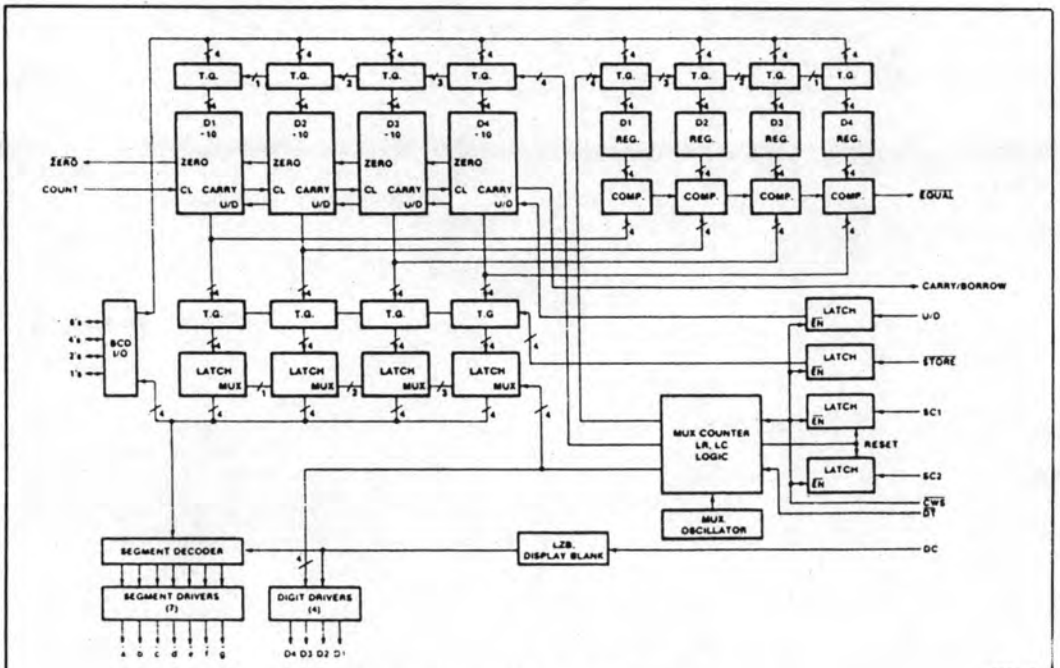


Figure 2: ICM7227 Functional Diagram

ICM7217/ICM7227

INTERSIL

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ($V_{DD} - V_{SS}$) 6V
Input Voltage (any terminal) ..... (V_{DD} + 0.3V to V_{SS} − 0.3V) Note 2
Power Dissipation (common anode/Cerdip) .... 1W Note 1
Power Dissipation (common cathode/Plastic) ..... 0.5W Note 1
Operating Temperature Range ..... −25°C to +85°C
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (Soldering, 10sec) ..... 300°C

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

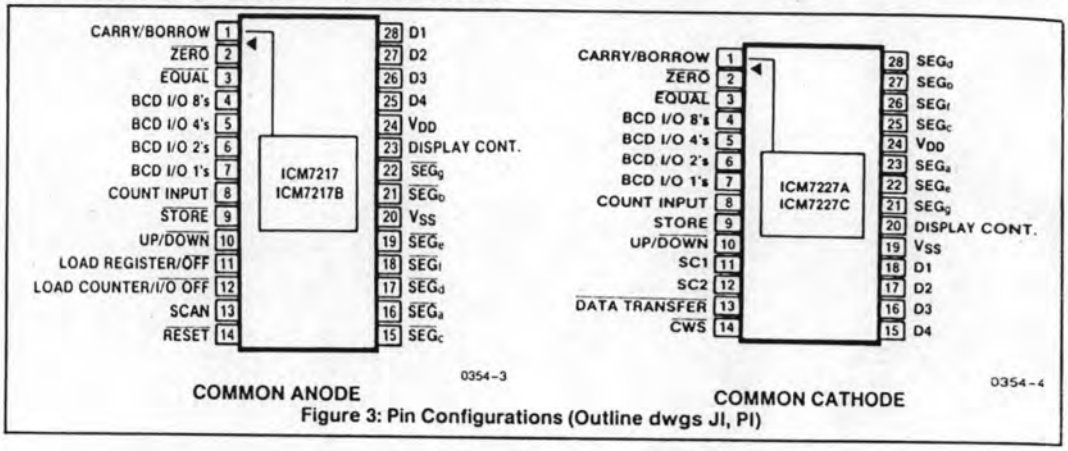


Figure 3: Pin Configurations (Outline dwgs JI, PI)

ELECTRICAL CHARACTERISTICS

(V_{DD} = 5V, V_{SS} = 0V, T_A = 25°C, Display Diode Drop 1.7V, unless otherwise specified)

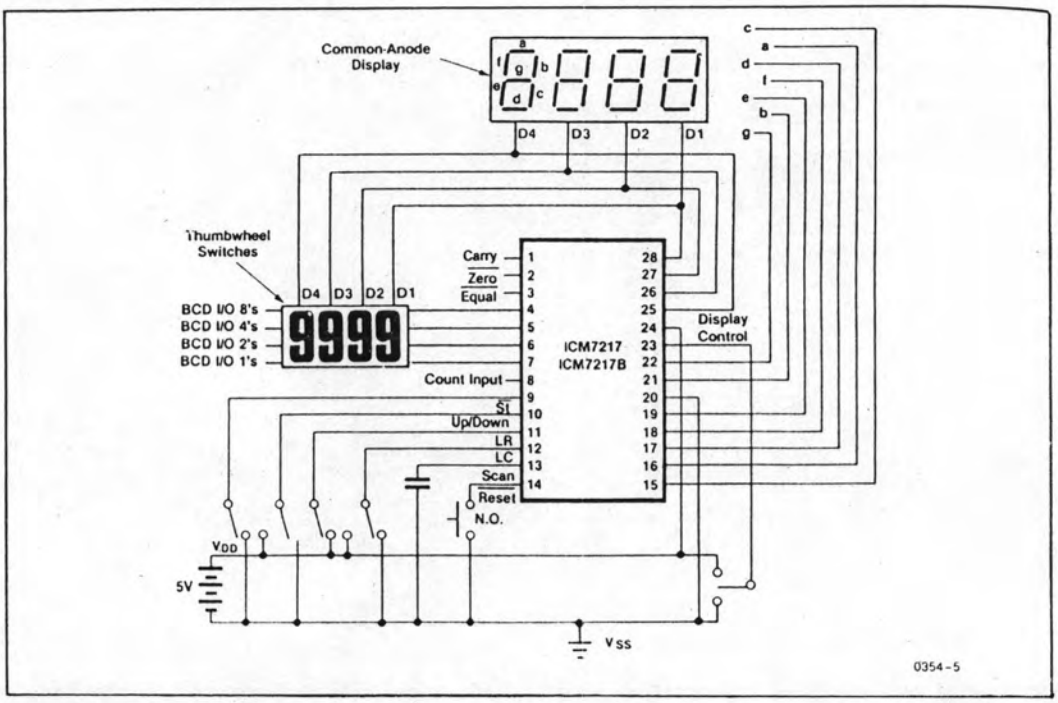
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{DD} (7217)	Supply Current (Lowest power mode)	Display Off, LC, DC, UP/DN, ST, RS, BCD I/O Floating or at V_{DD} (Note 3)		350	500	µA
I_{DD} (7227)	Supply current (Lowest power mode)	Display off (Note 3)		300	500	µA
I_{OP}	Supply Current OPERATING	Common Anode, Display On, all "8's"	140	200		mA
		Common Cathode, Display On, all "8's"	50	100		mA
V_{DD}	Supply Voltage		4.5	5	5.5	V
I_{DIG}	Digit Driver output current	Common anode, $V_{OUT} = V_{DD} - 2.0V$	140	200		mA peak
I_{SEG}	SEGment driver output current	Common anode, $V_{OUT} = +1.5V$	−20	−35		mA peak
I_{DIG}	Digit Driver output current	Common cathode, $V_{OUT} = +1.0V$	−50	−75		mA peak
I_{SEG}	SEGment driver output current	Common cathode $V_{OUT} = V_{DD} - 2V$	9	12.5		mA peak
I_P	$\overline{ST}$, $\overline{RS}$, UP/$\overline{DN}$ input pullup current	$V_{OUT} = V_{DD} - 2V$ (See Note 3)	5	25		µA
Z_{IN}	3 level input impedance		40		350	kΩ

ELECTRICAL CHARACTERISTICS (Continued) (V_{DD} = 5V, V_{SS} = 0V, T_A = 25°C, Display Diode Drop 1.7V, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{BIH}	BCD I/O input high voltage	ICM7217 common anode (Note 4)	1.5			V
		ICM7217 common cathode (Note 4)	4.40			V
		ICM7227 with 50pF effective load	3			V
V_{BIL}	BCD I/O input low voltage	ICM7217 common anode (Note 4)			0.60	V
		ICM7217 common cathode (Note 4)			3.2V	V
		ICM7227 with 50pF effective load			1.5	V
I_{BPU}	BCD I/O input pullup current	ICM7217 common cathode $V_{IN} = V_{DD} - 2V$ (Note 3)	5	25		μA
I_{BPD}	BCD I/O input pulldown current	ICM7217 common anode $V_{IN} = +2V$ (Note 3)	5	25		μA
V_{OH}	BCD I/O, $\overline{ZERO}$, $\overline{EQUAL}$ Outputs output high voltage	$I_{OH} = 100\mu A$	3.5			V
V_{OL}	BCD I/O, CARRY/BORROW $\overline{ZERO}$, $\overline{EQUAL}$ Outputs output low voltage	$I_{OL} = -1.6mA$			0.4	V
f_{in}	Count input frequency (Guaranteed)	$-20°C < T_A < +70°C$	0	5	2	MHz
V_{TH}	Count input threshold	(Note 5)		2		V
V_{HYS}	Count input hysteresis	(Note 5)		0.5		V
V_{CIL}	Count input LO				0.40	V
V_{CIH}	Count Input HI		3.5			V
f_{ds}	Display scan oscillator frequency	Free-running (SCAN terminal open circuit)			10	kHz

NOTES: 1. These limits refer to the package and will not be obtained during normal operation.

2. Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to a voltage greater than V_{DD} or less than V_{SS} may cause destructive device latchup. For this reason it is recommended that the power supply to the device be established before any inputs are applied and that in multiple systems the supply to the ICM7217/7227 be turned on first.
3. In the ICM7217 the UP/$\overline{DOWN}$, $\overline{STORE}$, $\overline{RESET}$ and the BCD I/O as inputs have pullup or pulldown devices which consume power when connected to the opposite supply. Under these conditions, with the display off, the device will consume typically 750 μA. The ICM7227 devices do not have these pullups or pulldowns and thus are not subject to this condition.
4. These voltages are adjusted to allow the use of thumbwheel switches for the ICM7217 versions. Note that a positive level is taken as an input logic zero for ICM7217 common-cathode versions.
5. Parameters not tested (Guaranteed by Design).



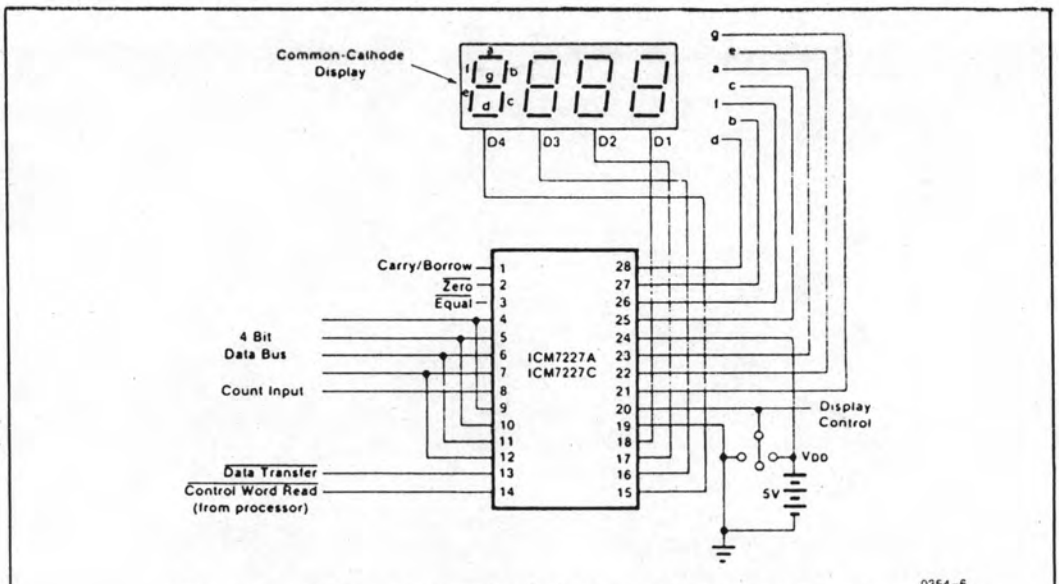
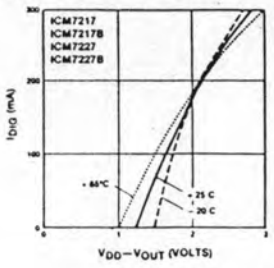


Figure 4: Test Circuits, showing the ICM7217 in the Common-Anode Version and the ICM7227 in the Common-Cathode Version

TYPICAL PERFORMANCE CHARACTERISTICS (DIGIT AND SEGMENT DRIVERS)



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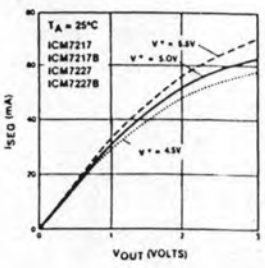
Typical I_{DIG} vs. $V_+ - V_{OUT}$, $4.5V \leq V^+ \leq 6.0V$



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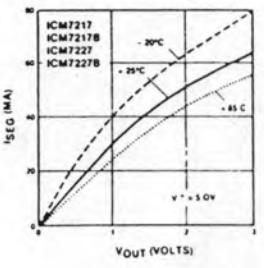
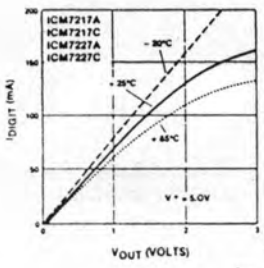
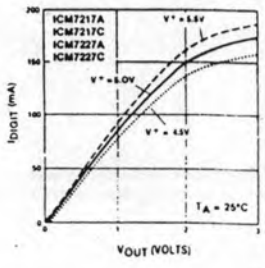


0354-9

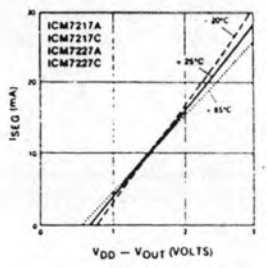
Typical I_{SEG} vs. V_{OUT}



0354-10



0354-11



0354-12

Typical I_{DIGIT} vs. V_{OUT}

Typical I_{SEG} vs. $V_{DD} - V_{OUT}$, $4.5 \leq V_{DD} - V_{SS} \leq 6.0V$

Table 2: Control Input Definitions ICM7217

Input	Terminal	Voltage	Function
$\overline{\text{STORE}}$	9	V_{DD} (or floating) V_{SS}	Output latches not updated Output latches updated
UP/$\overline{\text{DOWN}}$	10	V_{DD} (or floating) V_{SS}	Counter counts up Counter counts down
$\overline{\text{RESET}}$	14	V_{DD} (or floating) V_{SS}	Normal Operation Counter Reset
LOAD COUNTER/ $\overline{\text{I/O OFF}}$	12	Unconnected V_{DD} V_{SS}	Normal operation Counter loaded with BCD data BCD port forced to Hi Z condition
LOAD REGISTER/ $\overline{\text{OFF}}$	11	Unconnected V_{DD} V_{SS}	Normal operation Register loaded with BCD data Display drivers disabled; BCD port forced to Hi Z condition, mpx counter reset to D4; mpx oscillator inhibited
DISPLAY CONTrol (DC)	23 Common Anode 20 Common Cathode	Unconnected V_{DD} V_{SS}	Normal Operation Segment drivers disabled Leading zero blanking inhibited

Table 3: Control Input Definitions ICM7227

Input		Terminal	Voltage	Function
$\overline{\text{DATA TRANSFER}}$		13	V_{DD} V_{SS}	Normal Operation Causes transfer of data as directed by select code
Control Word Port "	STORE	9	V_{DD} (During $\overline{\text{CWS}}$ Pulse) V_{SS}	Output latches updated Output latches not updated
"	UP/$\overline{\text{DOWN}}$	10	V_{DD} (During $\overline{\text{CWS}}$ Pulse) V_{SS}	Counter counts up Counter counts down
" 2"	Select Code Bit 1 (SC1) Select Code Bit 2 (SC2)	11 12	V_{DD} = "1" V_{SS} = "0"	SC1, SC2 control:— 00 Change store and up/$\overline{\text{down}}$ latches. No data transfer. 01 Output latch data active 10 Counter to be preset 11 Register to be preset
$\overline{\text{Control Word Strobe (CWS)}}$		14	V_{DD} V_{SS}	Normal operation Causes control word to be written into control latches
DISPLAY CONTrol (DC)		23 Common Anode 20 Common Cathode	Unconnected V_{DD} V_{SS}	Normal operation Display drivers disabled Leading zero blanking inhibited

DETAILED DESCRIPTION

OUTPUTS

The CARRY/BORROW output is a positive going pulse occurring typically 500ns after the positive going edge of the COUNT INPUT. It occurs when the counter is clocked from 9999 to 0000 when counting up and from 0000 to 9999 when counting down. This output allows direct cascading of counters.

The $\overline{\text{EQUAL}}$ output assumes a negative level when the contents of the counter and register are equal.

The $\overline{\text{ZERO}}$ output assumes a negative level when the content of the counter is 0000.

The CARRY/BORROW, $\overline{\text{EQUAL}}$ and $\overline{\text{ZERO}}$ outputs will drive a single TTL load over the full range of supply voltage and ambient temperature; for a logic zero, these outputs will sink 1.6mA @ 0.4V (on resistance 250Ω), and for a logic one, the outputs will source > 60μA. A 10kΩ pull-up resistor to V_{DD} on the $\overline{\text{EQUAL}}$ or $\overline{\text{ZERO}}$ outputs is recommended for highest speed operation, and on the CARRY/BORROW output when it is being used for cascading.

The Digit and SEGment drivers provide a decoded 7 segment display system, capable of directly driving common anode LED displays at typical peak currents of 40mA/seg. This corresponds to average currents of 10mA/seg at a 25% multiplex duty cycle. For the common cathode versions, peak segment currents are 12.5mA, corresponding to average segment currents of 3.1mA. Figure 5 shows the multiplex timing, while Figure 6 shows the Output Timing. The DISPLAY pin controls the display output using three level logic. The pin is self-biased to a voltage approximately ½ (V_{DD}); this corresponds to normal operation. When this pin is connected to V_{DD}, the segments are inhibited, and when connected to V_{SS}, the leading zero blanking feature is inhibited. For normal operation (display on with leading zero blanking) the pin may be left open. The display may be controlled with a 3 position SPDT switch; see Figure 4.

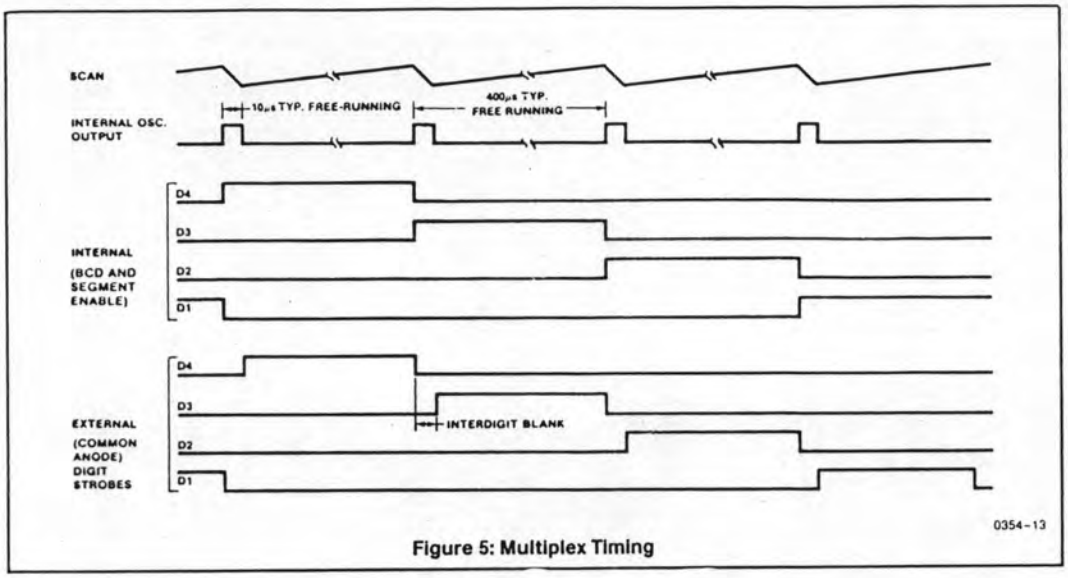
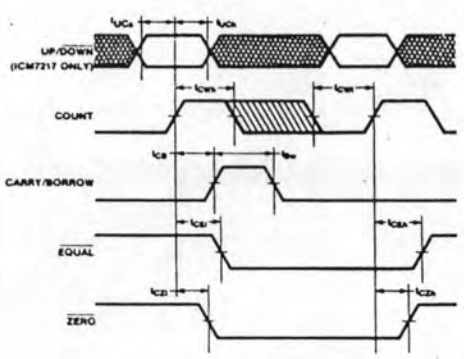


Figure 5: Multiplex Timing



Symbol	Description	Min	Typ	Max	Unit
t_{UCs}	UP/$\overline{DOWN}$ setup time (min)		300		
t_{UCh}	UP/$\overline{DOWN}$ hold time (min)		0		
t_{CUh}	COUNT pulse high (min)		100	250	ns
t_{CUl}	COUNT pulse low (min)		100	250	
t_{CB}	COUNT to CARRY/BORROW delay		750		
t_{Bw}	CARRY/BORROW pulse width		100		
t_{CEl}	COUNT to $\overline{EQUAL}$ delay		500		
t_{CZl}	COUNT to $\overline{ZERO}$ delay		300		

Figure 6: ICM7217/27 COUNT and Output Timing

Multiplex SCAN Oscillator

The on-board multiplex scan oscillator has a nominal free-running frequency of 2.5kHz. This may be reduced by the addition of a single capacitor between the SCAN pin and the positive supply (ICM7217 only). Capacitor values and corresponding nominal oscillator frequencies, digit repetition rates, and loading times are shown in Table 1 below.

The internal oscillator output has a duty cycle of approximately 25:1, providing a short pulse occurring at the oscillator frequency. This pulse clocks the four-state counter which provides the four multiplex phases. The short pulse width is used to delay the digit driver outputs, thereby providing inter-digit blanking which prevents ghosting. The digits are scanned from MSD (D4) to LSD (D1). See Figure 4 for the display digit multiplex timing.

Table 1: ICM7217 Multiplexed Rate Control

Scan Capacitor	Nominal Oscillator Frequency	Digit Repetition Rate	Scan Cycle Time (4 digits)
None	2.5kHz	625Hz	1.6ms
20pF	1.25kHz	300Hz	3.2ms
90pF	600Hz	150Hz	8ms

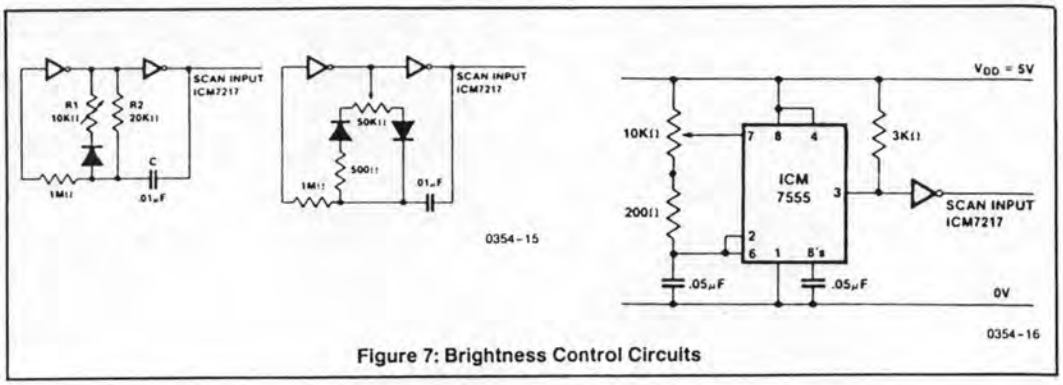


Figure 7: Brightness Control Circuits

During **load counter** and **load register** operations, the multiplex oscillator is disconnected from the SCAN input and is allowed to free-run. In all other conditions, the oscillator may be directly overdriven to about 20kHz, however the internal oscillator signal will be of the same duty cycle and phase as the overdriving signal, and the digits are blanked during the time the external signal is at a positive level. To insure proper leading zero blanking, the interdigit blanking time should not be less than about 2μs. Overdriving the oscillator at less than 200Hz may cause display flickering.

The display brightness may be altered by varying the duty cycle. Figure 7 shows several variable-duty-cycle oscillators suitable for brightness control at the ICM7217 SCAN input. The inverters should be CMOS CD4000 series and the diodes may be any inexpensive device such as IN914.

Counting Control

As shown in Figure 6, the counter is incremented by the rising edge of the COUNT INPUT signal when UP/$\overline{\text{DOWN}}$ is high. It is decremented when UP/$\overline{\text{DOWN}}$ is low. A Schmitt trigger on the COUNT INPUT provides hysteresis to prevent double triggering on slow rising edges and permits operation in noisy environments. The COUNT INPUT is inhibited during reset and **load counter** operations.

The $\overline{\text{STORE}}$ pin controls the internal latches and consequently the signals appearing at the 7-segment and BCD outputs. Bringing the $\overline{\text{STORE}}$ pin low transfers the contents of the counter into the latches.

The counter is asynchronously reset to 0000 by bringing the $\overline{\text{RESET}}$ pin low. The circuit performs the reset operation by forcing the BCD input lines to zero, and "presetting" all four decades of counter in parallel. This affects register loading; if LOAD REGISTER is activated when the $\overline{\text{RESET}}$ input is low, the register will also be set to zero. The $\overline{\text{STORE}}$, $\overline{\text{RESET}}$ and UP/$\overline{\text{DOWN}}$ pins are provided with pull-up resistors of approximately 75kΩ.

BCD I/O Pins

The BCD I/O port provides a means of transferring data to and from the device. The ICM7217 versions can multiplex data into the counter or register via thumbwheel switches, depending on inputs to the LOAD COUNTER or LOAD REGISTER pins; (see below). When functioning as outputs, the BCD I/O pins will drive one standard TTL load. Common anode versions have internal pull down resistors and common cathode versions have internal pull up resistors on the four BCD I/O lines when used as inputs.

LOADing the COUNTER and REGISTER

The BCD I/O pins, the LOAD COUNTER (LC), and LOAD REGISTER (LR) pins combine to provide presetting and compare functions. LC and LR are three-level inputs, being self-biased at approximately $\frac{1}{2}V_{DD}$ for normal operation. With both LC and LR open, the BCD I/O pins provide a multiplexed BCD output of the latch contents, scanned from MSD to LSD by the display multiplex.

When either the LOAD COUNTER (Pin 12) or LOAD REGISTER (Pin 11) is taken high, the drivers are turned off and the BCD pins become high-impedance inputs. When LC is connected to V_{DD}, the count input is inhibited and the levels at the BCD pins are multiplexed into the counter. When LR is connected to V_{DD}, the levels at the BCD pins are multiplexed into the register without disturbing the counter. When both are connected to V_{DD}, the count is inhibited and both register and counter will be loaded.

The LOAD COUNTER and LOAD REGISTER inputs are edge-triggered, and pulsing them high for 500ns at room temperature will initiate a full sequence of data entry cycle operations (see Figure 7). When the circuit recognizes that either or both of the LC or LR pins input is high, the multiplex oscillator and counter are reset (to D4). The internal oscillator is then disconnected from the SCAN pin and the

preset circuitry is enabled. The oscillator starts and runs with a frequency determined by its internal capacitor, (which may vary from chip to chip). When the chip finishes a full 4 digit multiplex cycle (loading each digit from D4 to D3 to D2 to D1 in turn), it again samples the LOAD REGISTER and LOAD COUNTER inputs. If either or both is still high, it repeats the load cycle, if both are floating or low, the oscillator is reconnected to the SCAN pin and the chip returns to normal operation. Total load time is digit "on" time multiplied by 4. If the Digit outputs are used to strobe the BCD data into the BCD I/O inputs, the input will be automatically synchronized to the appropriate digit (Figure 8). Input data must be valid at the trailing edge of the digit output.

When LR is connected to GROUND, the oscillator is inhibited, the BCD I/O pins go to the high impedance state, and the segment and digit drivers are turned off. This allows the display to be used for other purposes and minimizes power consumption. In this display off condition, the circuit will continue to count, and the CARRY/BORROW, $\overline{\text{EQUAL}}$, $\overline{\text{ZERO}}$, UP/$\overline{\text{DOWN}}$, $\overline{\text{RESET}}$ and $\overline{\text{STORE}}$ functions operate as normal. When LC is connected to ground, the BCD I/O pins are forced to the high impedance state without disturbing the counter or register. See "Control Input Definitions" (Table 2) for a list of the pins that function as three-state self-biased inputs and their respective operations.

Note that the ICM7217 and 7217B have been designed to drive common anode displays. The BCD inputs are high true, as are the BCD outputs.

The ICM7217A and the 7217C are used to drive common cathode displays, and the BCD inputs are low true. BCD outputs are high true.

Notes on Thumbwheel Switches & Multiplexing

The thumbwheel switches used with these circuits (both common anode and common cathode) are TRUE BCD coded; i.e. all switches open corresponds to 0000. Since the thumbwheel switches are connected in parallel, diodes must be provided to prevent crosstalk between digits. See Figure 8. In order to maintain reasonable noise margins, these diodes should be specified with low forward voltage drops (IN914). Similarly, if the BCD outputs are to be used, resistors should be inserted in the Digit lines to avoid loading problems.

Output and Input Restrictions

The CARRY/BORROW output is not valid during load counter and reset operations.

The $\overline{\text{EQUAL}}$ output is not valid during load counter or load register operations.

The $\overline{\text{ZERO}}$ output is not valid during a load counter operation.

The $\overline{\text{RESET}}$ input may be susceptible to noise if its input rise time (coming out of reset) is greater than about 500μs. This will present no problems when this input is driven by active devices (i.e., TTL or CMOS logic) but in hardwired systems adding virtually any capacitance to the $\overline{\text{RESET}}$ input can cause trouble. A simple circuit which provides a reliable power-up reset and a fast rise time on the $\overline{\text{RESET}}$ input is shown below.

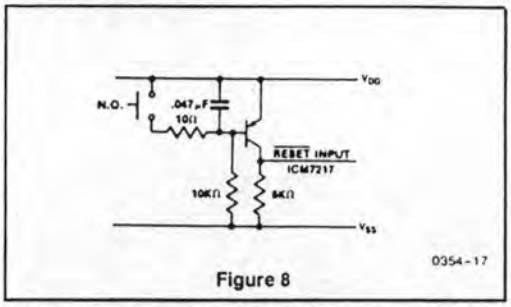


Figure 8

When using the circuit as a programmable divider (÷ by n with equal outputs) a short time delay (about 1μs) is needed from the $\overline{\text{EQUAL}}$ output to the $\overline{\text{RESET}}$ input to establish a pulse of adequate duration. (See Figure 9)

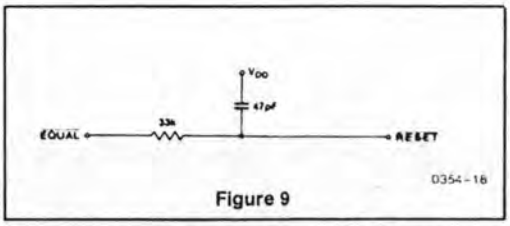


Figure 9

When the circuit is configured to reload the counter or register with a new value from the BCD lines (upon reaching $\overline{\text{EQUAL}}$), loading time will be digit "on" time multiplied by four. If this load time is longer than one period of the input count, a count can be lost. Since the circuit will retain data in the register, the register need only be updated when a new value is to be entered. $\overline{\text{RESET}}$ will not clear the register.

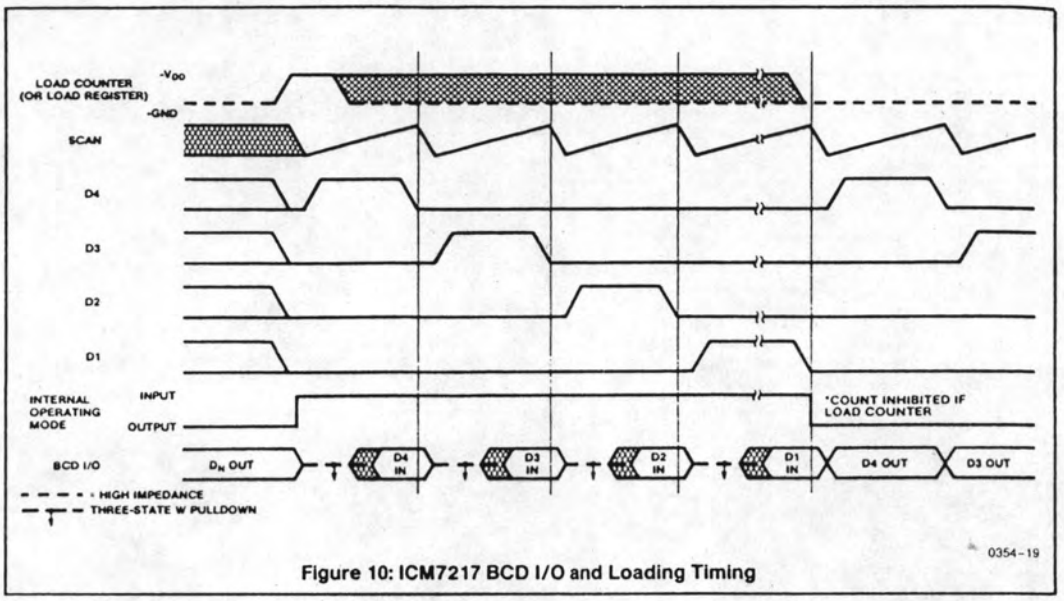
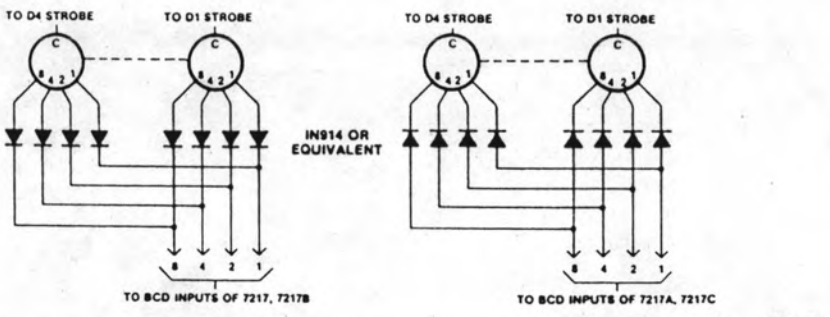


Figure 10: ICM7217 BCD I/O and Loading Timing



Note: If the BCD pins are to be used for outputs a 10kΩ resistor should be placed in series with each digit line to avoid loading problems through the switches.

Figure 11: Thumbwheel Switch/Diode Connections

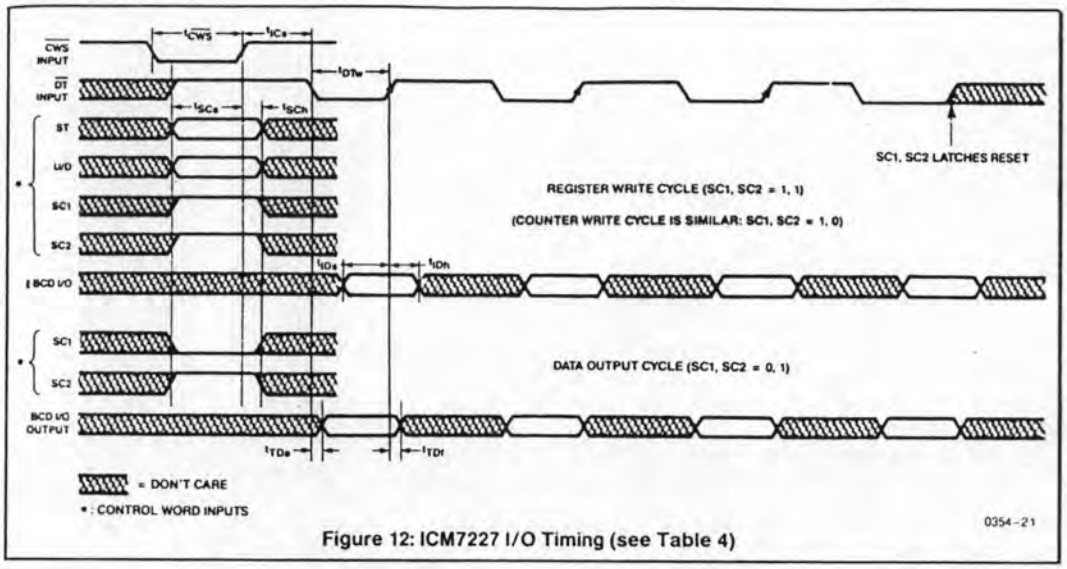


Figure 12: ICM7227 I/O Timing (see Table 4)

CONTROL OF ICM7227 VERSIONS

The ICM7227 series has been designed to permit microprocessor control of the inputs. BCD inputs and outputs are active high.

In these versions, the STORE, UP/$\overline{\text{DOWN}}$, SC1 and SC2 (Select Code bits 1 and 2) pins form a four-bit control word input. A negative-going pulse on the $\overline{\text{CWS}}$ (Control Word Strobe) pin writes the data on these pins into four internal control latches, and resets the multiplex counter in preparation for sequencing a data transfer operation. The select code 00 is reserved for changing the state of the Store and/or Up/$\overline{\text{Down}}$ latches without initiating a data transfer. Writing a one into the Store latch sets the latch and causes the data in the counter to be transferred into the output latches, while writing a zero resets the latches causing them to retain data and not be updated. Similarly, writing a one into the Up/$\overline{\text{Down}}$ latch causes the counter to count up and writing a zero causes the counter to count down. The state of the Store and Up/$\overline{\text{Down}}$ latches may also be changed with a non-zero select code.

Writing a nonzero select code initiates a **data transfer** operation. Writing select code of 01 (SC1, SC2) indicates that the data in the output latches will be active and enables the BCD I/O port to output the data. Writing a select code of 11 indicates that the register will be preset, and a 10 indicates that the counter will be preset.

When a nonzero select code is read, the clock of the four-state multiplex counter is switched to the $\overline{\text{DATA TRANSFER}}$ pin. Negative-going pulses at this pin then sequence a digit-by-digit data transfer, either outputting data or presetting the counter or register as determined by the select code. The output drivers of the BCD I/O port will be enabled only while $\overline{\text{DT}}$ is low during a data transfer initiated with a 01 select code.

The sequence of digits will be D4-D3-D2-D1, i.e. when outputting, the data from D4 will be valid during the first $\overline{\text{DT}}$ pulse, then D3 will be valid during the second pulse, etc. When presetting, the data for D4 must be valid at the positive-going transition (trailing edge) of the first $\overline{\text{DT}}$ pulse, the data for D3 must be valid during the second $\overline{\text{DT}}$ pulse, etc.

At the end of a **data transfer** operation, on the positive going transition of the fourth $\overline{\text{DT}}$ pulse, the SC1 and SC2 control latches will automatically reset, terminating the data transfer and reconnecting the multiplex counter clock to the oscillator. In the ICM7227 versions, the multiplex oscillator is always free-running, except during a **data transfer** operation when it is disabled.

Figure 12 shows the timing of data transfers initiated with a 11 select code (writing into the register) and a 01 select code (reading out of the output latches). Typical times during which data must be valid at the control word and BCD I/O ports are indicated in Table 4.

Table 4: ICM7227 I/O Timing Requirements

Symbol	Description	Min	Typ	Max	Units
$t_{\overline{CWS}}$	Control Word Strobe Width (min)		275		ns
t_{ICs}	Internal Control Set-up (min)		2.5	3	µs
$t_{\overline{DT}w}$	DATA TRANSFER pulse width (min)		300		ns
t_{SCs}	Control to Strobe setup (min)		300		ns
t_{SCh}	Control to Strobe hold (min)		300		ns
t_{IDs}	Input Data setup (min)		300		ns
t_{IDh}	Input Data Hold (min)		300		ns
t_{TDacc}	Output Data access		300		ns
t_{TDf}	Output Transfer to Data float		300		ns

ICM7217/ICM7227

INTERSIL

APPLICATIONS

FIXED DECIMAL POINT

In the common anode versions, a fixed decimal point may be activated by connecting the D.P. segment lead from the appropriate digit (with separate digit displays) through a 39Ω series resistor to Ground. With common cathode devices, the D.P. segment lead should be connected through a 75Ω series resistor to V_{DD}.

To force the device to display leading zeroes after a fixed decimal point, use a bipolar transistor and base resistor in a configuration like that shown below with the resistor connected to the digit output driving the D.P. for left hand D.P. displays, and to the next least significant digit output for right hand D.P. display. See Performance Characteristics for a similarly operating multi-digit connection.

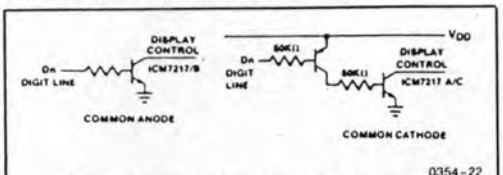


Figure 13: Forcing Leading Zero Display

DRIVING LARGER DISPLAYS

For displays requiring more current than the ICM7217/7227 can provide, the circuits of Figure 14 can be used.

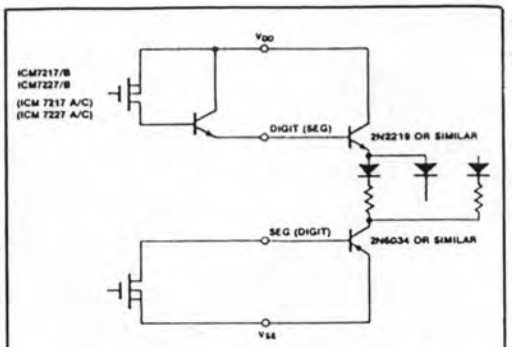


Figure 14: Driving High Current Displays

LCD DISPLAY INTERFACE

The low-power operation of the ICM7217 makes an LCD interface desirable. The Intersil ICM7211 4 digit BCD to LCD display driver easily interfaces to the ICM7217 as shown in Figure 15. Total system power consumption is less than 5mW. System timing margins can be improved by using capacitance to ground to slow down the BCD lines. A similar circuit can be used to drive Vacuum Fluorescent displays, with the ICM7235.

The 10 – 20kΩ resistors on the switch BCD lines serve to isolate the switches during BCD output.

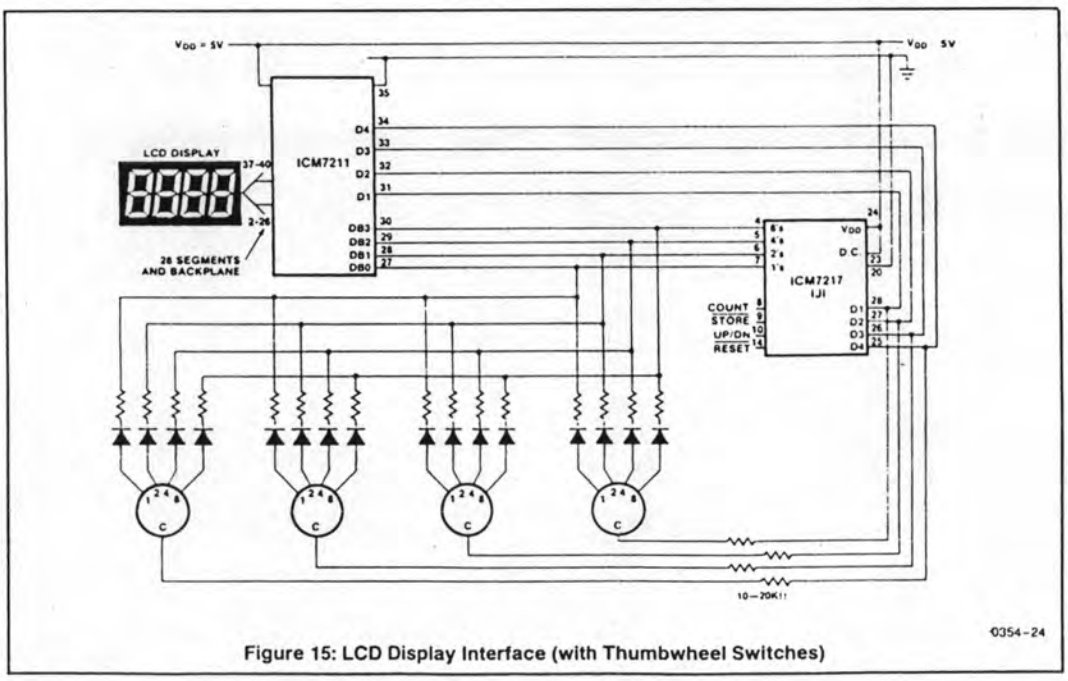


Figure 15: LCD Display Interface (with Thumbwheel Switches)

UNIT COUNTER WITH BCD OUTPUT

The simplest application of the ICM7217 is a 4 digit unit counter (Figure 16). All that is required is an ICM7217, a power supply and a 4 digit display. Add a momentary switch for reset, an SPDT center-off switch to blank the display or view leading zeroes, and one more SPDT switch for up/down control. Using an ICM7217A with a common-cathode calculator-type display results in the least expensive digital counter/display system available.

INEXPENSIVE FREQUENCY COUNTER/ TACHOMETER

This circuit uses the low power ICM7555 (CMOS 555) to generate the gating, $\overline{\text{STORE}}$ and $\overline{\text{RESET}}$ signals as shown in Figure 17. To provide the gating signal, the timer is configured as an astable multivibrator, using R_A, R_B and C to provide an output that is positive for approximately one second and negative for approximately 300 – 500μs. The positive waveform time is given by $t_{wp} = 0.693\ (R_A + R_B)C$ while the negative waveform is given by $t_{wn} = 0.693\ R_BC$. The system is calibrated by using a 5MΩ potentiometer for R_A as a "coarse" control and a 1kΩ potentiometer for R_B as a "fine" control. CD40106B's are used as a monostable multivibrator and reset time delay.

TAPE RECORDER POSITION INDICATOR/CONTROLLER

The circuit in Figure 18 shows an application which uses the up/down counting feature of the ICM7217 to keep track of tape position. This circuit is representative of the many applications of up/down counting in monitoring dimensional position. For example, an ICM7227 as a peripheral to a processor can monitor the position of a lathe bed or digitizing head, transfer the data to the processor, drive interrupts to the processor using the $\overline{\text{EQUAL}}$ or $\overline{\text{ZERO}}$ outputs, and serve as a numerical display for the processor.

In the tape recorder application, the LOAD REGISTER, $\overline{\text{EQUAL}}$ and $\overline{\text{ZERO}}$ outputs are used to control the recorder. To make the recorder stop at a particular point on the tape, the register can be set with the stop point and the $\overline{\text{EQUAL}}$ output used to stop the recorder either on fast forward, play or rewind.

To make the recorder stop before the tape comes free of the reel on rewind, a leader should be used. Resetting the counter at the starting point of the tape, a few feet from the end of the leader, allows the $\overline{\text{ZERO}}$ output to be used to stop the recorder on rewind, leaving the leader on the reel.

The 1MΩ resistor and .0047μF capacitor on the COUNT INPUT provide a time constant of about 5ms to debounce the reel switch. The Schmitt trigger on the COUNT INPUT of the ICM7217 squares up the signal before applying it to the counter. This technique may be used to debounce switch-closure inputs in other applications.

PRECISION ELAPSED TIME/ COUNTDOWN TIMER

The circuit in Figure 19 uses an ICM7213 precision one minute/one second timebase generator using a 4.1943MHz crystal for generating pulses counted by an ICM7217B. The thumbwheel switches allow a starting time to be entered into the counter for a preset-countdown type timer, and allow the register to be set for compare functions. For instance, to make a 24-hour clock with BCD output the register can be preset with 2400 and the $\overline{\text{EQUAL}}$ output used to reset the counter. Note the 10k resistor connected between the LOAD COUNTER terminal and Ground. This resistor pulls the LOAD COUNTER input low when not loading, thereby inhibiting the BCD output drivers. This resistor should be eliminated and SW4 replaced with an SPDT center-off switch if the BCD outputs are to be used.

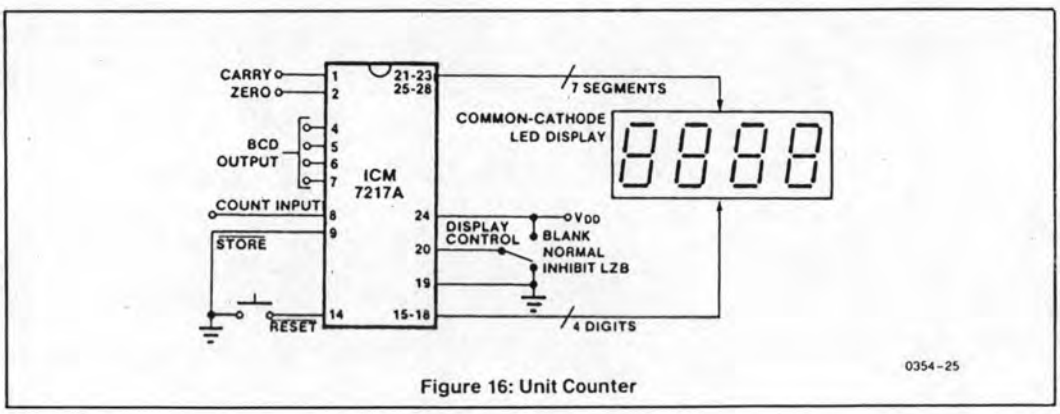


Figure 16: Unit Counter

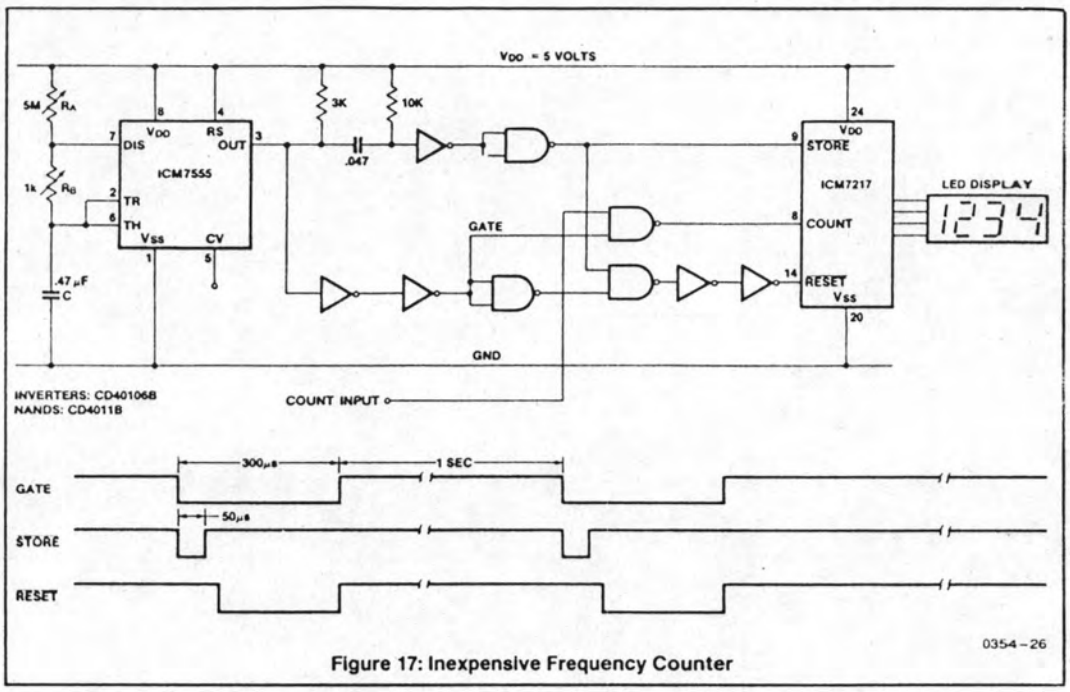


Figure 17: Inexpensive Frequency Counter

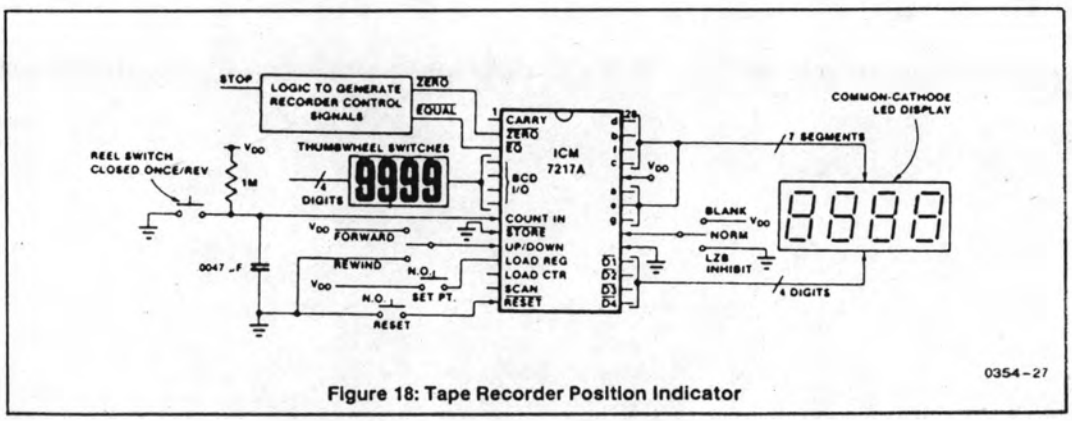
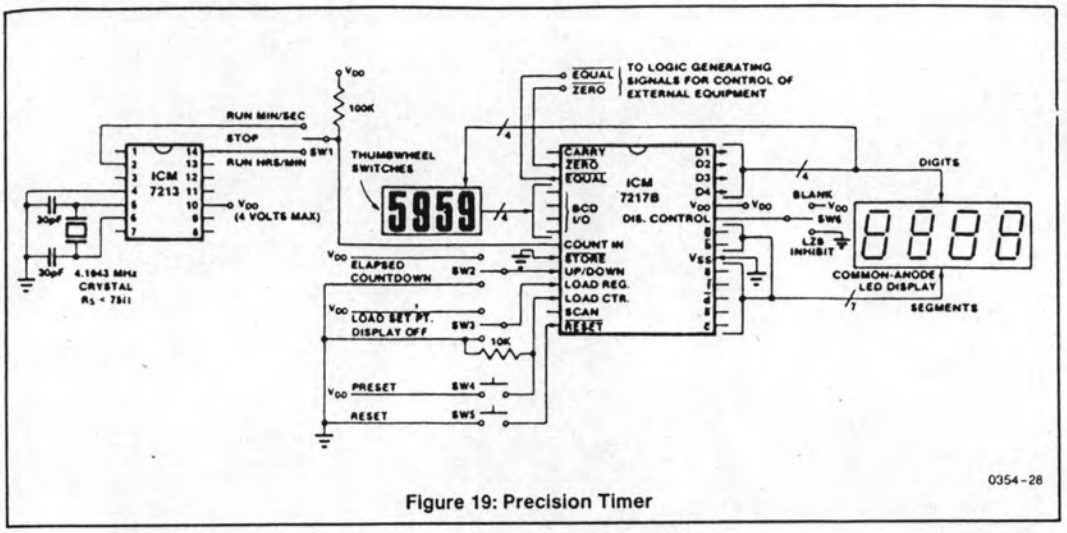
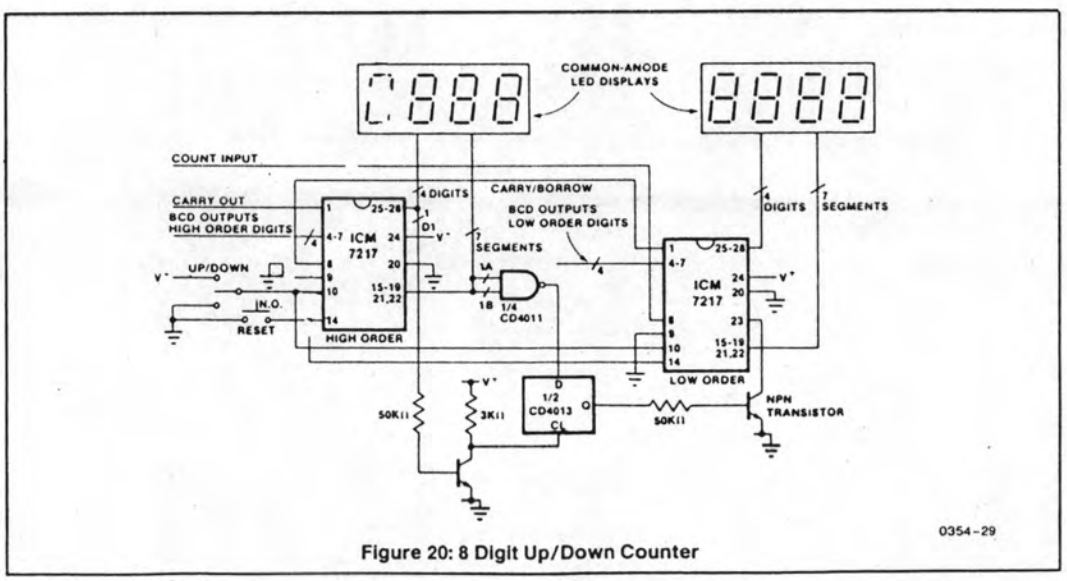


Figure 18: Tape Recorder Position Indicator



0354-28

Figure 19: Precision Timer



0354-29

Figure 20: 8 Digit Up/Down Counter

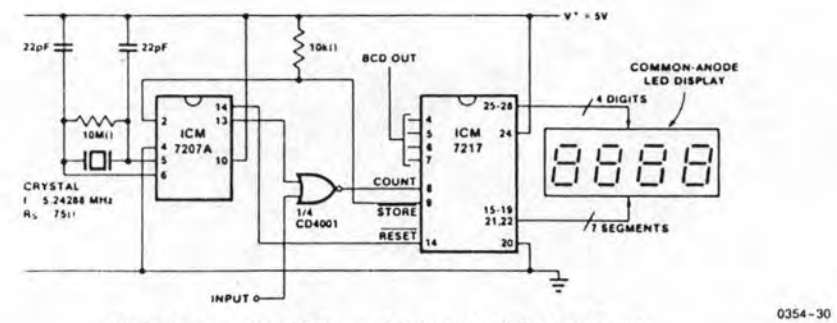


Figure 21: Precision Frequency Counter (MHz Maximum)

This technique may be used on any 3-level input. The 100kΩ pullup resistor on the count input is used to ensure proper logic voltage swing from the ICM7213. For a less expensive (and less accurate) timebase, an ICM7555 timer may be used in a configuration like that shown in Figure 17 to generate a 1Hz reference.

8-DIGIT UP/DOWN COUNTER

This circuit (Figure 20) shows how to cascade counters and retain correct leading zero blanking. The NAND gate detects whether a digit is active since one of the two segments $\overline{a}$ or $\overline{b}$ is active on any unblanked number. The flip flop is clocked by the least significant digit of the high order counter, and if this digit is not blanked, the Q output of the flip flop goes high and turns on the NPN transistor, thereby inhibiting leading zero blanking on the low order counter.

It is possible to use separate thumbwheel switches for presetting, but since the devices load data with the oscillator free-running, the multiplexing of the two devices is difficult to synchronize. This presents no problems with the ICM7227 devices, since the two devices are operated as peripherals to a processor.

PRECISION FREQUENCY COUNTER/ TACHOMETER

The circuit shown in Figure 21 is a simple implementation of a four digit frequency counter, using an ICM7207A to provide the one second gating window and the $\overline{\text{STORE}}$ and $\overline{\text{RESET}}$ signals. In this configuration, the display reads hertz directly. With Pin 11 of the ICM7027A connected to V_{DD}, the gating time will be 0.1 second; this will display tens of hertz as the least significant digit. For shorter gating times, an ICM7207 may be used (with a 6.5536MHz crystal), giving a 0.01 second gating with Pin 11 connected to V_{DD}, and a 0.1 second gating with Pin 11 open.

To implement a four digit tachometer, the ICM7207A with one second gating should be used. To get the display to read directly in RPM, the rotational frequency of the object to be measured must be multiplied by 60. This can be done electronically using a phase-locked loop, or mechanically by using a disc rotating with the object with the appropriate number of holes drilled around its edge to interrupt the light from an LED to a photo-dector. For faster updating, use 0.1 second gating, and multiply the rotational frequency by 600.

For more "intelligent" instrumentation, the ICM7227 interfaced to a microprocessor may be more convenient (see Figure 21). For example, an ICM7207A can be used with two ICM7227's to provide an 8 digit, 2MHz frequency counter. Since the ICM7207A gating output has a 50% duty cycle, there is 1 second for the processor to respond to an interrupt, generated by the negative going edge of this signal while it inhibits the count. The processor can respond to the interrupt using ROM based subroutines, to store the data, reset the counter, and read the data into main memory. To add simultaneous period display, the processor inverts the data and an ICM7218 Universal Display Driver stores and displays it.

AUTO-TARE SYSTEM

This circuit uses the count-up and count-down functions of the ICM7217, controlled via the $\overline{\text{EQUAL}}$ and $\overline{\text{ZERO}}$ outputs, to count in SYNC with an ICL7109 A/D Converter as shown in Figure 22. By $\overline{\text{RESET}}$ing the ICM7217 on a "tare" value conversion, and $\overline{\text{STORE}}$-ing the result of a true value conversion, an automatic tare subtraction occurs in the result.

The ICM7217 stays in step with the ICL7019 by counting up and down between 0 and 4095, for 8192 total counts, the same number as the ICL7109 cycle. See A047 for more details.

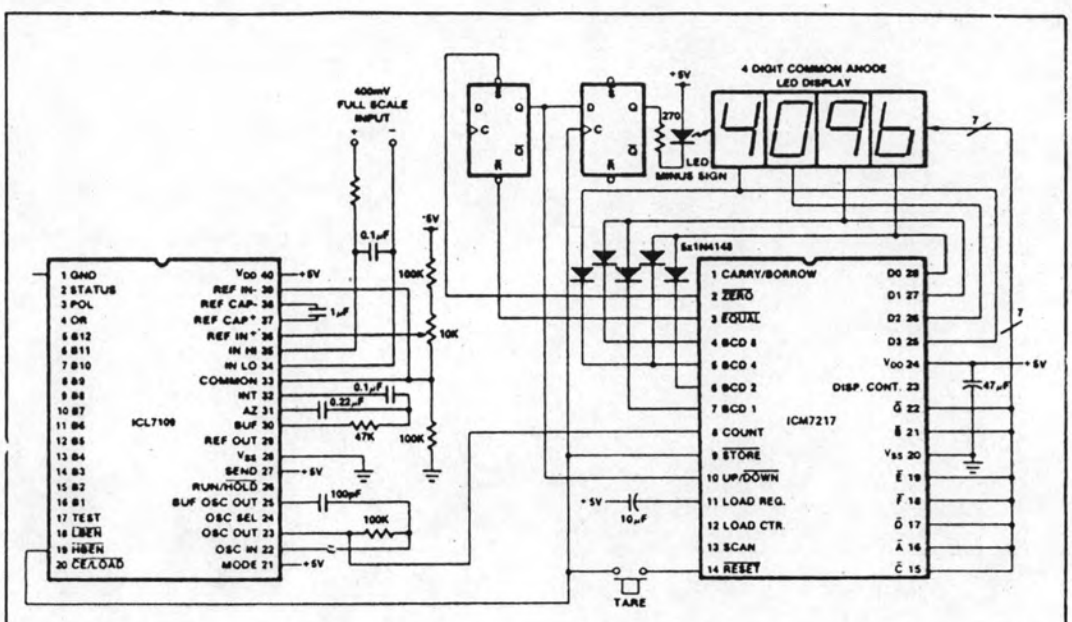


Figure 22: Auto-Tare System for A/D Converter

The LND Cross Reference Guide

Use this Cross Reference Guide to find the LND Geiger-Mueller Radiation Detectors you need.

LND, INC	*ZP/Pro Electron*	*Mullard*	*Philips/Valvo*
7121	ZP1200	MX146	18503
71210	ZP1201		
78016	ZP1210	MX120	18520
78017	ZP1220	MX145	18545
7807	ZP1221		
716	ZP1300	MX163	18529
714	ZP1310	MX151	18509
71412	ZP1311	MX189	ZP1100
7149	ZP1313		
713	ZP1320	MX164	18550
71313	ZP1321		
7139	ZP1324		
72118	ZP1330	MX177	18555
7124	ZP1400	MX147	18504
712	ZP1401		
7224	ZP1410	MX148	18505
72314	ZP1430	MX169	18526
72327	ZP1431	MX149	18506
7242	ZP1441	MX152	18515
72412	ZP1442		
7231	ZP1451	MX166	18536
72315	ZP1452		18516
73118	ZP1460	MX167	18546
72216	ZP1470	MX123	
72233	ZP1481	MX168	
72219	ZP1600	MX159	18507
4561	ZP1610	MX161	18511
740501	ZP1810		
721	ZP1850		
719	ZP1860		

ประวัติผู้เขียน

นายสุขใจ เกียรติศักดิ์วัฒนา เกิดเมื่อวันที่ 25 กรกฎาคม พ.ศ. 2505 ที่อำเภอเมือง จังหวัดนครศรีธรรมราช จบการศึกษาปริญญาตรีจากภาควิชาครุศาสตร์อุตสาหกรรม คณะครุศาสตร์อุตสหกรรมและวิทยาศาสตร์ สถาบันเทคโนโลยีพระจอมเกล้าเจ้าคุณทหารลาดกระบัง ในปี พ.ศ. 2528 จากนั้นเข้ารับการศึกษาต่อที่ภาควิชานิวเคลียร์เทคโนโลยี คณะวิศวกรรมศาสตร์ จุฬาลงกรณ์มหาวิทยาลัย ในปี พ.ศ. 2532 ปัจจุบันรับราชการที่ กองอุปกรณ์อิเล็กทรอนิกส์ สำนักงานพลังงานปรมาณูเพื่อสันติ ในตำแหน่ง วิศวกรนิวเคลียร์