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# APPENDIX A

# NUMERICAL METHODS

This appendix is the collections of the useful numerical methods used to evaluate the many quantities in many part of the thesis. The methods are applied in programs as listed in Appendix B.

**Cubic Spine Interpolations**

There are many method to approximate the values which do not appear in the collected data. The methods are collectively called the *interpolation.* One of the best interpolations is the approximation by the *spine function.* The spine function is the collection of the polynomial curve applying in each interval of the missing data. The curves were connected by the conditions of the continuity. The polynomial curves of the third degree, called the *cubic spine*, are the most popular .

Let consider a set of data $(x_i , y_i)$ , where $i = 0, 1, 2, 3, ..., n.$ Hence, there are n curves of the third degree polynomial which suffice to fill with all interval of the data. The function corresponding to the interval $i$ may be written as

$$y_i(x) = a_i x^3 + b_i x^2 + c_i x + d_i \qquad \text{(A1.1)}$$

There are four unknown variables for each interval and the 4n unknown variables for all intervals. The variables are satisfy the conditions of continuity as follows.

1) The function $y_i(x)$ give the corresponding value as the data at the terminals of the interval $i$, say

$$\left.\begin{aligned} y_i(x_{i-1}) &= y_{i-1} \\ y_i(x_i) &= y_i \end{aligned}\right\} \qquad \text{(A1.2)}$$

2) The first order derivative at a connection of the consecutive functions have to be the same value, i.e.,

$$y_i'(x_i) = y_{i+1}'(x_i) = y_i' \qquad \text{(A1.3)}$$

3) The second order derivative a connections of the consecutive functions have also the same value, i.e.,

$$y_i''(x_i) = y_{i+1}''(x_i) = y_i'' \qquad \text{(A1.4)}$$

From the conditions, they form the 2n + (n-1) + (n-1) (= 4n - 2) equation system. There are two remain equations to suffice for solve these system. These conditions depend on the nature of the measurement, but it is possible to assume that the second derivative of the first and the last points are zero in general case. The conditions form the matrix equation of dimensions in order of 4n. To solve this system directly, it consume a long time to accomplish. Fortunately, it is possible to modify the method. At first, we consider the first and second order derivatives of the (A1.1), we have

$$y_i''(x) = 6a_i x + 2b_i \tag{A1.5}$$

From the second derivative at $x_i$ and $x_{i-1}$, we can solve for $a_i$ and $b_i$, which are

$$a_i = \frac{y_i''(x_i) - y_i''(x_{i-1})}{6(x_i - x_{i-1})}$$

$$b_i = \frac{x_i y_i''(x_{i-1}) - x_{i-1} y_i''(x_i)}{2(x_i - x_{i-1})}.$$

According to (A1.4), $y_i''(x_i)$ can be written as $y_i''$. Substitute $a_i$ and $b_i$ to the (A1.5), we have

$$y_i''(x) = \left\{\frac{y_i''}{x_i - x_{i-1}}\right\}(x - x_{i-1}) - \left\{\frac{y_{i-1}''}{x_i - x_{i-1}}\right\}(x - x_i)$$

$$= \alpha_i (x - x_{i-1}) - \beta_i (x - x_i) \tag{A1.6}$$

where $\alpha_i$ and $\beta_i$ are constants depend on the interval. Integrating the (A1.6), we have

$$y_i(x) = \frac{\alpha_i}{6}(x - x_{i-1})^3 - \frac{\beta_i}{6}(x - x_i)^3 + \delta_i x + \gamma_i \qquad \text{(A1.7)}$$

The $\delta_i$ and $\gamma_i$ can be solved from the first condition. Since the $y_i$ has to pass the points $(x_{i-1}, y_{i-1})$ and $(x_i, y_i)$, we have

$$y_i = \frac{\alpha_i}{6}(x_i - x_{i-1})^3 + \delta_i x_i + \gamma_i$$

$$y_{i-1} = \frac{\beta_i}{6}(x_i - x_{i-1})^3 + \delta_i x_i + \gamma_i$$

From the above equations, we have

$$\delta_i = \frac{y_i - y_{i-1}}{x_i - x_{i-1}} - \frac{y_i''}{6}(x_i - x_{i-1}) + \frac{y_{i-1}''}{6}(x_i - x_{i-1})$$

$$\gamma_i = \frac{x_i y_{i-1} - x_{i-1} y_i}{x_i - x_{i-1}} + \frac{y_i''}{6} x_{i-1}(x_i - x_{i-1}) - \frac{y_{i-1}''}{6} x_i (x_i - x_{i-1})$$

Then substitute $\delta_i$ and $\gamma_i$ to (A1.7), we obtain

$$y_i(x) = \frac{y_i''}{6(x_i - x_{i-1})}(x - x_{i-1})^3 - \frac{y_{i-1}''}{6(x_i - x_{i-1})}(x - x_i)^3 + \left[\frac{-y_{i-1}}{x_i - x_{i-1}} + \frac{y_{i-1}''}{6}(x_i - x_{i-1})\right](x - x_i) + \left[\frac{y_i}{x_i - x_{i-1}} - \frac{y_i''}{6}(x_i - x_{i-1})\right](x - x_{i-1})$$

(A1.8)

In (A1.8), there are two unknown variables which are $y_i''$ and $y_{i-1}''$. Differentiating (A1.8), we have

$$y_i'(x) = \frac{3y_i''}{6(x_i - x_{i-1})}(x - x_{i-1})^2 - \frac{3y_{i-1}''}{6(x_i - x_{i-1})}(x - x_i)^2 + \left[\frac{-y_{i-1}}{x_i - x_{i-1}} + \frac{y_{i-1}''}{6}(x_i - x_{i-1})\right] + \left[\frac{y_i}{x_i - x_{i-1}} - \frac{y_i''}{6}(x_i - x_{i-1})\right]$$

Substitute the above equation by $x_i$ and $x_{i-1}$ , then

$$y_i'(x_i) = \frac{-2y_i''}{6}(x_i - x_{i-1}) + \frac{y_{i-1}''}{6}(x_i - x_{i-1}) + \frac{y_i - y_{i-1}}{x_i - x_{i-1}}$$

$$y_{i+1}'(x_i) = \frac{y_{i+1}''}{6}(x_{i+1} - x_i) - \frac{2y_i''}{6}(x_{i+1} - x_i) + \frac{y_{i+1} - y_i}{x_{i+1} - x_i}$$

According to the second condition $y_i'(x_i) = y_{i+1}'(x_i)$, we equate the above equations and arrange the equation, the result is

$$(x_i - x_{i-1})y''_{i-1} + 2(x_{i+1} - x_{i-1})y''_i + (x_{i+1} - x_i)y''_{i+1} = \frac{6}{x_{i+1} - x_i}(y_{i+1} - y_i) - \frac{6}{x_i - x_{i-1}}(y_i - y_{i-1})$$

(A1.9)

The equation (A1.9) form the equation system. There have n-1 equations since the index $i$'s are in the range [0,n] . If we assume that the second derivatives of data at $x_o$ and $x_n$ equal to zero. Hence, they form the matrix equation as follow.

$$\mathbf{A\ p = q} \qquad \text{(A1.10)}$$

where **A** = square matrix [dimension = (n-1) x (n-1) ]

**p** = column matrix [ dimension (n-1) ]

**q** = column matrix [ dimension (n-1) ]

The elements of the matrix **A**, **p** and **q** are

$$a_{ij} = \begin{cases} x_i - x_{i-1} & ;\ j = i-1 \\ 2(x_{i+1} - x_{i-1}) & ;\ j = i \\ x_{i+1} - x_i & ;\ j = i+1 \\ 0 & ;\ \text{elsewhere} \end{cases}$$

$$p_i = y''_i$$

$$q_i = \frac{6}{x_{i+1} - x_i}(y_{i+1} - y_i) - \frac{6}{x_i - x_{i-1}}(y_i - y_{i-1})$$

The matrix **p** can be solve by many method such as the gaussian elimination. Thus we have all $y_i''$ 's which are the unknown variables in (A1.8) for all interval *i*. By this way, we can interpolate the value in the interval *i* by substitution the corresponding parameter to (A1.8).

**2-Dimension Integration by Mid-Point Method**

The numerical integration is commonly used in many fields of science. The simply mid-point integration is well-known in 1-dimensional case. It is rather rough approximation but it can be simply extended to the 2-dimension case.

Consider the integration *I* is performed on the function *F(x,y)* in the range of $x_o<x<x_o$ and $y_o<y<y_1$ , we have

$$I = \int_{y_o}^{y_1}\int_{x_0}^{x_1} F(x,y)dxdy \qquad \text{(A2.1)}$$

This integration coincide with the volume of solid confined by the xy plane and the surface *F(x,y)* . By the elementary calculus, the integration I can be written as

$$I = \lim_{\Delta y\to 0}\lim_{\Delta x\to 0}\sum_{j=0}^{m}\sum_{i=0}^{n} F(x_i,y_j)\cdot\Delta x\cdot\Delta y \qquad \text{(A2.2)}$$

where $x_i = x_o + i\Delta x$ ; $\Delta x = \dfrac{x_1 - x_o}{n}$

$$y_j = y_o + j\Delta y \quad ; \quad \Delta y = \frac{y_1 - y_o}{m}$$

It can be seen that the exact value can be obtained only when n and m are approached to the infinity or the interval of $x$ and $y$ are divided to the infinitesimal pieces. However, the approximation can be made for the equation. From (A2.2) it suggest that the integration is the summation of the small elements of the whole volume.

Let consider a small volume which confined by the area in xy plane which vertices are $(x_i,y_j)$, $(x_i,y_{j+1})$, $(x_{i+1},y_{j+1})$ and $(x_{i+1},y_j)$ . As the concept of mid-point, the small volume is considered as the 3-dimensional bar of high as the value of the function $F(x,y)$ at the middle point of that area, say

$$F(\frac{x_i + x_{i+1}}{2}, \frac{y_j + y_{j+1}}{2}) = F(x_i + \frac{\Delta x}{2}, y_j + \frac{\Delta y}{2})$$

$$= F(x_o + p_i, y_o + q_j)$$

where $p_i = (i + \frac{1}{2})\Delta x$ and $q_j = (j + \frac{1}{2})\Delta y$. Hence the integration (A2.2) may be written as follow.

$$I = \sum_{j=o}^{m}\sum_{i=o}^{n} F(x_o + p_i, y_o + q_j) \cdot \Delta x \cdot \Delta y \qquad \text{(A2.3)}$$

The value of $p_i$ and $q_j$ can found by iteration, say

$$p_{i+1} = p_i + \Delta x \quad ; \quad p_o = \frac{\Delta x}{2}$$

$$q_{j+1} = q_j + \Delta y \quad ; \quad q_o = \frac{\Delta y}{2}$$

The result is approached to the exact value when the range of x and y are divided smallest. In practice, the value can be accurate in a certain level since the limitation of the resolution of bits in the numerical type in computer.

**Nonlinear regression**

Before the nonlinear regression will be considered, it is useful to understand the classic polynomial regression. Let consider a set of data ($x_i$, $y_i$) where $i$ represent the order of data from 1 to N. If the data is predicted by the polynomial function of degree k, say

$$y(x) = \sum_{n=0}^{k} a_n x^n \qquad \text{(A3.1)}$$

The measured data are not exact the predicted value as (A3.1) but a small deviation may occur. It 's interesting what is the curve of the polynomial which collective deviation from the data is minimum. Let we define the collective *Residual* $V$, which is

$$V = \sum_{i=1}^{N} \left( y_i - y(x_i) \right)^2$$
$$= \sum_{i=1}^{N} y_i^2 - 2\sum_{i=1}^{N} y_i y(x_i) + \sum_{i=1}^{N} y^2(x_i)$$

To minimize the variance, we differentiate the variance with respect to the coefficient $a_m$ where $0 < m < k$. The result is

$$\frac{\partial V}{\partial a_m} = -2\sum_{i=1}^{N} y_i x^m + 2\sum_{n=0}^{k} a_n \left\{ \sum_{i=1}^{N} x^{m+n} \right\}$$

The minimization condition is accomplished when $\frac{\partial V}{\partial a_m} = 0$ , then we have

$$\sum_{n=0}^{k} a_n \left\{ \sum_{i=1}^{N} x^{m+n} \right\} = \sum_{i=1}^{N} y_i x^m \qquad \text{(A3.2)}$$

The above equation form the $k+1$ equation system. It can be represented by the matrix form as follow.

**Ap= q**

where **A** = squre matrix [dimension = $(k+1)$ x $(k+1)$ ]

**p** = column matrix [dimension = $(k+1)$]

**q** = column matrix [dimension = $(k+1)$]

The element of the matrix **A**, **p** and **q** can be written respectively as

$$a_{(m+1)(n+1)} = \sum_{i=1}^{N} x^{m+n}$$

$$p_{m+1} = a_m$$

$$q_{m+1} = \sum_{i=1}^{N} y_i x^m$$

When the all $a_n$'s are solve the curve which is the represented the data can be determined by substitute them to (A3.1).

In the most cases, the predicted function are not necessary to be polynomial function as indicate by (A3.1). However, it may be possible to induce the linear equation in some special cases. Let consider the predicted function as follow.

$$y(x) = \alpha k^{x^2 + \beta x} \tag{A3.3}$$

The above equation represent the exponential function of the quadratic equation. Take *log* to this function we obtain

$$\left.\begin{aligned} \log y &= (\log k)x^2 + (\beta \log k)x + \log \alpha \\ Y &= a_2 x^2 + a_1 x + a_o \end{aligned}\right\} \tag{A3.4}$$

It is obviously seen that the (A3.4) is the quadratic equation for $x$ and $Y$ which is corresponding to the second degree polynomial with coefficient $a_2$, $a_1$ and $a_0$ respectively. The classic polynomial regression can be performed to the variables $Y_i = \log y_i$ rather than the $y_i$ and the yields coefficients $a_n$ where $n = 0..2$ . For this case the unknown parameters for (A3.3) are calculated by substitute $a_n$ to the following equations.

$$\alpha = 10^{a_0} \quad ; \quad k = 10^{a_2} \quad ; \quad \beta = \frac{a_1}{a_2}$$

Then, the represented curve of the data can be found by substitution the unknown value to (A3.3).

# APPENDIX B

# SOFTWARE CONSIDERATIONS

This Appendix is dedicated to complete the contents in software aspects. Since there are too many source codes to show in the thesis, the basic concepts and some essential commands which is the core of programming. The used program can be divided in two categories, which are the controller of the DAM and the routine using to analysis purposes. The first part is how to write the generic codes for interfacing the software to the hardware. The last is brief discussion on the analysis routine. All codes are written in PASCAL language and compiling by the Borland Pascal version 7.0, which have support the programming in both low level assembly routine and the Object Oriented Programming (OOP).

**General Descriptions about Software Interfacing**

The most fundamental and fastest way to communicate with the computer is via machine language. Since inefficiency and cumbersome, the more accessible assembly language is introduced. However, a certain assembly code is the one-by-one representation of machine code which is operated only the simple way such as the data transfer or simple logical arithmetic, so the development of the complex application will be difficult. However, the some critical routines which require the high speed operation or intensive hardware controlled have to be involved.

To facilitate the more complex applications, high level languages are devised. The high level language offer the organized machine codes (or commands) and the abstract structure for development. The powerful programming can be accomplished by the appropriate combination of two level.

In Borland Pascal version 7.0, the assembly routine and direct machine code are available. The assembly routine can be identified by the `assembler` directive behind the routine declaration, such as

```
Procedure Assmbly_Routine : assembler ;
```

The parameters for such procedure may be passing via the global variable or stacks. In contrast to function which the parameters is passing by CPU registers. The detail information can be seen in Demas, 1990.

To communicate with port, the Borland Pascal provide another way instead of directly program in assembly code. The virtual array variables `Port` and `PortW` are represented the ports of 8-bit and 16-bit devices, respectively. By this way the data transfer can be accomplished in the input and output mode as following examples :

```
x := portW [PortNum] ;
PortW [PortNum] := x ;
```

The first one is to transfer the 16-bit data from the port specified by `PortNum` to the memory allocated be variable x or vice versa in the second.

The CPU registers are accessible from the record variable of type `registers`. The field of the variable of such type represent the specific register. For example,

```
var regs : registers
regs.ax := $00FF ;
regs.al := $FF   ;
```

The interrupt routine is identified by the directive `interrupt` in the same way of assembly routine and implemented by the command `SetIntVec` which have the syntax as follow :

```
Procedure SetIntVect (IntNum : byte ; Vector : pointer) ;
```

Where the `IntNum` and `Vector` represent the interrupt number and interrupt vector for the specific routine. This command have to declare before the interrupt routine will be used. There have two cautions for the usage of the interrupt routine. One is the old interrupt vector should be kept before the installation of the user-defined routine and restored after the usage to prevent the system crashing. The last is the interrupt routine cannot be accessed directly by routine software call as normal subroutine.

**Subroutine for Numerical Analysis**

The routines are arranged in Pascal units. The most is written as the object and partially functions or procedures. The objects can be considered as engines which operations are depend on a certain type of inputs. At first the engine have to install via constructors of the objects. The set of input data is sent to the engine by the individual way. The result is obtained from some method of the engines. This followings is the name and functions for each units.

EMATH : The extended mathematical functions which is not available in standard Pascal, e.g. the extended trigonometric functions, hyperbolic functions. The conversion between the various numerical formats is also provided.

MTX : The definition of the matrix object containing the fundamental matrix operation such as assign elements, transpose, multiplication and the more advance operation such as solve linear equations.

ASTRON : The definition of data structure representing the position and time notations including routine to interchange between them. Also the functions which is served for astronomical observation is provided and change automatically with the time base of computer.

EGRAPH and GRAPHOBJ:The enhancement of the GRAPH.TPU unit. The graphic object such as initiation of the graphic workspace, the numerous type of button, etc.

CUBIC : The engine for cubic spine interpolation. the set of input data is set via the constructor in the forms of text file or link-list header pointer of the specific type. The result is obtained by call a specific method which is the function of x value.

DFILTER : The engine for digital filter. The current version is support only the low-pass filter with Lanczos' window but another type will be extended in the next version. The input have to be inserted to complete the k index of the filter.

BEAM : The definition of TBEAM Object representing the 3-D normalized beam pattern of an antenna which the measured value for each plane is defined in the construction part of this object. The routines for calculation parameters for this antenna is also provide.

DAM : The control subroutines and the status flag for DAM controlling. Some routine is written in assembly code to obtain the high speed acquisition. The initialization of DAM is also provided in the most flexible and simple way.

RECEIVER : The conversion functions from the output voltage of the radio telescope receiver to the voltage and power at the antenna terminal. The functions are base on the assumption and calibration as described in this thesis.

The routines is distributed to many programs. The following is the descriptions of the importance programs which is written for this thesis.

BEAMANL : The program for analysis the antenna pattern. This program provide the 3-D plot for both linear and dB scale. The parameters of the antenna is calculated and the beam solid angle is estimated by mid-point integration.

FILDEMO : This is the demonstration program to test the digital filter. Graphic illustrations for the input and output signal is also support.

RATCON : The core program to control the acquisition of the radio telescope system. This program provide the GUI's to display the current value of observation. The system can be operate with both free running mode or recording mode. In recording mode, the storage media manager is handle.

RADIOSKY : The analysis program for the final result of the acquired data. The value is presented in the form of million Kelvin of system temperature and displayed graphically. By the aids of OOP, many set of data can be presented simultaneously with a tiny modification. The individual parameter such as the offset and gain can be defined in simple way.

# APPENDIX C

# SCHEMATIC DIAGRAMS

This appendix is the collections of the schematic diagrams of the original hardware which is devised to serve the data acquisition system. The concepts and block diagrams for each equipment is shown in chapter IV. There are three equipment which is constructed ,i.e. AT prototype card, Data Acquisition Module-DAM (indicated by code Hx-7M ) and Signal Conditioner, respectively. Each equipment have many sheets corresponding to the modular design concept. The name of each device and index of the sheet is indicated at the title block at the bottom of each sheet.

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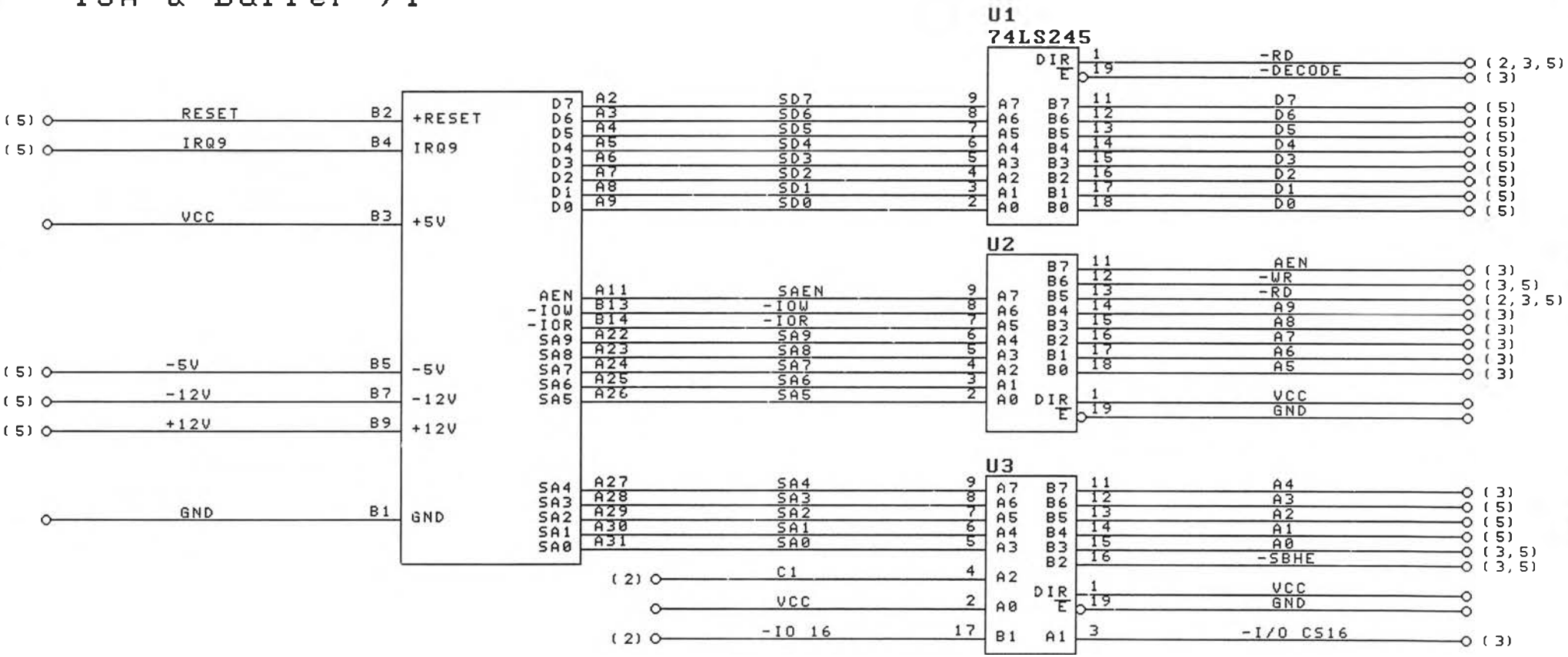
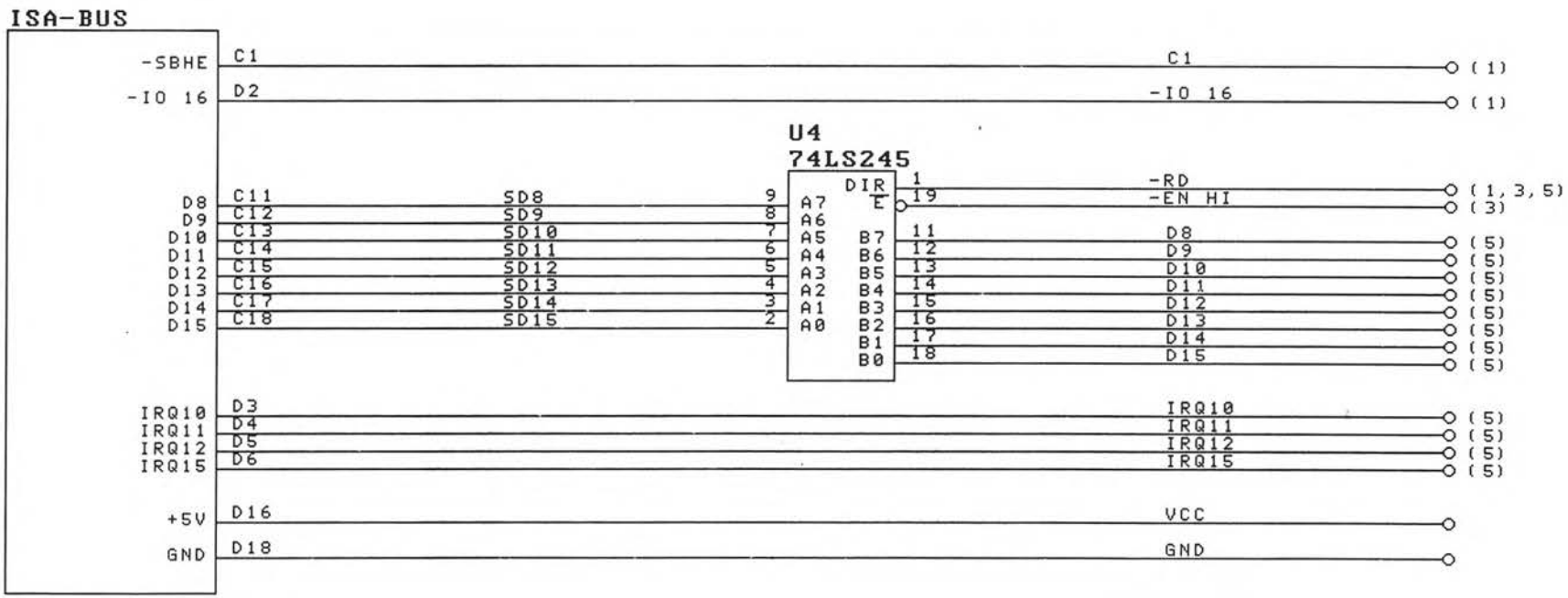
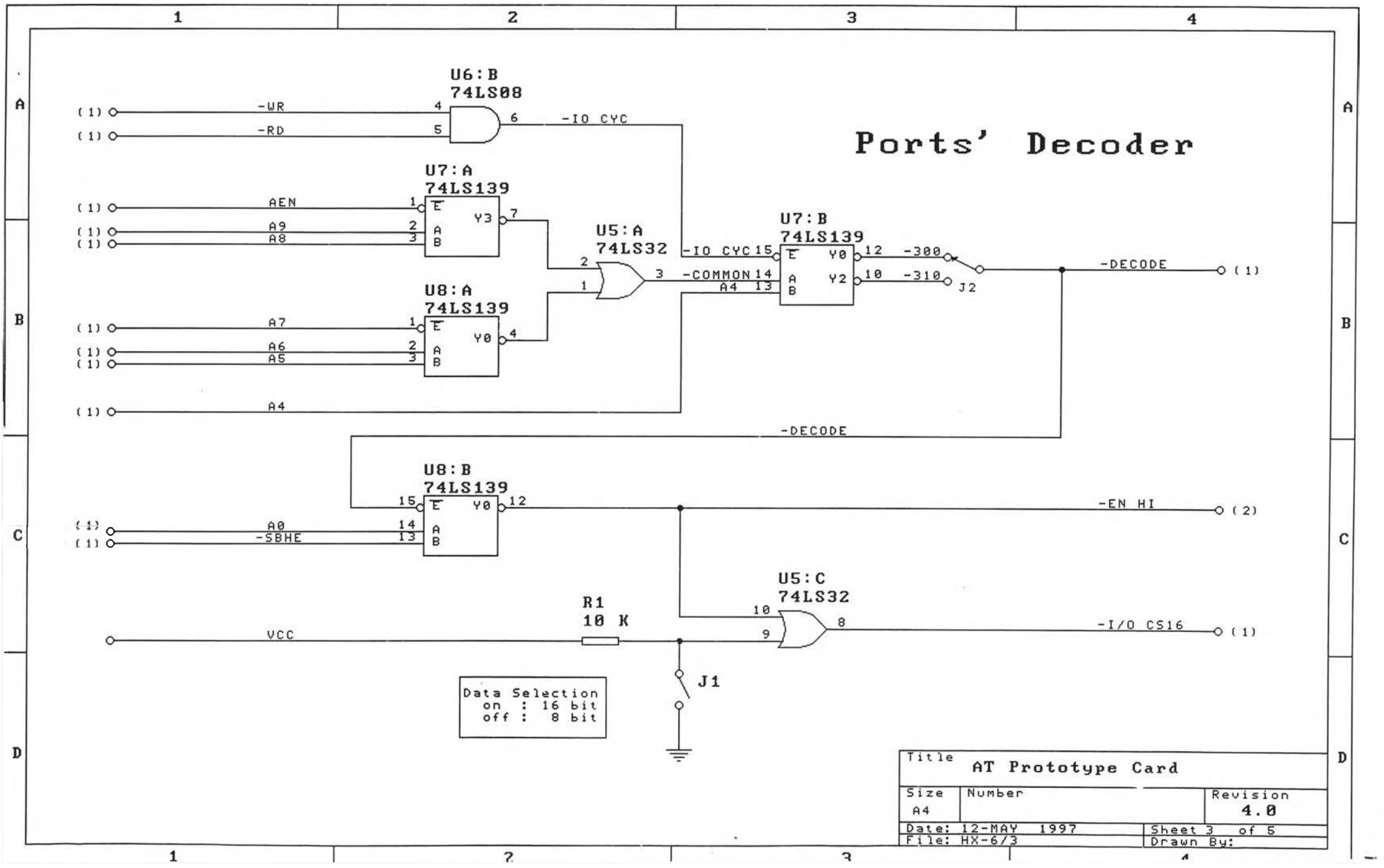



| | | |
|---|---|---|
| Title: AT Prototype Card | | |
| Size: A4 | Number: | Revision: 4.0 |
| Date: 12-MAY 1997 | | Sheet 1 of 5 |
| File: HX-6/1 | | Drawn By: |

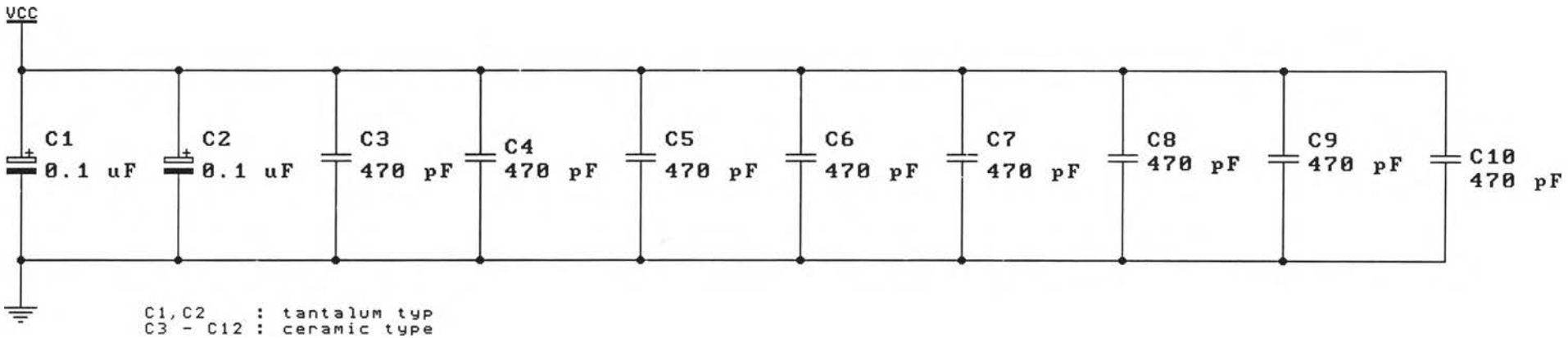
# ISA & Buffer /2




| | | |
|---|---|---|
| Title: AT Prototype Card | | |
| Size: A4 | Number: | Revision: 4.0 |
| Date: 12-MAY 1997 | Sheet 2 of 5 | |
| File: HX-6/2 | Drawn By: | |

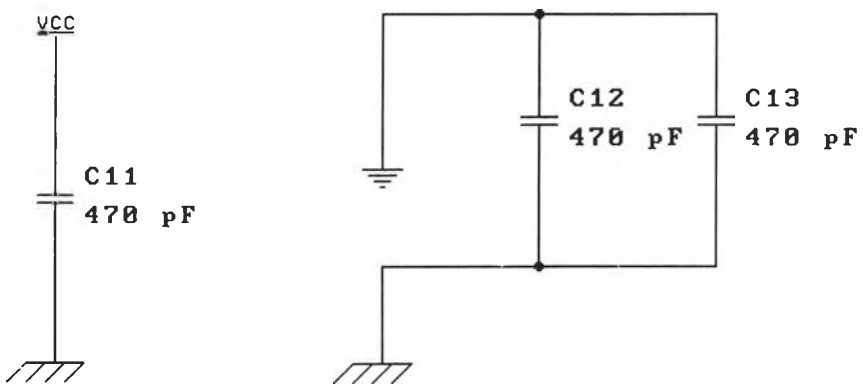

Ports' Decoder
U6:B
74LS08
-WR
-RD
-IO CYC
U7:A
74LS139
AEN
A9
A8
Y3
U5:A
74LS32
-IO CYC
-COMMON
U7:B
74LS139
-300
-310
J2
-DECODE
U8:A
74LS139
A7
A6
A5
Y0
A4
-DECODE
U8:B
74LS139
A0
-SBHE
-EN HI
U5:C
74LS32
R1
10 K
VCC
-I/O CS16
J1
Data Selection
on : 16 bit
off : 8 bit
Title
AT Prototype Card
Size
A4
Number
Revision
4.0
Date: 12-MAY 1997
Sheet 3 of 5
File: HX-6/3
Drawn By:

## Bulk & Decouplers



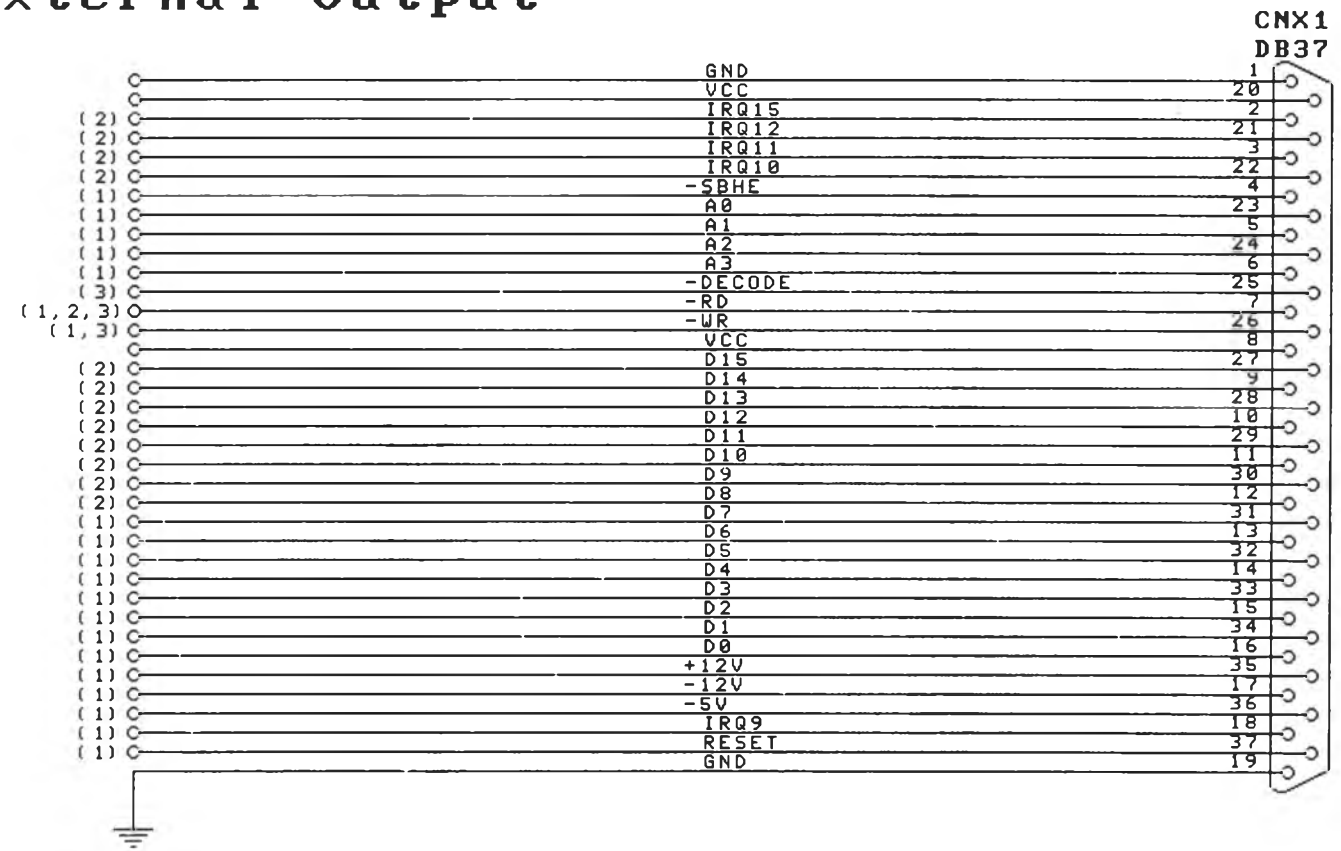

C1, C2 : tantalum typ
C3 - C12 : ceramic type

## Radiate Decoplers



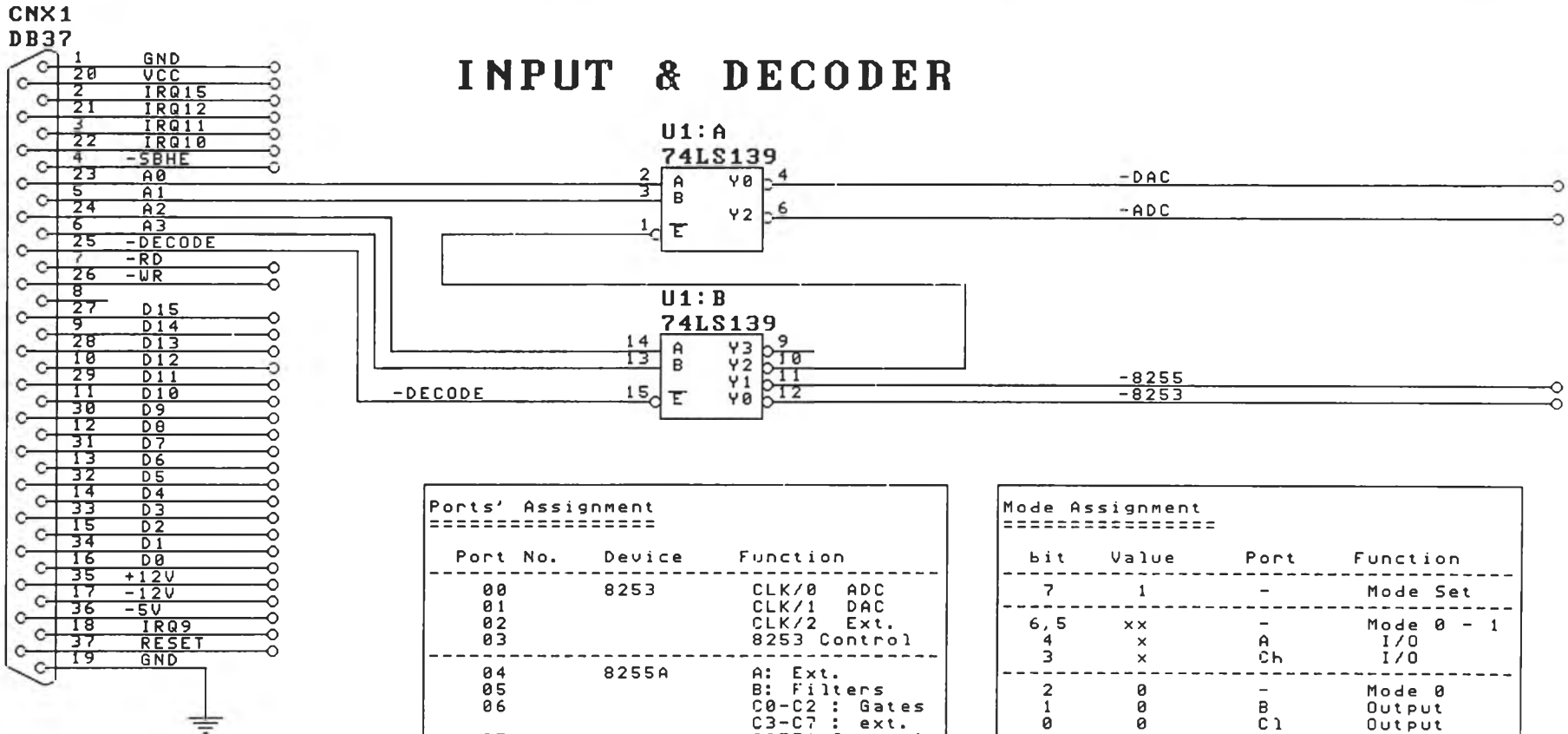

| | | |
|---|---|---|
| Title: AT Prototype Card | | |
| Size: A4 | Number: | Revision: 4.0 |
| Date: 12-MAY 1997 | | Sheet 4 of 5 |
| File: HX-6/4 | | Drawn By: |

# External Output




| | | |
|---|---|---|
| Title: AT Prototype Card | | |
| Size: A4 | Number: | Revision: 4.0 |
| Date: 12-MAY 1997 | | Sheet 5 of 5 |
| File: HX-6/5 | | Drawn By: |

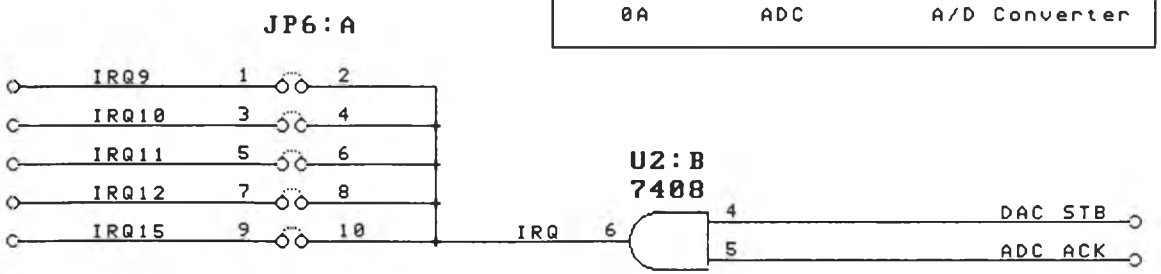
# INPUT & DECODER




| Ports' Assignment | | |
|---|---|---|
| Port No. | Device | Function |
| 00 | 8253 | CLK/0 ADC |
| 01 | | CLK/1 DAC |
| 02 | | CLK/2 Ext. |
| 03 | | 8253 Control |
| 04 | 8255A | A: Ext. |
| 05 | | B: Filters |
| 06 | | C0-C2 : Gates |
| | | C3-C7 : ext. |
| 07 | | 8255A Control |
| 08 | DAC | D/A Converter |
| 0A | ADC | A/D Converter |

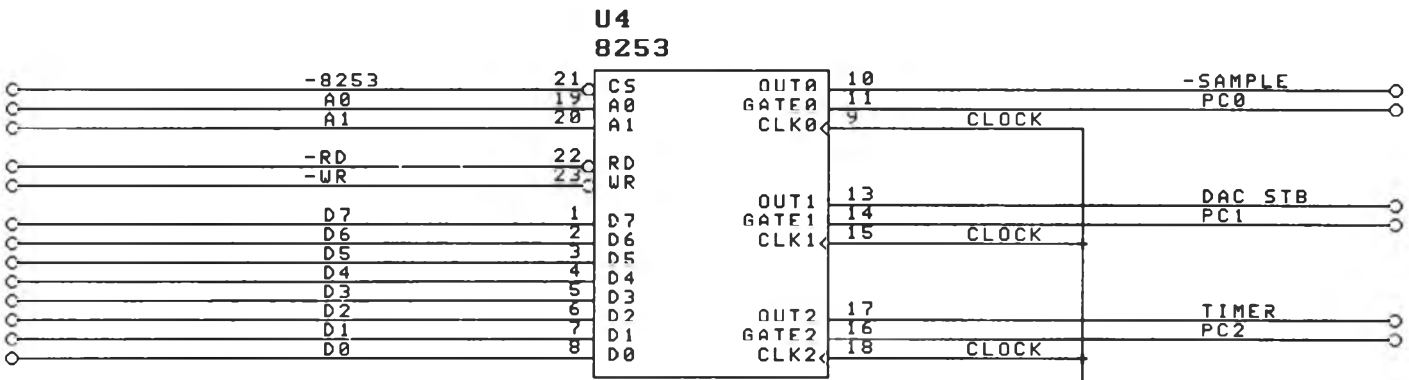
| Mode Assignment | | | |
|---|---|---|---|
| bit | Value | Port | Function |
| 7 | 1 | - | Mode Set |
| 6,5 | xx | - | Mode 0 - 1 |
| 4 | x | A | I/O |
| 3 | x | Ch | I/O |
| 2 | 0 | - | Mode 0 |
| 1 | 0 | B | Output |
| 0 | 0 | Cl | Output |

| Bit | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|
| set/reset | 0 | x | x | x | b3 | b2 | b1 | s/r |

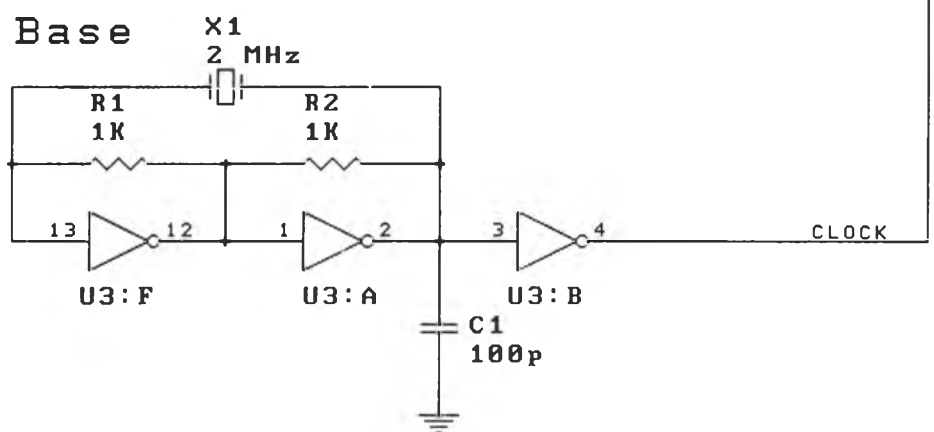



| Title | Hx-7M : Main Board | |
|---|---|---|
| Size A4 | Number | Revision |
| Date: 12-MAY 1997 | | Sheet 1 of 8 |
| File: MAIN/1 | | Drawn By: |

# Programable Timer




## Time Base



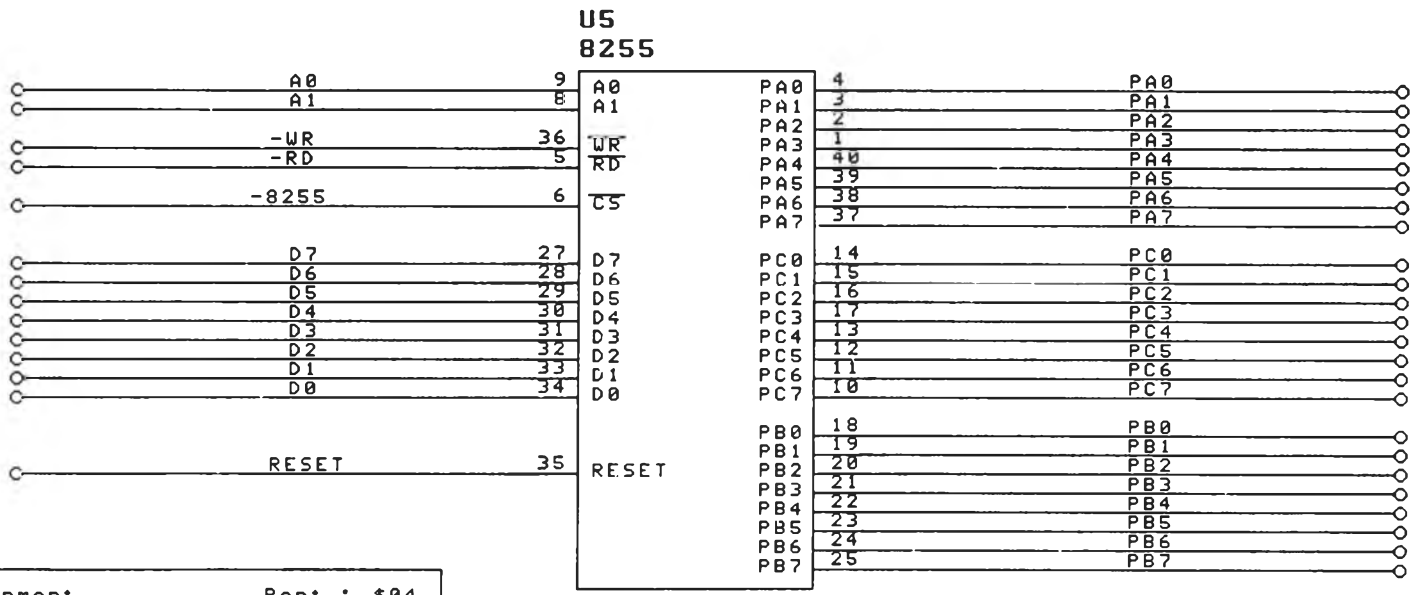

```
Information
===========

Base Port     : $00
Time base     : 0.5 uS/LSB
Counter       : Binary
Mode          : 2 [rate generator]
Control Word  : $B4 for Conter 0,1
Bytes' Order  : LSB -> MSB
```

| Gate | Function | Control Code |
|---|---|---|
| 0 | ADC Run/Stanby | $01 / $00 |
| 1 | DAC Strobe/DC | $03 / $02 |
| 2 | Timer Run/Stanby | $05 / $04 |

| | | |
|---|---|---|
| Title: Hx-7M : Main Board | | |
| Size: A4 | Number | Revision |
| Date: 12-MAY 1997 | | Sheet 2 of 8 |
| File: MAIN/2 | | Drawn By: |

# Digital Port Control



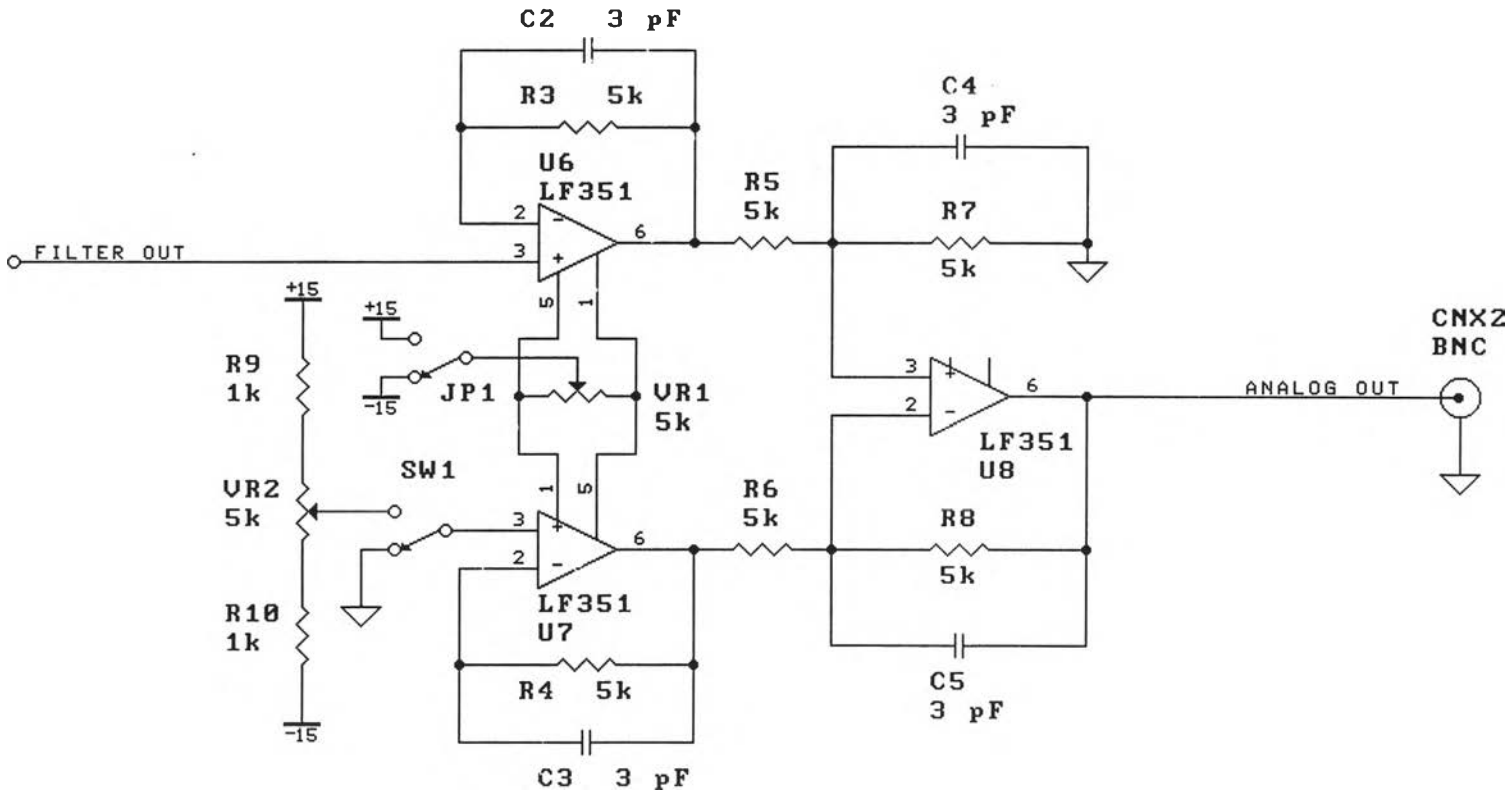

Mode Assignment — Port : $04

| bit | Value | Port | Function |
|---|---|---|---|
| 7 | 1 | - | Mode Set |
| 6,5 | xx | - | Mode 0 - 1 |
| 4 | x | A | I/O |
| 3 | x | Ch | I/O |
| 2 | 0 | - | Mode 0 |
| 1 | 0 | B | Output |
| 0 | 0 | Cl | Output |

| Bit | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|
| set/reset | 0 | x | x | x | b3 | b2 | b1 | s/r |

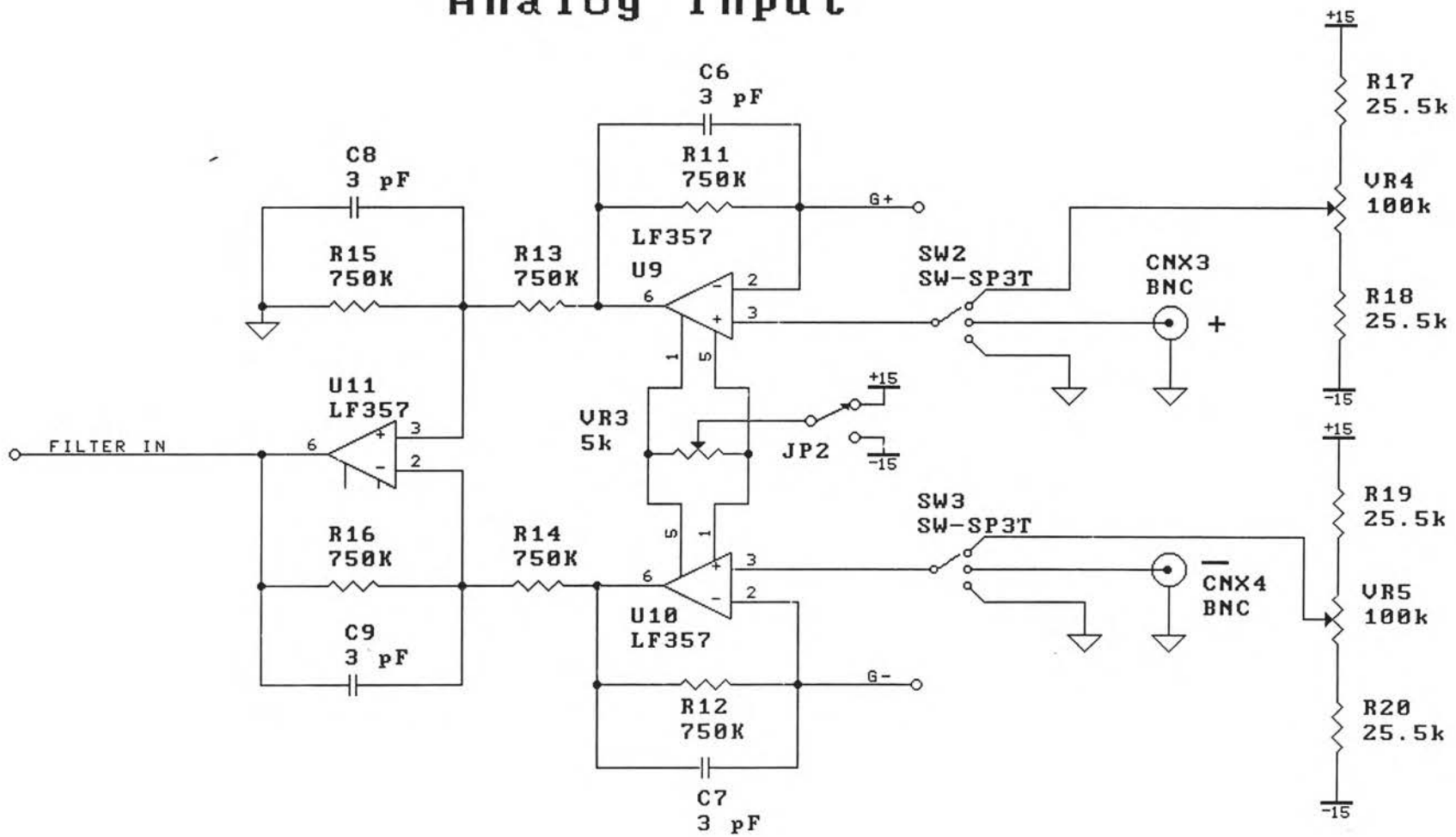
| | | |
|---|---|---|
| Title: Hx-7M : Main Board | | |
| Size: A4 | Number | Revision |
| Date: 12-MAY 1997 | | Sheet 3 of 8 |
| File: MAIN/3 | | Drawn By: |

# Analog Output



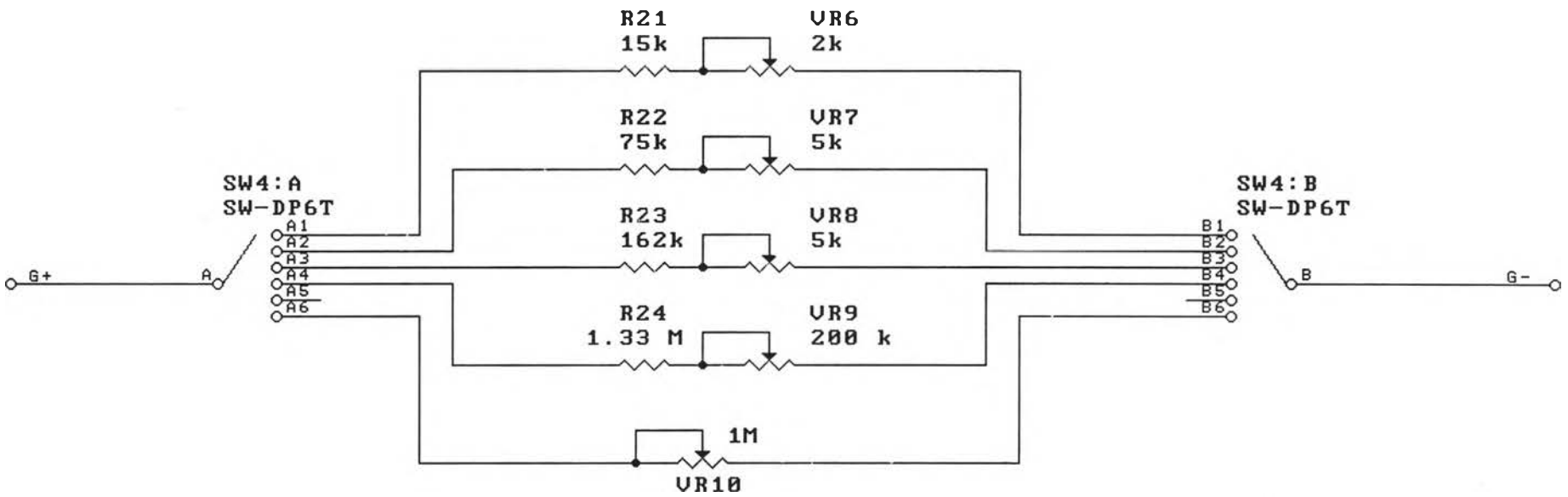

| | | |
|---|---|---|
| Title: Hx-7M : Main Board | | |
| Size: A4 | Number: | Revision: |
| Date: 12-MAY 1997 | | Sheet 4 of 8 |
| File: MAIN/4 | | Drawn By: |

# Analog Input




| | | |
|---|---|---|
| Title | Hx-7M : Main Board | |
| Size A4 | Number | Revision |
| Date: 12-MAY 1997 | | Sheet 5 of 8 |
| File: MAIN/5 | | Drawn By: |

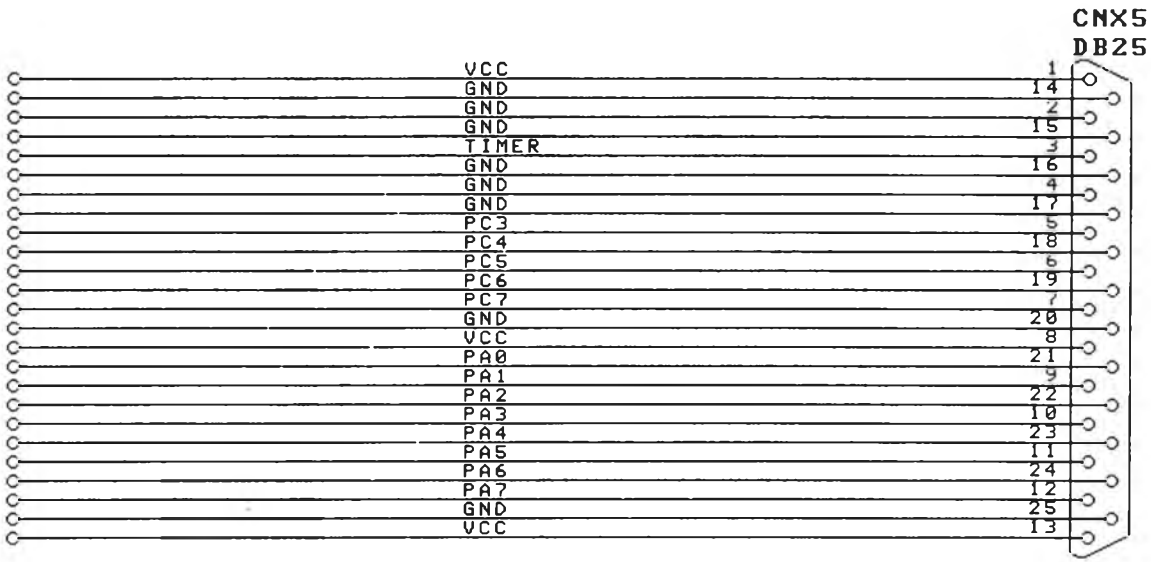
# Gain Selectors




Maximum Range and Gain

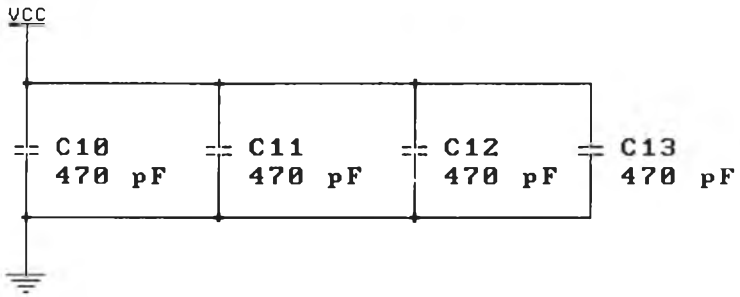
| Pos | Gain | 10Vspan | 20Vspan |
|---|---|---|---|
| 1 | x100 | 100 mV | 200 mV |
| 2 | x20 | 500 mV | 1 V |
| 3 | x10 | 1 V | 2 V |
| 4 | x2 | 5 V | 10 V |
| 5 | x1 | 10 V | 20 V |
| 6 | x2.5 - x10 | Adj. | Adj. |

| | | |
|---|---|---|
| Title: Hx-7M : Main Board | | |
| Size: A4 | Number: | Revision: |
| Date: 12-MAY 1997 | | Sheet 6 of 8 |
| File: MAIN/6 | | Drawn By: |

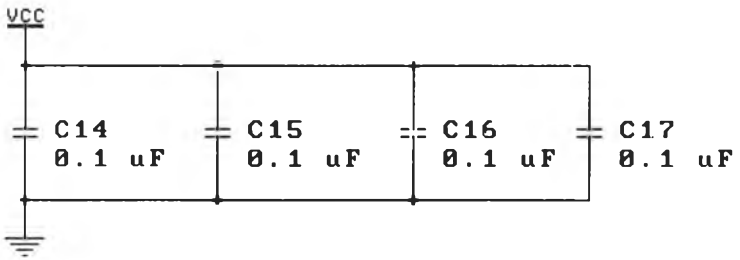



# External Connector

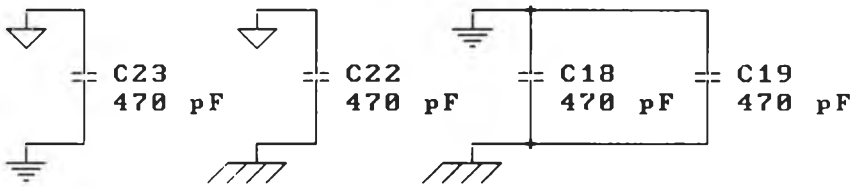
| | | |
|---|---|---|
| Title: Hx-7M : Main Board | | |
| Size: A4 | Number | Revision |
| Date: 12-MAY 1997 | | Sheet 7 of 8 |
| File: MAIN/7 | | Drawn By: |



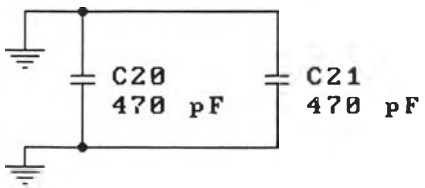

Decoupling




Bulk Capacitors

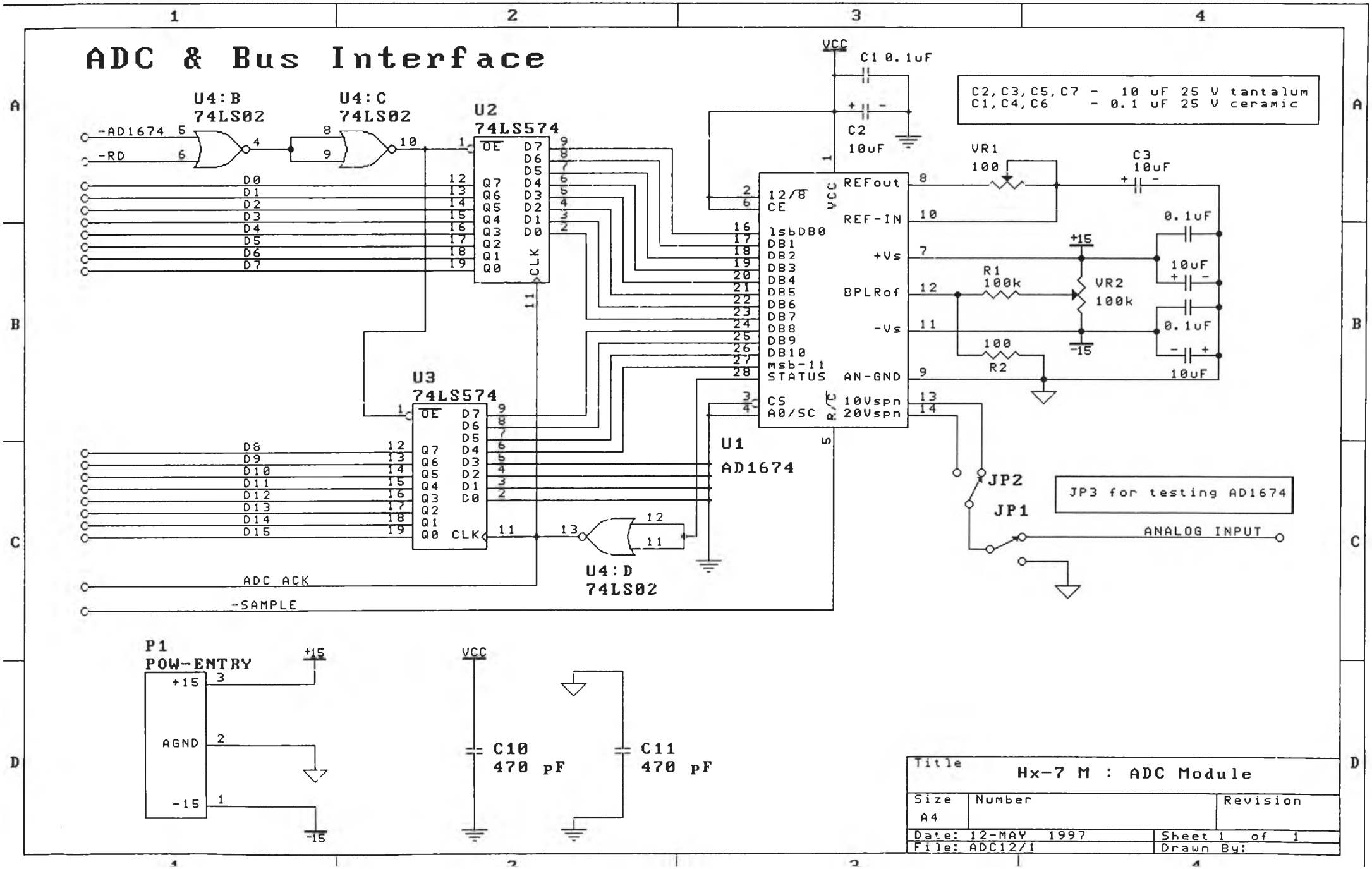



Ground Decoupling

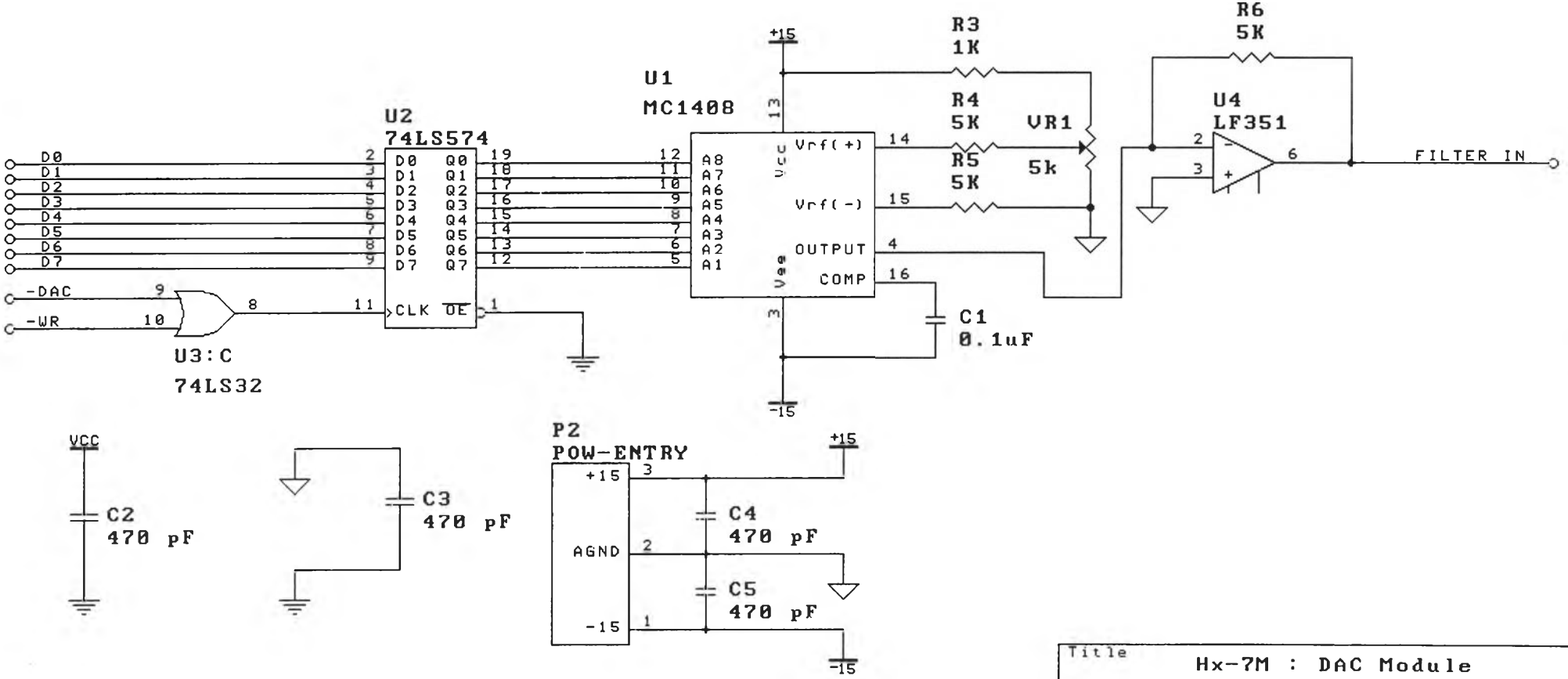



Radiate Decoupling

| | | |
|---|---|---|
| Title: Hx-7M : Main Board | | |
| Size: A4 | Number: | Revision: |
| Date: 12-MAY 1997 | | Sheet 8 of 8 |
| File: MAIN/8 | | Drawn By: |

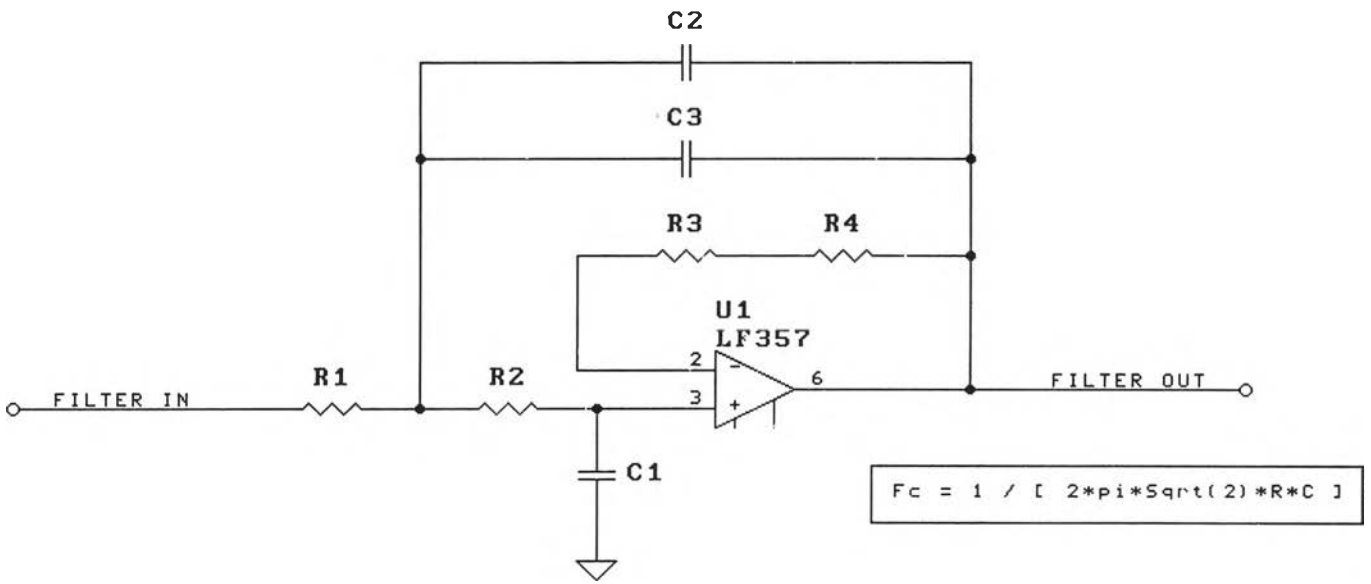

ADC & Bus Interface
U4:B
74LS02
U4:C
74LS02
U2
74LS574
U3
74LS574
U1
AD1674
U4:D
74LS02
-AD1674
-RD
D0
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
D15
ADC ACK
-SAMPLE
VCC
C1 0.1uF
C2
10uF
C3
10uF
C2, C3, C5, C7 - 10 uF 25 V tantalum
C1, C4, C6 - 0.1 uF 25 V ceramic
VR1
100
R1
100k
VR2
100k
R2
100
0.1uF
10uF
+15
-15
REFout
REF-IN
+Vs
BPLRof
-Vs
AN-GND
10Vspn
20Vspn
JP2
JP1
JP3 for testing AD1674
ANALOG INPUT
P1
POW-ENTRY
+15
AGND
-15
C10
470 pF
C11
470 pF
Title
Hx-7 M : ADC Module
Size
A4
Number
Revision
Date: 12-MAY 1997
Sheet 1 of 1
File: ADC12/1
Drawn By:

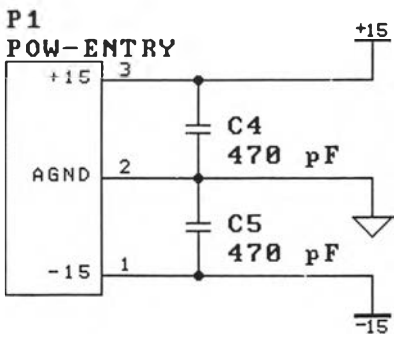
# D/A Converter



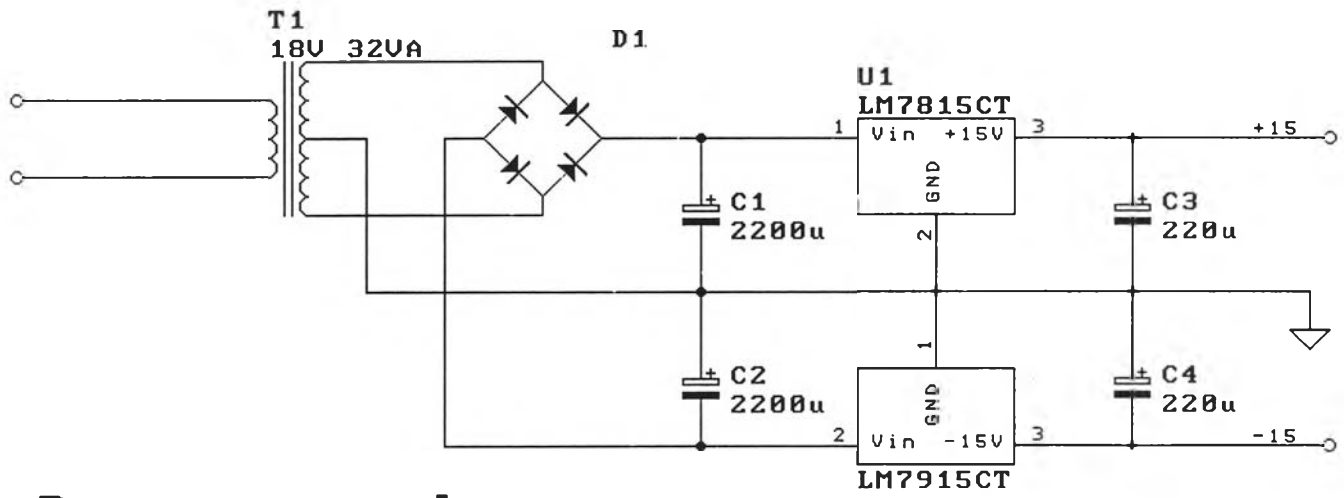

| | | |
|---|---|---|
| Title | Hx-7M : DAC Module | |
| Size A4 | Number | Revision |
| Date: 12-MAY 1997 | | Sheet 1 of 1 |
| File: DAC08/1 | | Drawn By: |

# Low-Pass Filter



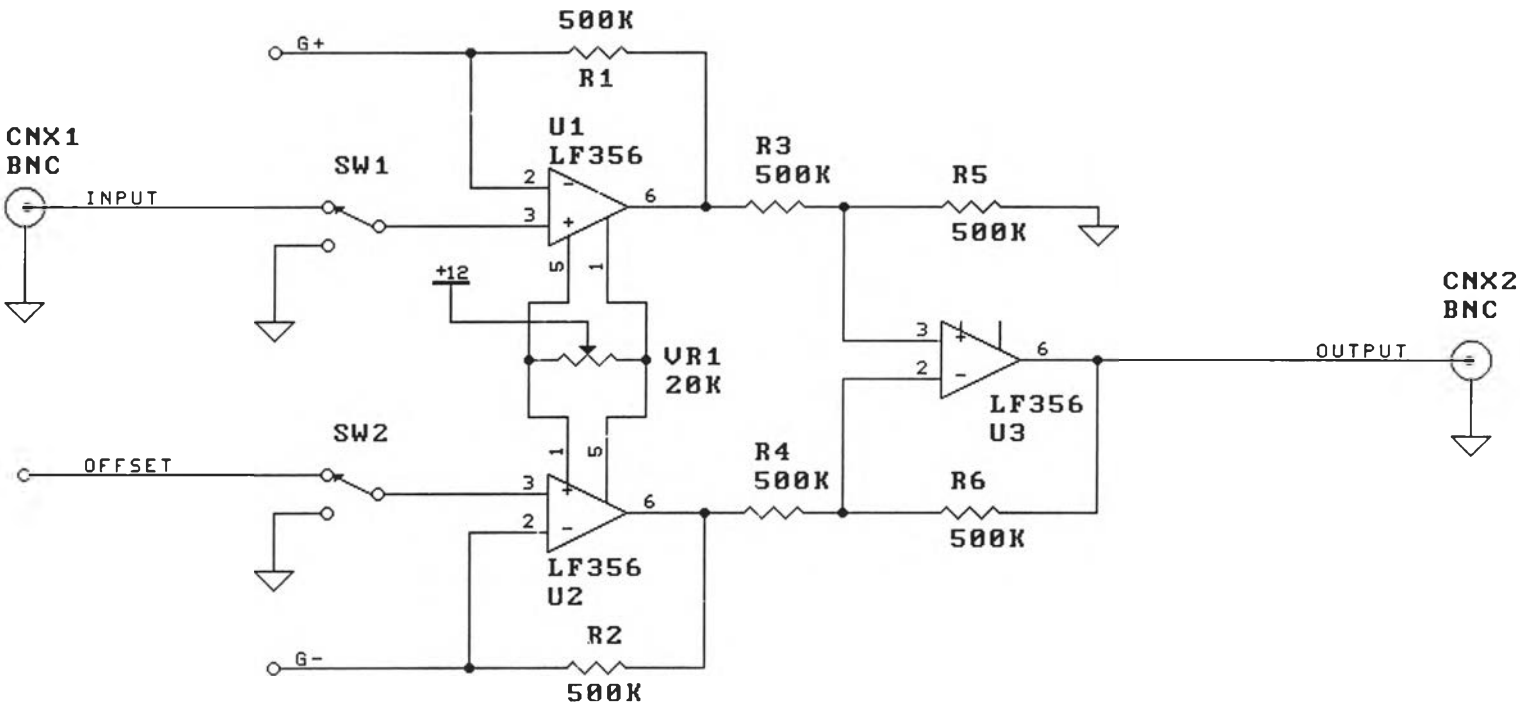

| | | |
|---|---|---|
| Title: Hx-7M: Filter Module | | |
| Size: A4 | Number: | Revision: |
| Date: 12-MAY 1997 | | Sheet 1 of 1 |
| File: LPFMIN/1 | | Drawn By: |




# DC Power supply

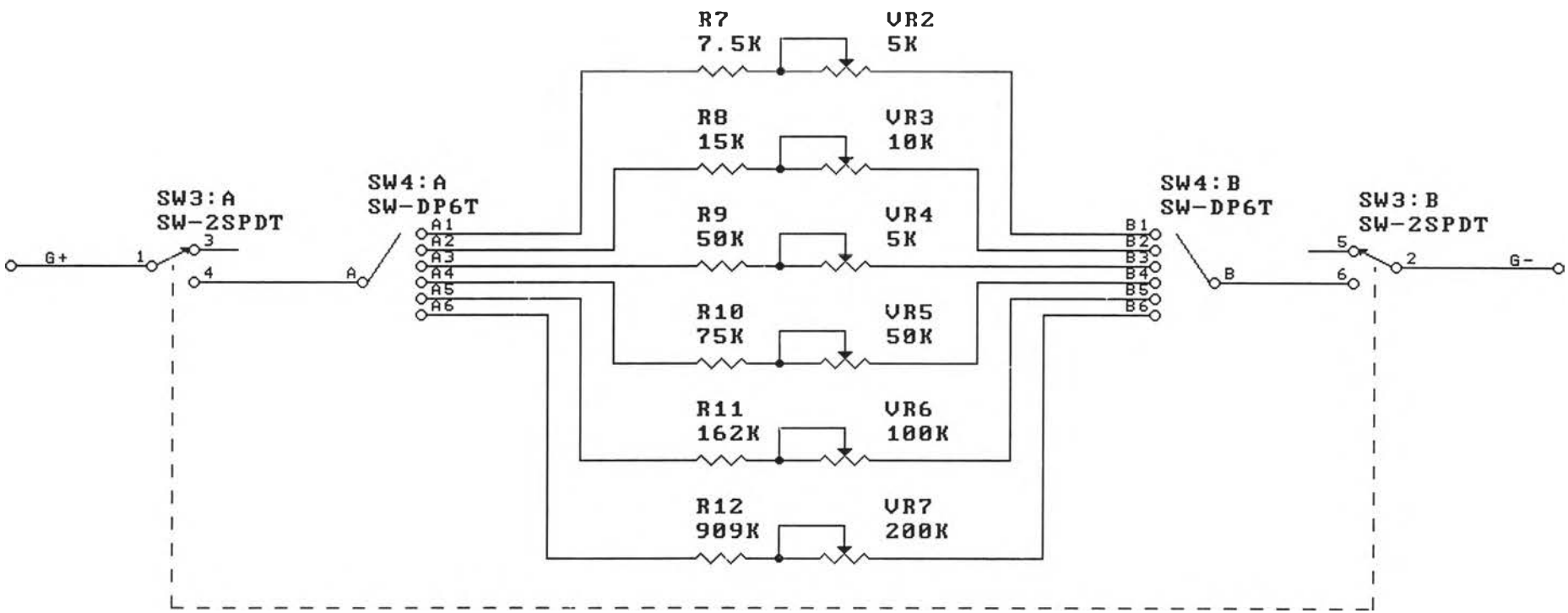
| | | | |
|---|---|---|---|
| Title | Hx-7M : Power Supply | | |
| Size A4 | Number | | Revision |
| Date: 12-MAY 1997 | | Sheet 1 of 1 | |
| File: POWER/1 | | Drawn By: | |

# Instrumentation Amp.




| | | |
|---|---|---|
| Title: Signal Conditioner | | |
| Size: A4 | Number: | Revision: |
| Date: 12-MAY 1997 | | Sheet 1 of 5 |
| File: HX-8/1 | | Drawn By: |

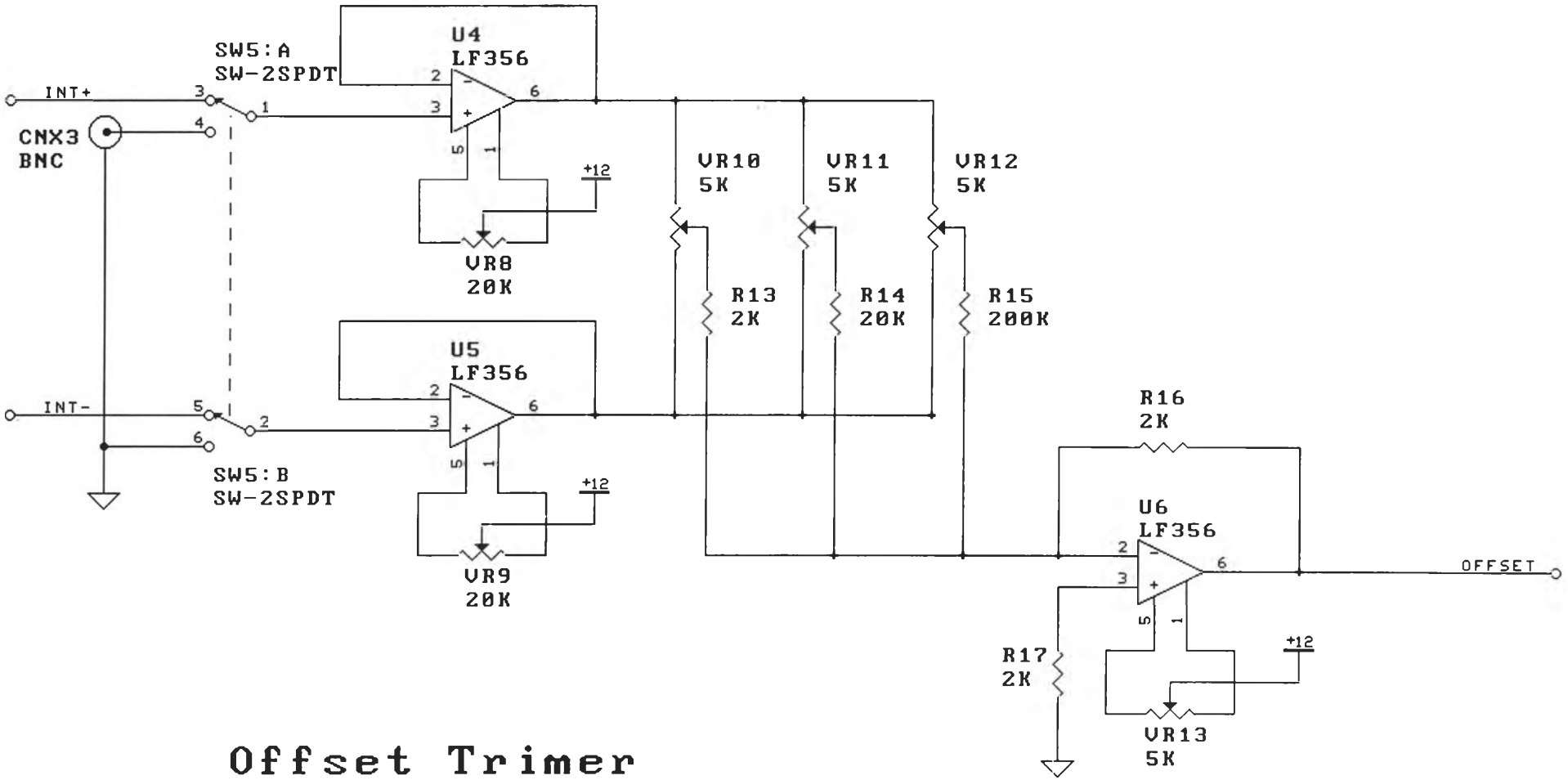
# Gain Selectors




Gain and Fine Adjust Resistor

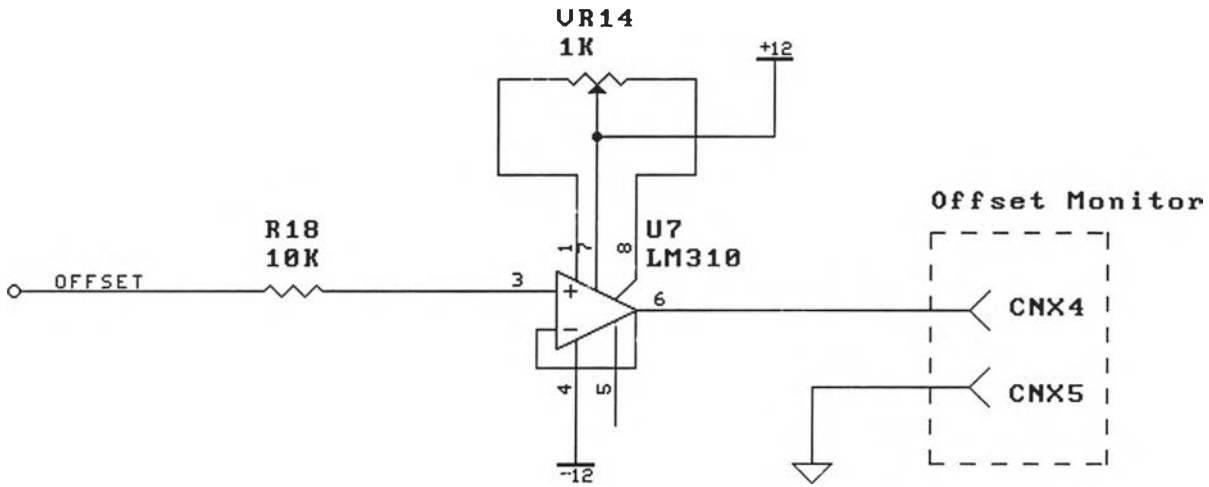
| Pos | Gain | Rx | Rfix | Radj. |
|---|---|---|---|---|
| 1 | x100 | 10.10 K | 7.5 K | 5 K |
| 2 | x50 | 20.40 K | 15 K | 10 K |
| 3 | x20 | 52.63 K | 50 K | 5 K |
| 4 | x10 | 111.11 K | 75 K | 50 K |
| 5 | x5 | 250.00 K | 162 K | 100 K |
| 6 | x2 | 1.00 M | 909 K | 200 K |

| | | |
|---|---|---|
| Title: Signal Conditioner | | |
| Size: A4 | Number | Revision |
| Date: 12-MAY 1997 | | Sheet 2 of 5 |
| File: HX-8/2 | | Drawn By: |




# Offset Trimer

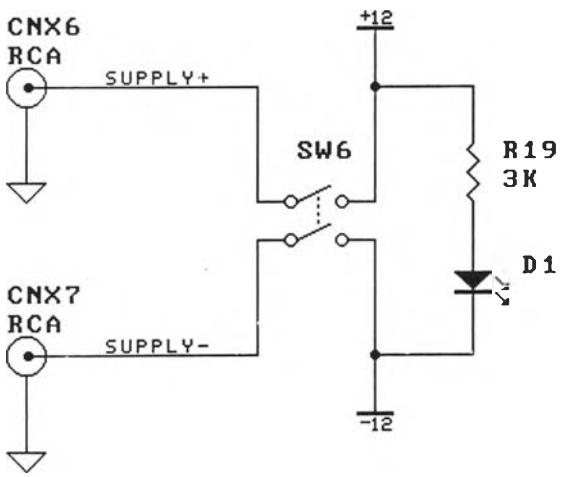
| | | |
|---|---|---|
| Title: Signal Conditioner | | |
| Size: A4 | Number | Revision |
| Date: 12-MAY 1997 | | Sheet 3 of 5 |
| File: HX-8/3 | | Drawn By: |

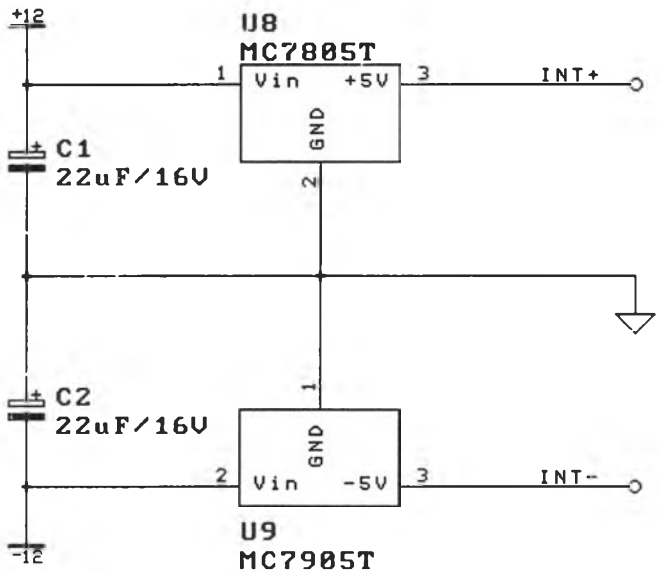



Ofs. Buffer/Monitor

| | | | |
|---|---|---|---|
| Title: Signal Conditioner | | | |
| Size: A4 | Number: | | Revision: |
| Date: 12-MAY 1997 | | Sheet 4 of 5 | |
| File: HX-8/4 | | Drawn By: | |

# Supply/Internal Ref.




| | | |
|---|---|---|
| Title: Signal Conditioner | | |
| Size: A4 | Number | Revision |
| Date: 12-MAY 1997 | | Sheet 5 of 5 |
| File: HX-8/5 | | Drawn By: |

# APPENDIX D

# ADC1674 DATA SHEETS

The following section is the data sheet for the 12-bit analog to digital converter AD1674 since the IC is not common electronic component in Thailand although it is available from some dealers in our country. All sheets are copied from the Data converter reference manual volumn II of Analog Devices Inc.

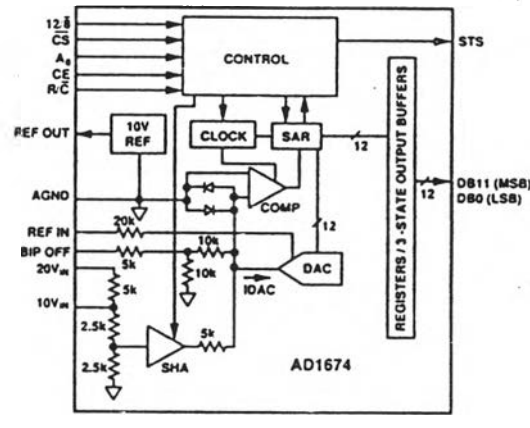
Since the information for other components is available in many reference books, the appendix need not to include.

# 12-Bit 100 kSPS A/D Converter

# AD1674*

**FEATURES**
- Complete Monolithic 12-Bit 10 µs Sampling ADC
- On-Board Sample-and-Hold Amplifier
- Industry Standard Pinout
- 8- and 16-Bit Microprocessor Interface
- AC and DC Specified and Tested
- Unipolar and Bipolar Inputs
- ±5 V, ±10 V, 0–10 V, 0–20 V Input Ranges
- Commercial, Industrial and Military Temperature Range Grades
- MIL-STD-883 Compliant Versions Available

**FUNCTIONAL BLOCK DIAGRAM**




## PRODUCT DESCRIPTION

The AD1674 is a complete, multipurpose, 12-bit analog-to-digital converter, consisting of a user-transparent on-board sample-and-hold amplifier (SHA), 10 volt reference, clock and three-state output buffers for microprocessor interface.

The AD1674 is pin compatible with the industry standard AD574A and AD674A, but includes a sampling function while delivering a faster conversion rate. The on-chip SHA has a wide input bandwidth supporting 12-bit accuracy over the full Nyquist bandwidth of the converter.

The AD1674 is fully specified for ac parameters (such as S/(N+D) ratio, THD, and IMD) and dc parameters (offset, full-scale error, etc.). With both ac and dc specifications, the AD1674 is ideal for use in signal processing and traditional dc measurement applications.

The AD1674 design is implemented using Analog Devices' BiMOS II process allowing high performance bipolar analog circuitry to be combined on the same die with digital CMOS logic.

Five different grades are available. The AD1674J and K grades are specified for operation over the 0°C to +70°C temperature range. The A and B grades are specified from −40°C to +85°C; the AD1674T grade is specified from −55°C to +125°C. The J and K grades are available in a 28-pin plastic DIP or 28-lead SOIC. All other grades are available in a 28-pin hermetically sealed ceramic DIP.

## PRODUCT HIGHLIGHTS

1. Industry Standard Pinout: The AD1674 utilizes the pinout established by the industry standard AD574A and AD674A. In stand-alone mode, the AD1674 has identical interface requirements as the AD574A and AD674A. In full control mode, the AD1674 requires slight control timing modification.
2. Integrated SHA: The AD1674 has an integrated SHA which supports the full Nyquist bandwidth of the converter. The SHA function is transparent to the user; no wait-states are needed for SHA acquisition.
3. DC and AC Specified: In addition to traditional dc specifications, the AD1674 is also fully specified for frequency domain ac parameters such as total harmonic distortion, signal-to-noise ratio and input bandwidth. These parameters can be tested and guaranteed as a result of the on-board SHA.
4. Analog Operation: The precision, laser-trimmed scaling and bipolar offset resistors provide four calibrated ranges: 0 to +10 V and 0 to +20 V unipolar, −5 V to +5 V and −10 V to +10 V bipolar. The AD1674 operates on +5 V and ±12 V or ±15 V power supplies.
5. Flexible Digital Interface: On-chip multiple-mode three-state output buffers and interface logic allow direct connection to most microprocessors.

*Protected by U. S. Patent Nos. 4,962,325; 4,250,445; 4,808,908; RE30586.

# AD1674—SPECIFICATIONS

## DC SPECIFICATIONS ($T_{min}$ to $T_{max}$, $V_{CC}$ = +15 V ± 10% or +12 V ± 5%, $V_{LOGIC}$ = +5 V ± 10%, $V_{EE}$ = −15 V ± 10% or −12 V ± 5% unless otherwise indicated)

| Parameter | AD1674J Min | AD1674J Typ | AD1674J Max | AD1674K Min | AD1674K Typ | AD1674K Max | Units |
|---|---|---|---|---|---|---|---|
| RESOLUTION | 12 | | | 12 | | | Bits |
| INTEGRAL NONLINEARITY (INL) | | | ±1 | | | ±1/2 | LSB |
| DIFFERENTIAL NONLINEARITY (DNL) (No Missing Codes) | 12 | | | 12 | | | Bits |
| UNIPOLAR OFFSET[1] @ 25°C | | | ±3 | | | ±2 | LSB |
| BIPOLAR OFFSET[1] @ 25°C | | | ±6 | | | ±4 | LSB |
| FULL-SCALE ERROR[1, 2] @ 25°C (with Fixed 50 Ω Resistor from REF OUT to REF IN | | 0.1 | 0.25 | | 0.1 | 0.25 | % of FS |
| TEMPERATURE RANGE | 0 | | +70 | 0 | | +70 | °C |
| TEMPERATURE DRIFT[3] | | | | | | | |
| Unipolar Offset[2] | | | ±2 | | | ±1 | LSB |
| Bipolar Offset[2] | | | ±2 | | | ±1 | LSB |
| Full-Scale Error[2] | | | ±6 | | | ±3 | LSB |
| POWER SUPPLY REJECTION | | | | | | | |
| $V_{CC}$ = 15 V ± 1.5 V or 12 V ± 0.6 V | | | ±2 | | | ±1 | LSB |
| $V_{LOGIC}$ = 5 V ± 0.5 V | | | ±1/2 | | | ±1/2 | LSB |
| $V_{EE}$ = −15 V ± 1.5 V or −12 V ± 0.6 V | | | ±2 | | | ±1 | LSB |
| ANALOG INPUT | | | | | | | |
| Input Ranges | | | | | | | |
| Bipolar | −5 | | +5 | −5 | | +5 | Volts |
| | −10 | | +10 | −10 | | +10 | Volts |
| Unipolar | 0 | | +10 | 0 | | +10 | Volts |
| | 0 | | +20 | 0 | | +20 | Volts |
| Input Impedance | | | | | | | |
| 10 Volt Span | 3 | 5 | 7 | 3 | 5 | 7 | kΩ |
| 20 Volt Span | 6 | 10 | 14 | 6 | 10 | 14 | kΩ |
| POWER SUPPLIES | | | | | | | |
| Operating Voltages | | | | | | | |
| $V_{LOGIC}$ | +4.5 | | +5.5 | +4.5 | | +5.5 | Volts |
| $V_{CC}$ | +11.4 | | +16.5 | +11.4 | | +16.5 | Volts |
| $V_{EE}$ | −16.5 | | −11.4 | −16.5 | | −11.4 | Volts |
| Operating Current | | | | | | | |
| $I_{LOGIC}$ | | 5 | 8 | | 5 | 8 | mA |
| $I_{CC}$ | | 10 | 14 | | 10 | 14 | mA |
| $I_{EE}$ | | 14 | 18 | | 14 | 18 | mA |
| POWER DISSIPATION | | 385 | 575 | | 385 | 575 | mW |
| INTERNAL REFERENCE VOLTAGE | 9.9 | 10.0 | 10.1 | 9.9 | 10.0 | 10.1 | Volts |
| Output Current (Available for External Loads) (External Load Should Not Change During Conversion) | | | 2.0 | | | 2.0 | mA |

NOTES
[1]Adjustable to zero.
[2]Includes internal voltage reference error.
[3]Maximum change from 25°C value to the value at $T_{min}$ or $T_{max}$.

Specifications shown in boldface are tested on all devices at final electrical test with worst case supply voltages at $T_{min}$, 25°C, and $T_{max}$. Results from those te are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested.

Specifications subject to change without notice.

| Parameter | AD1674A Min | AD1674A Typ | AD1674A Max | AD1674B Min | AD1674B Typ | AD1674B Max | AD1674T Min | AD1674T Typ | AD1674T Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| RESOLUTION | 12 | | | 12 | | | 12 | | | Bits |
| INTEGRAL NONLINEARITY (INL) @ 25°C | | | ±1 | | | ±1/2 | | | ±1/2 | LSB |
| $T_{min}$ to $T_{max}$ | | | ±1 | | | ±1/2 | | | ±1 | LSB |
| DIFFERENTIAL NONLINEARITY (DNL) (No missing codes) | 12 | | | 12 | | | 12 | | | Bits |
| UNIPOLAR OFFSET[1] @ 25°C | | | ±2 | | | ±2 | | | ±2 | LSB |
| BIPOLAR OFFSET[1] @ 25°C | | | ±6 | | | ±3 | | | ±3 | LSB |
| FULL-SCALE ERROR[1, 2] @ 25°C (with Fixed 50 Ω Resistor from REF OUT to REF IN) | | 0.1 | 0.25 | | 0.1 | 0.125 | | 0.1 | 0.125 | % of FSR |
| TEMPERATURE RANGE | −40 | | +85 | −40 | | +85 | −55 | | +125 | °C |
| TEMPERATURE DRIFT[3] | | | | | | | | | | |
| Unipolar Offset[2] | | | ±2 | | | ±1 | | | ±1 | LSB |
| Bipolar Offset[2] | | | ±2 | | | ±1 | | | ±2 | LSB |
| Full-Scale Error[2] | | | ±8 | | | ±5 | | | ±7 | LSB |
| POWER SUPPLY REJECTION | | | | | | | | | | |
| $V_{CC}$ = 15 V ± 1.5 V or 12 V ± 0.6 V | | | ±2 | | | ±1 | | | ±1 | LSB |
| $V_{LOGIC}$ = 5 V ± 0.5 V | | | ±1/2 | | | ±1/2 | | | ±1/2 | LSB |
| $V_{EE}$ = −15 V ± 1.5 V or −12 V ± 0.6 V | | | ±2 | | | ±1 | | | ±1 | LSB |
| ANALOG INPUT | | | | | | | | | | |
| Input Ranges | | | | | | | | | | |
| Bipolar | −5 | | +5 | −5 | | +5 | −5 | | +5 | Volts |
| | −10 | | +10 | −10 | | +10 | −10 | | +10 | Volts |
| Unipolar | 0 | | +10 | 0 | | +10 | 0 | | +10 | Volts |
| | 0 | | +20 | 0 | | +20 | 0 | | +20 | Volts |
| Input Impedance | | | | | | | | | | |
| 10 Volt Span | 3 | 5 | 7 | 3 | 5 | 7 | 3 | 5 | 7 | kΩ |
| 20 Volt Span | 6 | 10 | 14 | 6 | 10 | 14 | 6 | 10 | 14 | kΩ |
| POWER SUPPLIES | | | | | | | | | | |
| Operating Voltages | | | | | | | | | | |
| $V_{LOGIC}$ | +4.5 | | +5.5 | +4.5 | | +5.5 | +4.5 | | +5.5 | Volts |
| $V_{CC}$ | +11.4 | | +16.5 | +11.4 | | +16.5 | +11.4 | | +16.5 | Volts |
| $V_{EE}$ | −16.5 | | −11.4 | −16.5 | | −11.4 | −16.5 | | −11.4 | Volts |
| Operating Current | | | | | | | | | | |
| $I_{LOGIC}$ | | 5 | 8 | | 5 | 8 | | 5 | 8 | mA |
| $I_{CC}$ | | 10 | 14 | | 10 | 14 | | 10 | 14 | mA |
| $I_{EE}$ | | 14 | 18 | | 14 | 18 | | 14 | 18 | mA |
| POWER DISSIPATION | | 385 | 575 | | 385 | 575 | | 385 | 575 | mW |
| INTERNAL REFERENCE VOLTAGE | 9.9 | 10.0 | 10.1 | 9.9 | 10.0 | 10.1 | 9.9 | 10.0 | 10.1 | Volts |
| Output Current (Available for External Loads) (External Load Should Not Change During Conversion) | | | 2.0 | | | 2.0 | | | 2.0 | mA |

## AD1674—AC SPECIFICATIONS

($T_{min}$ to $T_{max}$ with $V_{CC}$ = +15 V ± 10% or +12 V ± 5%, $V_{LOGIC}$ = +5 V ± 10%, $V_{EE}$ = −15 V ± 10% or −12 V ± 5%, $f_{SAMPLE}$ = 100 kSPS, $f_{IN}$ = 10 kHz, stand-alone mode unless otherwise noted)[1]

| Parameter | AD1674J/A Min | AD1674J/A Typ | AD1674J/A Max | AD1674K/B/T Min | AD1674K/B/T Typ | AD1674K/B/T Max | Units |
|---|---|---|---|---|---|---|---|
| Signal to Noise and Distortion (S/N+D) Ratio[2, 3] | 69 | 70 | | 70 | 71 | | dB |
| Total Harmonic Distortion (THD)[4] | | −90 | −82 | | −90 | −82 | dB |
| | | | 0.008 | | | 0.008 | % |
| Peak Spurious or Peak Harmonic Component | | −92 | −82 | | −92 | −82 | dB |
| Full Power Bandwidth | | 1 | | | 1 | | MHz |
| Full Linear Bandwidth | | 500 | | | 500 | | kHz |
| Intermodulation Distortion (IMD)[5] | | | | | | | |
| Second Order Products | | −90 | −80 | | −90 | −80 | dB |
| Third Order Products | | −90 | −80 | | −90 | −80 | dB |
| SHA (specifications are included in overall timing specifications) | | | | | | | |
| Aperture Delay | | 15 | | | 15 | | ns |
| Aperture Jitter | | 150 | | | 150 | | ps |
| Acquisition Time | | 1 | | | 1 | | µs |

## DIGITAL SPECIFICATIONS

(for all grades $T_{min}$ to $T_{max}$ with $V_{CC}$ = +15 V ± 10% or +12 V ± 5%, $V_{LOGIC}$ = +5 V ± 10%, $V_{EE}$ = −15 V ± 10% or −12 V ± 5%)

| Parameter | | Test Conditions | Min | Max | Units |
|---|---|---|---|---|---|
| LOGIC INPUTS | | | | | |
| $V_{IH}$ | High Level Input Voltage | | +2.0 | $V_{LOGIC}$ +0.5 V | V |
| $V_{IL}$ | Low Level Input Voitage | | −0.5 | +0.8 | V |
| $I_{IH}$ | High Level Input Current ($V_{IN}$ = 5 V) | $V_{IN}$ = $V_{LOGIC}$ | −10 | +10 | µA |
| $I_{IL}$ | Low Level Input Current ($V_{IN}$ = 0 V) | $V_{IN}$ = 0 V | −10 | +10 | µA |
| $C_{IN}$ | Input Capacitance | | | 10 | pF |
| LOGIC OUTPUTS | | | | | |
| $V_{OH}$ | High Level Output Voltage | $I_{OH}$ = 0.5 mA | +2.4 | | V |
| $V_{OL}$ | Low Level Output Voltage | $I_{OL}$ = 1.6 mA | | +0.4 | V |
| $I_{OZ}$ | High-Z Leakage Current | $V_{IN}$ = 0 to $V_{LOGIC}$ | −10 | +10 | µA |
| $C_{OZ}$ | High-Z Output Capacitance | | | 10 | pF |

NOTES

[1] $f_{IN}$ amplitude = −0.5 dB (9.44 V p–p) 10 V bipolar mode unless otherwise indicated. All measurements referred to −0 dB (9.997 V p–p) input signal unless otherwise indicated.

[2] Specified at worst case temperatures and supplies after one minute warm-up.

[3] See Figures 12 and 13 for other input frequencies and amplitudes.

[4] See Figure 11.

[5] fa = 9.08 kHz, fb = 9.58 kHz with $f_{SAMPLE}$ = 100 kHz. See *Definition of Specifications* section and Figure 15.

Specifications shown in boldface are tested on all devices at final electrical test with worst case supply voltages at $T_{min}$, 25°C, and $T_{max}$. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested.

Specifications subject to change without notice.

## SWITCHING SPECIFICATIONS

(for all grades $T_{min}$ to $T_{max}$ with $V_{CC}$ = +15 V ± 10% or +12 V ± 5%, $V_{LOGIC}$ = +5 V ± 10%, $V_{EE}$ = −15 V ± 10% or −12 V ± 5%; $V_{IL}$ = 0.4 V, $V_{IH}$ = 2.4 V unless otherwise noted)

### CONVERTER START TIMING (Figure 1)

| Parameter | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Conversion Time | | | | | |
| 8-Bit Cycle | $t_C$ | | 7 | 8 | µs |
| 12-Bit Cycle | $t_C$ | | 9 | 10 | µs |
| STS Delay from CE @ 25°C | $t_{DSC}$ | | | 200 | ns |
| $T_{min}$ to $T_{max}$ | | | | 250 | ns |
| CE Pulse Width @ 25°C | $t_{HEC}$ | 50 | | | ns |
| $T_{min}$ to $T_{max}$ | | 75 | | | ns |
| $\overline{CS}$ to CE Setup | $t_{SSC}$ | 50 | | | ns |
| $\overline{CS}$ Low During CE High @ 25°C | $t_{HSC}$ | 50 | | | ns |
| $T_{min}$ to $T_{max}$ | | 75 | | | ns |
| R/$\overline{C}$ to CE Setup | $t_{SRC}$ | 50 | | | ns |
| R/$\overline{C}$ Low During CE High @ 25°C | $t_{HRC}$ | 50 | | | ns |
| $T_{min}$ to $T_{max}$ | | 150 | | | ns |
| $A_0$ to CE Setup | $t_{SAC}$ | 0 | | | ns |
| $A_0$ Valid During CE High | $t_{HAC}$ | 50 | | | ns |

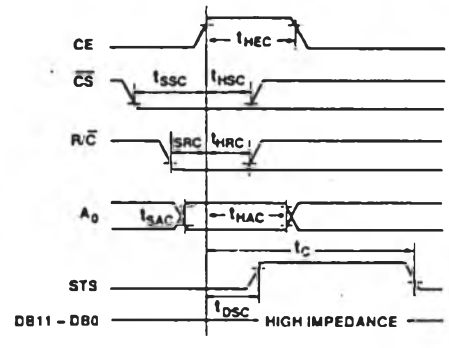



*Figure 1. Converter Start Timing*

### READ TIMING – FULL CONTROL MODE (Figure 2)

| Parameter | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Access Time | | | | | |
| $C_L$ = 100 pF | $t_{DD}$[1] | | 75 | 150 | ns |
| Data Valid After CE Low | $t_{HD}$ | 25 | | | ns |
| Output Float Delay | $t_{HL}$[2] | | | 150 | ns |
| $\overline{CS}$ to CE Setup | $t_{SSR}$ | 50 | | | ns |
| R/$\overline{C}$ to CE Setup | $t_{SRR}$ | 0 | | | ns |
| $A_0$ to CE Setup | $t_{SAR}$ | 50 | | | ns |
| $\overline{CS}$ Valid After CE Low | $t_{HSR}$ | 0 | | | ns |
| R/$\overline{C}$ High After CE Low | $t_{HRR}$ | 60 | | | ns |
| $A_0$ Valid After CE Low | $t_{HAR}$ | 50 | | | ns |

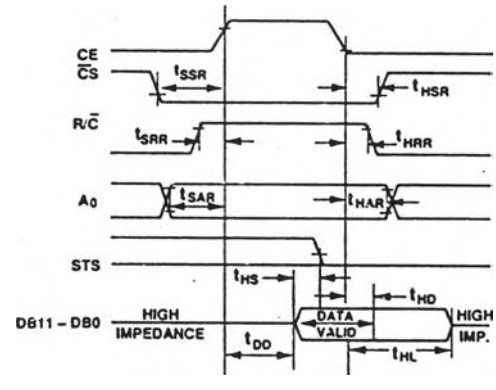



*Figure 2. Read Timing*

NOTES

[1] $t_{DD}$ is measured with the load circuit of Figure 3 and is defined as the time required for an output to cross 0.4 V or 2.4 V.

[2] $t_{HL}$ is defined as the time required for the data lines to change 0.5 V when loaded with the circuit of Figure 3.

Specifications shown in boldface are tested on all devices at final electrical test with worst case supply voltages at $T_{min}$, 25°C, and $T_{max}$. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested.

Specifications subject to change without notice.

| Test | $V_{CP}$ | $C_{OUT}$ |
|---|---|---|
| Access Time High Z to Logic Low | 5 V | 100 pF |
| Float Time Logic High to High Z | 0 V | 10 pF |
| Access Time High Z to Logic High | 0 V | 100 pF |
| Float Time Logic Low to High Z | 5 V | 10 pF |

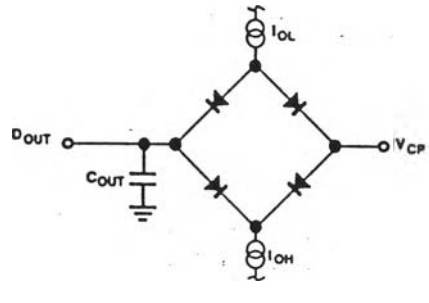



*Figure 3. Load Circuit for Bus Timing Specifications*

### TIMING – STAND-ALONE MODE (Figures 4a and 4b)

| Parameter | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Data Access Time | $t_{DDR}$ | | | 150 | ns |
| Low R/$\overline{C}$ Pulse Width | $t_{HRL}$ | 50 | | | ns |
| STS Delay from R/$\overline{C}$ @ 25°C | $t_{DS}$ | | | 200 | ns |
| $T_{min}$ to $T_{max}$ | | | | 250 | ns |
| Data Valid After R/$\overline{C}$ Low | $t_{HDR}$ | 25 | | | ns |
| STS Delay After Data Valid | $t_{HS}$ | 0.6 | 0.8 | 1.2 | µs |
| High R/$\overline{C}$ Pulse Width | $t_{HRH}$ | 150 | | | ns |

NOTE
Specifications shown in boldface are tested on all devices at final electrical test with worst case supply voltages at $T_{min}$, 25°C, and $T_{max}$. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested.

Specifications subject to change without notice.

### ABSOLUTE MAXIMUM RATINGS*

$V_{CC}$ to Digital Common . . . . . 0 to +16.
$V_{EE}$ to Digital Common . . . . . 0 to −16.
$V_{LOGIC}$ to Digital Common . . . . . 0 to +
Analog Common to Digital Common . . . . . ±
Digital Inputs to Digital Common . −0.5 V to $V_{LOGIC}$ +0.
Analog Inputs to Analog Common . . . . . $V_{EE}$ to
20 $V_{IN}$ to Analog Common . . . . . ±2
REF OUT . . . . . Indefinite Short to Comr
. . . . . Momentary Short to
Junction Temperature . . . . . +17
Power Dissipation . . . . . 825 r
Lead Temperature, Soldering . . . . . 300°C, 10
Storage Temperature . . . . . −65°C to +15

*Stresses above those listed under "Absolute Maximum Ratings" may c permanent damage to the device. This is a stress rating only and functi operation of the device at these or any other conditions above those indic in the operational section of this specification is not implied. Exposur absolute maximum rating conditions for extended periods may affect de reliability.

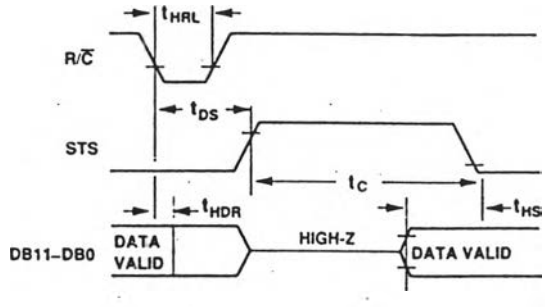



*Figure 4a. Stand-Alone Mode Timing Low Pulse for R/$\overline{C}$*

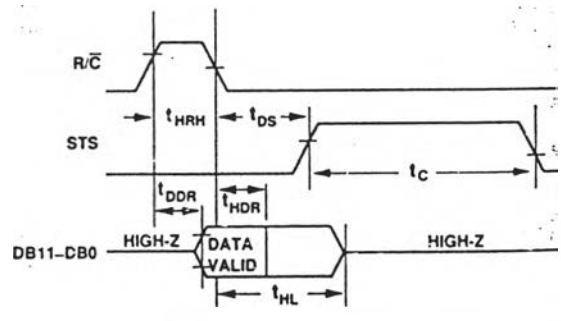



*Figure 4b. Stand-Alone Mode Timing High Pulse for R/*

**CAUTION:**
ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.


### ORDERING GUIDE

| Model[1] | Temperature Range | INL ($T_{min}$ to $T_{max}$) | S/(N+D) ($T_{min}$ to $T_{max}$) | Package Option[2] |
|---|---|---|---|---|
| AD1674JN | 0°C to +70°C | ±1 LSB | 69 dB | N-28A |
| AD1674KN | 0°C to +70°C | ±1/2 LSB | 70 dB | N-28A |
| AD1674JR | 0°C to +70°C | ±1 LSB | 69 dB | R-28 |
| AD1674KR | 0°C to +70°C | ±1/2 LSB | 70 dB | R-28 |
| AD1674AD | −40°C to +85°C | ±1 LSB | 69 dB | D-28A |
| AD1674BD | −40°C to +85°C | ±1/2 LSB | 70 dB | D-28A |
| AD1674TD | −55°C to +125°C | ±1 LSB | 70 dB | D-28A |

NOTES
[1]For details on grade and package offerings screened in accordance with MIL-STD-883, refer to the Analog Devices Military Products Databook or current AD1674/883B data sheet.
[2]N = Plastic DIP; D = Hermetic Ceramic DIP; R = plastic SOIC. For outline information see Package Information section.

## DEFINITION OF SPECIFICATIONS

### INTEGRAL NONLINEARITY (INL)
The ideal transfer function for an ADC is a straight line drawn between "zero" and "full scale." The point used as "zero" occurs 1/2 LSB before the first code transition. "Full scale" is defined as a level 1 1/2 LSB beyond the last code transition. Integral nonlinearity is the worst-case deviation of a code from the straight line. The deviation of each code is measured from the middle of that code.

### DIFFERENTIAL NONLINEARITY (DNL)
A specification which guarantees no missing codes requires that every code combination appear in a monotonic increasing sequence as the analog input level is increased. Thus every code must have a finite width. The AD1674 guarantees no missing codes to 12-bit resolution; all 4096 codes are present over the entire operating range.

### UNIPOLAR OFFSET
The first transition should occur at a level 1/2 LSB above analog common. Unipolar offset is defined as the deviation of the actual transition from that point at 25°C. This offset can be adjusted as shown in Figure 6.

### BIPOLAR OFFSET
In the bipolar mode the major carry transition (0111 1111 1111 to 1000 0000 0000) should occur for an analog value 1/2 LSB below analog common. The bipolar offset error specifies the deviation of the actual transition from that point at 25°C. This offset can be adjusted as shown in Figure 7.

### FULL-SCALE ERROR
The last transition (from 1111 1111 1110 to 1111 1111 1111) should occur for an analog value 1 1/2 LSB below the nominal full scale (9.9963 volts for 10 volts full scale). The full-scale error is the deviation of the actual level of the last transition from the ideal level at 25°C. The full-scale error can be adjusted to zero as shown in Figures 6 and 7.

### TEMPERATURE DRIFT
The temperature drifts for full-scale error, unipolar offset and bipolar offset specify the maximum change from the initial (25°C) value to the value at $T_{min}$ or $T_{max}$.

### POWER SUPPLY REJECTION
The effect of power supply error on the performance of the device will be a small change in full scale. The specifications show the maximum full-scale change from the initial value with the supplies at various limits.

### FREQUENCY-DOMAIN TESTING
The AD1674 is tested dynamically using a sine wave input and a 2048 point Fast Fourier Transform (FFT) to analyze the resulting output. Coherent sampling is used, wherein the ADC sampling frequency and the analog input frequency are related to each other by a ratio of integers. This ensures that an integral multiple of input cycles is captured, allowing direct FFT processing without windowing or digital filtering which could mask some of the dynamic characteristics of the device. In addition, the frequencies are chosen to be "relatively prime" (no common factors) to maximize the number of different ADC codes that are present in a sample sequence. The result, called Prime Coherent Sampling, is a highly accurate and repeatable measure of the actual frequency-domain response of the converter.

### NYQUIST FREQUENCY
An implication of the Nyquist sampling theorem, the "Nyquist Frequency" of a converter is that input frequency which is one-half the sampling frequency of the converter.

### SIGNAL-TO-NOISE AND DISTORTION (S/N+D) RATIO
S/(N+D) is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for S/(N+D) is expressed in decibels.

### TOTAL HARMONIC DISTORTION (THD)
THD is the ratio of the rms sum of the first six harmonic components to the rms value of a full-scale input signal and is expressed as a percentage or in decibels. For input signals or harmonics that are above the Nyquist frequency, the aliased component is used.

### INTERMODULATION DISTORTION (IMD)
With inputs consisting of sine waves at two frequencies, fa and fb, any device with nonlinearities will create distortion products, of order (m+n), at sum and difference frequencies of mfa ± nfb, where m,n = 0,1,2,3... Intermodulation terms are those for which m or n is not equal to zero. For example, the second order terms are (fa + fb) and (fa − fb) and the third order terms are (2fa + fb), (2fa − fb), (fa + 2fb) and (fa − 2fb). The IMD products are expressed as the decibel ratio of the rms sum of the measured input signals to the rms sum of the distortion terms. The two signals are of equal amplitude and the peak value of their sums is −0.5 dB from full-scale. The IMD products are normalized to a 0 dB input signal.

### FULL-POWER BANDWIDTH
The full-power bandwidth is that input frequency at which the amplitude of the reconstructed fundamental is reduced by 3 dB for a full-scale input.

### FULL-LINEAR BANDWIDTH
The full-linear bandwidth is the input frequency at which the slew rate limit of the sample-hold-amplifier (SHA) is reached. At this point, the amplitude of the reconstructed fundamental has degraded by less than −0.1 dB. Beyond this frequency, distortion of the sampled input signal increases significantly.

### APERTURE DELAY
Aperture delay is a measure of the SHA's performance and is measured from the falling edge of Read/Convert (R/$\overline{C}$) to when the input signal is held for conversion.

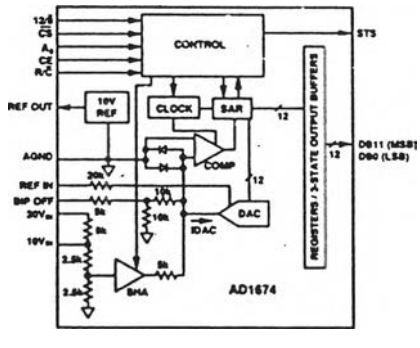
### APERTURE JITTER
Aperture jitter is the variation in aperture delay for successive samples and is manifested as noise on the input to the A/D.

## PIN DESCRIPTION

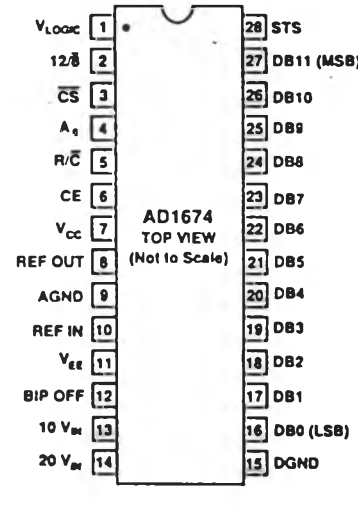
| Symbol | Pin No. | Type | Name and Function |
|---|---|---|---|
| AGND | 9 | P | Analog Ground (Common). |
| $A_0$ | 4 | DI | Byte Address/Short Cycle. If a conversion is started with $A_0$ Active LOW, a full 12-bit conversion cycle is initiated. If $A_0$ is Active HIGH during a convert start, a shorter 8-bit conversion cycle results. During Read ($R/\overline{C}$ = 1) with $12/\overline{8}$ LOW, $A_0$ = LOW enables the 8 most significant bits (DB4–DB11), and $A_0$ = HIGH enables DB3–DB0 and sets DB7–DB4 = 0. |
| BIP OFF | 12 | AI | Bipolar Offset. Connect through a 50 Ω resistor to REF OUT for bipolar operation or to Analog Common for unipolar operation. |
| CE | 6 | DI | Chip Enable. Chip Enable is Active HIGH and is used to initiate a convert or read operation. |
| $\overline{CS}$ | 3 | DI | Chip Select. Chip Select is Active LOW. |
| DB11–DB8 | 27–24 | DO | Data Bits 11 through 8. In the 12-bit format (see $12/\overline{8}$ and $A_0$ pins), these pins provide the upper 4 bits of data. In the 8-bit format, they provide the upper 4 bits when $A_0$ is LOW and are disabled when $A_0$ is HIGH. |
| DB7–DB4 | 23–20 | DO | Data Bits 7 through 4. In the 12-bit format these pins provide the middle 4 bits of data. In the 8-bit format they provide the middle 4 bits when $A_0$ is LOW and all zeroes when $A_0$ is HIGH. |
| DB3–DB0 | 19–16 | DO | Data Bits 3 through 0. In both the 12-bit and 8-bit format these pins provide the lower 4 bits of data when $A_0$ is HIGH; they are disabled when $A_0$ is LOW. |
| DGND | 15 | P | Digital Ground (Common). |
| REF OUT | 8 | AO | +10 V Reference Output. |
| $R/\overline{C}$ | 5 | DI | Read/Convert. In the full control mode $R/\overline{C}$ is Active HIGH for a read operation and Active LOW for a convert operation. In the stand-alone mode, the falling edge of $R/\overline{C}$ initiates a conversion. |
| REF IN | 10 | AI | Reference Input is connected through a 50 Ω resistor to +10 V Reference for normal operation. |
| STS | 28 | DO | Status is Active HIGH when a conversion is in progress and goes LOW when the conversion is completed. |
| $V_{CC}$ | 7 | P | +12 V/+15 V Analog Supply. |
| $V_{EE}$ | 11 | P | −12 V/−15 V Analog Supply. |
| $V_{LOGIC}$ | 1 | P | +5 V Logic Supply. |
| 10 $V_{IN}$ | 13 | AI | 10 V Span Input, 0 to +10 V unipolar mode or −5 V to +5 V bipolar mode. When using the AD1674 in the 20 V Span 10 $V_{IN}$ should not be connected. |
| 20 $V_{IN}$ | 14 | AI | 20 V Span Input, 0 to +20 V unipolar mode or −10 V to +10 V bipolar mode. When using the AD1674 in the 10 V Span 20 $V_{IN}$ should not be connected. |
| $12/\overline{8}$ | 2 | DI | The $12/\overline{8}$ pin determines whether the digital output data is to be organized as two 8-bit words ($12/\overline{8}$ LOW) or a single 12-bit word ($12/\overline{8}$ HIGH). |

TYPE: AI = Analog Input
AO = Analog Output
DI = Digital Input
DO = Digital Output
P = Power

### FUNCTIONAL BLOCK DIAGRAM




### PIN CONFIGURATION



## GENERAL CIRCUIT OPERATION

The AD1674 is a complete 12-bit, 10 μs sampling analog-to-digital converter. A block diagram of the AD1674 is shown on the previous page.

When the control section is commanded to initiate a conversion (as described later), it places the sample-and-hold amplifier (SHA) in the hold mode, enables the clock, and resets the successive approximation register (SAR). Once a conversion cycle has begun, it cannot be stopped or restarted and data is not available from the output buffers. The SAR, timed by the clock, will sequence through the conversion cycle and return an end-of-convert flag to the control section when the conversion has been completed. The control section will then disable the clock, switch the SHA to sample mode, and delay the STS LOW going edge to allow for acquisition to 12-bit accuracy. The control section will allow data read functions by external command anytime during the SHA acquisition interval.

During the conversion cycle, the internal 12-bit, 1 mA full-scale current output DAC is sequenced by the SAR from the most significant bit (MSB) to the least significant bit (LSB) to provide an output that accurately balances the current through the 5 kΩ resistor from the input signal voltage held by the SHA. The SHA's input scaling resistors divide the input voltage by 2 for the 10 V input span and by 4 for the 20 V input span, maintaining a 1 mA full-scale output current through the 5 kΩ resistor for both ranges. The comparator determines whether the addition of each successively weighted bit current causes the DAC current sum to be greater than or less than the input current. If the sum is less, the bit is left on; if more, the bit is turned off. After testing all the bits, the SAR contains a 12-bit binary code which accurately represents the input signal to within ±1/2 LSB.

## CONTROL LOGIC

The AD1674 may be operated in one of two modes, the full-control mode and the stand-alone mode. The full-control mode utilizes all the AD1674 control signals and is useful in systems that address decode multiple devices on a single data bus. The stand-alone mode is useful in systems with dedicated input ports available and thus not requiring full bus interface capability. Table I is a truth table for the AD1674, and Figure 5 illustrates the internal logic circuitry.

| CE | $\overline{CS}$ | R/$\overline{C}$ | 12/$\overline{8}$ | $A_0$ | Operation |
|---|---|---|---|---|---|
| 0 | X | X | X | X | None |
| X | 1 | X | X | X | None |
| 1 | 0 | 0 | X | 0 | Initiate 12-Bit Conversion |
| 1 | 0 | 0 | X | 1 | Initiate 8-Bit Conversion |
| 1 | 0 | 1 | 1 | X | Enable 12-Bit Parallel Output |
| 1 | 0 | 1 | 0 | 0 | Enable 8 Most Significant Bits |
| 1 | 0 | 1 | 0 | 1 | Enable 4 LSBs +4 Trailing Zeroes |

*Table I. AD1674A Truth Table*

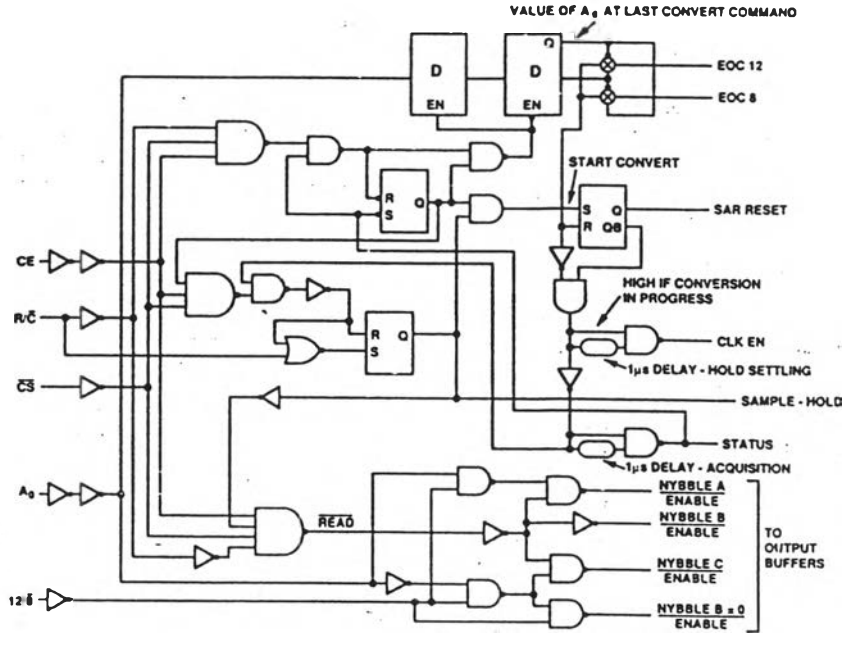



*Figure 5. Equivalent Internal Logic Circuitry*

## FULL-CONTROL MODE

In full-control mode, the AD1674 departs slightly from the AD674A timing requirements. These differences are discussed in Table II. In full-control mode, AD1674 timing should be reviewed for compliancy with AD674A applications.

| Specification | AD674A | AD1674 |
|---|---|---|
| $t_{HRC}$ | 50 ns (min) | 50 ns @ 25°C<br>150 ns $T_{min}$ to $T_{max}$ |
| $t_{HRR}$ | 0 ns (min) | 60 ns |
| $t_{DSC}$ | 200 ns (max) | 200 ns @ 25°C<br>250 ns $T_{min}$ to $T_{max}$ |
| $t_{HS}$ | 600 ns (max) | 1 µs |

*Table II.*

Chip Enable (CE), Chip Select ($\overline{CS}$) and Read/Convert (R/$\overline{C}$) are used to control Convert or Read modes of operation. Either CE or $\overline{CS}$ may be used to initiate a conversion. Note that the shortest delay path to the SHA control is from the R/$\overline{C}$ input (see Figure 5). SHA accuracy has been optimized for use in stand-alone mode and consequently results in the Table II differences for the full-control mode of operation. The state of R/$\overline{C}$ when CE and $\overline{CS}$ are both asserted determines whether a data Read (R/$\overline{C}$ = 1) or a Convert (R/$\overline{C}$ = 0) is in progress. R/$\overline{C}$ should be LOW before both CE and $\overline{CS}$ are asserted; if R/$\overline{C}$ is HIGH, a Read operation will momentarily occur, possibly resulting in system bus contention.

## STAND-ALONE MODE

The AD1674 can be used in a "stand-alone" mode, which is useful in systems with dedicated input ports available and thus not requiring full bus interface capability. Stand-alone mode applications are generally able to issue conversion start commands more precisely than full-control mode. This improves ac performance by reducing the amount of control-induced aperture jitter.

In stand-alone mode, the control interface for the AD1674 and AD674A are identical. CE and 12/$\overline{8}$ are wired HIGH, $\overline{CS}$ and $A_0$ are wired LOW, and conversion is controlled by R/$\overline{C}$. The three-state buffers are enabled when R/$\overline{C}$ is HIGH and a conversion starts when R/$\overline{C}$ goes LOW. This gives rise to two possible control signals — a high pulse or a low pulse. Operation with a low pulse is shown in Figure 4a. In this case, the outputs are forced into the high-impedance state in response to the falling edge of R/$\overline{C}$ and return to valid logic levels after the conversion cycle is completed. The STS line goes HIGH 200 ns after R/$\overline{C}$ goes LOW and returns low 1 µs after data is valid.

If conversion is initiated by a high pulse as shown in Figure 4b, the data lines are enabled during the time when R/$\overline{C}$ is HIGH. The falling edge of R/$\overline{C}$ starts the next conversion and the data lines return to three-state (and remain three-state) until the next high pulse of R/$\overline{C}$.

## CONVERSION TIMING

Once a conversion is started, the STS line goes HIGH. Convert start commands will be ignored until the conversion cycle is complete. The output data buffers can be enabled up to 1.2 µs prior to STS going LOW. The STS line will return LOW at the end of the conversion cycle.

The register control inputs, $A_0$ and 12/$\overline{8}$, control conversion length and data format. If a conversion is started with $A_0$ a full 12-bit conversion cycle is initiated. If $A_0$ is HIGH d a convert start, a shorter 8-bit conversion cycle results.

During data read operations, $A_0$ determines whether the t state buffers containing the 8 MSBs of the conversion resu ($A_0$ = 0) or the 4 LSBs ($A_0$ = 1) are enabled. The 12/$\overline{8}$ pi termines whether the output data is to be organized as two words (12/$\overline{8}$ tied LOW) or a single 12-bit word (12/$\overline{8}$ tied HIGH). In the 8-bit mode, the byte addressed when $A_0$ is contains the 4 LSBs from the conversion followed by four ing zeroes. This organization allows the data lines to be ov lapped for direct interface to 8-bit buses without the need external three-state buffers.

## INPUT CONNECTIONS AND CALIBRATION

The 10 V p–p and 20 V p–p full-scale input ranges of the AD1674 accept the majority of signal voltages without the for external voltage divider networks which could deteriora accuracy of the ADC.

The AD1674 is factory trimmed to minimize offset, linearit and full-scale errors. In many applications, no calibration t ming will be required and the AD1674 will exhibit the acc limits listed in the specification tables.

In some applications, offset and full-scale errors need to be trimmed out completely. The following sections describe th correct procedure for these various situations.

## UNIPOLAR RANGE INPUTS

Figure 6 illustrates the external connections for the AD167 unipolar-input mode. The first output-code transition (from 0000 0000 0000 to 0000 0000 0001) should nominally occur an input level of +1/2 LSB (1.22 mV above ground for a 1 range; 2.44 mV for a 20 V range). To trim unipolar offset t this nominal value, apply a +1/2 LSB signal between Pin 1 ground (10 V range) or Pin 14 and ground (20 V range) and just R1 until the first transition is located. If the offset trim not required, Pin 12 can be connected directly to Pin 9; the resistors and trimmer for Pin 12 are then not needed.

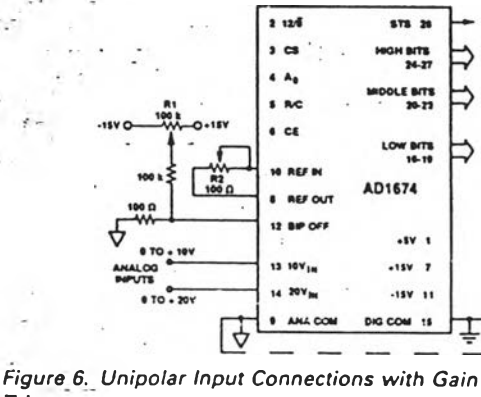



*Figure 6. Unipolar Input Connections with Gain and C Trims*

The full-scale trim is done by applying a signal 1 1/2 LSB b the nominal full scale (9.9963 V for a 10 V range) and adjus R2 until the last transition is located (1111 1111 1110 to 111 1111 1111). If full-scale adjustment is not required, R2 shou be replaced with a fixed 50 Ω ±1% metal film resistor. If R OUT is connected directly to REF IN, the additional full-sc error will be approximately 1%.

## BIPOLAR RANGE INPUTS

The connections for the bipolar-input mode are shown in Figure 7. Either or both of the trimming potentiometers can be replaced with 50 Ω ± 1% fixed resistors if the specified AD1674 accuracy limits are sufficient for the application. If the pins are shorted together, the additional offset and gain errors will be approximately 1%.

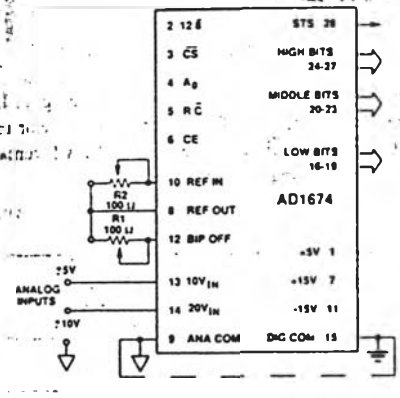



*Figure 7. Bipolar Input Connections with Gain and Offset Trims*

To trim bipolar offset to its nominal value, apply a signal 1/2 LSB below midrange (−1.22 mV for a ±5 V range) and adjust R1 until the major carry transition is located (0111 1111 1111 to 1000 0000 0000). To trim the full-scale error, apply a signal 1 1/2 LSB below full scale (+4.9963 V for a ±5 V range) and adjust R2 to give the last positive transition (1111 1111 1110 to 1111 1111 1111). These trims are interactive so several iterations may be necessary for convergence.

A single-pass calibration can be done by substituting a negative full-scale trim for the bipolar offset trim (error at midscale), using the same circuit. First, apply a signal 1/2 LSB above minus full scale (−4.9988 V for a ±5 V range) and adjust R1 until the minus full-scale transition is located (0000 0000 0001 to 0000 0000 0000). Then perform the gain error trim as outlined above.

## REFERENCE DECOUPLING

It is recommended that a 10 μF tantalum capacitor be connected between REF IN (Pin 10) and ground. This has the effect of improving the S/(N+D) ratio through filtering possible broad-band noise contributions from the voltage reference.

## BOARD LAYOUT

Designing with high resolution data converters requires careful attention to board layout. Trace impedance is a significant issue. At the 12-bit level, a 5 mA current through a 0.5 Ω trace will develop a voltage drop of 2.5 mV, which is 1 LSB for a 10 V full-scale range. In addition to ground drops, inductive and capacitive coupling need to be considered, especially when high accuracy analog signals share the same board with digital signals. Finally, power supplies should be decoupled in order to filter out ac noise.

The AD1674 has a wide bandwidth sampling front end. This means that the AD1674 will "see" high frequency noise at the input, which nonsampling (or limited-bandwidth sampling) ADCs would ignore. Therefore, it's important to make an effort to eliminate such high frequency noise through decoupling or by using an anti-aliasing filter at the analog input of the AD1674.

Analog and digital signals should not share a common path. Each signal should have an appropriate analog or digital return routed close to it. Using this approach, signal loops enclose a small area, minimizing the inductive coupling of noise. Wide PC tracks, large gauge wire, and ground planes are highly recommended to provide low impedance signal paths. Separate analog and digital ground planes are also desirable, with a single interconnection point to minimize ground loops. Analog signals should be routed as far as possible from digital signals and should cross them (if necessary) only at right angles.

The AD1674 incorporates several features to help the user's layout. Analog pins are adjacent to help isolate analog from digital signals. Ground currents have been minimized by careful circuit architecture. Current through AGND is 2.2 mA, with little code-dependent variation. The current through DGND is dominated by the return current for DB11–DB0.

## SUPPLY DECOUPLING

The AD1674 power supplies should be well filtered, well regulated, and free from high frequency noise. Switching power supplies are not recommended due to their tendency to generate spikes which can induce noise in the analog system.

Decoupling capacitors should be used in very close layout proximity between all power supply pins and ground. A 10 μF tantalum capacitor in parallel with a 0.1 μF disc ceramic capacitor provides adequate decoupling over a wide range of frequencies.

An effort should be made to minimize the trace length between the capacitor leads and the respective converter power supply and common pins. The circuit layout should attempt to locate the AD1674, associated analog input circuitry, and interconnections as far as possible from logic circuitry. A solid analog ground plane around the AD1674 will isolate large switching ground currents. For these reasons, the use of wire-wrap circuit construction is not recommended; careful printed-circuit construction is preferred.

## GROUNDING

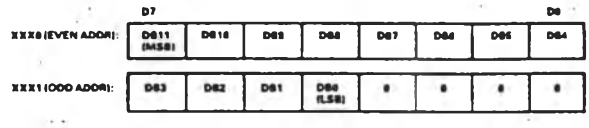
If a single AD1674 is used with separate analog and digital ground planes, connect the analog ground plane to AGND and the digital ground plane to DGND keeping lead lengths as short as possible. Then connect AGND and DGND together at the AD1674. If multiple AD1674s are used or the AD1674 shares analog supplies with other components, connect the analog and digital returns together once at the power supplies rather than at each chip. This prevents large ground loops which inductively couple noise and allow digital currents to flow through the analog system.

## GENERAL MICROPROCESSOR INTERFACE CONSIDERATIONS

A typical A/D converter interface routine involves several operations. First, a write to the ADC address initiates a conversion. The processor must then wait for the conversion cycle to complete, since most ADCs take longer than one instruction cycle to complete a conversion. Valid data can, of course, only be read after the conversion is complete. The AD1674 provides an output signal (STS) which indicates when a conversion is in progress. This signal can be polled by the processor by reading it through

an external three-state buffer (or other input port). The STS signal can also be used to generate an interrupt upon completion of a conversion, if the system timing requirements are critical (bear in mind that the maximum conversion time of the AD1674 is only 10 microseconds) and the processor has other tasks to perform during the ADC conversion cycle. Another possible time-out method is to assume that the ADC will take 10 microseconds to convert, and insert a sufficient number of "no-op" instructions to ensure that 10 microseconds of processor time is consumed.

Once it is established that the conversion is finished, the data can be read. In the case of an ADC of 8-bit resolution (or less), a single data read operation is sufficient. In the case of converters with more data bits than are available on the bus, a choice of data formats is required, and multiple read operations are needed. The AD1674 includes internal logic to permit direct interface to 8-bit or 16-bit data buses, selected by the 12/$\overline{8}$ input. In 16-bit bus applications (12/$\overline{8}$ HIGH) the data lines (DB11 through DB0) may be connected to either the 12 most significant or 12 least significant bits of the data bus. The remaining four bits should be masked in software. The interface to an 8-bit data bus (12/$\overline{8}$ LOW) contains the 8 MSBs (DB11 through DB4). The odd address ($A_0$ HIGH) contains the 4 LSBs (DB3 through DB0) in the upper half of the byte, followed by four trailing zeroes, thus eliminating bit masking instructions.




*AD1674 Data Format for 8-Bit Bus*

## 8085A INTERFACE

Figure 8 illustrates the use of the AD1674 operating in full-control mode from the 8085A. This provides an example of the implementation of the timing modifications necessary when using the AD1674 in place of an existing AD674A application, discussed in Table II and associated text. Figure 9 shows the convert start timing diagram; Figure 10 provides information on read timing.

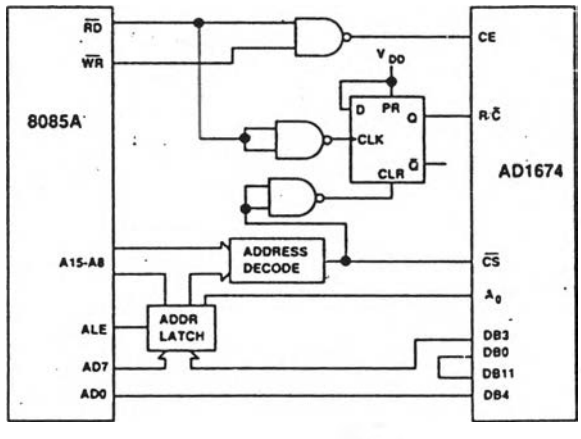



*Figure 8. 8085A – AD1674 with R/$\overline{C}$-Delayed Control Interface*

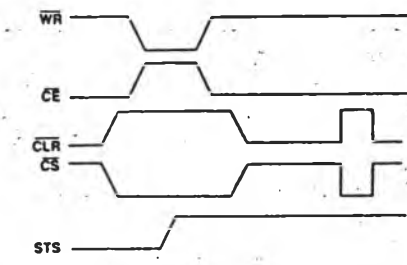



*Figure 9. 8085A Convert Start*

The convert start cycle starts when the WR signal goes LOW, forcing CE to go HIGH. With $\overline{CLR}$ signal LOW prior to this, R/$\overline{C}$ is set LOW. When $\overline{CLR}$ goes HIGH, R/$\overline{C}$ will remain LOW until the next rising edge of CLK.

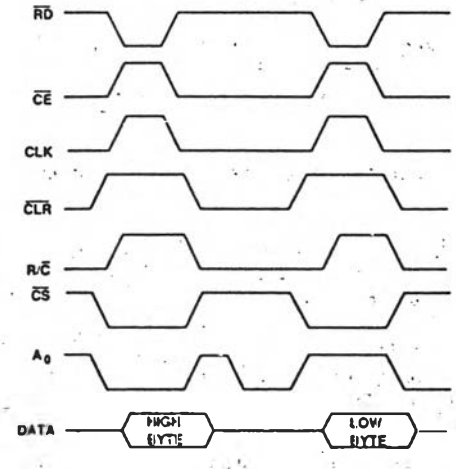



*Figure 10. 8085A Read*

The High Byte is read first. The Read cycle starts when $\overline{RD}$ goes LOW, causing CE to go HIGH. $\overline{CS}$ is already LOW, making $\overline{CLR}$ and PR HIGH on the D-flop. This causes R/$\overline{C}$ to go HIGH on the rising edge of CLK. R/$\overline{C}$ will not go LOW until $\overline{CS}$ goes HIGH, forcing $\overline{CLR}$ to go LOW thus putting the D-flop in a steady state of Q LOW. The cycle repeats for the Low Byte read.

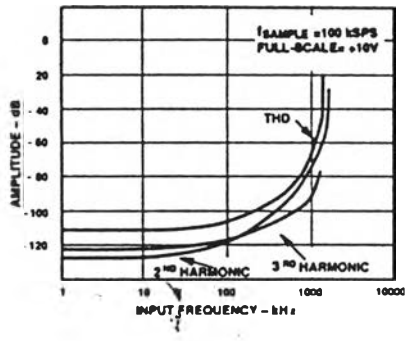



Figure 11. Harmonic Distortion vs. Input Frequency

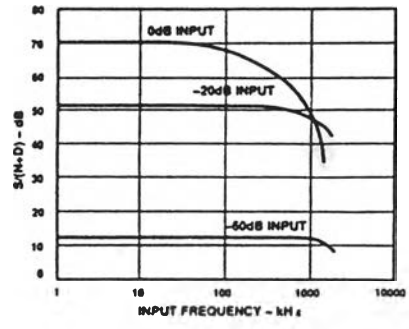



Figure 12. S/(N+D) vs. Input Frequency and Amplitude

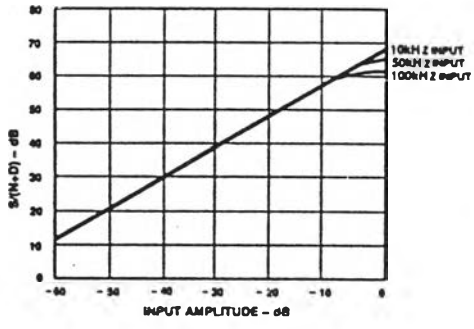



Figure 13. S/(N+D) vs. Input Amplitude

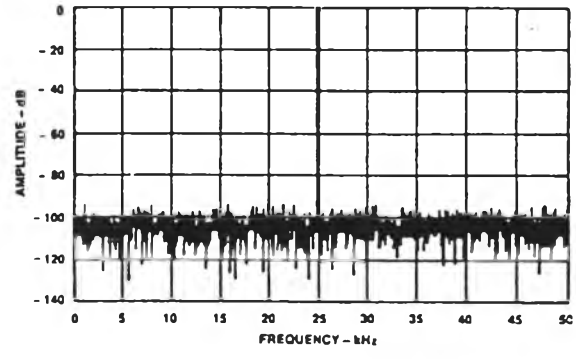



Figure 14. Nonaveraged 2048 Point FFT at 100 kSPS, $f_{IN}$ = 25.049 kHz

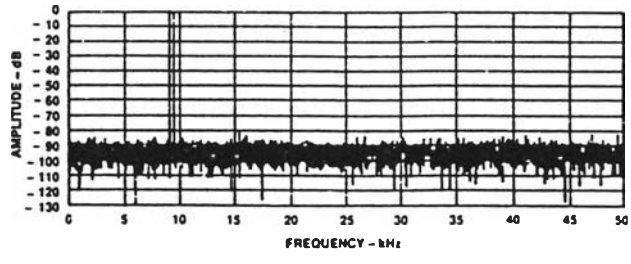



Figure 15. IMD Plot for $f_{IN}$ = 9.08 kHz (fa), 9.58 kHz (fb)

# CURRICULUM VITAE

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