CHAPTER V

SYSTEM DESIGN AND CALIBRATION RESULTS

The previous chapters described the general information for observation and instrumentation for a small radio telescope system which is controlled by a computer. This chapter is oriented to the process of design and construction of the equipment to accomplish the final purposes. The calibrations for many part and the result are also provided in this chapter.

General Description of the System

The radio telescope system which is devised for the thesis can be written in block diagram as shown in Fig 5.1. The rudimentary function of each part can be described as follow.

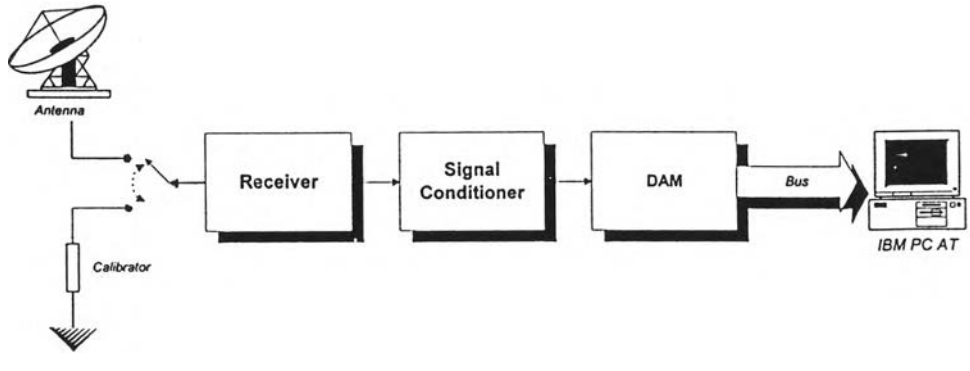

Fig 5.1 Radio telescope system block diagram.

The signal from the antenna is fed through the superheterodyne receiver. Then, the RF signal from antenna is detected and its frequency is converted to the DC audio frequency with the considerable gain. Sometimes, antenna is replaced with the fixed resistor of the same impedance to calibrate the internal noise of the receiver. Afterwards, the audio output is fed through the Signal Conditioner (SC), in which the gain and offset can be adjusted to the proper value by the aids of the differential input properties of the embedded instrumentation amplifier.

The signal is then fed through the Data Acquisition Module (DAM). The amplification is occurred again by another instrumentation amplifier in DAM. The frequencies above the Nyquist's frequency of the amplified signal are filter out by the anti-aliasing filter which is arranged to have the unity gain for the pass-band. Finally, the analog signal is converted to binary code by the 12-bit ADC which is controlled by interrupt scheme by the PC. However, the control of the ADC have to be supported be many digital components such as the sampling rate generator. The port numbers of them are decoded individually in DAM and the separation for the other peripheral port attached in the PC is decoded at the AT prototype card.

The antenna is the log-periodic dipole type with directivity about 18 dB (see in the latter section) and operation frequency is between 100 - 120 MHz which is devised by Mr. Chaiwat Kittinunprakorn for his senior project course (ชัยวัฒน์, 2536).

The receiver is the adapted from the commercial FM Tuner of ROY HIFI SERVICE. However, SC, DAM and AT prototype card is originally designed and constructed to serve the functions as the previous description. The schematic diagrams of those parts

can be provided in the Appendix C and the brief discussion of design concept and functions are appear in the following sections.

AT Prototype Card

The AT prototype card is the extension card attached directly to the PC/AT slot. It serve as the digital buffer and provide the sufficient control signals for 16-bit parallel interfacing with the original prototype device.

The parallel interfacing is more flexible than the serial interfacing such as MOUSE or MODEM which the accessible port number, transfer rate and the transfer protocol are the limitations of this methods. However, The parallel interfacing require full 16-bit data bus and other control bus to interconnect with the bus system for the specific devices, in contrast to the serial interfacing which only requirement is a wire for data transmission and some wires carrying the control signals. Basically, the serial interfacing is based on the parallel interfacing.

The port assignment for prototype card for IBM PC/AT and the compatible is confined in 300H-31FH. From experiment, only the port occupy the even number can be used for 16-bit interface. The MSB byte can not be activated if the 16-bit interfacing is assigned for port with odd number. Since the architecture of the PC AT also support the 8-bit extension card, the slots is physically divided in two part. In the interface aspect, it is possible to consider there are two part, one for the lower byte which is the same consideration as 8-bit interface and the other for the higher byte which is the complement for 16-bit interface. The block diagram for the AT prototype card can bee seen in Fig 5.2

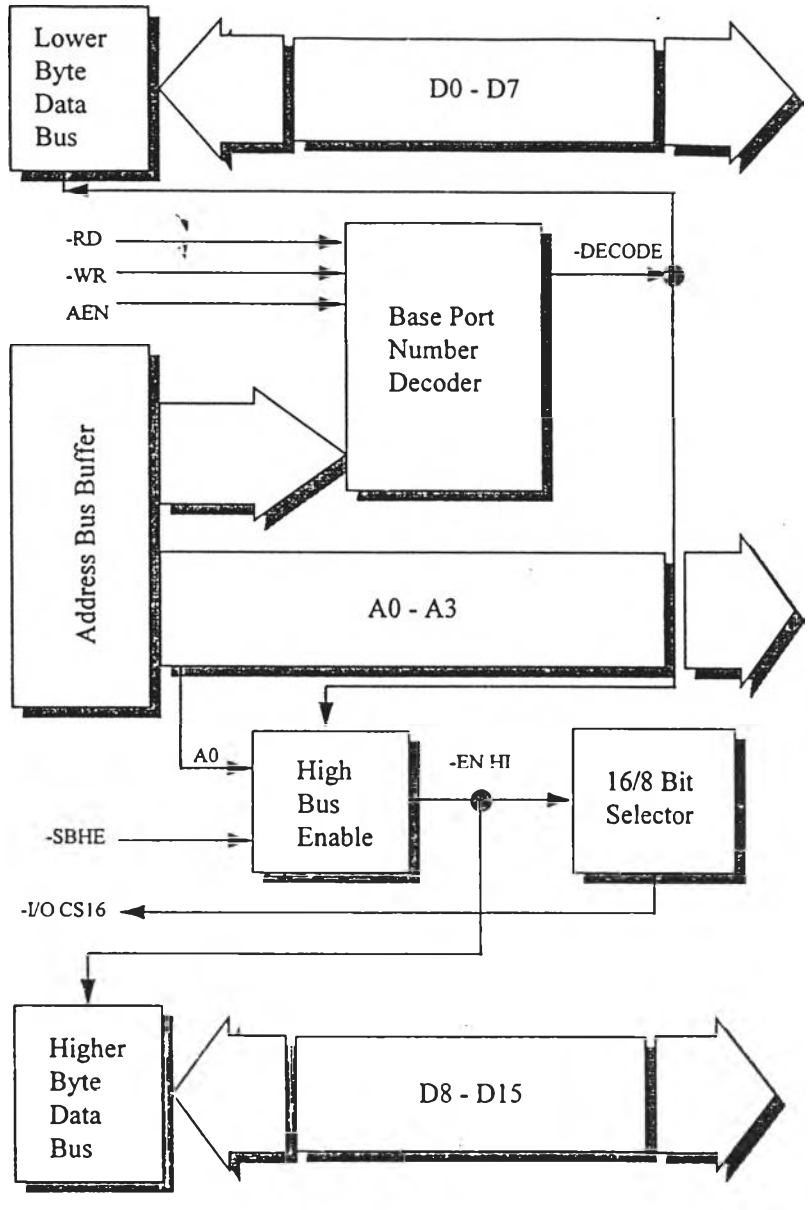

Fig. 5.2 Block diagram for AT prototype card.

For the 8-bit interface, The data bus buffer for the lower byte will be activate only when the signal to indicate the transfer data, i.e., -RD or -WR have to be sent from the CPU. The Address Enable (AEN) signal have also decoded since this signal indicate the data transfer via port to CPU rather than to memory in DMA process. This AEN have to hold the "low" state for the port transfer. Moreover, the ports

number for the devices attached to this card have to be confined in 300H-31FH (32 Port) which is decode by the binary value of data bus. By the addressing A5-A9 of the address bus, the confinement of the port number can be accomplished. It is more convenient to allow an devices attached to the prototype card can access many ports with common basis port number (e.g. 300H or 310H) than independent decode for each individual ports in that device. Hence it is flexible to use the A4 of the address bus to separate the port into two group. Each group occupies 16 port numbers and can be selected by set jumper in the card. The previous control signals, have to be used to generate pulse, called -DECODE, to activate the data buffers . For 8-bit interface, the scheme is complete by attached to the enable pin of the data buffer for lower byte transfer.

There are some additional consideration about 16-bit interfacing. The signal indicating the full 16-bit have to generate. The CPU will sent negative pulse called the Bus High Enable (-SBHE). It have to be encode with the A0 from address bus for restriction of the even port ,and the -DECODE signal for bus interface to generate the -EN HI pulse to activate the data buffer for higher byte. This signal will be encoded with a logical selector for 8- or 16-bit to generate input signal -I/O CS16 to the CPU for indicate the type of interfacing. Normally the -I/O CS16 have the "high" state which is automatically supported the 8-bit interfacing. This signal have to be "low" when the 16-bit interface is occur. In the PC/AT Technical Reference, the simple voltage level according to logic state is sufficient with no any decoder circuit for the -I/O CS16, but from experiment with the compatible version, The direct assignment may cause the problem in the bootstrap process.

Data Acquisition Module

The Data Acquisition Module (DAM) is rather complex system. It is designed to support many form of data transfer. Not only the conversion between analog and digital signal but also for normal digital data transfer is also supported. DAM have the programmable timer to generate the accurate sampling signal for ADC or the strobe signal for ADC 's reconstruction. Thus, the rate generating signals are programmed and independent on the CPU speed.

Since the complexity of the instrument, the modular design concept should be applied. Some module will be implemented to the main board. For more flexible, the PCB layout of the main board is designed to support the "overdrive" of some modules. Each module will be constructed in an individual PCB with the pins matched to the socket in the main board. For example, the ADC module have a socket in the main board with a certain pins' assignment. The socket can be attached to any ADC PCB module with the same pin assignment with the socket's pin. The ADC module can be afterwards designed for any resolution. The 12-bit ADC module may be easily replaced with the 16-bit ADC with no reconstruction over all main board again.

At first, it should be considered the function and then draft block diagram for DAM. The block diagram for control signals in the DAM is shown in Fig. 5.3. There are four importance parts in DAM, say programmable timer, digital interfacing controller, A/D converter and D/A converter. The individual port numbers for each part are decoded by the decoder section. The programmable timer is controlled by the 8253 with the time base 2 MHz. There are three independent 16-Bit counters. The first

is assigned to generate the sampling signal for A/D converter. The second is for reconstruction the signal from the binary code by D/A converter and the last is for the external clock generations. Each counter have to program the function such as waveform and the counter word before used by sending the command bytes to the control port of 8253 (See Appendix D). The first two counter is program to mode 2 (rate generator). The counters are activated by the signal from port C of in the digital interface controller section.

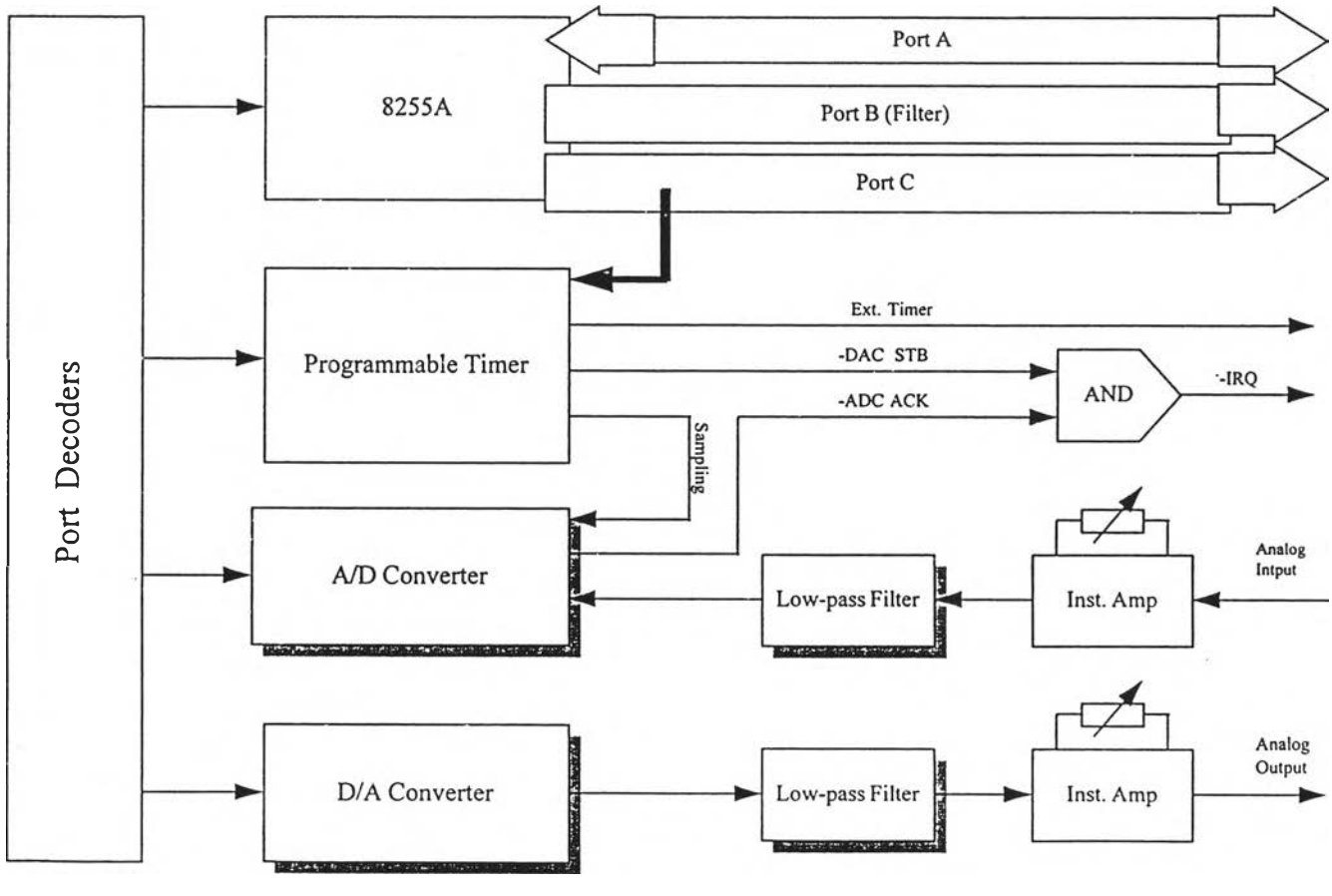

Fig 5.3 Block diagram for DAM.

The digital interface controller is used the 8255A. The chip have 3 ports, say A, B and C. The function of each port can be programmable as the same way of 8253. For the most flexible the bit C0 - C3 is dedicated to control the gate of the counter. The port A is for the external usage and port B be is routed to the filter for control the cut-off frequency which may be implemented in the future.

The A/D converter is construction in the form of plug-in module. There is the socket in the main board which provide the full 16-bit data bus, the sampling signal, acknowledge signals and the other important signals for interface. The analog input is amplified by the instrumentation amplifier with the certain gain and offset. The signal is filtered by anti-aliasing filter and fed through the A/D converter module. The A/D module start conversion when the sampling signal is sent from the counter. After complete conversion the acknowledge signal will send back to the CPU via interrupt process. The interrupt routine is written to transfer data to memory. The chip A/D converter which use in this observation is the 12-bit ADC1674. The chip use successive approximation method with the maximum conversion rate as 100 kSPS (sampling per second). The package is also include sample hold circuit. The mode of operation is free-running and unipolar as described in Appendix D.

On the other hand, DAM provide the D/A converter which support the reconstruction signal from the storage data. The scheme of the conversion start with the ADC STB signal from counter which the rate is programmed corresponding to sampling rate of the original signal is sent to the IRQ of the CPU. The routine is written to send the data in a location in memory to the port. The analog output signal

from DAC is filtered at the Nyquist's frequency and amplified by adjustable instrumentation amplifier with trimmed offset.

The filter and the instrumentation amplifier are designed in the same way for both analog input and output. The filter is designed to be modules but the instrumentation amplifier is implemented in the main board. The filter which we used is second order low-pass filter with the fixed cut-off frequency of 64 Hz (a half of the sampling rate).

The instrumentation amplifiers is designed as the analog buffer to separate the external source from DAM. The gain are adjustable. The both differential inputs can be selected to be external, ground or DC voltage which is internally trimmed by potentiometer. This arrangement of input is designed for the flexibility of applications.

Signal Conditioner

Although DAM have support the differential input signal which provide the adjustable offset, the precise monitor and fine adjust for the offset is the requirement for some small signal measurement. The signal conditioner (SC) is designed to support the previous functions. Not only the offset but the differential gain of SC can be adjustable. It is designed to be directly attachable to the analog input of DAM. SC can be used for adjust the offset and gain to confine the signal to the range of ADC, on the other hand it may be used for adjust DC level of DAC. The block diagram of SC is shown in Fig 5.4.

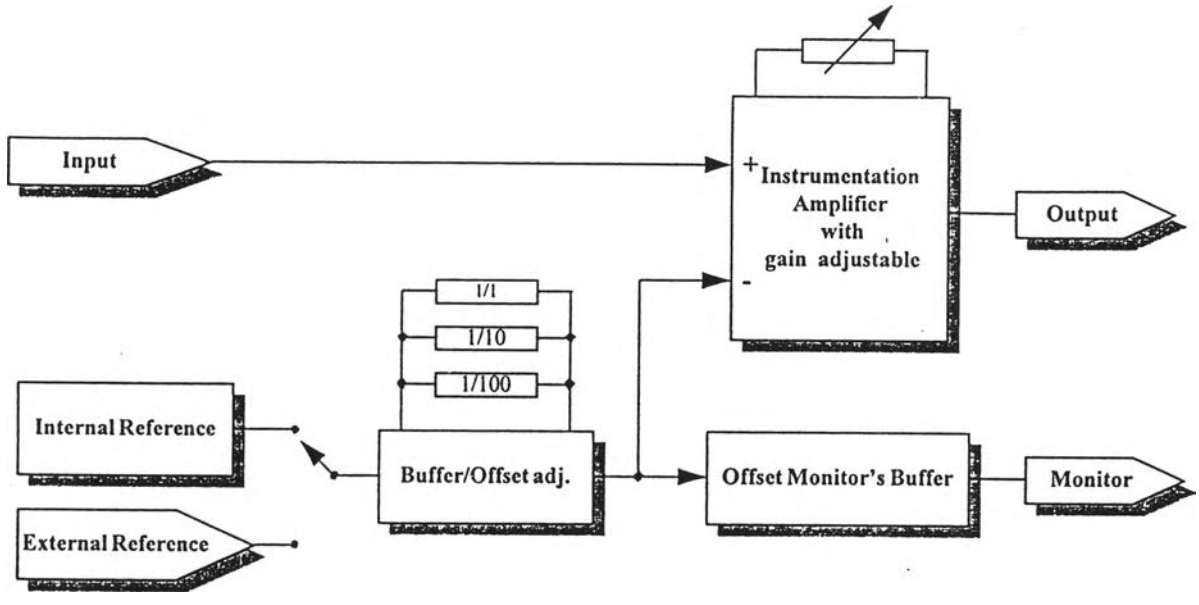

Fig. 5.4 Block diagram of the Signal Conditioner.

SC can be divided in two main part, the adjustable gain amplifier and the offset level adapter. The adjustable gain amplifier is devised from the instrumentation amplifier circuit as the analog input buffer of DAM. The gain is trimmed to 1,2,5,10,20,50 and 100 and selected by the push-button and rotary switch. The push-button is used to select gain to be unity or higher which are defined by the position of the rotary switch. The instrumentation amplifier have the two differential input one for the input signal and the other for offset level adapter. The source of offset level can be selected from the external source and the internal DC. source. The offset signal is fed through the offset buffer and can be trimmed by external potentiometer which is arranged into three gang with difference maximum ranges, say 1/1, 1/10 or 1/100 of the offset source. The output from each gang will be combined to the offset level of the instrumentation amplifier. Hence fine tune function for the offset is accomplished.

If the offset have to be monitored, the analog buffer have to be inserted between the offset wire and the voltage monitor equipment. From the experiment, a small drift of the offset can be occurred when the long time operation.

Antenna Pattern Measurement

From the Chapter II, we concentrate in the power pattern rather than the physical structure of the antenna. From chapter III, we can see that the most antenna properties can be induced from the pattern. Hence, it is important to estimate the pattern from measurement as described in the chapter III.

The dimension of the used log-periodic antenna refer to the Fig. 3.-- is shown in Table 5.1

n	l_n(m)	s_n(m)
1	1.019	0.362
2	1.082	0.384
3	1.148	0.408
4	1.219	0.433
5	1.294	0.459
6	1.374	0.488
7	1.458	0.518
8	1.548	0.550
9	1.644	0.583
10	1.745	-

Table 5.1 Dimension for each elements of the used log-periodic antenna (ชัยวัฒน์, 2536).

The data from measurement of the log-periodic dipole antenna in E-Plane and H-Plane at 110 MHz is shown in Table 5.2. and Table 5.3 respectively. The data is measured by moving the transmitter every 10 degree around the fixed antenna and the signal is fed through the radio telescope system and average over 30 second. The measurement operate at the midnight to prevent the interference of the man-made noise. The separation between the antenna and the transmitter is 9 m (the minimum distance is 2.24 m). The angle for both plane refer to the main beam direction of the theoretical antenna and the angle will be adjusted to the standard notation afterwards.

Angle (degree)	Power (nW)
-170	5.678
-160	5.678
-150	5.678
-140	5.795
-130	10.143
-120	0.718
-110	0.179
-100	0.082
-90	0.368
-80	0.399

-70	2.057
-60	0.167
-50	0.086
-40	0.038
-30	67.973
-20	111.935
-10	2.950
00	2.348
10	589.449
20	3743.760
30	2735.709
40	2.950
50	111.935
60	67.973
70	0.038
80	0.086
90	0.167
100	2.057
110	0.400

120	0.368
130	0.0822
140	0.178
150	0.718
160	10.143
170	5.795
180	5.678

Table 5.2 The measurement data for E-Plane of the log-periodic dipole antenna.

Angle (degree)	Power(nW)
-170	3.144
-160	3.144
-150	1.217
-140	0.323
-130	2.174
-120	2.348
-110	17.508
-100	0.471

-90	0.054
-80	0.022
-70	0.072
-60	0.277
-50	2.682
-40	26.848
-30	16.762
-20	189.263
-10	136.121
00	8682.252
10	9852.293
20	6932.883
30	136.121
40	189.263
50	16.762
60	26.848
70	2.683
80	0.277
90	0.072

100	0.022
110	0.05
120	0.471
130	17.508
140	2.348
150	2.175
160	0.323
170	1.217
180	3.144

Table 5.3 The measurement data for H-Plane of the log-periodic dipole antenna.

Since the data are discrete, the interpolation should be applied for each plane. It is useful to note that the principal axis of the measured pattern may not coincide with the principal axis in the theoretical antenna, which is usually coincided with the orientation of physical structure because it difficult to construct the perfect antenna in the real world. Some measure have to be used to compensate in real situation.

The complete 3-dimension pattern from each principal-plane should be obtained by the equally contribution of each plane. The best approximation and reasonable is the multiply each plane together which is

$$P_n(\theta,\phi) = P_n(\theta) * P_n(\phi) \qquad (5.1)$$

where $P_n(\theta,\phi)$ = normalized power pattern of an antenna

$P_n(\theta)$ = normalized power pattern along the vertical direction

$P_n(\phi)$ = normalized power pattern along the horizontal direction

The result is equivalence to the multiply of the measured power in each corresponding component of the direction and normalized by the factor which the multiplication of the maximum value in each direction .

The beam sold angle Ω_A of the antenna will be evaluated after the $P_n(\theta,\phi)$ is found by numerical process which is discussed previously. By the definition (3.1), the beam solid angle can be found by surface integration over the solid angle 4π of the normalized power pattern. Also the two dimension numerical integration is applied. The detail information of the two dimension mid-point integration which is used in this thesis is provided in the Appendix A.

By mean of the equation (3.4) and (3.8) the directivity D and the effective aperture, Ae are calculated respectively.

The result for log-periodic dipole antenna can be seen in 3-D diagram for linear and logarithmic scale can be seen in Fig. 5.5 and Fig. 5.6. The diagram is the result from the analysis by the program BEAMANL.PAS as Appendix B.

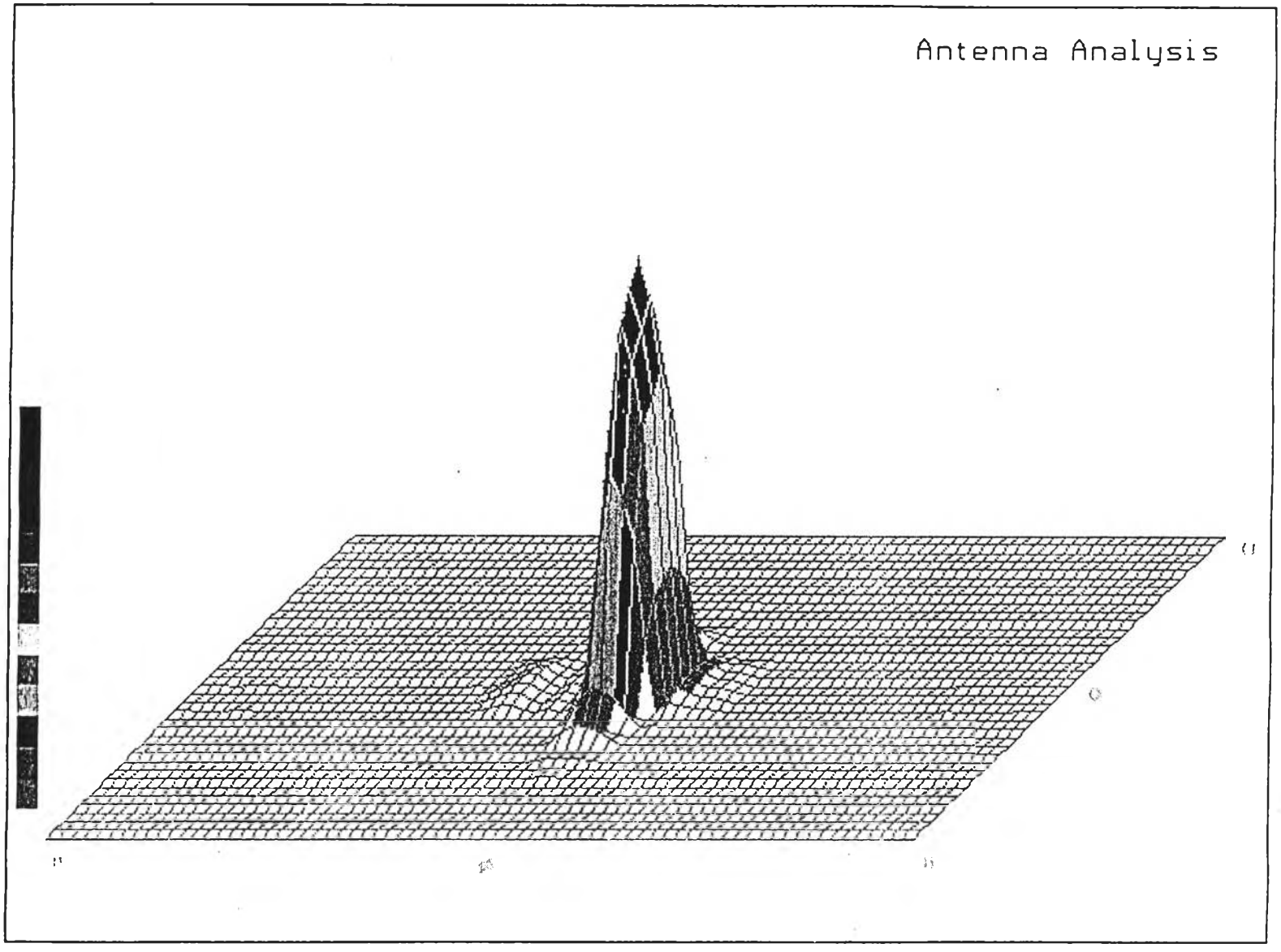

Fig. 5.5 3-D log-periodic dipole pattern in linear scale.

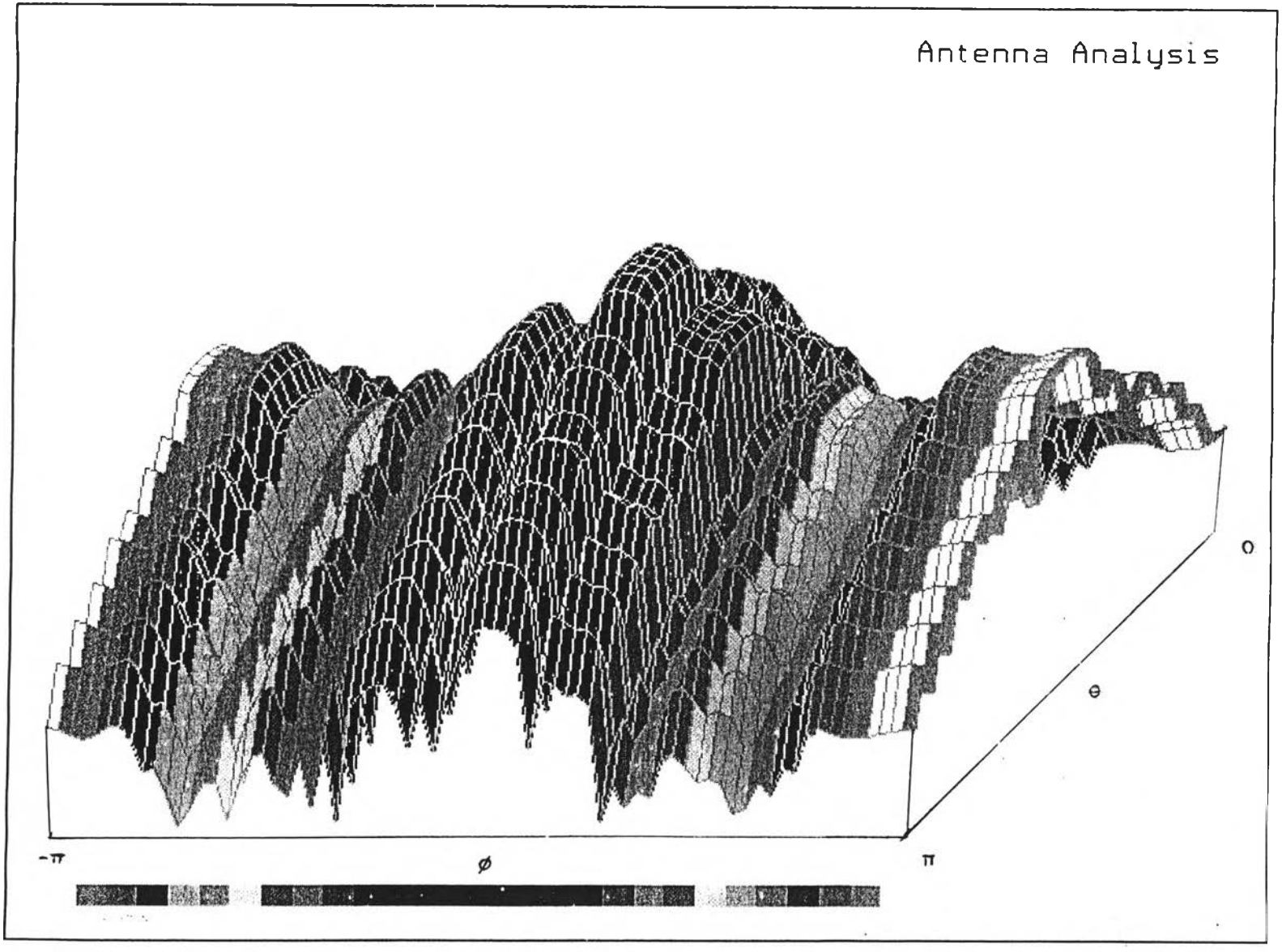

Fig. 5.6 3-D log-periodic dipole pattern in logarithmic scale.

Hence, the results when the numerical integration perform on the resolution 0.5^{o} x 0.5^{o} are

Ω_A = 0.16931256512143 sr

A_e = 43.93068242508353 m^2

D = 74.21995293348119

G = 18.70520674605382 dB

The main beam deviation are 20^{o} and 10^{o} for E-Plane and H-Plane respectively. Comparing to the theoretical pattern in Fig 3.8 and the measured pattern in Fig 5.6, it can be seen that the both pattern are rather similar.

Receiver Parameters' Estimation

The used receiver is adapted from the commercial FM tuner. The tuner is the superheterodyne receiver which block diagram can be shown partially in Fig 5.7. The Tuner provide the front end and the back end circuit separately. The front end compose of the RF amplifier, the local oscillator and the mixer. The output voltage is the IF signal. Unfortunately, the gain of the front end is not available from specification and there is no equipment to measure, but it should be varied in power gain from 10 to 30 dB (or about 10 - 1000 in linear scale). We estimate the RF gain to be 20 dB (100 in linear scale) and the measured power should be varied in order of 0.01 to 10 from the exact value.

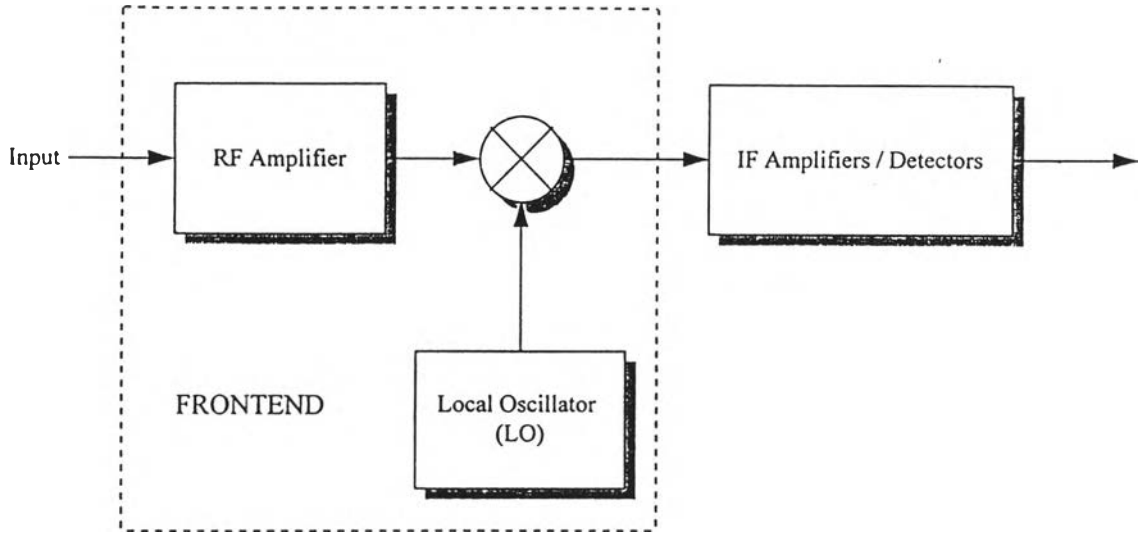

Fig. 5.7 Partial block diagram for the RF Tuner.

The IF signal is fed to the Integrated Circuit FM IF System HA1137 which is equivalent to IC CA3089, but different only in manufacturer. CA3089 contain the IF amplifier and the FM detector in its package. There are 3 stages IF amplifier. Each stage have a level detector and the IF signal from front end can be monitor by at the pin 13 (tuning meter out) which characteristic curve is shown in Fig 5.8.

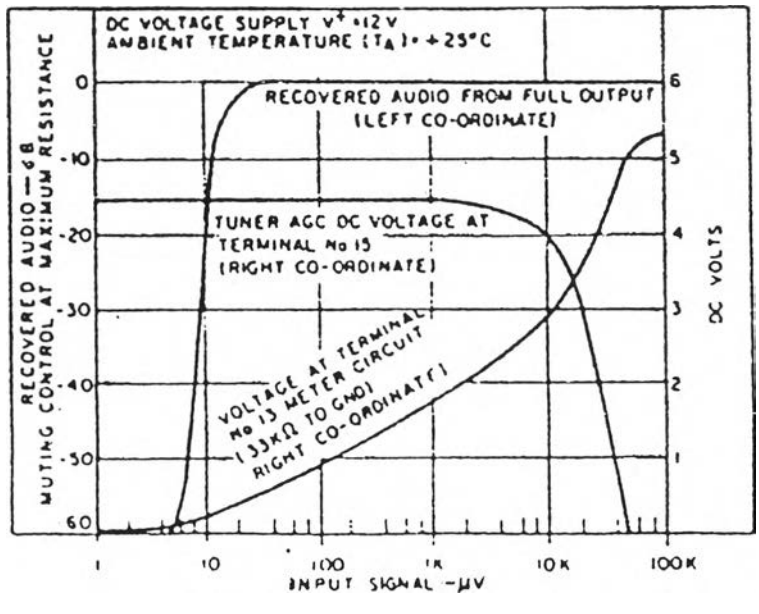

Fig 5.8 Characteristic curve of IF amplifier .

It is clearly that the curve is non-linear. The input signal is plot in logarithmic scale and the DC output is plot in linear scale. The Bode's plot is enlarger and the value of in y-axis is measure in centimeters with the marked value in the x-axis. For more precision, there are 4 times to measure and all data is averaged. By the calibration with the length of 6 V in the right side of the plot, the output voltage can be estimate. Since it is more convenient for the future software implementation to fit the input voltage to be function of the DC output voltage, the result is shown by opposite sense of the Fig 5.8 as Table 5.4.

This data is processed by the non-linear curve fit. From trial and error, it is found that the best model which satisfied the characteristic curve of the IF amplifier can be written in the form of

$$y(x) = \alpha k^{x^2 + \beta x} \qquad (5.2).$$

where y = IF input voltage level (V_i).

x = DC output voltage from pin 13 of CA3089

α, k, β = arbitrary constant.

The function is the same form of (A3.3) in Appendix A. By non-linear curve fit the coefficient of terms in the quadratic function corresponding to this curve can be written as

$a_0 = -5.3708$

$a_1 = 1.6547$

$a_2 = -0.1723$

This model have the standard deviation (square root of the collective residual) as SD = $5.37086056582795 \times 10^{-4}$. By the convert relation from (A3.4), the final result for the constants in (5.1) is

$\alpha = 4.2574 \times 10^{-6}$

$k = 0.6726$

$\beta = -9.6058$

Vo (V)	Vi (μV)
0.000	1.00
0.039	2.00
0.090	4.00
0.128	6.00
0.177	8.00
0.226	10.00
0.409	20.00
0.618	40.00

0.744	60.00
0.842	80.00
0.944	100.00
1.145	200.00
1.415	400.00
1.558	600.00
1.678	800.00
1.774	1000.00
2.045	2000.00
2.371	4000.00
2.592	6000.00
2.753	8000.00
2.887	10000.00
3.574	20000.00
4.673	40000.00
5.145	60000.00
5.284	80000.00
5.322	100000.00

Table 5.4 IF amplifier characteristic data.

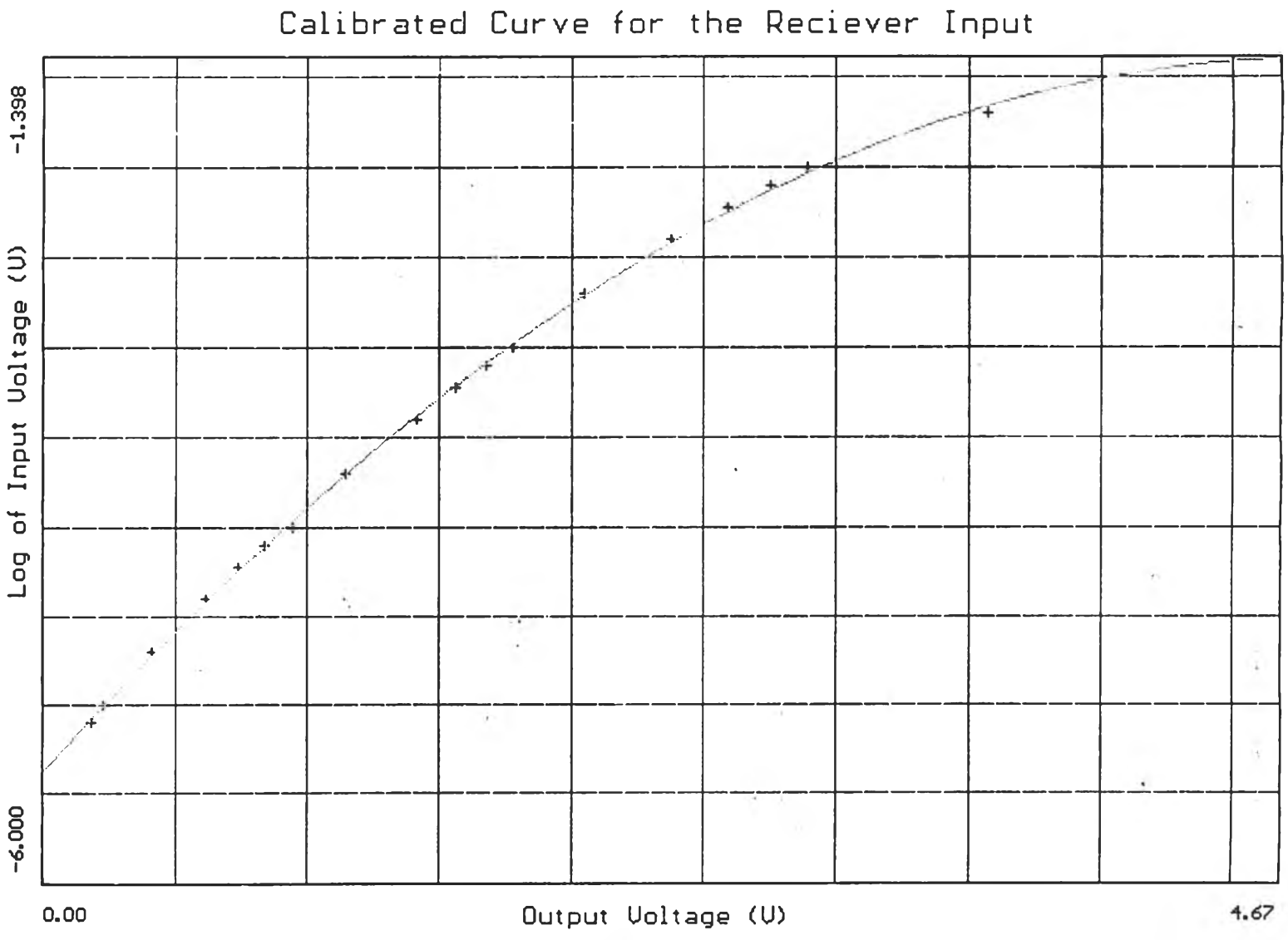

Fig. 5.9 Curve fit for IF amplifier compare to the original data.

Another consideration for the system is the predetection bandwidth of the receiver which is also the system bandwidth (because of the broadband property of the log-periodic dipole antenna). From the experiment, the output voltage will be decrease to the half-power point at the frequency 109.912 and 110.095 MHz, so the half-power bandwidth of the receiver operate at 110 MHz frequency is about 183 kHz.

Digital Low-pass Filter Test

However, the digital filter is well established in the last chapter, it is necessary to test the routine and define the proper parameter of the filter, e.g. the cut off frequency and the width of the Lanczos' window. The low-pass filter is implemented to the Pascal unit DFILTER.TPU (DFILTER.PAS for the source code). The detail can be seen in Appendix B.

To test the filter we define the functions as the input signals and sampling it. The form of the input signals are form by many way. To fit to the monitor display it is assumed that the horizontal scan represent a second or 600 pixel per sec. and the window have N = 20. The result of the test can be seen as follow.

At first, the common 5 Hz sinusoidal wave (dashed line) is applied to the filter. We assign the cut-off frequency to be 50 Hz. From Fig 5.10a, we can see that the filtered signal (solid line) is the same. If the cut-off frequency is set to 0.01 Hz for the same input signal, the input signal is vanished as shown in Fig 5.10b.

If the frequency of the input signal is near the cut-off frequency the effect of truncation for the infinite Fourier's series should be considered. The example can be

seen in Fig. 5.11. The cut-off frequency for both signal is 20 Hz. The input signal is 5 Hz (a) and 50 Hz (b).

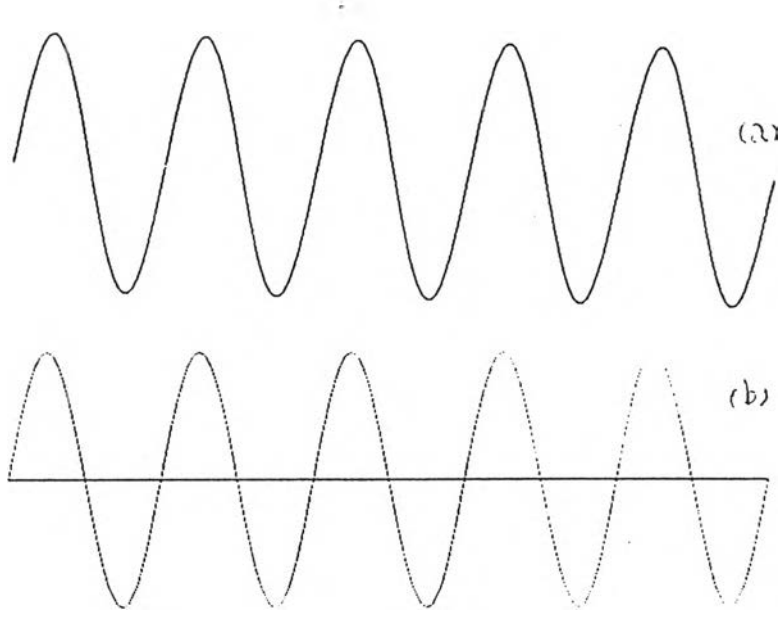

Fig 5.10 Effect of digital low-pass filter to the sinusoidal wave at frequency 5 Hz at the cut-off frequency 50 Hz (a) and 0.01 Hz (b).

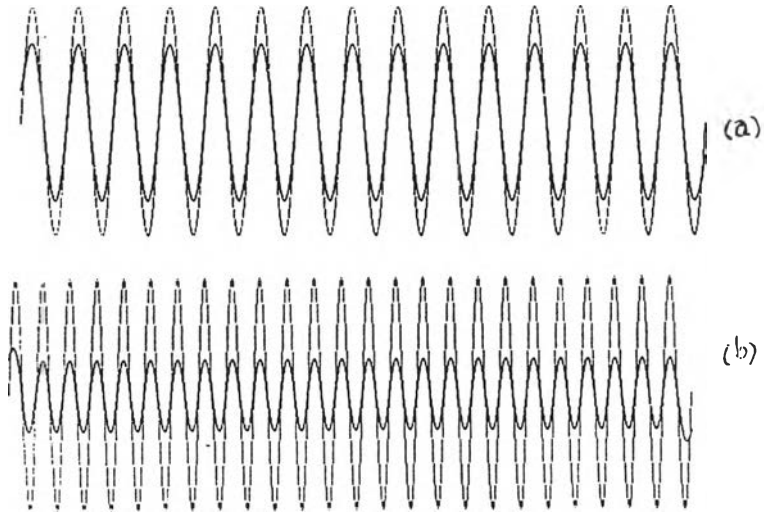

Fig 5.11 Effect of the truncation of the Fourier's series for the input signals of frequency near the cut-off frequency (20 Hz). The frequency of the input signal is 5 Hz (a) and 50 Hz (b).

If the signal is the composition of two sinusoidal waves with difference frequency, one below and the other is above the cut-off frequency. The result can be seen in Fig. 5.12. It can be seen the effect of the transition band from the truncation of Fourier's series.

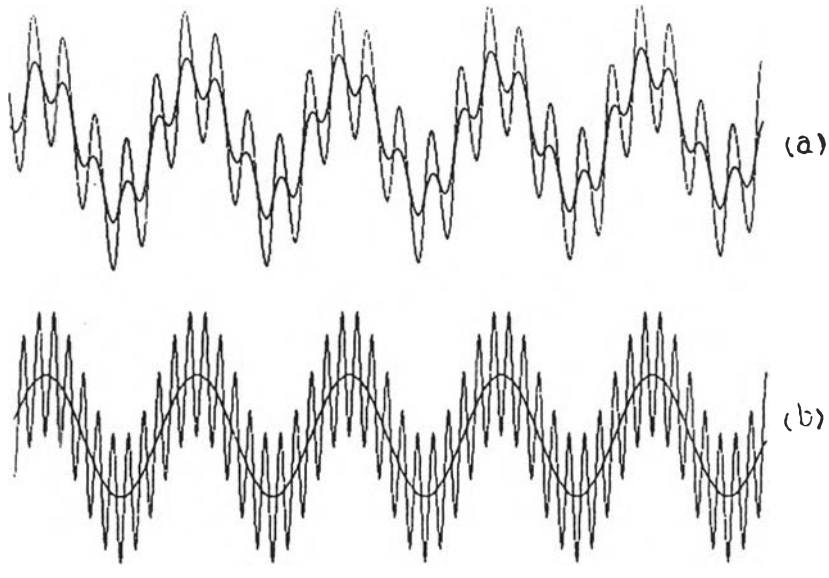

Fig 5.12 Effect of the filter for the signal of two frequency component and the cut-off frequency is 20 Hz. The frequency components of input signal are 5 and 25 Hz in (a) and 5 and 50 Hz in (b).

Hence, the digital filter is effective as we expected. However, the transition band of the filter as (4.28) should be considered.