QUALITY IMPROVEMENT OF PCBA MANUFACTURING PROCESS BY DMAIC APPROACH

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การปรับปรุงคุณภาพกระบวนการประกอบแผงวงจรโดยวิธีการดีมาอิก (ดี-เอ็ม-เอ-ไอ-ซี)

นางกุลชลี นราลัย

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The aim of this research is to improve the quality of PCBA manufacturing process of the case study company's a core product by focusing on reduction of high defect rate found at Surface Mount Assembly processes which were key assembly processes and mainly contributed the defects to the product. This is considered as Critical To Quality (CTQ) and high impact to the company performance as one of the company's balance score card. The theme of this study is to identify the AS IS quality problems by historical DPPMc chart overtime which the based line of defect rate was at 4804 DPPMc and to improve by adopting and deploying the DMAIC approach to the goal at 680 DPPMc.

To achieve that, various quality tools were systematically applied as working tools to each DMAIC phase. Top major defects were defined by Pareto Chart, the first rank defect which was the Non-wetting Soldering defect with >90% contribution was picked up for improvement priority. Causes of non-wetting soldering defects were determined by Cause & Effect Diagram and prioritized by FMEA technique with RPN number. The top three likely causes with highest RPN number were candidates and tested for significant effect by DOE technique. Solutions were achieved by optimized causing parameters (Stencil Aperture related, Reflow Peak Temperature and Reflow Time). Improvement results were verified significantly improved and achieved the goal. The on-going results were about 599 DPPMc (87.53% Improved) after improvement. Proper control mechanisms have been put in place and maintained.

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วิทยานิพนธ์ฉบับนี้มีวัตถุประสงค์ เพื่อทำการปรับปรุงคุณภาพของกระบวนการประกอบแผงวงจรของบริษัทศึกษาในหนึ่งผลิตภัณฑ์หลักของบริษัท ที่มีอัตราของเสียอยู่ในระดับสูงอย่างต่อเนื่องโดยมุ่งเน้นทำการลดอัตราของเสียที่กระบวนการ (Surface Mount Assembly) ซึ่งเป็นกระบวนหลักและ มีผลต่อการเกิดของข้อบกพร่องต่อผลิตภัณฑ์ ซึ่งส่งผลกระทบอย่างรุนแรงต่อคุณภาพ และผลงานของบริษัท แนวทางการศึกษาจะทำการระบุปัญหาคุณภาพในสภาพที่เป็นอยู่โดยใช้แผนภูมิรายงานอัตราของข้อบกพร่อง โดยอัตราข้อบกพร่องซึ่งถือเป็นระดับฐานก่อนทำการปรับปรุงจะอยู่ที่ 4804 DPPMc และทำการปรับปรุงโดยนำหลักการ DMAICมาใช้โดยมุ่งไปสู่เป้าหมายที่ระดับ 680 DPPMc.

เพื่อมุ่งสู่ผลสำเร็จ ได้มีการนำเอาเครื่องมือคุณภาพต่างๆ มาใช้อย่างเป็นระบบในแต่ละเฟสของ DMAIC ลำดับของข้อบกพร่องถูกแสดงโดยแผนภูมิพาเรโต โดยข้อบกพร่องอันดับหนึ่งซึ่งได้แก่ Non-wetting Soldering ซึ่งมีสัดส่วนมากกว่า90% ของทั้งหมดได้รับการเลือกเพื่อทำการปรับปรุงเป็นลำดับแรก โดยมีการใช้แผนภูมิเหตุและผลในการกำหนดสาเหตุที่เป็นไปได้ของปัญหา และจัดลำดับความสำคัญโดยใช้เทคนิคแผนภูมิการวิเคราะห์ข้อบกพร่อง/ FMEA และเลขลำดับความเสี่ยง (RPN) ในการเลือกตัวแปรที่น่าจะมีผลต่อข้อบกพร่อง มาทำการพิสูจน์ว่ามีผลอย่างมีนัยสำคัญหรือไม่ โดยใช้เทคนิคการออกแบบการทดลอง (DOE) ในการพิสูจน์ และได้แนวทางในการแก้ปัญหา สำหรับค่าของตัวแปรที่เป็นสาเหตุของปัญหาที่มีประสิทธิภาพ/ ภาวะที่ดีที่สุด (Stencil Aperture Related, Reflow Peak Temperature and Reflow Time). ผลการปรับปรุงได้รับการทวนสอบว่ามีความแตกต่างอย่างมีนัยสำคัญ และบรรลุเป้าหมาย ผลการติดตามหลังการปรับปรุงพบว่าอัตราข้อบกพร่องอยู่ในระดับ 599 DPPMc โดยเฉลี่ย (ดีขึ้น 87.53%) โดยกลไกของการควบคุมที่เหมาะสมได้มีการนำไปปฏิบัติและ คงรักษาไว้

ศูนย์ระดับภูมิภาคทางวิศวกรรมระบบการผลิต ลายมือชื่อนิสิต Kulchalee .....

สาขา : วิชาการจัดการทางวิศวกรรม ..... ลายมือชื่อ อ.ที่ปรึกษาวิทยานิพนธ์หลัก .....

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Contents

Page

Page

Page

List of Tables

List of Figures

Page

CHAPTER I

INTRODUCTION

There is an increasing of business challenges and competition throughout all businesses and industries including the manufacturing industry. The better in quality and more profitable with competitive advantages are key drivers. Long term sustainability and profitability with pleasing customers and stakeholders with good quality products and service, competitive cost and effective operations are still considered as the key success factors. To achieve those, the quality concepts/ philosophy and tools are required to support for achievement. The traditional quality tools and techniques are still valid and workable but required more strategic, organized and systematic process and approach.

This research adopts the six sigma quality philosophy but mainly focus on DMAIC approach as a theme for strategic implementation of the quality improvement.

1.1 Case Study Company and background of the research

The company in this case study is an Electronics Manufacturing Service provider (EMS). It is a Thailand Contract Manufacturer and a subsidiary of one of the top ten EMS provider in the world. The company's main business is the manufacturing electronics products and providing setrvices to Original Equipment Manufacturers (OEMs) of following industries.

- Computer and related products for business enterprises
- Telecommunication equipment
- Industrial control equipment
- Medical devices
- Testing and instrumentation products

The major manufacturing services offered are

- Print Circuit Board Assembly (PCBA) and Test
- Flex Circuit Assembly & Test
- Mechanical Assembly and Box Build
- System Assembly & Test

Due to the nondisclosure agreement and related concerns, the company is named "ABC Electronic" or ABC in short throughout the research. The research is focused on the Printed Circuit Board Assembly processes specific at the surface mounting process as the front end as the key process of Printed Circuit Board Assembly (PCBA).

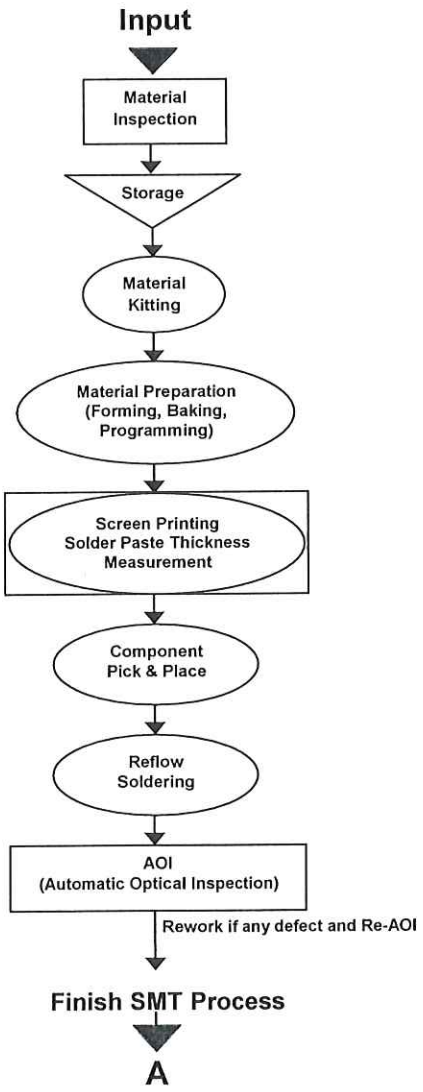
The PCBA is a main part in various types of electronic products of the company. In a single electronic product, it may consist of one or multiple PCBAs inside performing functions according to intended design. Like a box build/ finished product assembly, the Print Circuit Board Assembly is the main component. A box build product may consist of single PCBA or multiple PCBAs inside.

The PCBA assembly processes are core sub-assembly processes of the company business. The manufacturing of PCBA consists of multiple operations starting from material receiving up to the PCBA final inspection and testing. The PCBA is a kind of Electronic Assembly which is about how to assemble together a Print Circuit Board and multiple of electronic components to form a working, reliable appliance.

The electronics assembling requires that a number of methods of printed circuit board manufacturing be available for the purpose of combining components. Typically, combinations of two or more of these methods are used to create single assembly. (Brindley, 1993)

- Through-hole circuits
- Hybrid circuits
- Surface mounted circuits

The product under studying is the combinations of the Surface Mounted and Through-hole Components under multiple steps of manufacturing processes. The company generic manufacturing process flow is illustrated as figure 1.1. The manufacturing is the combination of automated machine and human to perform the tasks. The company needs to get good quality of PCBAs to make reliable products to deliver to the company's customers or OEMs and competes in the customer satisfaction in product quality to other competitors. The company has utilized manufacturing technologies and machines to relevant processes and applied some controls and quality measuring to critical processes. However, with each step of the manufacturing, it could generate its own variability and thus contributing to the overall defect rate.



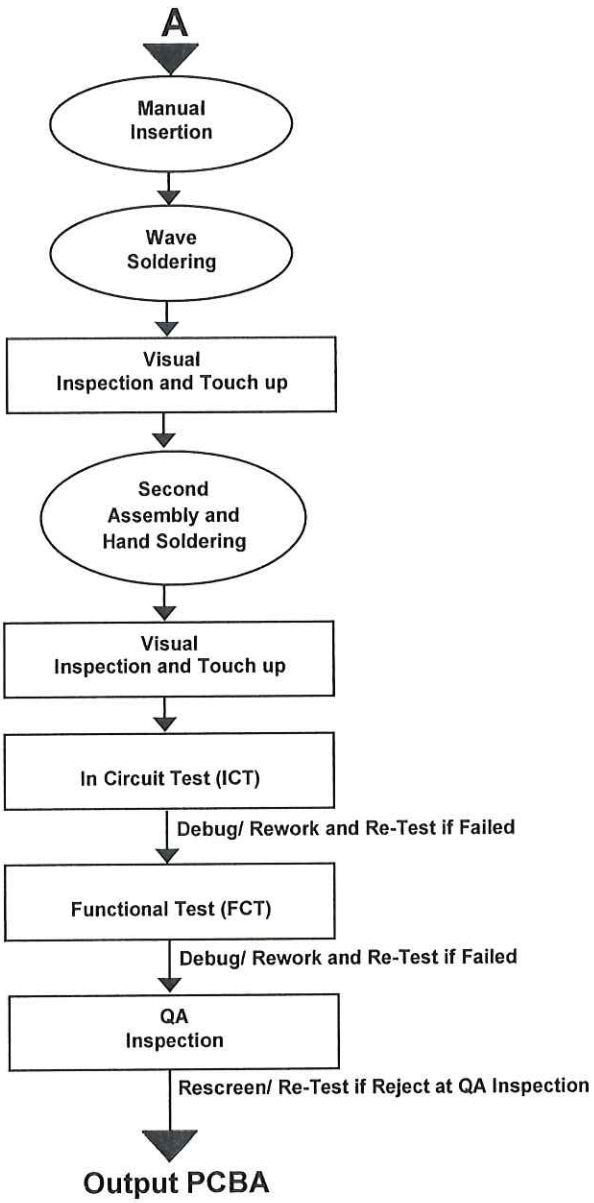


Figure 1.1 Generic PCBA Manufacturing Processes of the Company: ABC

To those concerned operations, the SMT processes which consist of the solder paste screen printing, component pick and place, reflow soldering are considered as key major processes mostly populate the components and contribute to the quality of PCBA and subsequently affecting/ being bottle neck to overall throughputs and the performance of next processes and overall efficiency and effectiveness of manufacturing. The quality of SMT process is detected by AOI (Automatic Optical Inspection) on the PCBAs out of Reflow soldering, measured as good or defect call,

recorded into the company data tracking, calculated to be the defect rate and reflected as one of key performance indicators of the company balanced score card which is under critical to quality (COQ) and the factory performance.

Among many products that the company has been running, the product AZY PCBA, see figure 1.2 is one of high runner and contributing to overall defect rate. The product had been started for production in the beginning of the year 2011and continued for high defect rate at surface mount processes and caused cost of poor quality on the rework tasks/ re-inspection and low throughput. According to the process performance data of the year 2011 (Q1-Q3'12), see figure 1.3, the defect rate of the Surface Mount Technology (SMT) processes of the product AZY was about 4804 DPPMc which was highly above the company target at 680 DPPMc (4.7 Sigma) according to the product category and complexity. This performance status was critical and essential to the company for the need of the breakthrough improvement strategy to reduce the defect and sustain the good process performance which quality improvement with DMAIC approach is required to be applied to the research study.

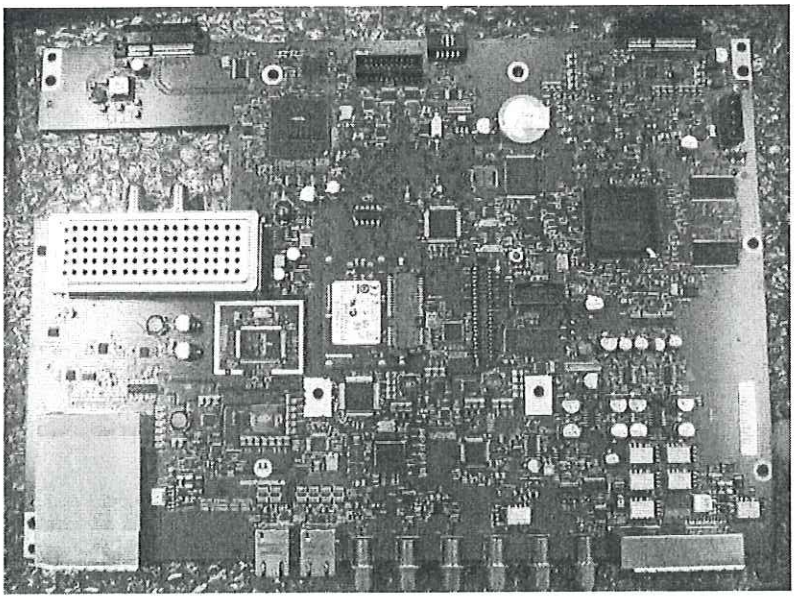
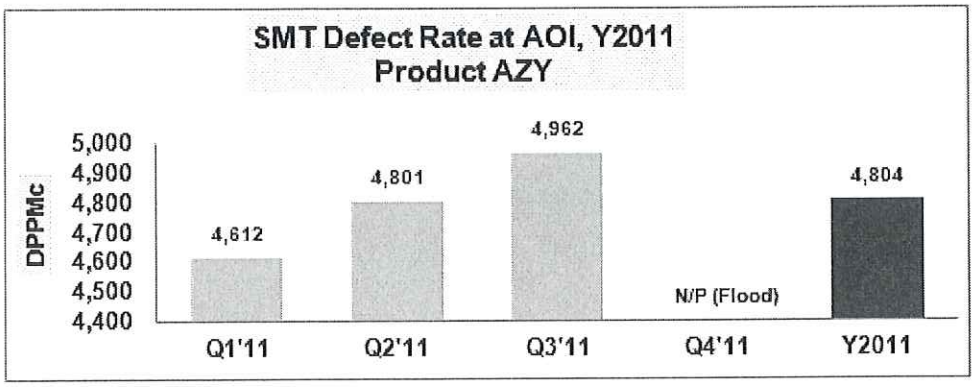


Figure 1.2 Product AZY PCBA



	Q1'11	Q2'11	Q3'11	Q4'11	Y2011
Total	1,133	1,124	1,391	N/P	3,648
Total Points	2,100,582	2,083,896	2,578,914	N/P	6,763,392
Defect Points	9,687	10,004	12,797	N/P	32,488
DPPMc	4,612	4,801	4,962		4,804

Figure 1.3 Historical SMT Process Defect Rate of the Product AZY of ABC Electronics

Different organizations may use different approaches, methodologies and tools for implementing a quality management program. Regardless of the methodology, approach, tool or the name of the improvement programs, each organization will certainly need a proper selection or combination of different approaches, tools and techniques in its implementation process as appropriate (Sokovic, M., Pavletic,D., Kern, P.K., 2010). This research considered to adopt DMAIC approach for the improvement program of the case study company with the following key reasons and requirements.

- Creating a system in problem solving

DMAIC is a systematic and structured approach for process and quality improvement. For academic point of view, although the general problem solving methodologies like PDCA (PLAN-DO-CHECK-ACT) and other basic tools can be used to fix existing problems, but there are differences among those generic tools and DMAIC approach on what and how it is deployed. The DMAIC is fact and data driven. It focuses on reducing the variations in the process by using statistical methods to define, analyse a business problem and seek for solutions then applied back to the business. The

hypothesis and experiment or proving is thought about and tested to find out what works and what to implement as main keys of success. Also in today business problem, the issue is quite complex and complicate, the typical PDCA or tools may not adequately work in this regard and they typically aim for resolution in short time like days, while the complex issue needs longer time and sophisticate approach to handle (Sokovic et.al., 2010). With the challenging of the business and high competition in the market and industry, the company really needs a system in problem solving and extending the best practice across organization to gain better performance and be more competitive.

- Getting Breakthrough Results

DMAIC approach yields significant or breakthrough improvement results. Based on literature reviews of improvement by DMAIC or Six Sigma approach, there are a number of researches that were done and proved significantly improved the results as listed on the chapter II Literature Review on previous works that support in this regard. (Achareeya, 2000), (Woraphoom, 2004), (Tsung, 2004), (Yang, 2008), (Nazaripooya, 2009), (Chulajata, 2011), (Matathil, Ganapathi, and Ramachandran, 2012), (Kumar, Satsangi and Prajapati, 2011), (Yamolyong, 2007)

1.2 Statement of Problems

The high defect rate and negative trend of SMT process performance caused impacts to the company in term of product quality, cost of poor quality and productivity. The company needs to do improvement to improve the quality performance/ reduce the defect rate at the SMT processes.

1.3 Objectives

The objective of this research is to reduce the defect rate/ improve the quality level at the SMT Processes of the PCBA manufacturing of the product AZY PCBA to meet the company target by DMAIC approach.

1.4 Scope of the Research

- The research focuses on the product AZY PCBA of the company ABC.
- The research aims for the quality improvement to reduce the defect rate detected at the inspection operation of the PCBA which is Auto Optical Inspection (AOI) by focusing on top defect(s) which is induced from either of the following processes where applicable;
  - Screen Printing Operation
  - Surface Mount Device Mounting
  - Reflow Soldering

1.5 Expected Benefits

- Reduced Defect rate and improved process performance/ product quality
- Reduced rework/ cost of poor quality
- Improved quality performance of subsequent processes
- Improvement Project base for other products
- Improved overall throughput/ productivity

1.6 Definitions

The related terms, terminologies are defined by which these terms and terminologies are used throughout the research as followings;

- Unit of the quality measure/ defect rate in this research is expressed in term of DPPMc.
- DPPMc stands for Defects Per Million Opportunities by components/ parts which the calculation is based on Total Number of Defects counted by the defect criteria on components found defects divided by Total Opportunities by the number of total components/ parts. (Total number of product units x opportunities i.e. number of components/ unit) then multiplied by 1,000,000 or [Total number of Defects/(Total number of products x number of part/unit)] X1,000,000

1.7 Methodology

- Research about related literatures, journals, Internet and research studies in which the information related to the research topic and contents.
- Review and study the researched information.
- Research about PCBA manufacturing processes and other related information.
- Gather the relevant data under selected processes and scope of study.
- Review and Analyze the collected data by DMAIC approach.

Define

- Identify the project that is measurable and critical to key indicators
- Define the improvement opportunity and the demands of the processes and customer.

Applied Techniques and Tools where appropriate:

Trend Chart, Bar Graph, Process Flow Diagram, SIPOC (Supplier, Input, Process, Output, Customer), Pareto, Gantt Chart etc.

Measure

- Measure the current level of quality into Sigma Level/ suitable measure.
- Pinpoint the area/ what contributes problems. It forms the basis of the problem solving.
- Identify project defects and all possible and potential scope for such problems.
- Confirm validity of the measured data/ measuring system.
- Confirm process capability or machine capability to confirm the variation is not induced by the machine capability itself.

Applied Techniques and Tools where appropriate:

Process Mapping, Pareto, Measurement System Analysis (GR&R), Histogram/ Process, Machine Capability etc

Analysis

- Investigate when and where the defect occurs.
- Create comprehensive list of the potential causes of the problems
- Carry out statistical or appropriate analysis to reduce the potential causes into few causes and test for significant effect to confirm the cause(s)

Applied Techniques and Tools where appropriate:

Cause and Effect Diagram, Failure Mode and Effect Analysis, Hypothesis Testing, Analysis of Variance (ANOVA), DOE etc

Improve

- Identify solutions to the identified problem (s)/ cause(s). Carry out improvement for the valid causes identified
  The choices are how to change, fix and modify the related process or parameter.
- Carry out a trial run for a planned period of time to ensure the revisions and improvements implemented in the process result in achieving the targeted values. The trial runs may be repeated if necessary.

Applied Techniques and tools where appropriate:

Design of Experiment, Analysis of Variance (ANOVA), Hypothesis Test,. Trend Chart, Bar Graph, Pareto, etc

Control

- Establish proper control and maintaining of the improved states and regularize to be the new method.
- Document the results and accomplishments of all the improvement activities. Put in place the continuous monitoring of whether the improved process is well maintained.
- Collect and compare the data between improved method and the existing method also against the expectation/ target.

Applied Techniques and tools where appropriate:

Documented procedure/ instruction, FMEA and Control Plan, Process Control and Monitoring, Histogram/ Process Capability Study etc

- Conclude the result, achievement after implementation, Limitation of the research and suggestion for further improvement
- Prepare thesis report and submit.

CHAPTER II

RELATED LITERATURE AND THEORETICAL REVIEW

2.1 Previous research works

There have been a number of researches concerning the improvements of process and/ or product quality relating to industry or manufacturing by using Six Sigma/ DMAIC methods or other quality tools and techniques as following examples.

(Achareeya, 2000)

The research did improvement on the process of monitoring tester performance by applying the six sigma method. Achievement is using manufacturing tested data to replace the current process that was running three master standards on a group of testers. The research used six sigma approach and quality tools in defining the problem, studying measurement system analysis, analysis cause and implement actions and control, for example : Cause and Effect diagram, Pareto, FMEA , SPC etc. The effectiveness in detecting tester performance is up to 78 %.

(Woraphoom, 2004)

The research was about the improvement of Hard Drive Component Packaging by using the six sigma methodology. The six sigma methodology is used in packaging development process and can help Seagate reduce the packaging cost per Head Stack Assembly (HSA) from 0.598 US dollar to 0.156 US dollar and the freight cost per HSA from 0.582 US dollar to 0.205 US dollar.

(Tsung, 2004)

The research improved the sigma level of the screen printing process of the PCBA manufacturing through DMAIC approach. Team used the Process Capability Study and Statistical Process Control for measure and analysis of current process performance, later used Design of Experiment (DOE) to determine optimal settings

critical to quality factors in the screen printing process. The desired six sigma level can be achieved.

(Yang, 2008)

The research improved the process capability of the process screen printing process of PCBA by DMAIC approach. The variation of solder paste thickness was reduced. Process Mapping and Critical to Quality were identifying in the Define Phase, X bar, R Chart and Process Capability Study were used in the Measure Phase. Analysis of Variance (ANOVA) was used in the Analyze Phase. Design of Experiment (DOE) was used in the Improvement Phase. Finally, X bar, R chart was used in the control phase. The estimated standard deviation of solder paste thickness was reduced from 13.69 to 6.04 and the Process Capability Index was improved from 0.487 to 1.432.

(Nazaripooya, 2009)

He and his team at Iran Khodro Company (BB) used cross functional team and Six Sigma tools with DMAIC cycle to reduce defect of noise in 405 Peugeot cars which can fix one of the chronic problem and customer satisfaction.The research can improve more than 60 % DPU (Defect per unit) improvement.

(Chulajata, 2011)

The researched reduced blistering/ solvent boil defective and dust contamination defective in vintage car repainting by using DMAIC approach. 100 % defect rate resulting from dirty equipment and wrong using of equipment and material was reduced 81.5% for the blistering/ solvent boil defect and 59.02% for the dust contamination defect.

(Matathil, Ganapathi, and Ramachandran, 2012)

The research was highly successful in scrap reduction in an Electronic Assembly Line by systematic application of DMAIC approach. The results showed 88% reduction of scrap cost within 6 months of work with tangible and intangible benefits.

(Kumar, Satsangi and Prajapati, 2011)

The research applied Six Sigma Tool/ DMAIC Approach for process improvement of a foundry by getting optimized parameters of differential housing castings and resulting in superior quality and stability than previous/ before improvement.

(Yamolyong, 2007)

The research was about the reduction of scrap and scrap cost per unit and cycle time of the Fused Biconic Taper Coupler process by DMAIC approach to identify the causes. The new process design was a solution. The research achieved 94% improvement in scrap reduction and 1-2 second reduced cycle time.

2.2 Six Sigma

"Six Sigma" is a smarter way to manage a business or department. Six Sigma puts the customer first and uses *facts* and *data* to drive better solutions." (Pande et. al. ,2002). Six Sigma focuses on three main areas; 1) Customer satisfaction improvement 2) Cycle time reduction 3) Defects reduction. The benefits to the business or department are significant cost saving, customer retaining and good reputation in products and services. The six sigma methods can be adopted into the organization as the problem solving approach without major changes in the organization but creating benefit in focusing on the major issues to address their root causes, data analysis systematically.

"Six Sigma" is an organized and systematic method for strategic process improvement and new product and service development that relies on statistical methods and the scientific method to make dramatic reductions in customer defined defect rates."(Linderman et. al. 2003)

Moore (2006) defines and included Six Sigma in his book (The Right Manufacturing Improvement Tools) and gave short briefs of case study on the manufacturer implementing the six sigma approach to the process and quality improvement.

Similarly, many relevant text books and Journals have defined the terminology and approaches in the same way. Literally, Six Sigma, is a statistical term which characterizes the quality less than 3.4 defects per million for a give product or process specification. Six Sigma is a methodology for reducing the variability of processes and the result is greater quality and consistent performance. It is not a new set of tools but it's tools and techniques all are found in the TQM (Total Quality Management). What appears to be different is that the Six Sigma method requires extensive data collection, measurement and analysis. Six Sigma's methodology for completed projects usually includes five phases (DMAIC) for process improvement. (a) Define, (b) Measure, (c) Analyze, (d) Improve, and (e) Control. "DMAIC is closely related to the Shewhart Cycle (Variously called the Deming Cycle or the PDCA cycle." (Montgomery, 2005).

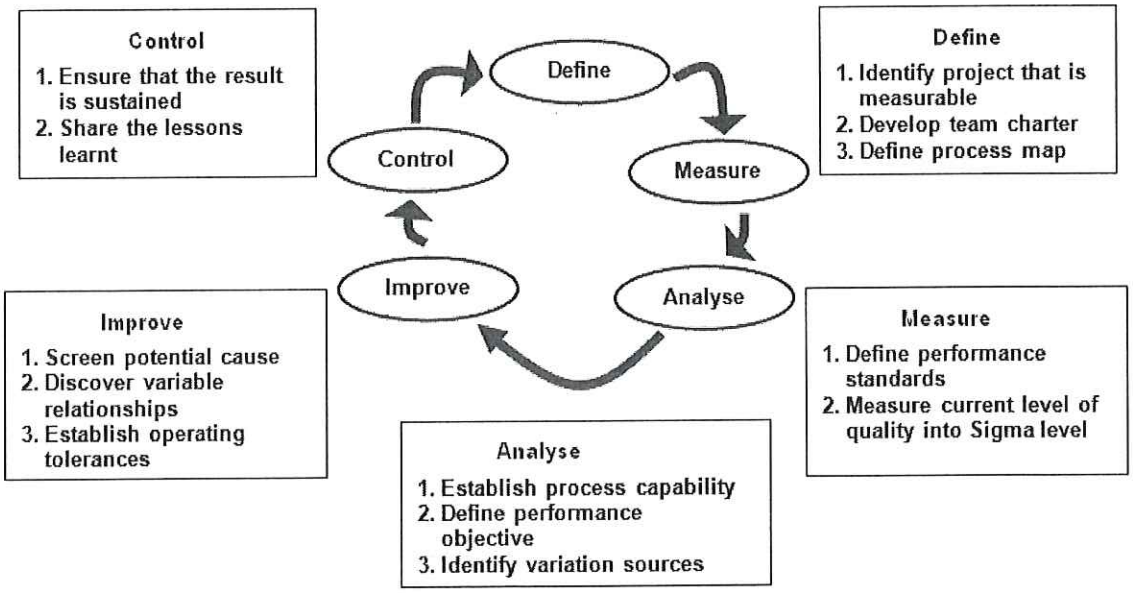


Figure 2.1DMAIC Cycle (Source: BSI website www. Bsieducation.org/standardsinaction)

2.3 DMAIC Problem Solving Approach

The Define, Measure, Analyze, Improve, Control (DMAIC) for quality improvement is considered as a disciplined methodology that uses data and statistical analysis for improving a company's operational performance by identifying and eliminating defects/ costly variations in manufacturing processes and business processes. DMAIC is fairly known as the best component of the Six Sigma which helps a lot in eliminating the defects

In brief, in a business, the leader Defines which metrics are critical/ important, Measures historical performance, Analyzes top opportunity/ variations for improving each metric, Improves underlying processes and supports the long term Controls.

2.3.1 Define (D) Phase

The purpose of the Define phase is to identify the problem and select the project for improvement.

(Pyzdek & Keller, 2010)

It is imperative to focus on selecting high-impact projects and understanding which underlying metric(s) would reflect success. A company high level business metrics can be deployed to the lower or their subset metrics. The drivers or poor performance to be improved can be considered as Critical to Quality (CTQ), Critical to Cost (CTC), or Critical to Schedule (CTS). This phase links the business priorities/ driver to specific project like 80/20 Pareto Principle rule. The Define phase ensures the critical opportunities are addressed and the goals are properly defined from the beginning.

To address the biggest improvement opportunities, some of key questions are;

- What matters to the business needs/ customers?
- Where is inconsistent/ poor performance creating high impact to the quality, cost or customer satisfaction?

Critical to Quality Metrics can be;

- DPMO, DPPM
- Process Defect Rates, P chart, X bar control chart
- Process Capability Indices
- Rolled Throughput Yield and Sigma Level

- What defects/ metrics should be improved? By how much and by when?
- What is the current rate of defects/ metrics (if available)?
- Who will be in the project team and supporting?

Deliverable and tools applicable for the Define phase are as followings:

- Team/Project Charter

  This document includes the problem description, project scope, objectives and goals, the business need, Team information, Deliverables and scheduling.

- Trend Chart

  This exhibits the trend of defect occurring over a period of time.

- Pareto Analysis

  This is used to analyze which and what proportion of defect mode contributes to total defects and how its criticality is. The Pareto Principle states that 20% of all potential defects will produce 80% of the potential Impacts to the business.

- Process Flow Chart/ Map

  This is to understand how the current process steps are and the current process functions

- SIPOC; Suppliers-Inputs-Process-Outputs-Customers

  It is a high level diagram of the five key elements that are parts of creating and delivering the value required by the customers.

  - Suppliers: The suppliers of materials, service, information used in the process to create the value sold to the customers
  - Inputs: The actual materials, service and information used to create the value
  - Process: The sequence of events used the processes, organization to transform the material, service, information into value.
  - Outputs: The value created by the organization to satisfy the customers' demands.
  - Customers : The users of the value created by the organization.

- Gantt Chart/ Time Line

  This is to support the scheduling of the project.

2.3.2 Measure (M) Phase

The purpose of the Measure Phase is to understand the current performance by ensuring the specific process under studying is clearly defined (Process Definition), to define a reliable means of measuring the process, relative to the project deliverables (Metric Definition), to quantify the current operating results and to substantiate improvement results (Baseline Establishing) and to validate the reliability of the measurement data (Measurement System Evaluation)

- Process Definition

This is to understand/ document the underlying specific process and the relevant processes with identified inputs and outputs so as to understand the relevant outputs and all potential inputs that may impact each output.

- Metric Definition

The suitable process metrics related to the previously defined project deliverable need to be defined and measured or validated how it is measured. It is imperative to focus on what is worth measuring, can be measured and determined overall success.

  - Defects per opportunity (DPO)

    It is the ratio of the defects found on all the units to the total number of opportunities.

    DPO = defects/ (Opportunity x units)

    DPMO = Defects/ (Opportunity x units x 1000000)

- Process Baseline Estimates

This is to estimate the current operating performance as the reference point for assertions of improvement/ benefits attained.

- Measurement Systems Evaluation

This is to evaluate the accuracy and variation of the measurement system used to determine the process performance. The Gauge R&R is at least required to be done to ensure the measured process performance is reliable

Key questions to address this phase are:

- What is the underlying process? How does it work?
- What outputs affect CTQ most?
- Which inputs affect outputs most?

- Are there any measurements/ metrics in place to monitor performance in these areas and what is the current performing?
- If there is not a performance measure in place for a critical-to-customer / quality/ cost area, how can it be developed?

Applicable Tools and Techniques

- Process Box Diagram
- Process Mapping
- Trend Chart
- Pareto
- Histogram Distribution
- Gage Repeatability and Reproducibility (GR&R)

  It determines how much of observed process variation is due to the measurement system variation.

  ➢ Attribute Agreement Analysis for Assessments

It is used to assess the agreement between the rating made by appraisers and the known standards, also accuracy of the assessments made by appraisers (Winsor, 2003) by considering of;

- The % of the agreement between the appraisals and the standard.
- The % of the agreement between the appraisals and the standard adjusted by the % of agreement by chance (Kappa statistics).
- Under within Appraisers, Between Appraisers, Each Appraiser vs Standard, All Appraisers vs Standard.
- KAPPA Statistic

Proportion of agreements between appraisers after chance agreement has been removed

Kappa = P observed - P chance/ P chance

$$K = \frac{Pr(a) - Pr(e)}{1 - Pr(e)}$$

- Effectiveness, False Alarm Rate and Miss Rate Analysis
- The general acceptance criteria good to excellent agreement is under the kappa value >0.75, and poor agreement if the value is less than 0.4.

2.3.3 Analyze (A) Phase

The purpose of this phase is to understand the source of variation that contributes to the defects or the drivers that correlate to the CTQ, CTC or CTS and identify ways to eliminate the gap between the current performance and the desired performance.

Some key questions to support this phase are;

- Which inputs actually affect the CTQ, CTC or CTS?
- By how much?
- Do combinations of variables affect outputs?
- If the input is changed, then would the output be changed?
- How many of observations are required?
- What is the level of confidence?

Applicable Tools or Techniques

- Value Stream Analysis
- Cause and Effect Diagrams (C&E Diagram)

Also known as a fishbone diagram, It is used to visualize the link between the different causes to an outcome or effect. In general, more than one cause to an effect. It will help to analyse, systemize and link of possible causes of an effect but it does not quantify. Further statistical analysis is required to go in dept which causes contribute the most to generate the effect.

- Failure Mode and Effect Analysis (FMEA)

The FMEA is a well accepted approach and described in the number of international standards and text book including Stamatis (2003).There are several types of FMEA but what is used to this research is the Process FMEA which is used to analyse a process or many processes. The Process-FMEA is used for analysis of manufacturing and assembly processes. The focus of a Process-FMEA is failure modes caused by deficiencies in processes or assemblies, assessing the potential effects of the failures, potential causes, process parameters/ characteristics to control for prevention or detection of the failure or cause (Stamatis, 2003).

Typically, the FMEA classified the failure modes based on three perspectives; evaluation of Severity (S) of the potential failure effect, Occurrence (O) and detectability (D) with rating scales ranged from 1 to 5 or from 1 to 10. The high number represents the high risk, for example 10 is very likely to occur, 1 is unlikely to occur. The quantitative rating guides by Stamatis (2003) are shown in Appendix A, B and C respectively. However, the specific rating descriptions and criteria may be defined by the organization to fit the products or processes that are being analyzed (Stamatis, 2003).

The Risk Priority Number (RPN) resulting from the multiplication of the Severity (S), Occurrence (O) and Detection (D) of each of potential failure is used to rank the priority of need of addressing of actions. The RPN considered for actions may be considered as a threshold of a given statistical confidence. For Example, if the statistical confidence is 90% with a scale of 1 to 10, then the threshold becomes 100.

On the other hand, the RPN considered for action priority may be considered as the top RPNs although the RPN value is not high as the threshold. There are some strategies recommended to reduce the total RPN by reducing severity, occurrence and/ or detection (Stamatis, 2003).

- Severity Rating reduction by design or manufacturing process change
- Occurrence Rating reduction by design or manufacturing process change
- Detection Rating reduction by the detection control improvement or inspection frequency increasing but these kinds of reductions are quite costly and generally reactive, so it should be used as a last.

- Normality Test/ Boxplots
- Statistical Inference
- X2, T and F distribution
- Hypothesis Testing

A hypothesis is a value judgment, a statement based on an opinion about a population or inference of population and hypothesis testing is the assessing the validity of a hypothesis about a population.

Null hypothesis denoted as H0

Alternate Hypothesis denoted as H1

Test Statistic

$$Z= \frac{\overline{X} - \mu}{\sigma / \sqrt{n}}$$

And the t formula is used when the samples are smaller;

$$t= \frac{\overline{X} - \mu}{s / \sqrt{n}}$$

- Significant Level or Risk Level

It addresses the risk of failing to reject a hypothesis when it is actually false, Type I error or Alpha error or rejecting a hypothesis when it is actually true, Type II or Beta error.

Testing Of Sample Mean

Ho: μ =xx

H1: μ # xx

t= $\frac{\overline{X} - \mu}{s / \sqrt{n}}$

Testing Of Proportion

Ho: ρ =xx

H1: ρ # xx

Z= $\frac{\hat{\rho} - \rho}{\sqrt{\frac{\rho q}{n}}}$

Testing Of two sample variances

F= $\frac{s_1^2}{s_2^2}$

Ho: $s_1^2 = s_2^2$

H1: $s_1^2 \# s_2^2$

Testing of a Standard Deviation Compared to a Standard Value

$X^2 = \frac{(n-1)s^2}{\sigma^2}$

Testing of Normality of Data

Ho: The data are normally distributed

H1: The data are not normally distributed

- Regression and Correlation Analysis
- Scatter Diagrams
- Correlation and Regression
- Linear Models

- Least-Squares Fit
- Designed Experiments (DOE)

  Design Characteristics

  Replication

  Randomization

  ➢ Types of Design

  Fixed-effects model

  Random-effects model

  Mixed model

  Completely randomized design

  Randomized-block design

Since the experimental units may not be all homogeneous, so the factors may be grouped into blocks so that in each block, the treatment could be varied and compared. Since the comparisons are made within blocks, the error variation does not include the effects of the blocks or the block to block variations.

- One-Way ANOVA (Completely Randomized Experimental Design)

This compares sample means if there is significant difference. A single input factor is varied a different levels with comparing the means of replications of the experiments. The null hypothesis will be rejected when the variation in the response variable is not due to random errors but to variation between treatment levels.

- Two-Way ANOVA

It is the factorial design which consider the effect of noise factors

- Factorial Design with Two Factors

The level of every treatment is tested for all treatments simultaneously. The row effects and the column effects are called the main effects. The combined effects of the rows and the columns are called the interaction effect. The Two- Way ANOVA may be with No Replicates and with Replicates.

- Factorial Design with More Than Two Factors (2**k)

Some situation, more than two factors affect the response factor. Two levels with k factors design is an approach. The two levels, high (+1) and low (-1) for each factor would result in 2**k trials.

- Power and Sample Size

Minitab's power and sample size function was used to find out the appropriate sample size in the design and running of the experiment. Before the data was collected, it is important to ensure that the experiment would have enough power to detect the differences (effects) in the response variable. Design sensitivity can be enhanced by increasing the sample size or by taking measures to decrease the error variance. However, cost consideration needs to be taken into account.

- Testing Common Assumptions
  - Normality Assumption
  - Linear Model Assumption
  - Analysis of Categorical Data

- Making comparisons using Chi-Square Tests

This test compares the observed values to the expected values to determine if they are significantly difference when the data being analysed do not fit into the t-test assumption.

Ho: $\rho_1 = \rho_2$

H1: $\rho_1 \# \rho_2$

$$X^2 = \sum \frac{(f_a - f_e)^2}{f_e}$$

f_e is the expected frequency and f_a is as the actual frequency. df=k-1

- Making comparisons using Non-Parametic test/ Mann-Whitney U test
  - ➢ Hypothesis;

    Ho: The quality Level of before improvement (A) is the same as the one for after improvement (B)

    H1: The quality level of before improvement (A) is different from the one for after improvement (B)
  - ➢ Analyze the data

    ω_1 Sum of the ranks of the observations for group A

    ω_2 Sum of the ranks of the observations for group B
  - ➢ Determine the value of the U static

$$U_1 = n_1 n_2 + \frac{n_1(n_1 + 1)}{2} - \omega_1$$

$$U_1 = n_1 n_2 + \frac{n_1(n_1 + 1)}{2} - \omega_2$$

The test static U will be smallest of U_1 and U_2

2.3.4 Improve (I) Phase

This phase focuses on developing means to remove variation root causes, testing, standardizing the solutions which includes identifying ways to remove causes of variation, determine relationships between variables and optimize the process variables/ inputs or flow which also use customer demands to make improvement decisions.

Some key questions to address this phase are;

- How will the known most affecting inputs to outputs be managed?
- How many trials are needed to find and confirm the optimum of key inputs?
- What is to be improved or changed based on the new process?
- How much defects are decreased?

Applicable Tools and Techniques are

- Process Mapping
- Process Capability Analysis after improvement to confirm the improvement is really attained in preventing defects.

  DOE, a planned set of tests to define the optimum setting to obtain the desired output and validate improvement

2.3.5 Control (C) Phase

The purpose of this phase is to establish standard measures to maintain the achieved performance and to correct problems as needed including the measurement system including

- Validate the new process design
- Business Process Control Planning
- Maintaining Gains
- Using SPC for Ongoing Control
- Preparing the Process Control Plan

CHAPTER III

PRINTED CIRCUIT BOARD ASSEMBLY

SURFACE MOUNT TECHNOLOGY AND ASSEMBLY PROCESSES

Surface mount technology (SMT) is the technique of attaching components and devices to the surface of the printed circuit board, only the board pads are solder (Manko, 1995). This technology is a revolutionary change in the electronics industries. It was emerged in the late 1950s with the advantage of capability to place components on both sides of the printed circuit board. It had been increasing importance during the late 1970s when the through hole technology was up to the limitation in meeting the higher need for higher densities and technology which there were difficulties in drilling more holes with smaller holes for smaller pitch dimension and higher cost. It was then rapid increasing interest in the SMT and availability of various surface mount devices (SMDs) as practical supporters. The Surface Mount Technology became the key assembly technology of the Printed Circuit Board Assembly since then. The benefits of SMT allow a higher density, speed, automation, lower cost and better performance and reliability with reduction and simplification of interconnects.

3.1 Surface Mount Components

Various different surface mounted devices or component are available to any type of application of printed circuit boards. The physical size of components of devices is imposed restricted by the surface mounting process and mostly designed for power dissipation not higher than 1 to 2 of width. Typically, the type can be classified according to the method of attachment as;

- Leaded devices: Lead shape is conductive to a surface connection and
- Leadless devices: No lead but the body itself has metalized termination contacting to a surface

Most commonly used surface mount devices are as followings

3.1.1 Leadless Chips (capacitors, resistors, inductors)

Considered as the simplest devices and generally passive components, chip resistor consists of a rectangular ceramic substrate body with a metalized termination, usually palladium –silver on both terminal ends; chip capacitor is the multilayer ceramic chip, consisting of multiple layers of precious metal electrodes separated by layers of ceramic dielectrics which the required capacitance is obtained by the stacked layers; chip inductor consists a ceramic or ferrite core wrapped around by an polyurethane enameled fine copper wire and usually potted in an epoxy resin for easy handling.

3.1.2 Discrete Semiconductor (Small outline compliant-leaded)

Such as diodes, transistors, similar packages are utilized, typically SOT-23 (Low power single diode), SOT-143 (Low power dual diode), SOT-89 (High current device)

3.1.3 Integrated Circuits (ICs)

Surface mount integrated circuits are packaged in a variety of forms. Commonly used types are SOIC (small-outline integrated circuit), TSOP (thin small-outline package), PLCC (plastic leaded chip carrier), LCCC (leadless ceramic chip carrier, QFP (quad flat pack), BGA (ball grid array). The IC package lead configurations are classified into five major categories i.e. Gull Wing, J-Lead, Butt-Lead, Leadless metallization, Ball-Lead.

3.1.4 Leadless, Leaded Chip Carriers

These devices are ultimate density packaging type

3.2 Surface Mount Assembly Technology

Surface Mounted Devices can be mounted to Printed Circuit Boards with either with adhesive bond, direct flux and hot solder application (Molten solder application) or the solder paste with flux followed by reflow (Pre-paste then heat) or conductive adhesive curing (not commonly used). The suitable assembly technology choosing

depends on the board layout and if there are through hole component to be attached. Typically, the surface mount assembly processes can be classified into;

- Type I: Required solder paste with reflow soldering process for both sides Both sides of a board are with Surface Mount Devices (SMD) only
- Type II: Required both reflow and wave processes
  One side of a board has both SMDs and through hole parts, another side has chip components. The process applied to this is reflow soldering for the SMD and following by wave soldering for through hole and chip components. Through hole parts can be inserted after adhesive of chip components has been cured.
- Type III: Required only wave soldering process
  One side of a board has only through-hole parts and the other side has chip components. Through hole parts can be inserted either before or after the populating of chip components.

3.2.1 Surface Mount Soldering Processes

➢ Reflow Soldering

The solder paste, pre-blended of solder powder and flux, is deposited on the PCB pads through stencil printing then SMDs are placed. The solder paste applied acts as holding of SMD to the PCB prior to reflow soldering process. In the reflow oven, the solder joint will be formed between the component termination and PCB pads by the heat which the temperature above the liquidus temperature of solder to reflow the solder powder with flux reaction and removal of the oxide of solder powder and metallization of leads and pads.

➢ Wave Soldering

Typically, the wave soldering has been used for bonding of through hole components to the PCB. The PCB with inserted through-hole

components are pre-fluxed via spray/ foam fluxer then passed thru single solder wave for soldering. However, when use with the SMD soldering, it needs to be a dual wave with proper preheating to avoid shadow effect and thermal shock. The wave soldering used for SMD on the bottom side is a dual wave with a turbulent wave to ensure the wetting of all leads with subsequent the laminar wave to remove excessive solder to avoid solder bridging between leads. However, this soldering process is suitable for small SMDs only while large SMDs or fine pitch components are still concerned for solder bridging under this process.

3.2.2 Solder Alloys Materials

The solder paste is the key material/ chemicals used in the SMT reflow soldering process. With the limitation of wave soldering technology, solder paste and reflow soldering can replace the glue dispensing and wave soldering which may encounter the shadow effect/ insufficient solder. Also the deposition of solder paste via stencil screen printing, dispensing or pin transferring processes can be sure on consistency of solder volume on pads to form the joints and particularly reduce solder bridging occurrence in case of fine pitch component. The use of solder paste with reflow process can control heating profile so it can avoid potential damages to the SMDs.

- Solder Paste Composition

The solder paste is composed of the individual solder powder and flux blended together. The solder paste composition/ powder size & % metal content, solder density is varied depending on the application. In general, the power size used should be no bigger than 1/7 of aperture size for printing application. The solder deposition performance is affected by the solder volume fraction so the solder content should be adjusted in order to maintain proper volume fraction of solder in solder paste.

The surface mount industry has standardized on the same alloys used in wave soldering process with some medications. The traditional tin-lead alloys have continued to dominate market and much more use of the eutectic 63%Sn/ 37% Pb. However, there are other solder alloys in use with the different purposes like the environment friendly support which are the Lead-free Solders which restrict the use of the hazardous substance especially lead.

➢ Solder Paste Properties

Followings are the various rheological properties of a solder paste

- Viscosity: Degree to which the material resists tendency to flow.

  When solder paste is moved by the squeegee on the stencil, the physical stress applied to the paste causes the viscosity to break down, thinning the paste and helping it flow easily through the apertures on the stencil. When the stress on the paste is removed it regains it shape, preventing it from flowing on the circuit board. The viscosity for a particular paste is available from the manufacturer's catalog.

- Slump: The characteristic of a material's tendency to spread after application

  Slump could create the risk of forming solder bridges between two adjacent pads, a paste's slump should be minimized or having not a high slump value.

- Working life: The amount of time solder paste can stay on a stencil without affecting its printing properties.
  Generally, the paste manufacturer advises this information.

➢ Paste Deposition

The Stencil Screen Printing is mostly common used in solder paste deposition to the PCB pads comparing with many other technologies. Its benefits are higher speed/ throughputs, better pattern registration and precisely control of solder paste volume deposition, effectively used with fine pitch component bonding.

➢ Paste Handling and Storage

Solder paste is required to be stored in freezer because it is sensitive to heat and humidity. Heat is concerned to the reaction between solder powder and flux or a separation of solder powder and flux. Humidity or air exposure may get solder paste dry, oxidized or moisture absorption. When to use, the solder paste needs to be left in the ambient temperature when out from the refrigerator prior to exposing to the air to avoid moisture condensation. The de-freezing time is depending on the container size and storage temperature.

3.2.3 Stencil

A stencil is basically formed of metal foil with opening apertures matching with the pads on the PCB where the screened solder paste is needed. When printing, the stencil needs to be placed on top of a PCB with a properly registered pattern, then solder paste is deposited onto the top side of the stencil then the squeegee wipes solder paste across stencil, later the PCB is detached from the stencil, the consequence is the solder paste deposited on top of the pasted pads. The key control of the stencil printing process is the requirement of a flat substrate surface for the stencil to be placed on.

3.2.4 Squeegee

The squeegee is used to force the solder paste through the aperture across the stencil surface. The edge of the squeegee wipes the solder paste from the stencil surface and leaves the defined solder paste on the PCB pad when departs from the

stencil. The squeegee can be classified into two types based on the material used which are the polyurethane rubber and metal type. The polyurethane rubber squeegee is likely to press into the aperture and scoop the solder paste due to the rubber softness while the hard metal blade edge has no concern about the scooping effect but maintain a flat cut when wiping through the aperture. With the proper squeegee angle and pressure, the metal squeegee can be used with both a flat surface also a step-stencil. When printed, the solder paste is left exposure in front of the squeegee blade resulting deterioration due to moisture absorption, oxidation and solvent loss. Recently, with the new printing technology, the solder paste is retained in a closed chamber during printing. The elimination of paste exposure can deal with the drying, oxidation and moisture absorption and ensure aperture filling and better printing quality. Conversely, there are some disadvantages about the thick up solder paste or leak out of the chamber.

3.3 Surface Mount Assembly Processes

Recently, the surface mount components have been used as mostly and virtually all PCB assembly. In today's products and the very high demand placed on quality, the surface mount assembly process is critical to the success of the products that are manufactured. Core Surface Mount Assembly processes and manufacturing line are shown as figure 3.1 and figure 3.2 respectively and the details of the processes are described as follows.

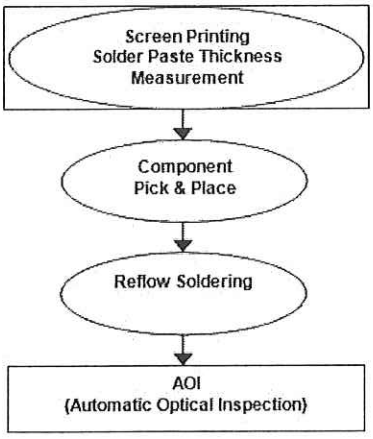


Figure 3.1 Surface Mount Assembly Processes

Figure 3.2 Surface Mount Assembly Line

3.3.1 Solder Paste Printing and Inspection Process

The solder paste is loaded onto the stencil after the stencil is well installed with the printing machine. The amount is per the type or per manufacturing recommendation. The printer can be set up for the on-contact or off-contact mode with the proper snap off value and separation between stencil and deposited paste. Off contact printing mode can reduce the smear printing however the on-contact mode typically provides more accurate printing. Generally, the slow snap out speed could help to achieve the good printing quality. The smaller the component fine pitch, the slower the squeegee speed needed, however if it is too slow, then the paste will not roll and flow to the aperture opening vice versa if it is too fast, then the paste will slide and skip the openings and cause insufficient solder paste. However, the higher demand on output is needed so the faster squeegee speed is desired with the good printing quality. Upon the printing, the paste deposition should be inspected on the representing characteristics by laser-based sensor scanned over the pads for solder paste height measurement. The light from a laser diode is reflected from the object surface and imaged onto a detector array. For a manually operated optical inspection device, when measuring the solder paste height, it needs to position the video measurement lines horizontally on the laser stripe

over the solder paste and over the board surface. The difference is the solder paste height and the value is displayed on the monitor.

3.3.2 Pick and Place Operation

After printed the solder paste, the PCB will be passed to the pick and place operation which the surface mount devices will be mounted on the PCB by the pick and place machine.

3.3.3 Reflow Soldering Operation

The board with the placed components from the pick and place operation will be passed to reflow soldering for bonding. The reflow soldering is the heating process with preplaced flux and solder using an oven or a vapor phase reflow. The oven may operate in air, nitrogen. In soldering with the heat, the flux cleans off the tarnish, the solder melts and wets the surfaces, the fillet solidifies upon cooling and the solder joint is resulted. A standard profile commonly used is generally recommended by the solder paste manufacturers or component manufacturers.

➢ Profile Stages

The SMT profile is broken down into 4 phases as illustrated on figure 3.3 with following descriptions.

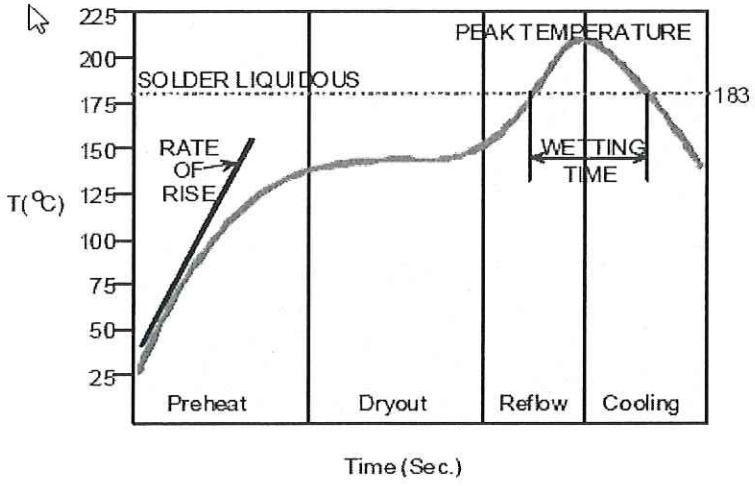


Figure 3.3 SMT Profile Stages

- Preheat

  This phase preconditions the PCB assembly before actual reflow. It removes flux volatiles and reduces thermal shock to the PCBA. Rate of Rise or Ramp Rate is the slope of temperature versus time for the heating part of the profile. The improper temperature rate dT/dt; likes too rapid rate would cause mismatching in thermal expansion coefficient/ thermal stress building up and result in cracking to the components, also affect to the solder paste viscosity due to rapidly dried out solvent and cause solder slump or solder beading problem around components

- Dry Out/ Pre-reflow

  This phase the flux activator removes any existing surface oxide from the component leads and PCB pad finishes including any oxide on the powder particles within the solder paste itself to be ready for surfaces to be joined.

- Reflow

  This phase involves the creation of a mechanical and electrical bond through the formation of tin copper intermetallics by two key parameters i.e. peak temperature and time above liquidus (TAL).

- Cooling

  This phase determines the grain structure of the solder joint. A fine grain provides reliable bond which can be achieved by a rapid cooling rate to transform from liquid to solid. However if the rate is too fast, the thermal stress or fracture could occur.

3.3.4 PCBA Inspection Process (Auto-Optical Inspection), AOI

Automatic or automated optical inspection (AOI), is a key technique used in the manufacturing and testing of printed circuit boards, PCBs and printed circuit board

assemblies, PCBAs. The AOI enables fast and accurate inspection to ensure that the quality of product leaving the production line is high and the items are built correctly and without manufacturing defects. This technique replaces the old typical visual inspection especially the complexity of assemblies under the surface mount technology with the compacted and crowded components and solder joints. Presently, the smaller components and higher component densities on PCBs have driven manufacturers to use AOI on their production lines. Only visual inspection by human no longer performs reliable, consistent inspection of fine-pitch components and maintains an accurate observations and measurements. The benefits of automated inspection lie in its repeatable and accurate measurements.

- The principle of an AOI

AOI systems use visual methods to monitor the assemblies for effects. It uses the captured image which is processed and then compared with the knowledge the machine has of what the board should look like. Using this comparison the AOI system is able to detect and highlight any defects. One of the key elements of an AOI, automated optical inspection system is the image capture system. This captures an image of the printed circuit board, PCB assembly which is then analyzed by the processing software within the AOI system. There are many variants of image capture system dependent upon the exact application and the complexity of the AOI system. When analysing an image of a board, the AOI system looks for a variety of specific features: component placement, component size, board fiducials, label patterns/ bar codes, background colour and reflectivity, etc. As an important element of its task the AOI system also inspects the soldered joints to ensure they indicate that the joints are satisfactory. It also takes into account many variations between good boards.

- Where to put AOI

To find the source of all defects, we would have to provide for 100% in-line inspection after each manufacturing but may be costly so it needs to consider the cost

of inspecting PCBs against the profits gained from increasing PCB yields. In general, the AOI can be put at any of four places on a production line; AOI used after paste printing, after chip placement, and after component placement, or after reflow soldering.

- AOI after Reflow Soldering

After reflow soldering, an AOI is used for inspecting of missing, offset, and skewed components, any polarity defects including solder defects such as non-wetting, insufficient solder, solder bridges etc. Mostly, an AOI is focused on the post solder inspection which is more closed loop process control and more significant role in increasing the production yield or reducing the defect rate.

3.4 Common PCBA Surface Mount Assembly Process/ Product Defects

The following defects (Non-fulfillment of a requirement related to an intended or specified use) are considered as the common PCBA SMT process defects, the terms and definitions are described in the IPC-T-50H (Terms and Definitions for Interconnecting and Packaging Electronic Circuits). Followings are some key common defects of Surface Mount Assembly processes.

3.4.1 Non-wetting

The inability of molten solder to form a metallic bond with the basis material

3.4.2 Solder Ball

A small sphere of solder adhering to a laminate, resist or conductor surface

3.4.3 Solder Bridging

The unwanted formation of a conductive path of solder between conductors

3.4.4 Tombstone

A defect condition whereby a leadless device has only one of its metalized terminations soldered to a land and has the other metalized termination elevated above and not soldered to its land

3.4.5 Insufficient Solder fillet/ connection

A solder connection that is characterized by the incomplete coverage of one or more of the surfaces of the connected metals and/or by the presence of incomplete solder fillets

CHAPTER IV

DMAIC APPROACH, RESULTS, ANALYSIS AND DISCUSSION

The DMAIC approach was adopted and applied in the research as followings.

4.1 D- Define Phase

4.1.1 SIPOC (Supplier, Input, Process, Outputs, Customers, Requirements)

SIPOC Diagram is used to illustrate the product flow and related processes of the Printed Circuit Board Assembly of the company ABC as defined in the figure 4.1

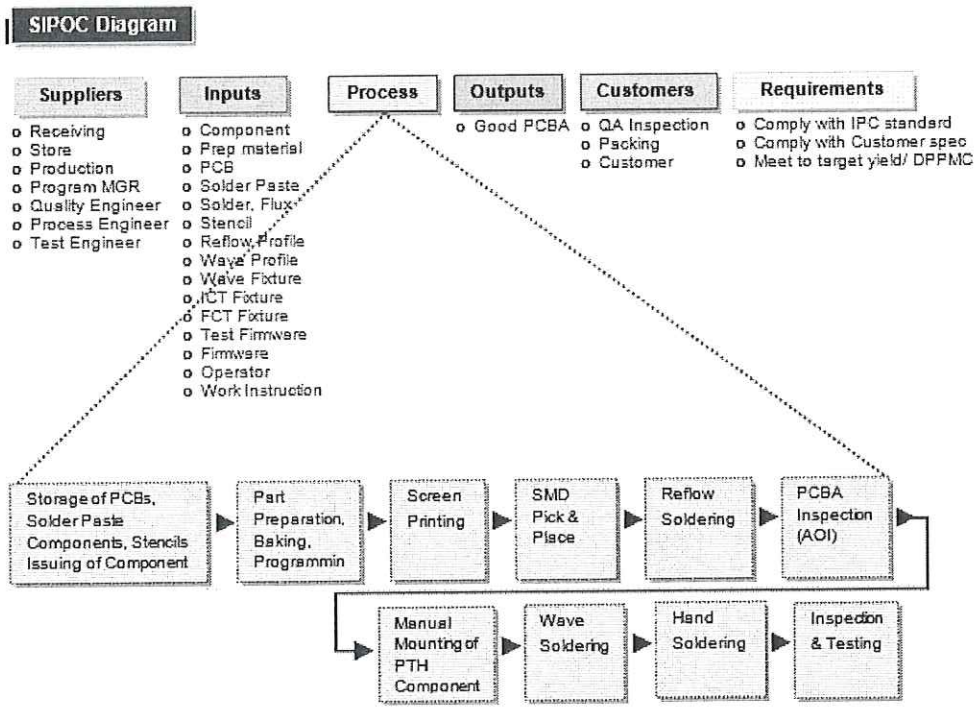
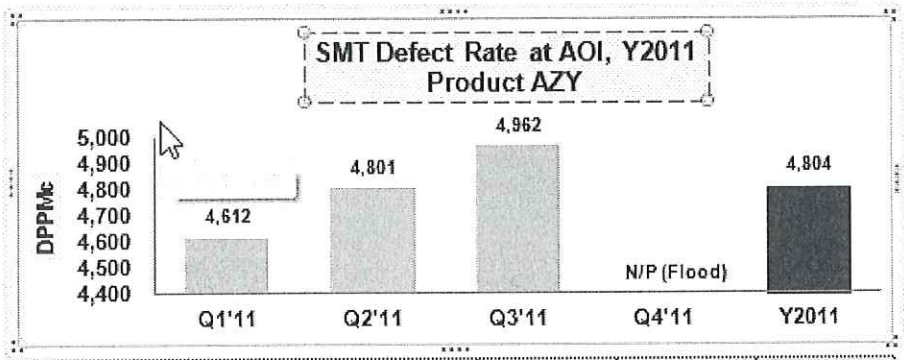


Figure 4.1 SIPOC Diagram of Printed Circuit Board Assembly of ABC Company

4.1.2 Historical Process Performance/ Defect Rate

Historical defect rates of PCBA SMT processes are measured at PCBA Inspection (AOI) after SMT process. The research will focus only on front processes / SMT as the priority which is considered as key upstream processes and high

contribution of the defect rate. The historical data of PCBA Inspection (AOI) after SMT process is shown on the figure 4.2.



	Q1'11	Q2'11	Q3'11	Q4'11	Y2011
Total	1,133	1,124	1,391	N/P	3,648
Total Points	2,100,582	2,083,896	2,578,914	N/P	6,763,392
Defect Points	9,687	10,004	12,797	N/P	32,488
DPPMc	4,612	4,801	4,962		4,804

Figure 4.2 Historical Data of SMT Process PCBA Defects, Y2011

According to the SIPOC diagram and historical data of process performance/ defect rate and targeted project scope, the project charters are developed and described as follows and reference appendix Project Charters of Product AYZ Defect Rate improvement

4.1.3 Project Charters

➢ Problem Statement

The Product AZY PCBA production has negative trend and high defect rate. The defect rate/ DPPMc at SMT processes had been increasing over time and higher than the company target goal which is Critical to Quality, Process Efficiency and Cost of Quality to the company. The historical data in the 2011 was shown high DPPMc of SMT processes; DPPMc in average was about 4804 which was far away from the company goal at 650 DPPMc and continuously negative trend from 4612 DPPMc since the beginning of the year 2011to 4962 DPPMc at the third quarter of the year 2011.

➢ Project Objectives

To reduce the DPPMc of SMT process defect rate from current state at 4804 DPPMc in average of Y2001 to 680 DPPMc within 6 months which would result in less defect rate, less rework and cost effect.

- Matrix is the Defect Rate: DPPMc
- Based Line: 4804 DPPMc in average for the year 2011 and negative trend
- Goal: 680 DPPMc in Q3'13

➢ Project Scope

The scope of studying and improvement is limited to only the Product Group AZY of the company ABC and at the related SMT processes which can be illustrated by the dash box of Scope of Research/ Studying as depicted in the figure 4.3 and SIPOC analysis in the table 4.1: SIPOC Analysis of SMT Processes

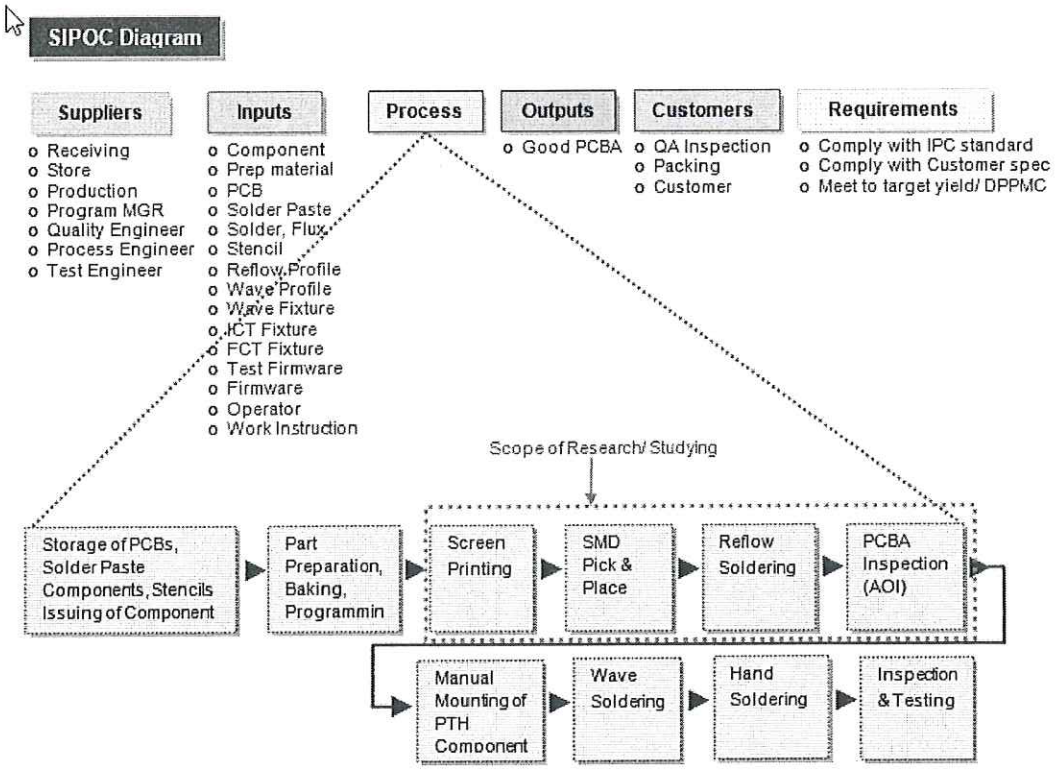


Figure 4.3: Studying Project Scope

	Screen Printing Process	Pick and Place Process	Reflow Process	AOI Process
Supplier	• Material Suppliers • Stencil Manufacturers • Operators • Technicians	• Material Suppliers • Machine Suppliers • Operators • Technicians	• Machine Suppliers • Operators • Technicians	• Machine Suppliers • Operators • Technicians
Inputs	• PCB • Stencil • Solder Paste • Work Instruction	• Solder Paste Printed PCB • Pick and Place Program • Components • Work Instruction	• Reflow Profile Program • PCB with Populated Component • Work Instruction	• Soldered PCBAs • AOI Program • Work Instruction
Process	• Print Solder Paste on to PCB pads • Screen Printing Machine • Printing Parameters • Set Up	• Pick and Place component on to the printed PCB • Process Parameters • Set UP	• Reflow Soldering • Reflow Oven • Process Parameters • Set Up	• Inspection by AOI Machine • AOI Machine • Process Parameters • Set up
Outputs	• Solder Paste Printed PCB	• Printed PCB with Populated Components	• Reflowed/ Soldered PCBAs	• Inspected PCBA (Accepted PCBAs, Rejected PCBAs with Defects) • Defect Call Report
Customer	• Pick and Place Operation	• Reflow Soldering Operation	• AOI Operation	• Next process

Table 4.1 SIPOC of SMT Processes

- Expected Benefits

The expected benefits from the improvement would result in;

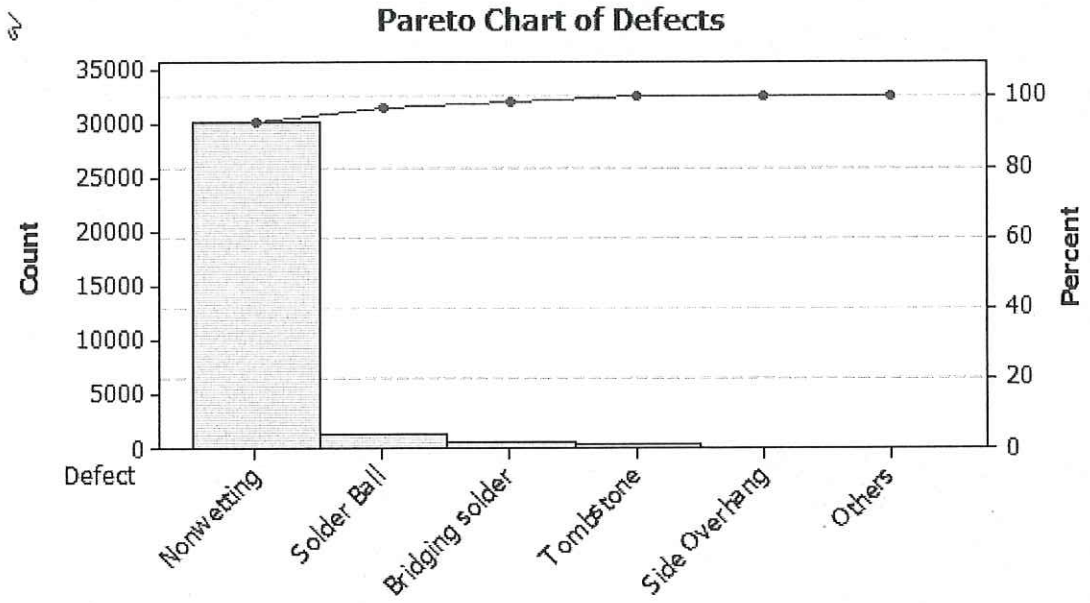
- Reduced Defect rate and improved quality of products
- Improved PCBA process performance
- Improved throughputs/ productivity
- Less rework / cost of poor quality
- Improvement Project Base for other products

4.2 M – Measure Phase

4.2.1 Data Collection

Defect Rate is collected per the established methodology at AOI operation separated by product part number, each applicable defect criteria/ mode detected. The DPPMc is calculated by the number of defect points divided by the number of

opportunities considered as the number of components for this study. The study will focus on the top defect(s) contributing high DPPMc rate, to get that, the Pareto by defect mode/ criteria is broken down as shown in the figure 4.4.



Count	30148	1336	558	378	60	8
Percent	92.8	4.1	1.7	1.2	0.2	0.0
Cum %	92.8	96.9	98.6	99.8	100.0	100.0

Figure 4.4 Pareto Chart by Defect Criteria

From the Defect Pareto, the top defects are Non-wetting, Solder Ball and Bridging Solder. However, the Non-wetting defect is obviously high contribution (92.8%) comparing to the other two and the rest (27.2%) and mostly contributing to the overall defect rate.

To achieve significant improved results, basically, it requires selecting the vital few project(s)/ defect(s) as well as the useful many. However, with the concerns on resources and project timeframe, the vital few project(s)/ defect(s) are the major contributor in achievement (Juran, 1999)

With the defect contribution rational and the pareto concept, which the vital few defects (20%) are responsible for most of the reported problems (80%). The improvement efforts should be focused on the vital 20 %/ significant few defect(s), the

great improvement can be seen. Therefore, the non-wetting defect is firstly picked and focused for improvement as the first priority. The details will be further discussed in the next phase.

Prior to going further for analysis phase, the followings are confirmed for sure in term of capability and validity of the manufacturing machine and measurement system of the related data and scope.

4.2.2 Pick and Place Machine Capability

To make sure the SMT Pick and Place machine is capable to perform its function and no abnormal variation induced from the machine capability itself, the machine capability is performed by the placement accuracy examination system developed by the machine manufacturer on key parameters. The results are shown as figure 4.5.

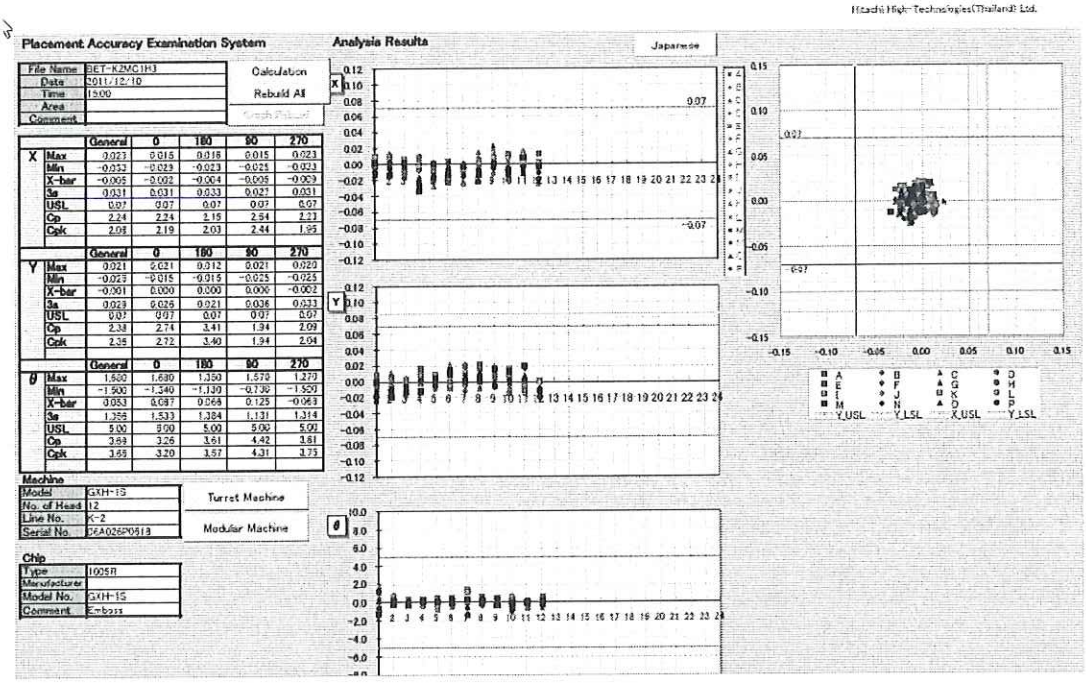


Figure 4.5: Pick and Place Machine Placement Accuracy Examination

The machine performance is proven capable on the Cp and Cpk indexes higher than 1.33 which is acceptance index number for general and the industry.

4.2.3 Gauge Repeatability and Reproducibility (GR&R) of AOI Machines

The data collected as the defects are appearance verification and justified as accept or reject to the established criteria set up in the inspection machine. Attribute GR&R is performed on the AOI machines, see figure 4.6 and 4.7 used for inspecting the defects. The study evaluated the measurement performance by using Attribute Agreement Analysis. The known production sample attributes and studying data is shown in the table 4.2 and following Minitab Analysis Results.

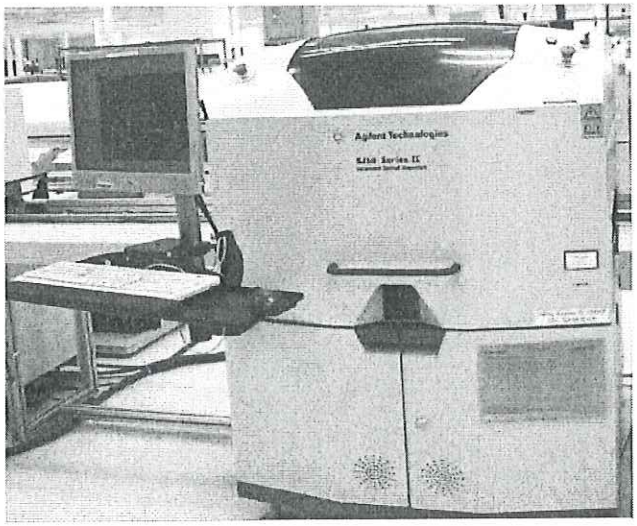


Figure 4.6 AOI Machine# 1

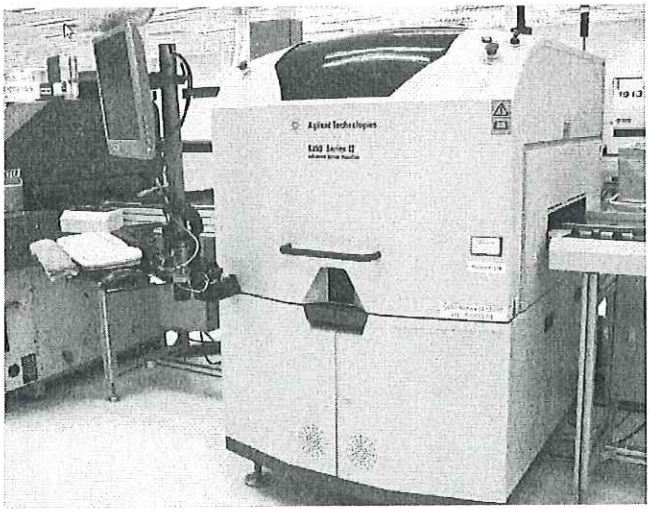
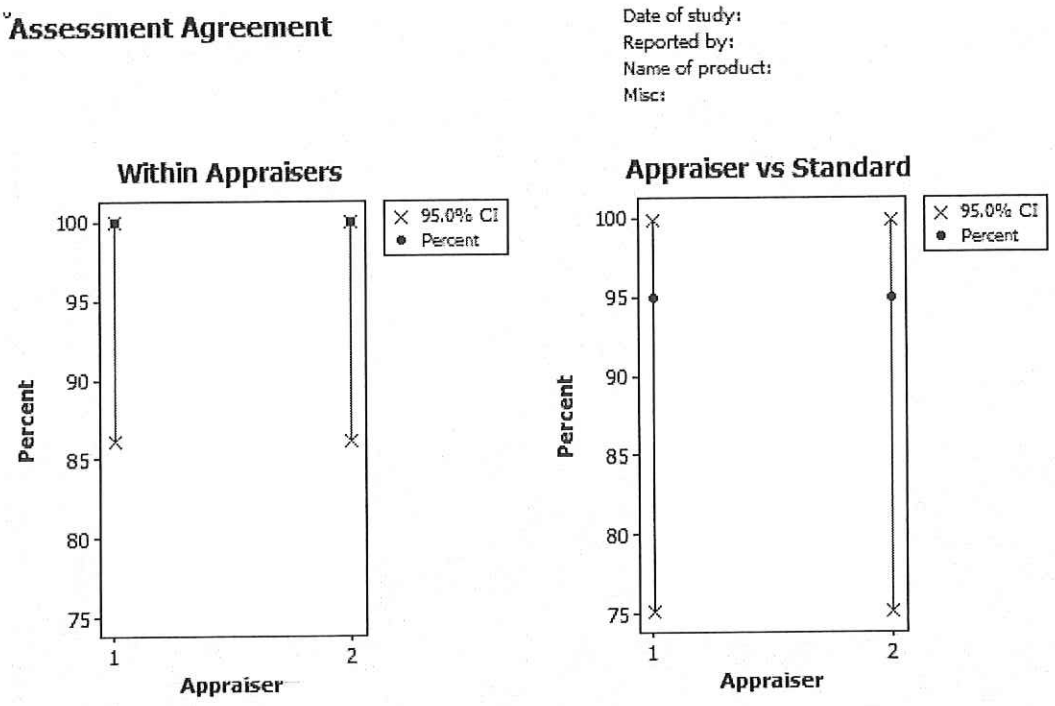


Figure 4.7 AOI Machine# 2

Attribute Gage R & R					
Known Production		Operation/ Machine# 1		Operation/ Machine# 2	
Sample#	Attribute	Trial# 1	Trial# 2	Trial# 1	Trial# 2
1	Pass	Pass	Pass	Pass	Pass
2	Pass	Pass	Pass	Pass	Pass
3	Fail	Fail	Fail	Fail	Fail
4	Pass	Pass	Pass	Pass	Pass
5	Fail	Fail	Fail	Fail	Fail
6	Fail	Fail	Fail	Fail	Fail
7	Fail	Fail	Fail	Fail	Fail
8	Pss	Pass	Pass	Pass	Pass
9	Pass	Pass	Pass	Pass	Pass
10	Pass	Pass	Pass	Pass	Pass
11	Fail	Fail	Fail	Fail	Fail
12	Pass	Fail	Fail	Fail	Fail
13	Fail	Fail	Fail	Fail	Fail
14	Fail	Fail	Fail	Fail	Fail
15	Fail	Fail	Fail	Fail	Fail
16	Pass	Pass	Pass	Pass	Pass
17	Pass	Pass	Pass	Pass	Pass
18	Pass	Pass	Pass	Pass	Pass
19	Pass	Pass	Pass	Pass	Pass
20	Fail	Fail	Fail	Fail	Fail

Table 4.2 Attribute Gage Repeatability and Reproducibility data of AOI Machines

Minitab Result of Gage R& R Study



Attribute Agreement Analysis for Assessments

Within Appraisers

Assessment Agreement

Appraiser	# Inspected	# Matched	Percent	95% CI
1	20	20	100.00	(86.09, 100.00)
2	20	20	100.00	(86.09, 100.00)

Matched: Appraiser agrees with him/herself across trials.

Fleiss' Kappa Statistics

Appraiser	Response	Kappa	SE Kappa	Z	P(vs > 0)
1	Fail	1	0.223607	4.47214	0.0000
	Pass	1	0.223607	4.47214	0.0000
2	Fail	1	0.223607	4.47214	0.0000
	Pass	1	0.223607	4.47214	0.0000

Cohen's Kappa Statistics

Appraiser	Response	Kappa	SE Kappa	Z	P(vs > 0)
1	Fail	1	0.223607	4.47214	0.0000
	Pass	1	0.223607	4.47214	0.0000
2	Fail	1	0.223607	4.47214	0.0000
	Pass	1	0.223607	4.47214	0.0000

Each Appraiser vs Standard

Assessment Agreement

Appraiser	# Inspected	# Matched	Percent	95% CI
1	20	19	95.00	(75.13, 99.87)
2	20	19	95.00	(75.13, 99.87)

Matched: Appraiser's assessment across trials agrees with the known standard.

Assessment Disagreement

Appraiser	# Pass / Fail	Percent	# Fail / Pass	Percent	# Mixed	Percent
1	0	0.00	1	9.09	0	0.00
2	0	0.00	1	9.09	0	0.00

Pass / Fail: Assessments across trials = Pass / standard = Fail.
Fail / Pass: Assessments across trials = Fail / standard = Pass.
Mixed: Assessments across trials are not identical.

Fleiss' Kappa Statistics

Appraiser	Response	Kappa	SE Kappa	Z	P(vs > 0)
1	Fail	0.899749	0.158114	5.69051	0.0000
	Pass	0.899749	0.158114	5.69051	0.0000
2	Fail	0.899749	0.158114	5.69051	0.0000
	Pass	0.899749	0.158114	5.69051	0.0000

Cohen's Kappa Statistics

Appraiser	Response	Kappa	SE Kappa	Z	P(vs > 0)
1	Fail	0.9	0.157321	5.72078	0.0000
	Pass	0.9	0.157321	5.72078	0.0000
2	Fail	0.9	0.157321	5.72078	0.0000
	Pass	0.9	0.157321	5.72078	0.0000

Between Appraisers

Assessment Agreement

# Inspected	# Matched	Percent	95% CI
20	20	100.00	(86.09, 100.00)

Matched: All appraisers' assessments agree with each other.

Fleiss' Kappa Statistics

Response	Kappa	SE Kappa	Z	P(vs > 0)
Fail	1	0.0912871	10.9545	0.0000
Pass	1	0.0912871	10.9545	0.0000

All Appraisers vs Standard

Assessment Agreement

# Inspected	# Matched	Percent	95% CI
20	19	95.00	(75.13, 99.87)

Matched: All appraisers' assessments agree with the known standard.

Fleiss' Kappa Statistics

Response	Kappa	SE Kappa	Z	P(vs > 0)
Fail	0.899749	0.111803	8.04760	0.0000
Pass	0.899749	0.111803	8.04760	0.0000

Cohen's Kappa Statistics

Response	Kappa	SE Kappa	Z	P(vs > 0)
Fail	0.9	0.111243	8.09040	0.0000
Pass	0.9	0.111243	8.09040	0.0000

Summary of Assessment Disagreement with Standard

Appraisers			1		2
Sample	Standard	Count	Percent	Count	Percent
1	Pass	0	0.00	0	0.00
2	Pass	0	0.00	0	0.00
3	Fail	0	0.00	0	0.00
4	Pass	0	0.00	0	0.00
5	Fail	0	0.00	0	0.00
6	Fail	0	0.00	0	0.00
7	Fail	0	0.00	0	0.00
8	Pass	0	0.00	0	0.00
9	Pass	0	0.00	0	0.00
10	Pass	0	0.00	0	0.00
11	Fail	0	0.00	0	0.00
12	Pass	2	100.00	2	100.00
13	Fail	0	0.00	0	0.00
14	Fail	0	0.00	0	0.00
15	Fail	0	0.00	0	0.00
16	Pass	0	0.00	0	0.00
17	Pass	0	0.00	0	0.00
18	Pass	0	0.00	0	0.00
19	Pass	0	0.00	0	0.00
20	Fail	0	0.00	0	0.00

➢ Attribute Agreement Analysis for Assessments

To determine the level of the agreement, the study uses kappa value to measure the overall agreement between the appraisers' assessments within appraisers and those between two appraisers in rating the same objects and the standard.

- Within Appraisers

  The kappa value shows 1 on each which indicates perfect agreements within appraisers

- Between Appraisers

  The kappa values show 1 which the analysis indicates that all appraisers show good agreement between each other.

- Each Appraiser VS Standard

  The agreement of each appraiser to the reference/ known standard shows good agreement with the standard with the kappa value 0.9.

- All Appraisers VS Standard

  The kappa values show 0.9 for all appraisers which show good agreement among all appraisers to the standards.

Note*: The general acceptance criteria of relating kappa to the performance, >/= .9 Excellent, .7-.9 Good, </= .7 Needs Improvement.

- Effectiveness, False Alarm Rate and Miss Rate Analysis
  - Effectiveness

    Hypothesis

    Ho : The effectiveness of Appraisers is the same

    H1 : The effectiveness of Appraisers is not the same

According to the minitab analysis as follows, since the effective rate of each appraiser falls within the confidence interval of the other so the null hypothesis cannot be rejected that indicates no significant difference between two appraisers (AOI1&AOI2) also to the reference standards.

Minitab Analysis Result

Within Appraisers

Assessment Agreement

Appraiser	# Inspected	# Matched	Percent	95% CI
1	20	20	100.00	(86.09, 100.00)
2	20	20	100.00	(86.09, 100.00)

Each Appraiser vs Standard

Assessment Agreement

Appraiser	# Inspected	# Matched	Percent	95% CI
1	20	19	95.00	(75.13, 99.87)
2	20	19	95.00	(75.13, 99.87)

All Appraisers vs Standard

Assessment Agreement

# Inspected	# Matched	Percent	95% CI
20	19	95.00	(75.13, 99.87)

Considering for each appraiser results, the Effectiveness, Miss Rate and Fault Alarm Rate are also taken into consideration.

Effectiveness Rate = 100(number of correct decisions/ total opportunities of a decision)

= 95% for AOI1 and AOI2

Justification and Result: Both AOI1 and AOI2 are acceptable for Effectiveness per acceptance criteria at >/= 90% per Guideline on Table 4.3.

- False Alarm Rate

Fault Alarm Rate = 100(Number of fault alarm/ Number of opportunities for fault alarm)

= 100*(2/40) = 5 % for Appraiser AOI1 and AOI2

Justification and Result : Both AOI1 and AOI2 are acceptable for False Alarm Rate per acceptance criteria at </= 5% per Guideline on Table 4.3.

- Miss Rate

Miss Rate = 100(Number of misses/ Number of opportunities for a miss)

= 100*(0/40) = % for AOI1 and AOI2

Justification and Result : Both AOI1 and AOI2 are acceptable Miss Rate per AIAG reference acceptance criteria at </= 2% per Guideline on Table 4.3.

Decision Measurement system	Effectiveness	Miss Rate	False Alarm Rate
Acceptable for the appraiser	≥ 90%	≤ 2%	≤ 5%
Marginally acceptable for the appraiser – may need improvement	≥ 80%	≤ 5%	≤ 10%
Unacceptable for the appraiser – needs improvement	< 80%	> 5%	≤ 10%

Table 4.3 Effectiveness Acceptance Criteria Guidelines

➢ Conclusion:

The AOI machines used for inspecting the PCBA after SMT process under this research are acceptable per the Attribute Measurement System Study.

4.3 A-Analyze Phase

4.3.1 Identification of cause(s) of defect

According to the identification of the defect pareto and prioritization of the defect criteria to be focused for improvement in the Measure phase, the top defect selected is the Non-wetting defect.

The research further analyzed to see where/ what locations on assemblies were mostly found the non-wetting defect by the pareto of defect locations to focus and analyze for the contributing cause(s). The results as illustrated on the figure 4.8 show majority of locations found the defect on the resister locations; network resistors under the same design of land pads and same/ similar parts.

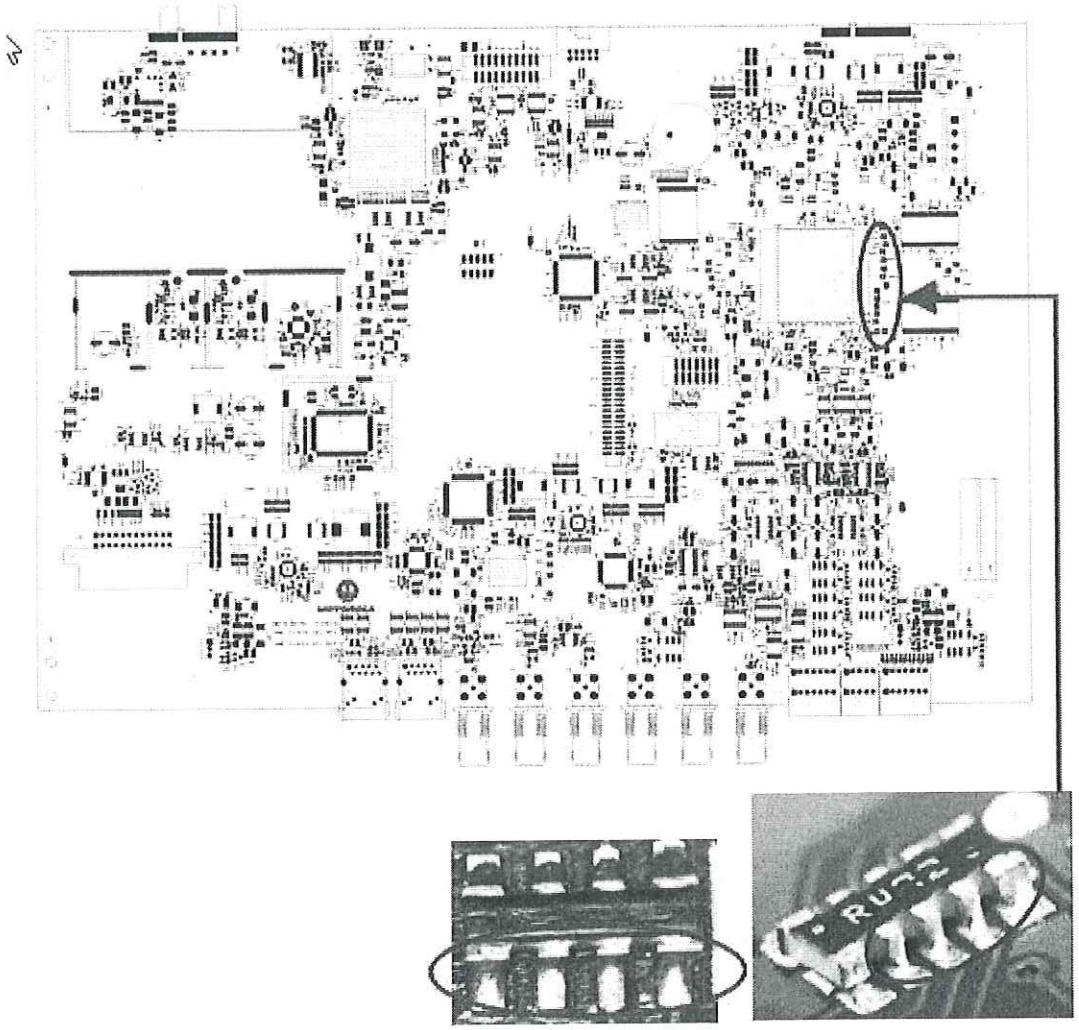


Figure 4.8 PCBA Drawing/ Lay-out & Non-wetting Defect Photos

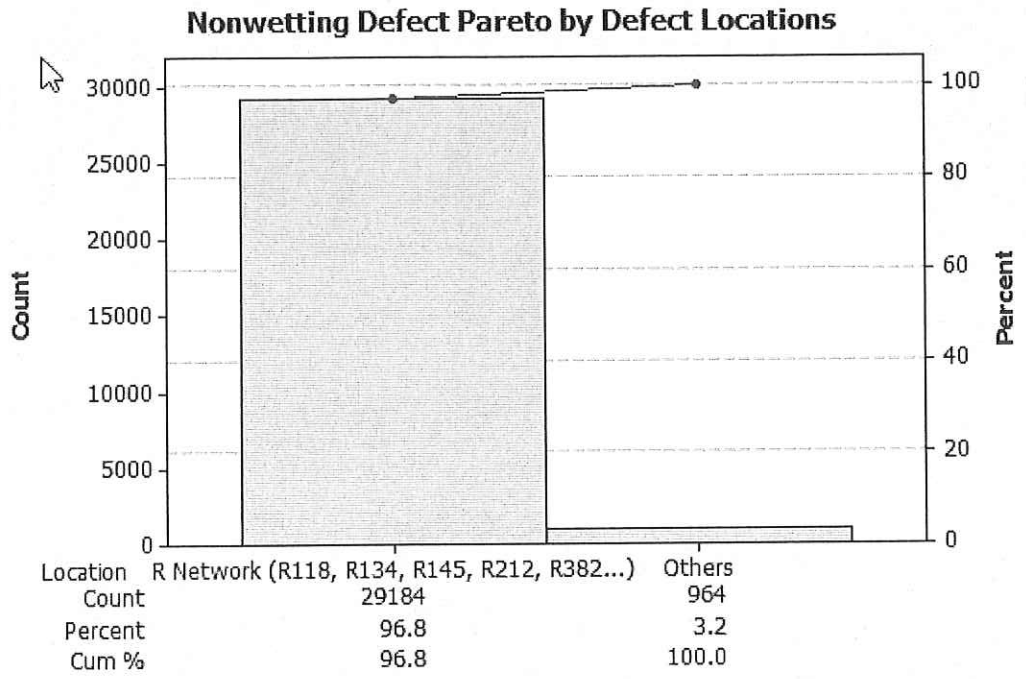


Figure 4.9 Pareto by defect locations of the Non-wetting Defect of the Product AZY

To identify the possible causes of the defect, the research adopted the cause & effect diagram, brainstorming technique. The brainstorming was done among the related members of concerned parties and process experts. The result is shown as the figure 4.8.

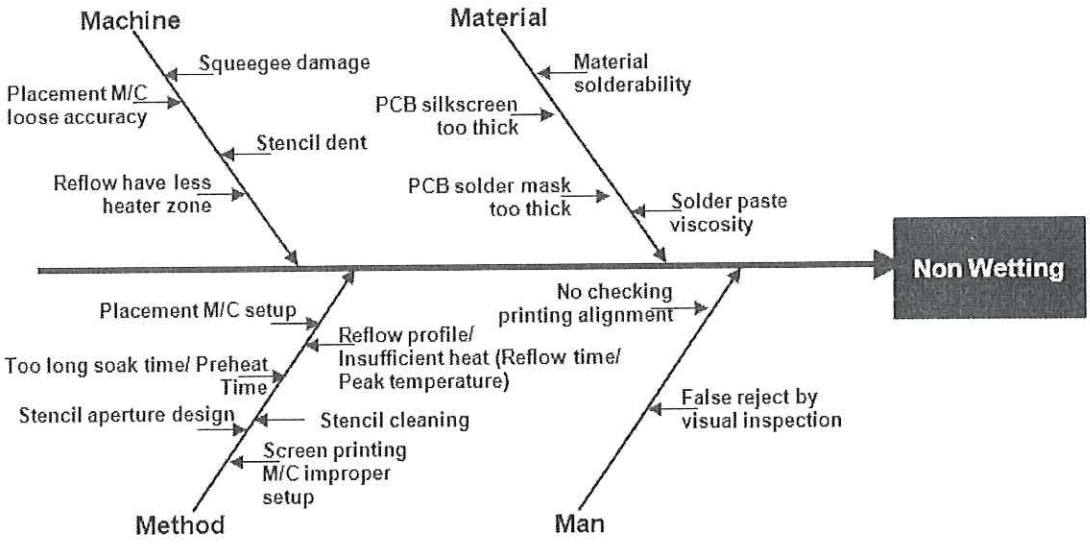


Figure 4.10 Cause & Effect Diagram of Non-wetting Defect of the Product AZY

According to those possible causes defined, to scope down the candidates mostly likely contribute to the defect, the research applied the Failure Mode and Effect Analysis Techniques with the rating guides of Severity, Occurrence and Detection as adopted from traditional quantitative rating (Stamatis, 2003) and adapted to be specific rating and criteria suitable for the product AZY or processes that are being studies, like other cases of researches for example Chulajata, (2011) applied FMEA Technique to analyse failure characteristics and effects including risk defining key process input variables that are critical to the defect and set the specific criteria for rating by modifying from the traditional rating to be suitable with the product that was under studying.

The rating guide of Severity, Occurrence and detection adapted to be suitable for the studying product and processed are shown on Appendix A, B, and C respectively.

According to the FMEA result per Appendix A, the summary of the Severity, Occurrence, Detection and RPN of the high potential causes are shown as table 4.4. The candidates to be tested for significant effects to the defect were selected based on the RPN Value> 100 or top three RPN numbers and supporting rational as follows.

Factor	Severity	Occurrence	Detection	RPN
Stencil Aperture Related	6	6	4	144
Peak Temperature	6	6	3	108
Reflow Time	6	6	3	108

Table 4.4 Failure Mode and Effect Analysis top RPNs of cause candidates of the Non-wetting Defect, Product AZY

According to the Bill of Material review, product lay out drawing on the most locations found non-wetting, they are majority the resistor network locations which are lead free parts while the process itself considering of the rest of the components on the board and the solder paste used is the tin-lead solder (63/37). The terminations of the resistors are made of lead-free solder material which melts at a higher temperature

(217'c) compared to the 63/37 solder which melts at a lower temperature (183'c). According to the Failure Mode and Effect Analysis, the potential factors of Peak Temperature, Reflow Time (Time above Melting Point), Stencil Aperture Design related/ screened solder not properly aligned with the pad most likely contribute the defects with supporting high number of RPNs.

Followings are descriptions and elaborations of those factors.

- Reflow Peak Temperature

Maximum allowable temperature of the entire reflow soldering process. Too high temperature may cause damage to the components as well as intermetallic growth. Conversely, too low temperature may prevent the paste from reflowing appropriately and result in poor wetting. A standard guideline is to subtract 5 °C from the maximum temperature that the most vulnerable component can sustain to arrive at the maximum temperature for process.

- Reflow Time above liquidus (TAL)/ Wetting Time

Time above liquidus" (TAL), or time above reflow, measures how long the solder is a liquid. The flux reduces surface tension at the juncture of the metals to accomplish metallurgical bonding, allowing the individual solder powder spheres to combine. An insufficient time/temperature causes a decrease in the flux's cleaning action, resulting in poor wetting. If the profile time exceeds the manufacturer's specification or too long, the result may be premature flux activation or consumption and cause drying the paste before formation of the solder joint. The reflow time should not be too long but at least a certain time to reduce the chances of an unmeasured area not reflowing. A high minimum reflow time also provides a margin of safety against oven temperature changes. Too little time above liquidus may trap solvents and flux and create the potential for cold or dull joints as well as poor wetting. Additional time above liquidus may cause excessive intermetallic growth, which can lead to joint brittleness.

The board and components may also be damaged at extended times over liquidus. Most components have a well-defined time limit for how long they may be exposed to temperatures over a given maximum.

The reflow oven machine and the reflow process profile are shown as figure 4.11 and 4.12 respectively.

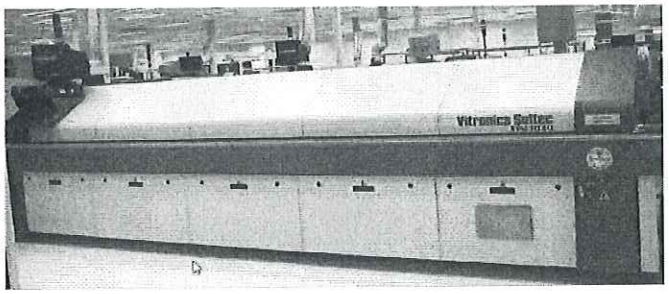


Figure 4.11 Reflow Oven under research

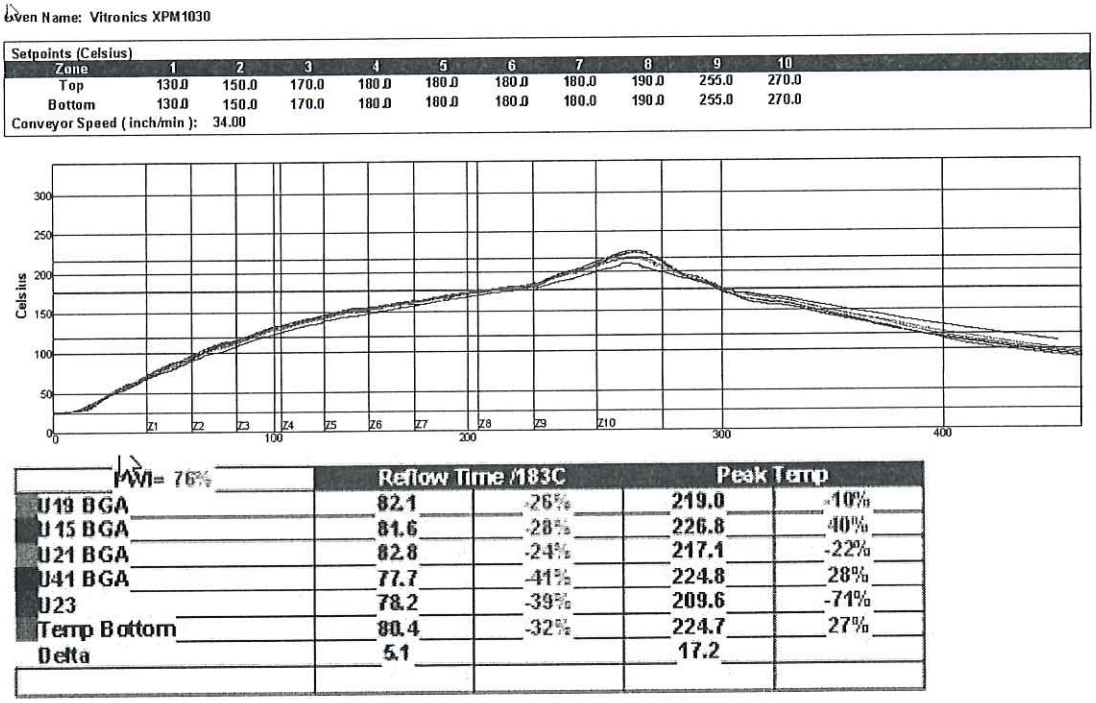


Figure 4.12 Reflow Profile (AS IS)

- Stencil Aperture Opening/ Length

The primary goal of stencil printing is to put the proper amount of solder in the proper location repeatably. The aperture size, shape, and stencil thickness determine the amount of solder deposited, while the position of the aperture determines the location of the deposit.

The opening of stencil aperture which allows the solder paste to be screened on pad should be aligned on pad to ensure proper wetting of solder to the component termination. The length of aperture openings of two counterparts is considered to be a likely potential cause.

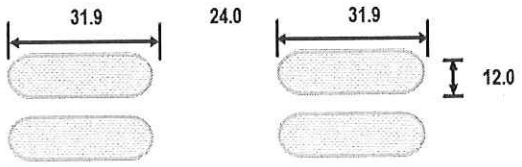


Figure 4.13 Stencil Aperture Opening/ Length

4.3.2 Hypothesis Testing/ Design of Experiment

Typically, the hypothesis testing is used to confirm the validity of the candidates to significantly affect to the occurring of the defects but with the manufacturing practicability and cost concern, this research applied the designed experiments which involve varying two or more variables/ high ranked RPN factors simultaneously for testing the significant effect of the candidates.

The related hypotheses were defined as follows.

- The first hypothesis; the stencil aperture length does not make any difference on the non-wetting defect rates.

Ho: Ps1=Ps2

Where Ps1 and Ps2 are the defect rates of the non-wetting defect of the stencil aperture length treatments

- The second hypothesis; there is no difference between the defect rates of the reflow temp treatments.

  Ho: Pt1=Pt2

Where Pt1, Pt2 are the non-wetting defect rates of the reflow temp treatments

- The third hypothesis; there is no difference between the defect rates of the reflow time above liquidus temp (TAL) treatments.

  Ho: Ptt1=Ptt2

Where Ptt1=Ptt2 are the non-wetting defect rates of the reflow time (TAL) treatments.

- The fourth hypothesis; the effect of the interaction of the two main effects is zero.

The two-level factorial design with two replicates and a center point are used in creating factorial design together with the low level and high level of each candidate parameters adopted from the existing condition of stencil, targeted stencil length per the designed and location of pads, and recommended range of profile parameters by the solder paste manufacturer or manufacturing industry. The experimented design and responses which were recorded in term of defect rate (DPPMc), non-wetting solder defects counted by rejected components per total number of components opportunities of the experimented PCBAs are as detailed in the table 4.5 and 4.6.

Factors/ Parameters	Low Level (-1)	High Level (+1)	Center Point
Aperture Length (Aperture L)	31.9 mm	32.9 mm	32.4
Reflow Peak Temp (Peak Temp)	222'c	240'c	231'c
ReflowTime above Liquidus (TAL)	60 sec	90 sec	75'c

Table 4.5 Experimented Parameters and Levels

StdOrder	RunOrder	CenterPt	Blocks	Aperture L	Peak Temp	TAL	Response
11	1	1	1	30	240	60	4315
14	2	1	1	32	222	90	431
	3	1	1	30	222	60	6149
13	4	1	1	30	222	90	3776
15	5	1	1	30	240	90	1079
17	6	0	1	31	231	75	2373
4	7	1	1	32	240	60	1798
3	8	1	1	30	240	60	4854
12	9	1	1	32	240	60	1654
6	10	1	1	32	222	90	647
7	11	1	1	30	240	90	1618
5	12	1	1	30	222	90	3236
16	13	1	1	32	240	90	144
2	14	1	1	32	222	60	2697
10	15	1	1	32	222	60	2481
9	16	1	1	30	222	60	6257
8	17	1	1	32	240	90	216

Table 4.6 Experimented Parameters and Results with Center Point

The DOE factorial analysis results from minitab analysis are shown and can be discussed as follows.

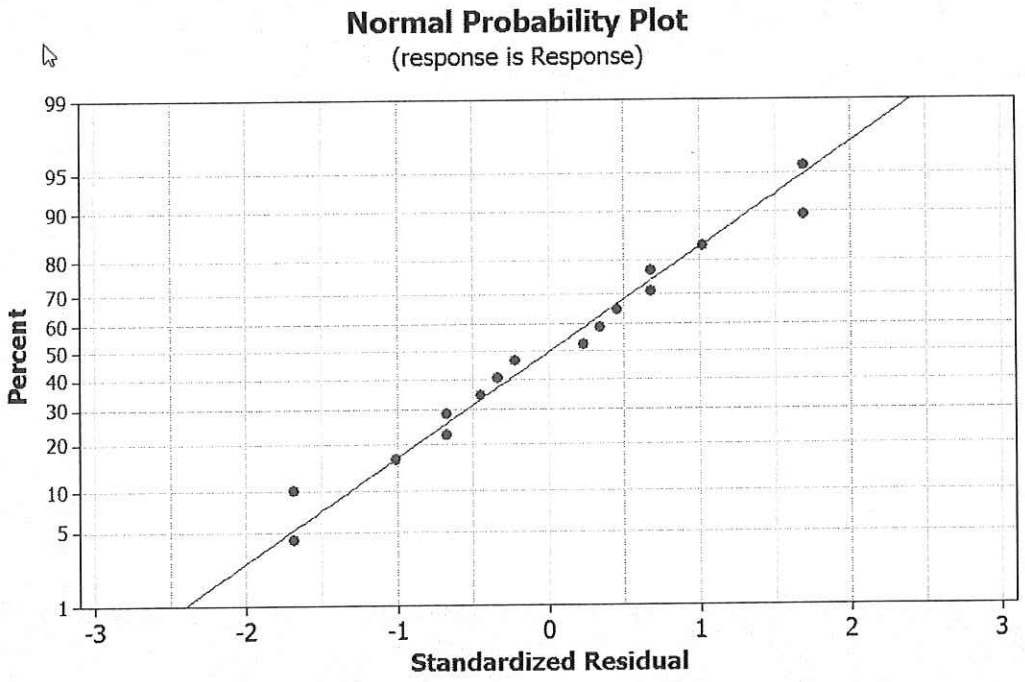


Figure 4.14 Residuals from Experimental Model

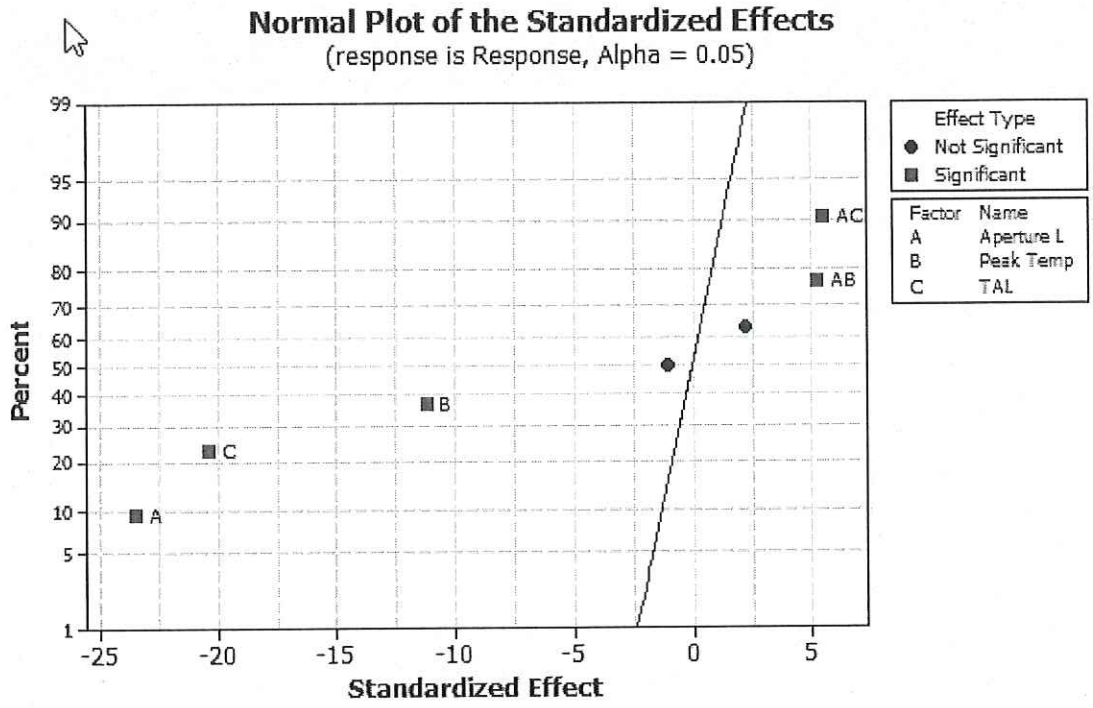


Figure 4.15 Significant Factor Effects

Results for: MINITABNWFNEW.MTW

Factorial Fit: Response versus Aperture L, Peak Temp, TAL

Estimated Effects and Coefficients for Response (coded units)

Term	Effect	Coef	SE Coef	T	P
Constant		2585	62.61	41.28	0.000
Aperture L	-2652	-1326	62.61	-21.18	0.000
Peak Temp	-1250	-625	62.61	-9.98	0.000
TAL	-2382	-1191	62.61	-19.03	0.000
Aperture L*Peak Temp	638	319	62.61	5.10	0.001
Aperture L*TAL	584	292	62.61	4.67	0.002
Peak Temp*TAL	-9	-4	62.61	-0.07	0.945
Aperture L*Peak Temp*TAL	261	130	62.61	2.08	0.071
Ct Pt		-212	258.13	-0.82	0.436

S = 250.427 PRESS = 2057740
R-Sq = 99.18% R-Sq(pred) = 96.62% R-Sq(adj) = 98.35%

Analysis of Variance for Response (coded units)

Source	DF	Seq SS	Adj SS	Adj MS	F	P
Main Effects	3	57079087	57079087	19026362	303.39	0.000
Aperture L	1	28132050	28132050	28132050	448.58	0.000
Peak Temp	1	6246096	6246096	6246096	99.60	0.000
TAL	1	22700942	22700942	22700942	361.98	0.000
2-Way Interactions	3	2996023	2996023	998674	15.92	0.001
Aperture L*Peak Temp	1	1629699	1629699	1629699	25.99	0.001
Aperture L*TAL	1	1366005	1366005	1366005	21.78	0.002
Peak Temp*TAL	1	319	319	319	0.01	0.945
3-Way Interactions	1	271772	271772	271772	4.33	0.071
Aperture L*Peak Temp*TAL	1	271772	271772	271772	4.33	0.071
Curvature	1	42109	42109	42109	0.67	0.436
Residual Error	8	501709	501709	62714		
Pure Error	8	501709	501709	62714		
Total	16	60890701				

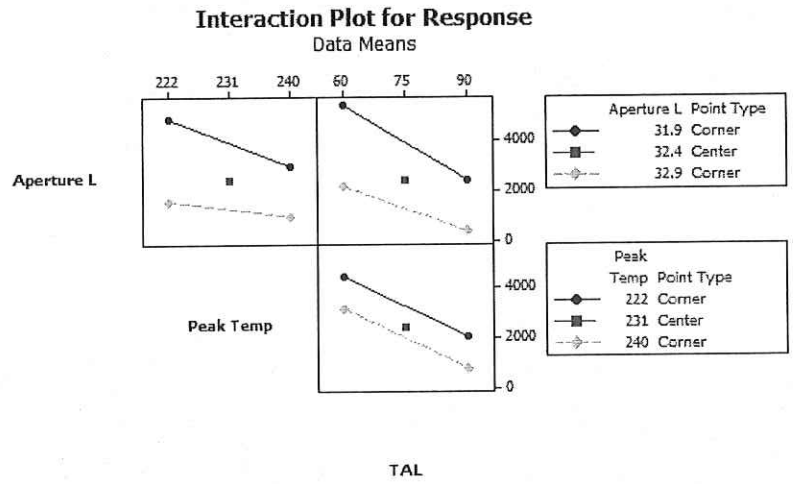


Figure 4.16 Interaction Plot for Response

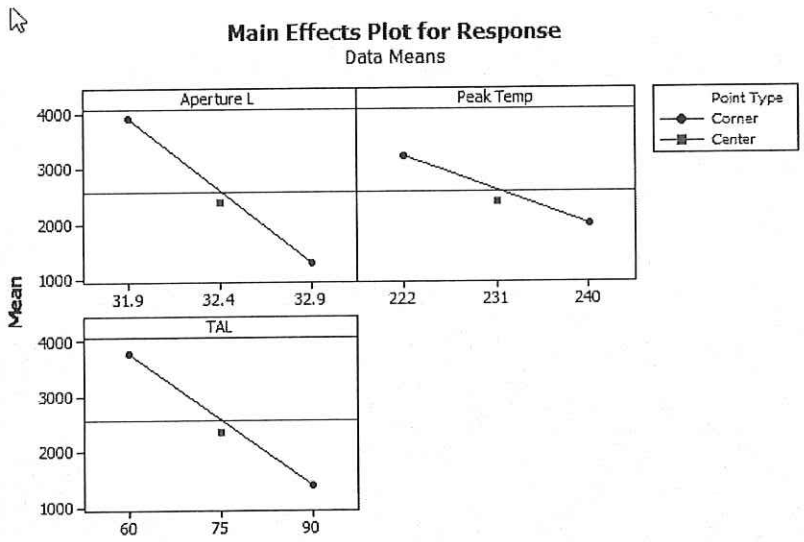


Figure 4.17 Main Effects Plot for Response

According to the Minitab statistical plots and analysis results, Figure 4.12 shows a normal probability plot of the experimental effects. Most residuals fall along a straight line which the fit of the model was adequate. The minitab analysis and normal plot of the standardized effects, per figure 4.13 indicate that factor A (Aperture Length), factor B (Peak Temp), factor C (Reflow Time), AB (Aperture Length and Peak Temp) and AC (Aperture Length and Reflow Time) produce significant effects and account for by random variation (P value>0.05). The center point/ curvature were confirmed no significant effect and the model could be assumed as linear relationship. The interaction plot and main effects plot for response of the significant factors are graphed in figure 4.14 and 4.15 respectively.

Since the analysis showed that the factor BC and AB do not produce significant effects and no curvature effect, then those factors were omitted from the analysis or reduced from the model. The experimented parameters and results were shown as table 4.7. The minitab analysis was redone and results were shown as figure 4.16, 4.17, 4.18, 4.19 and minitab outputs

StdOrder	RunOrder	CenterPt	Blocks	Aperture L	Peak Temp	TAL	Response
11	1	1	1	30	240	60	4315
14	2	1	1	32	222	90	431
1	3	1	1	30	222	60	6149
13	4	1	1	30	222	90	3776
15	5	1	1	30	240	90	1079
4	7	1	1	32	240	60	1798
3	8	1	1	30	240	60	4854
12	9	1	1	32	240	60	1654
6	10	1	1	32	222	90	647
7	11	1	1	30	240	90	1618
5	12	1	1	30	222	90	3236
16	13	1	1	32	240	90	144
2	14	1	1	32	222	60	2697
10	15	1	1	32	222	60	2481
9	16	1	1	30	222	60	6257
8	17	1	1	32	240	90	216

Table 4.7 Experimented Parameters and Results without Center Point

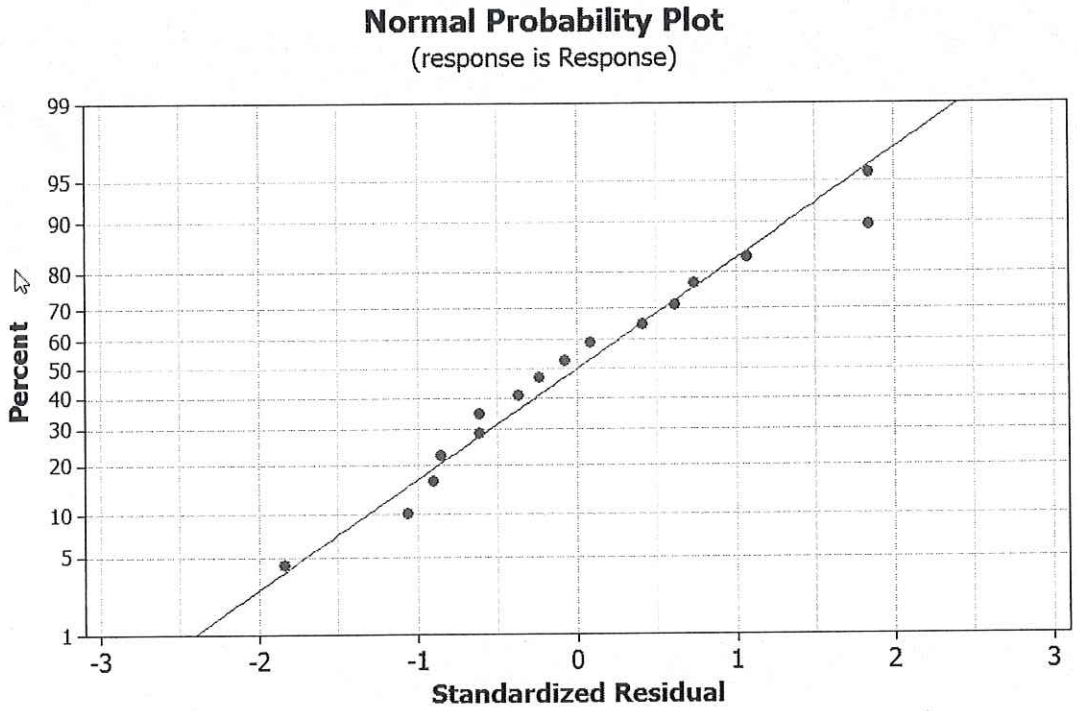


Figure 4.18 Residuals from Experimental Model

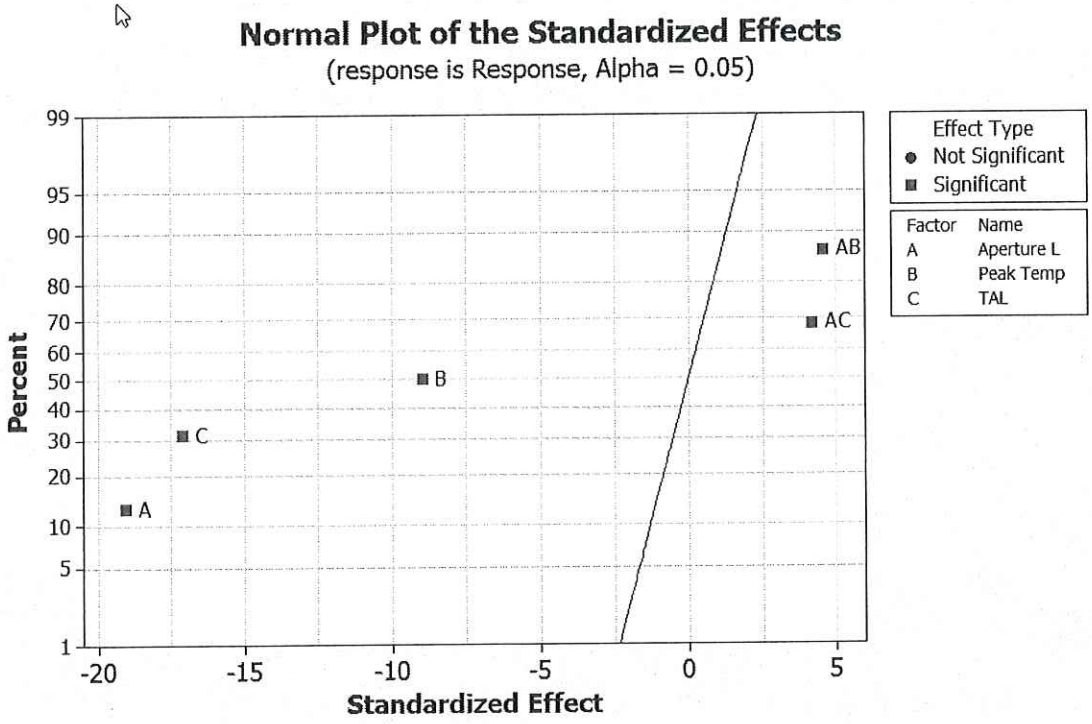


Figure 4.19 Significant Factors Effects

Factorial Fit: Response versus Aperture L, Peak Temp, TAL

Estimated Effects and Coefficients for Response (coded units)

Term	Effect	Coef	SE Coef	T	P
Constant		2585	69.54	37.16	0.000
Aperture L	-2652	-1326	69.54	-19.07	0.000
Peak Temp	-1250	-625	69.54	-8.98	0.000
TAL	-2382	-1191	69.54	-17.13	0.000
Aperture L*Peak Temp	638	319	69.54	4.59	0.001
Aperture L*TAL	584	292	69.54	4.20	0.002

S = 278.173 PRESS = 1980928
R-Sq = 98.73% R-Sq(pred) = 96.74% R-Sq(adj) = 98.09%

Analysis of Variance for Response (coded units)

Source	DF	Seq SS	Adj SS	Adj MS	F	P
Main Effects	3	57079087	57079087	19026362	245.88	0.000
Aperture L	1	28132050	28132050	28132050	363.56	0.000
Peak Temp	1	6246096	6246096	6246096	80.72	0.000
TAL	1	22700942	22700942	22700942	293.37	0.000
2-Way Interactions	2	2995704	2995704	1497852	19.36	0.000
Aperture L*Peak Temp	1	1629699	1629699	1629699	21.06	0.001
Aperture L*TAL	1	1366005	1366005	1366005	17.65	0.002
Residual Error	10	773800	773800	77380		
Lack of Fit	2	272091	272091	136046	2.17	0.177
Pure Error	8	501709	501709	62714		
Total	15	60848591				

Estimated Coefficients for Response using data in uncoded units

Term	Coef
Constant	736001
Aperture L	-21957.6
Peak Temp	-2367.41
TAL	-1341.61
Aperture L*Peak Temp	70.9256
Aperture L*TAL	38.9566

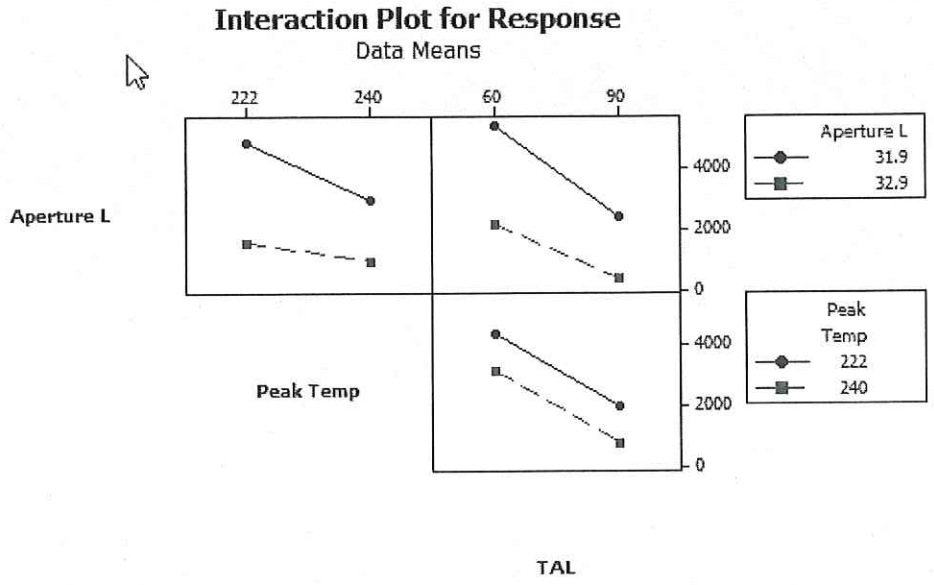


Figure 4.20 Interaction Plot for Response

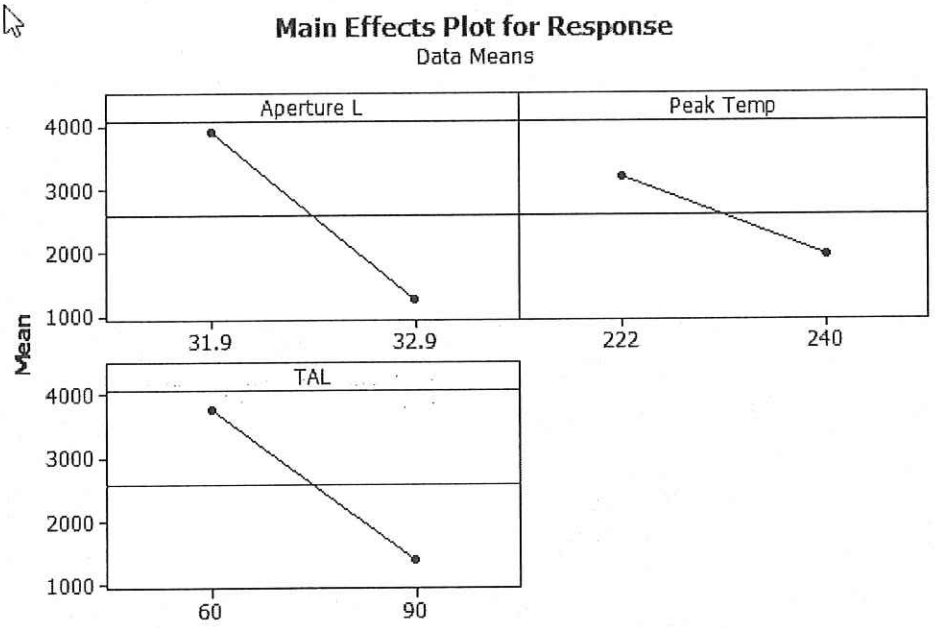


Figure 4.21 Main Effect Plot for Response

The Minitab results confirm the similar result as before with P value > 0.05 tell that the stencil aperture design (Aperture length/ L), Reflow Peak Temperature (Peak Temp) and Reflow Time (Time above Liquidius / TAL) including the interaction of Aperture L and Peak Temp, Aperture L and TAL significantly affect to the defect rate of

the PCBA of Product AYZ. The lack of fit is not significant (P value <0.05) which support this model is fine with the below coefficients.

Estimated Coefficients for Response using data in uncoded units

Term	Coef
Constant	736001
Aperture L	-21957.6
Peak Temp	-2367.41
TAL	-1341.61
Aperture L*Peak Temp	70.9256
Aperture L*TAL	38.9566

The linear model for estimating the defect rate was found to be;

Y= 736001-21957.6 Aperture L-2367.41Peak Temp-1341.61TAL+70.9256 Aperture L*Peak Temp+38.9566 Aperture L*TAL

4.4 I-Improvement Phase

According to the Minitab analysis, the defect rate model was found to be Y= 736001-21957.6 Aperture L-2367.41Peak Temp-1341.61TAL+70.9256 Aperture L*Peak Temp+38.9566 Aperture L*TAL

4.4.1 Optimization

- Stencil Aperture Length

  The stencil aperture length was increased to be longer as figure 4.20. The new stencil was ordered and implemented to replace the existing one.

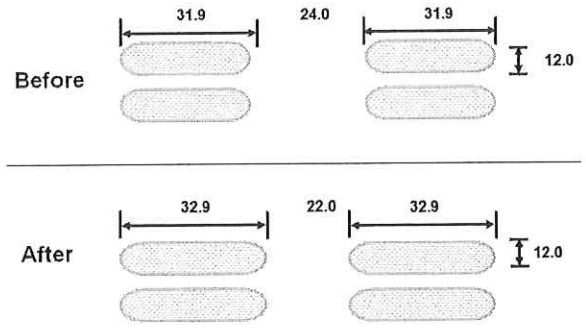


Figure 4.22 Stencil Aperture Improvement

➢ Peak Temperature and Reflow Temperature (TAL)

With the optimization plot by minitab per figure 4.21, it was found that the best/ minimum response that could get is at 53.9273 DPPMc at the high level of the significant effect factors. However, despite the improved non-wetting solder defect rate, it is noticed that at the uppermost of general recommended range of reflow peak temp and reflow time, the components on assemblies could be affected such as burnt/ crack or reliability related. With these concerns together related recommendation by the components manufacturers, the selected limits of peak temp were put the guard band down 5'c from the generic allowable max limit which is around 235'c. According to the simulation of the optimization plot for the peak team at 235'c, the defect rate is higher and up to around 221 DPPM, see figure 4.22 which is considered still acceptable per the proportion of improvement of non-wetting defect to support the overall DPPMs rate.

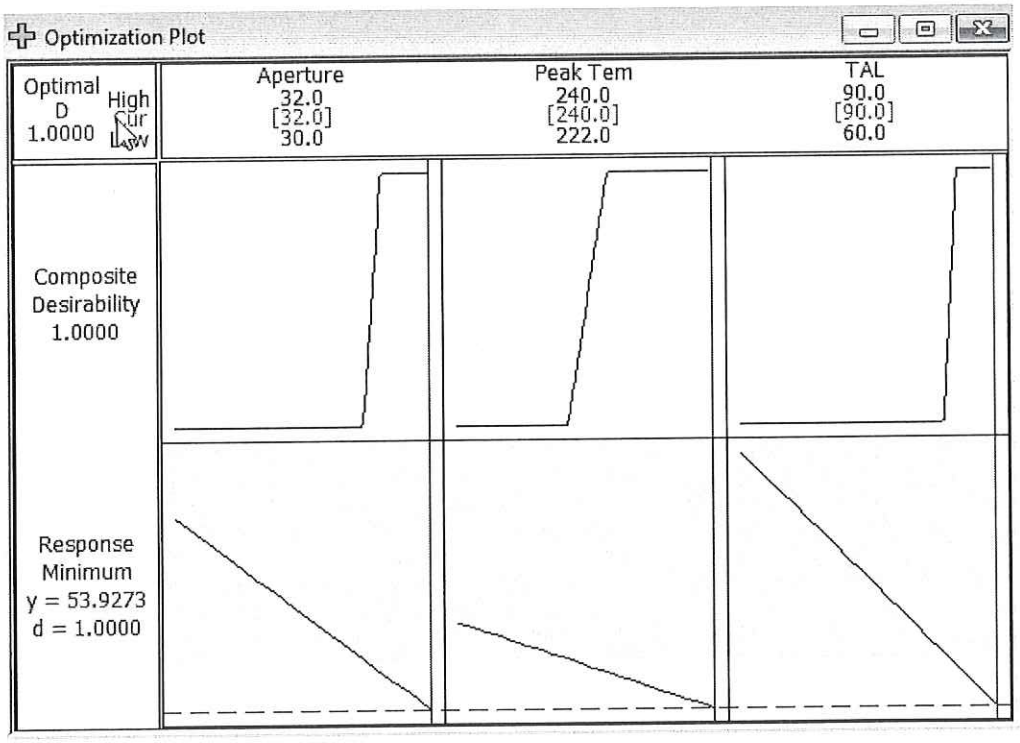


Figure 4.23 Optimization Plot

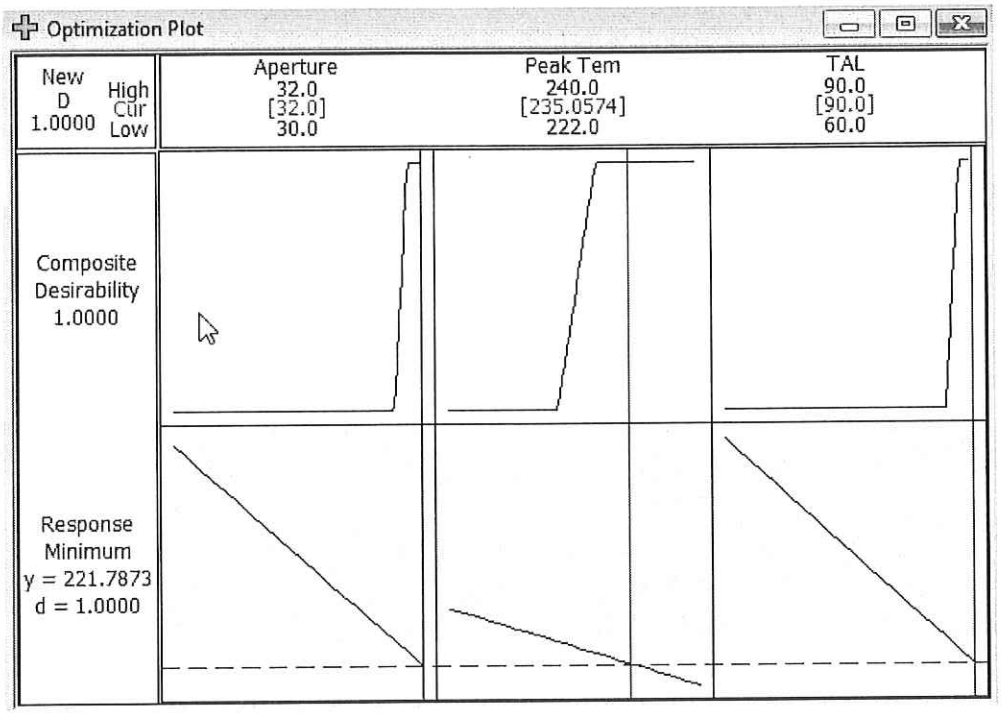
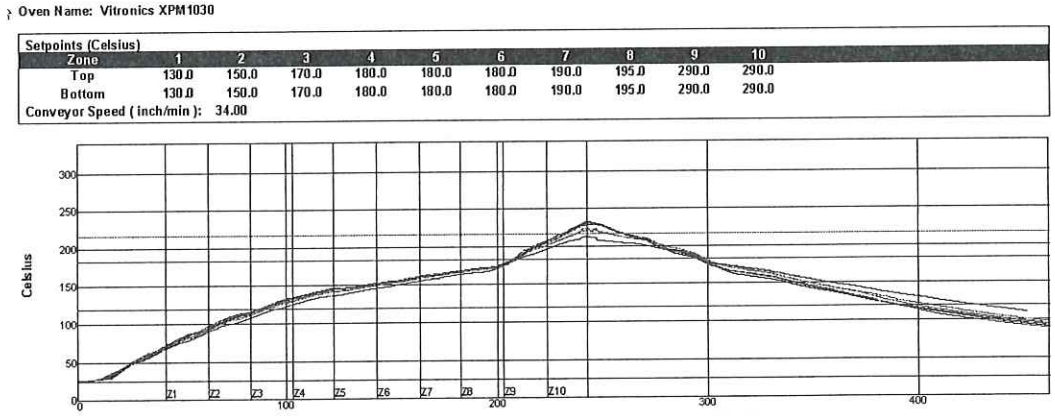


Figure 4.24 Optimization Plot upon reduced peak temp 5'c

4.4.2 Verify improved results by actual set up, run and confirm results

The experiment settings and results are confirmed with the actual runs with a number of repeating per optimized parameters considering of interaction of affecting factors and main affect factors. The profile readings of reflow time and peak temp measured on critical locations on PCBA are shown as figure 4.25.



	Reflow Time /183C	Peak Temp
U19 BGA	90.4	225.7
U15 BGA	89.9	235.1
U21 BGA	91.0	223.7
U41 BGA	85.7	233.1
U23	86.0	213.9
Temp Bottom	89.8	233.3
Delta	5.2	25.6

Figure 4.25 Reflow Profile per the optimized parameters and readings

The experimented results before and after improvements are shown on table 4.8 and 4.9 for Non-wetting defect rate and overall defect rate respectively.

No.	Non-wetting Defect Rate	
	Before Improvement	After improvement
1	4465	216
2	4565	270
3	4289	216
4	4462	216
5	4715	324
6		270
7		270
8		216
9		270
10		216
Average	4499	248
Median	4465	243

Table 4.8 DPPMc data of Non-wetting defect before and after Improvement

Mann-Whitney Test and CI: Before, After

```
         N  Median
Before   5  4465.0
After   10   243.0

Point estimate for ETA1-ETA2 is 4246.0
95.7 Percent CI for ETA1-ETA2 is (4072.9,4445.1)
W = 65.0
Test of ETA1 = ETA2 vs ETA1 not = ETA2 is significant at 0.0027
The test is significant at 0.0020 (adjusted for ties)
```

From the confirmed results and minitab analysis output of Non-wetting Defect rate, the DPPMc after improvement is significantly different from before improvement. The P-value of 0.002 is less than 0.05 (α level of 0.05), we can reject the null hypothesis and conclude that there is significant difference between before and after improvements.

Other then the non-wetting defect is confirmed significantly improved, the overall defect rate are also confirmed reduced and significantly improved and no negative side effect of non-wetting issue fixing to create other defects or increase in overall defect rate

but conversely the overall defect rate is confirmed significantly improved and satisfy the set goals.

No.	Oveall Defect Rate	
	Before Improvement	After improvement
1	4612	591
2	4801	608
3	4962	615
4	4908	562
5	5070	560
6		634
7		587
8		569
9		621
10		554
Average	4871	587
Median	4908	589

Table 4.9 DPPMc data of Overall defect before and after Improvement

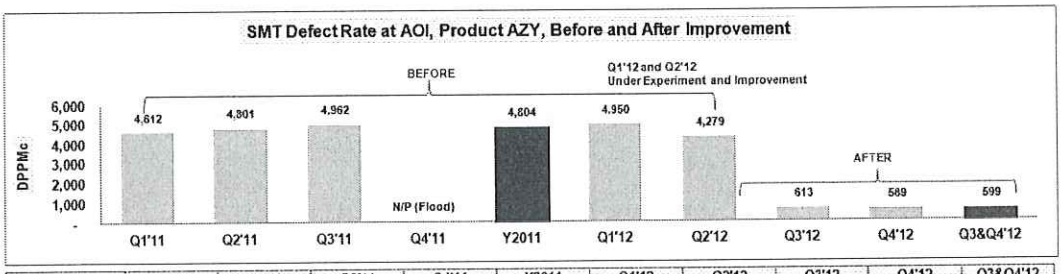
Mann-Whitney Test and CI: Alldefectbefore, Afterdefectafter

```
                    N  Median
Alldefectbefore     5  4908.0
Afterdefectafter   10   589.0

Point estimate for ETA1-ETA2 is 4319.0
95.7 Percent CI for ETA1-ETA2 is (4052.0,4449.0)
W = 65.0
Test of ETA1 = ETA2 vs ETA1 not = ETA2 is significant at 0.0027
```

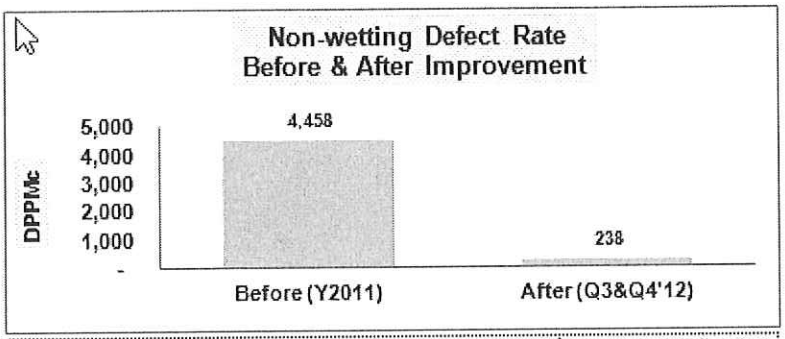
4.4.3 On-going Results

The on-going production run has been continued with result monitoring as shown in figure 4.26 for overall performance, figure 4.27 for Non-wetting Defect Rate comparison between Y2011(before improvement) and Q3 and Q4 of Y2012 (after improvement) and figure 4.28 for comparison against the company goal.



	Q1'11	Q2'11	Q3'11	Q4'11	Y2011	Q1'12	Q2'12	Q3'12	Q4'12	Q3&Q4'12
Total	1,133	1,124	1,391	N/P	3,648	1,296	1,499	1,349	1,755	3,104
Total Points	2,100,582	2,083,896	2,578,914	N/P	6,763,392	2,402,784	2,779,146	2,501,046	3,253,770	5,754,816
Defect Points	9,687	10,004	12,797	N/P	32,488	11,894	11,891	1,532	1,915	3,447
DPPMc	4,612	4,801	4,962		4,804	4,950	4,279	613	589	599

Figure 4.26 Historical Performance of SMT Defect Rate Before and After Improvement



	Before (Y2011)	After (Q3&Q4'12)
Total Units	3,648	3,104
Total Component Points	6,763,392	5,754,816
Non-wetting Defect Points	30,148	1,370
DPPMc	4,458	238

Figure 4.27 Non-wetting Defect Rate Before and After Improvement

	BEFORE	AFTER	
	Y2011 DPPMc	Q3&Q4'12 DPPMc	Goal DPPMc
Overall Defect Rate	4,804	599	680
Non-wetting Defect Rate	4,458	238	N/A

Figure 4.28 Before and After Improvement Defect Rate Comparison VS Goal

4.5 C-Control Phase

In order to ensure the long lasting result, the changes made in the Improve Phase need to be controlled. From the Improved Phase, the set up and controlled parameters need to be documented for set up procedures to follow, also monitored periodically or when set up. Followings are what are implemented to be the controls.

4.5.1 Process FMEA and Control Plan update to reflect the new changes

The product FMEA and Control Plan were updated to reflect the solutions and controls put in place per Appendix F and G.

4.5.2 Reflow Profile Set Up Parameter Log Record

Based on the finalized optimized parameters, the Reflow Oven Set Up Parameters for each Zone are settled by the machine programming and updated into the Log Record to be record and guideline for Technician for reference of future set up or when need to set up on other SMT line which is needed to support on production of this product. See figure 4.29.

ABC Electronics — **Reflow Profile Record** — Revision: B

Record Owner: Process Engineer

LINE #: 9

MACHINE NO.: XPM1030 — ASSY. NO. : AZY001

MACHINE NAME: VITRONICS SOLTEC — ASSY. NAME : AZY

MACHINE TYPE: HOT AIR REFLOW — PROFILE NAME : A9351CB

NO	ZONE NAME	PARAMETER SETUP			
1	ZONE 1 TOP	130.0	130.0		
2	ZONE 2 TOP	150.0	150.0		
3	ZONE 3 TOP	170.0	170.0		
4	ZONE 4 TOP	190.0	190.0		
5	ZONE 5 TOP	185.0	185.0		
6	ZONE 6 TOP	180.0	180.0		
7	ZONE 7 TOP	180.0	210.0		
8	ZONE 8 TOP	190.0	195.0		
9	ZONE 9 TOP	255.0	200.0		
10	ZONE 10 TOP	270.0	210.0		
		Rev. A	Rev. B		
BELT SPEED		2.8 in/min	3.1 in/min		
DATE		Jan 05 '11	Jan 21'12		
ENGINEER/TECHNICIAN		[illegible]	[illegible]		
REMARK		ADJUST for Rev. B	ADJUST for Rev. B	ADJUST	ADJUST
Tolerance :		☐ Preheat time	☐ Preheat time	☐ Preheat time	☐ Preheat time
+/-10 degree C for Present Value		☐ Soaking time	☐ Soaking time	☐ Soaking time	☐ Soaking time
		☐ Reflow time	☑ Reflow time	☐ Reflow time	☐ Reflow time
		☐ Slope	☐ Slope	☐ Slope	☐ Slope
		☐ Max temperature	☑ Max temperature	☐ Max temperature	☐ Max temperature
		☑ Others :	☐ Others :	☐ Others :	☐ Others :
		REASON : New SETUP	REASON : Optimize Parameters	REASON :	REASON :

Figure 4.29 Reflow Profile Log

4.5.3 Reflow Profile Report

The profile is recommended to check by running through the profile board with thermocouple on every set up to monitor and ensure on set up and control, see figure 4.30. The Profile Report is printed by running through the profile board with thermo couple attached on the critical components and passing through the oven to measure and get the profiling of each step of the process, see figure 4.31.

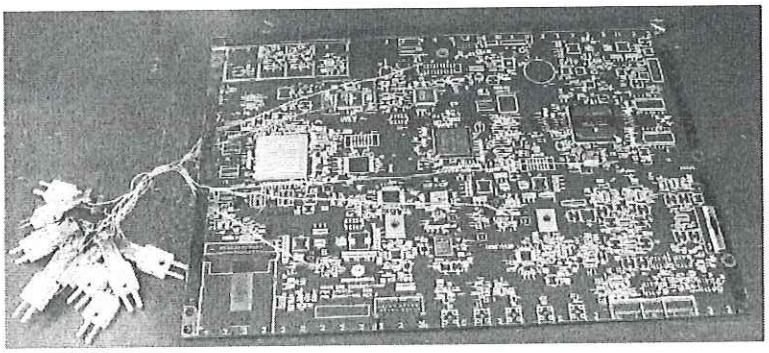


Figure 4.30 Profile Board and Thermocouple

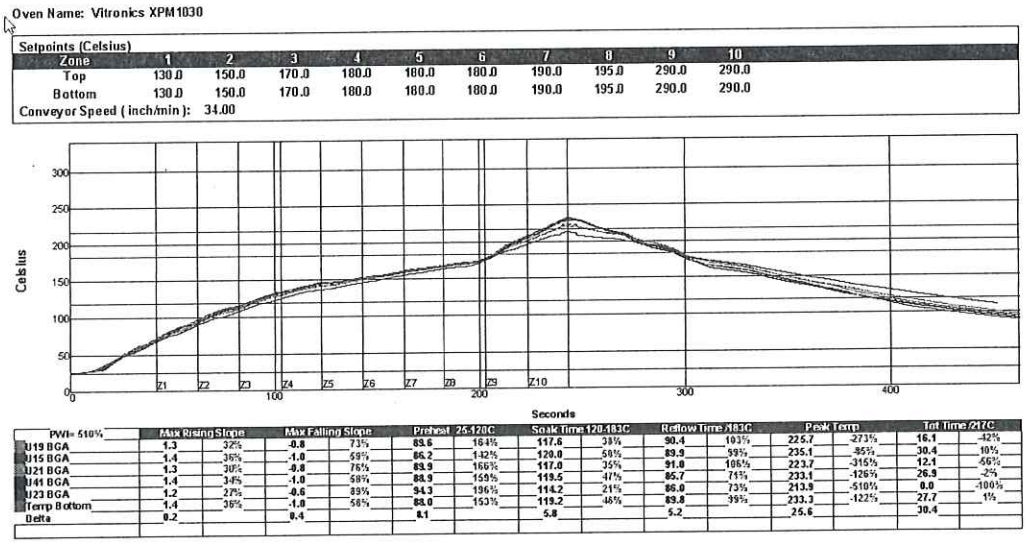


Figure 4.31 Reflow Profile Report

4.5.4 Defect Tracking and DPPMc Monitoring Control Chart

The statistical control chart by DPPMc has been implemented and maintained to monitor the defect rate performance and control, see figure 4.32.

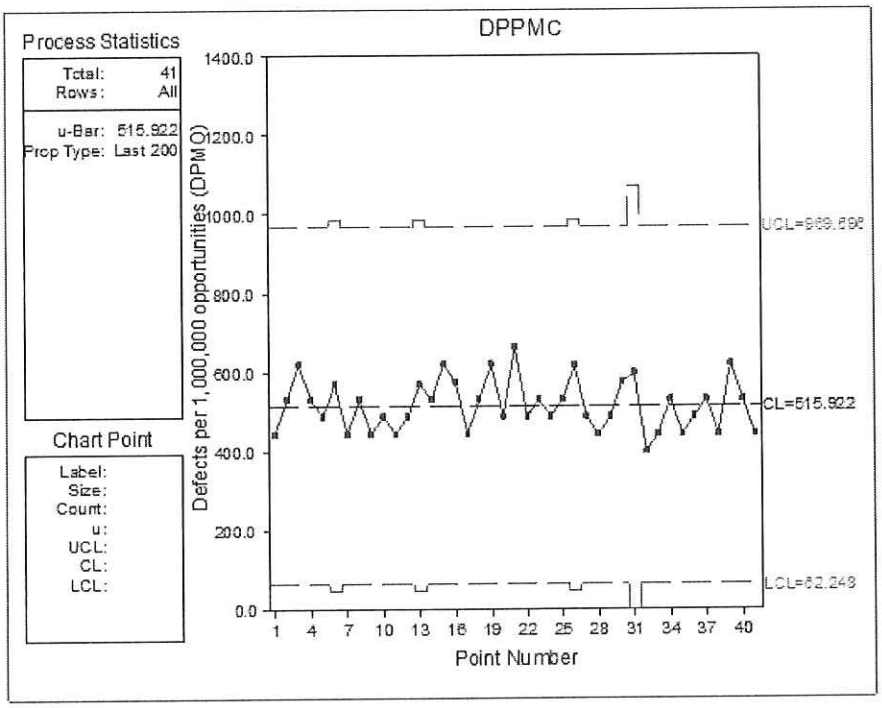


Figure 4.32 On-going Defect Rate Tracking and Statistical Control

4.5.5 Ongoing Process Audit and Control

The reflow temperature set up by each zone should be audited periodically by checking the reading on machine screen showing to ensure the proper set up is maintained per log record. The monitoring result record is shown as appendix H.

4.5.6 New Production Order Set Up Check List

The list of items to be ensured for every set up of SMT process including correct stencil, reflow profile has been used to control of set up and release for every production order set up, see appendix I.

CHAPTER V
CONCLUSION AND RECOMMENDATION

A lot of quality problems or defects in manufacturing are generally considered as typical and chronic issues for many manufacturing companies despite the differences in the business. The approach in problem solving like DMAIC approach can be adopted by any company or business no matter big or small or what type of businesses are. Followings are the conclusion of the research, limitation and further recommendations to again benefits from this research.

5.1 Conclusion of the Research

The objectives of this research were met. This research had implemented the DMAIC approach to the quality improvement of Printed Circuit Board Assembly that helped to Define the right project for improvement by focusing at the SMT processes which mainly contribute high defects and were bottle neck to other subsequent processes due to time loss in reworking, Measure the data to prioritize what defects mostly contributed to the overall defect rate, confirm the validity of the data, Analyse the potential cause (s) to see what significantly affect to the studied defects , Improve by identifying and implementing the optimal settings of the critical to quality factors inducing the defects by DOE and verifying results, with the results, the reflow profile parameters i.e. Peak Temperature and Reflow Time were adjusted together with the replacing with the new designed stencil with extending in length to enhance the alignment of printed solder paste to the PCB pad to support of better solder wetting and put in Control for those optimized setting and achieved results. With those, the company could achieve in reducing process variations, defect rate according to the improvement objectives. The research was successful by leading the case study company to apply the DMAIC concept for improvement of the on-going and chronic problem of a key product and achieve the improvement objectives. The key of success is applying the right approach, using right tools and maintaining the gains.

The research confirmed that the quality level of the PCBA manufacturing process could be improved from 4804 DPPMc to be 599 DPPMc (87.53% improved)

with DMAIC approach. The factors confirmed significantly affect to the defect rate of the top defect focused in improvement (non-wetting soldering defect) are the reflow profile peak temperature, reflow time/ TAL (time above liquidius) and solder paste screening stencil aperture opening length to align with the pads of PCB. The outcome of this case study is the optimized process parameters of those affecting factors; the reflow profile peak temperature: 240'c, Reflow Time: 90 sec. Solder paste screening stencil aperture opening length to align with the pads of PCB : 32.9 mm. However, the peak temperature was a bit reduced to 235'c to be safe to the components based on the recommendation of component manufacturing and observation of component burnt during experiment. With those optimized parameter implementation, the result showed improvement 87.53% over a monitoring studying period. It is concluded from the study that the quality level is lying with the related manufacturing process and the improvement could be achieved by the systematic applying of DMAIC approach.

5.2 Limitation of the Research

There were some limitations of this research which were financial aspects and some others as following.

5.2.1 Financial Aspects and other benefits measurements

This research lacked of financial aspects in the determination of the improvements in term of cost saving aspect other than the significantly reduced defect rate including other measurements of success or benefits to other subsequent processes or other performances as resulted from the improvement other than the defect rate reduction of the improvement project itself. However it can be assumed that by significant improving defect rate of the high contributing processes, the case study company is expected to gain higher profitability, productivity and other benefits by less rework, less cost of poor quality, being quick and high throughputs, less in manufacturing cycle time and higher efficiency in operations. Moreover, the research did not take into account of the cost required in establishing the efforts to carry out the improvement project.

5.2.2 Further Improvements

The limitations also include lacking of further improvement to further drive the defect rate to be lower by considering and extending to other low priority concerned factors that might contribute and be ongoing inducing variations and contributing some on-going defects or other defects.

5.2.3 More choices of solution/ opportunity in getting better results

There might be other alternatives to support lower defect rate which this research were not taken into account for examples;

- The review of the product design/ component on board layout change that might resolve the issue. Anyway, there would be cost effect and the limitation of design change due to turned key design or flexibility/ concern of the customer for accepting of the product design change.

- Fine tuned parameter adjustment

  The peak temperature was deviated from the originally optimized and best result due to component safety factor recommendation from the manufacturer. However, from the optimization plot, it was seen that there might be some room for better fine tune of peak temperature to get the better defect rate. Instead of one time reduction 5'c from the best optimized parameter and result, the fine tune in reduction of temperature to sustain the results or gain better result than the research result within the tolerable range of component to heat.

5.3 Extension/ Recommendations

Certainly, although the results of improvement can achieve according to the objective of the project according the complexity of the product and the defined project time frame, to achieve the world class manufacturing level, and support continuing

improvement to achieve six sigma quality level including some limitations as mentioned previously, further improvements should be continued as follows;

Extending to other potential factors/ causes under lower Rank Priority Number (RPN) as defined on the FMEA and Cause and Effect Analysis for further room of improvements including consideration of further improvement of other defects which are on the pareto analysis.

Further studying and considering of other solutions like as mentioned before in the perspective of product design change/ component layout change that would support in defect rate improvement including more fine tune in DOE to get better results resulting from higher peak temperature instead of 5'c reduction at once.

Besides that, according to the lesson learned and knowledge gained from the research, it is suggested to transfer the best practice to expand the learning to other products/ other areas in the organization to enhance the achievements and support overall company performance, not only the manufacturing issues but also other issues/ problems across the company which the DMAIC approach can be adopted and applied as appropriate.

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Appendices

Appendix A Qualitative Scale for the Severity Index (S)

Rank	Effect	Criteria: Severity of Effect on Process (Manufacturing/Assembly Effect)
10	**Failure to Meet Safety and/or Regulatory Requirements**	May endanger operator (machine or assembly) without warning.
9		May endanger operator (machine or assembly) with warning.
8	**Major Disruption**	100% of product may have to be scrapped. Line shutdown or stop ship.
7	**Significant Disruption**	A portion of the production run may have to be scrapped. Deviation from primary process including decreased line speed or added manpower.
6	**Moderate Disruption**	100% of production run may have to be reworked off line and accepted.
5		A portion of the production run may have to be reworked off line and accepted.
4	**Moderate Disruption**	100% of production run may have to be reworked in station before it is processed.
3		A portion of the production run may have to be reworked in-station before it is processed
2	**Minor Disruption**	Slight inconvenience to process, operation, or operator.
1	**No effect**	No discernible effect.

Appendix B Qualitative Scale for the Occurence Index (O)

Likelihood of Failure	Criteria: Occurrence of Cause - PFMEA (Incidents per items)	Rank
Very High	≥ 100 per thousand ≥ 1 in 10	10
High	50 per thousand 1 in 20	9
	20 per thousand 1 in 50	8
	10 per thousand 1 in 100	7
Moderate	2 per thousand 1 in 500	6
	1 per thousand 1 in 2,000	5
	.1 per thousand 1 in 10,000	4
Low	.01 per thousand 1 in 100,000	3
	≤.001 per thousand 1 in 1,000,000	2
Very Low	Failure is eliminated through preventive control.	1

Appendix C Qualitative Scale for the Detectability Index (D)

Likelihood of Detection	Opportunity for Detection	Opportunity for Detection			Criteria: Likelihood of Detection by Process Control	Rank
		A	B	C		
Almost Impossible	No detection opportunity			X	No current process control; Cannot detect or is not analyzed.	10
Very Remote	Not likely to detect at any stage			X	Failure Mode and/or Error (Cause) is not easily detected (e.g., random audits).	9
Remote	Problem Detection Post Processing		X	X	Failure Mode detection post-processing by operator through visual/tactile/audible means.	8
Very Low	Problem Detection at Source		X	X	Failure Mode detection in-station by operator through visual/tactile/audible means or post-processing through use of attribute gauging (go/no-go, manual torque check/clicker wrench, etc.).	7
Low	Problem Detection Post Processing		X		Failure Mode detection post-processing by operator through use of variable gauging or in-station by operator through sue of attribute gauging (go/no-go, manual torque check/clicker wrench, etc.).	6
Moderete	Problem Detection at Source		X		Failure Mode or Error (Cause) detection in-station by operator through use of variable gauging or by automated controls in-station that will detect discrepant part and notify operator (light, buzzer, etc.).Gauging performed on setup and first-piece check (for set-up causes only).	5
Moderately High	Problem Detection Post Processing	X			Failure Mode detection post-processing by automated controls that will detect discrepant part and lock part to prevent further processing.	4
High	Problem Detection at Source	X			Failure Mode detection in-station by automated controls that will detect discrepant part and automatically lock part in station to prevent further processing.	3
Very High	Error Detection and/or Problem Prevent	X			Error (Cause) detection in-station by automated controls that will detect error and prevent discrepant part from being made.	2
Almost Certain	Detection not applicable ; Error Prevention	N/A			Error (Cause) prevention as a result of fixture design, machine design or part design. Discrepant parts cannot be made because items has been error-proofed by process/product design	1

Inspection Types:

A. Automatic
B. Gauging Detection
C. Manual Inspection

N/A. Error-proofed at design step

Appendix D Quality Improvement Project Charter

Project: Date: Project type:	Quality Improvement of PCBA Manufacturing Process by DMAIC Approach Jan.7, 2012 Quality Improvement
Problem Statement:	The high defect rate and negative trend of SMT process performance cause impacts to the company in term of; product quality, cost of poor quality and productivity. The company needs to do improvement to improve the quality performance/ reduce the defect rate at the SMT processes
Goal Statement:	Metric: Overall Defect Rate; (DMMPc) Baseline: 4804; (DMMPc) Goal: 680
Project Scope and Approach:	• The research will cover the product AZY • The research will aim for the quality improvement to reduce the defect rate of the PCBA core manufacturing processes (SMT) which are o Screen Printing Operation o Surface Mount Device Mounting o Reflow Soldering o Auto Optical Inspection (AOI) & Visual Inspection
Team members:	Process Engineer Quality Engineer Test Engineer Production Supervisor Leader: Process Engineer Sponsor: General Manager Advisor: Mrs. Kulchalee Naralai/ Author
Timing: Target completion:	Define: 01/07/2012; Measure: 02/01/2012; Analysis: 05/20/2012; Improve: 06/01/2012; Control: 07/04/2012
Data issues: 01/07/12	

Appendix E Failure Mode and Effects Analysis of Non-wetting Defect (Before Improvement)

Process Function/ Operation	Requirements	Potential Failure Mode	Potential Effect of Failure	Severity	Potential Cause of Failure	Current Process Control Prevention	Occurrence	Current Process Control Detection Cause	Detection	RPN
Reflow Soldering	Good solder welting per IPC-A-610 Class 2	Non-wetting	Long-term joint strength and potential for functional failure.	6	***Material***					
					PCB Silkscreen too thick	Supplier data	1	Material First Article Inspection	1	6
					PCB Soldermask too thick	Supplier data	1	Material First Article Inspection	1	6
					Material Solderability	Datecode Control at Incoming, Storage and Shelf Life Control at Store and Mfg floor	3	IQA Solderability test	2	36
					Solder paste viscosity	Shelf life and storage control	2	Viscosity check at IQA	1	12
					Machine					
					Placement M/C loose accuracy	SMT setup process	3	First piece inspection	2	36
					Reflow have loss heater zone	Machine specification / maintenance	2	Buy-off process	2	24
					Squeegee damage	SMT set up process	3	Setup / First piece check / routine check	2	36
					Stencil Dent	SMT set up process and Stencil maintenance	3	Stencil inspection	2	36
					Stencil aperture related	IPC-7525 Stencil Design Guidelines	6	Visual Inspect of solder paste on pad	4	144
					Method					
					Placement M/C setup	SMT set up process	3	Buy off process	3	54
					Reflow profile / insufficient heat (Reflow time / peak temperature.	Use the right reflow profile with the process and components, Review type of components, follow the recommended profile	6	Temperature profile measurement and compare with the std profile/ recommended profile	3	108
					Too long soak time / preheat time	Use the right reflow profile with the process and components, Review related factors and follow the recommended profile	3	Temperature profile measurement and compare with the std profile/ recommended profile	3	54
					Stencil cleaning	Follow proper cleaning period and instruction	2	Stencil inspection and screen printing visual inspection	4	48
					Screen M/C improper setup	Screen Printing Set up	2	Solder paste thickness and visual inspection	2	24
					Man					
					No checking printing alignment	Training / certify program	3	Rowing audit	2	36
					Fault reject by visual inspection	Training / certify program	3	IPC-A-610 certification program	3	54

Appendix F Failure Mode and Effects Analysis of Non-wetting Defect (After Improvement)

Process Function/ Operation	Requirements	Potential Failure Mode	Potential Effect of Failure	Severity	Potential Cause of Failure	Current Process Control Prevention	Occurrence	Current Process Control Detection/ Cause	Detection	RPN	Recommended Action	Responsability & Target Completion Date	Action Taken & Effective Date	Severity	Occurrence	Detection	RPN
Reflow Soldering	Good solder welting per IPC-A-610 Class 2	Non-wetting	Long-term joint strength and potential for functional failure.	6	***Material*** PCB Silkscreen too thick	Supplier data	1	Material First Article Inspection	1	6							
					PCB Soldermask too thick	Supplier data	1	Material First Article Inspection	1	6							
					Material Solderability	Datecode Control at Incoming, Storage and Shelf Life Control at Store and Mfg floor	3	IQA Solderability test	2	36							
					Solder paste viscosity	Shelf life and storage control	2	Viscosity check at IQA	1	12							
					Machine Placement M/C loose accuracy	SMT setup process	3	First piece Inspection	2	36							
					Reflow have less heater zone	Machine specification / maintenance	2	Buy-off process	2	24							
					Squeegee damage	SMT set up process	3	Setup / First piece check / routine check	2	36							
					Stencil Dent	SMT set up process and Stencil maintenance	3	Stencil inspection	2	36							
					Stencil aperture related	IPC-7525 Stencil Design Guidelines	6	Visual inspect of solder paste on pad	4	144	Increase aperture length	PE, June'12	Done, Jun 2012	6	2	4	48
					Method Placement M/C setup	SMT set up process	3	Buy off process	3	54							
					Reflow profile / insufficient heat (Reflow time / peak temperature	Use the right reflow profile with the process and components. Review type of components. follow the recommended profile	6	Temperature profile measurement and compare with the std profile/ recommended profile	3	108	Increase peak temperature and time above liquid	PE, June'12	PE, June'12	6	2	3	36
					Too long soak time / preheat time	Use the right reflow profile with the process and components. Review related factors and follow the recommended profile	3	Temperature profile measurement and compare with the std profile/ recommended profile	3	54							
					Stencil cleaning	Follow proper cleaning period and instruction	2	Stencil Inspection and screen printing visual inspection	4	48							
					Screen M/C improper setup	Screen Printing Set up	2	Solder paste thickness and visual inspection	2	24							
					Man No checking printing alignment	Training / certify program	3	Roving audit	2	36							
					Fault reject by visual inspection	Training / certify program	3	IPC-A-610 certification program	3	54							

Appendix G Process Control Plan (After Improvement)

Process Function / Requirement	Machine, Device, Jig, Tools for Mfg.	Characteristics		Methods		Sample		Control Method	Reaction Plan
		Product	Process	Product/Process Specification/ Tolerance	Evaluation Measurement Technique	Size	Freq.		
Print Solder Paste	Stencil Printer		Correct stencil used	Correct stencil ID#AY3C18	Visual check stencil ID number	N/A	Every start up	SMT set up and release record	Stop and notify Technician/Engineer
		Solder Paste on Pads		Solder on a Intended Pads	Visual Inspection by Magnifier/Solder Paste Inspection Machine	100%	100%	Inspection Record	Stop Production If Any Pads Do Not Have Solder Paste. Notify Engineering. Segregate to Clean
Smt Component Placement Top Bottom (as Required)	Placement Machine	Component Alignment	Automatic Machine Placement	By Product Drawing and Specification	Visual Inspection X-Ray Inspection	1st Article	Every Run	QC First Article Inspection	Stop The Line and Report To Supervisor and Engineer. Segregate Suspect Units For Inspection. Modify Assembly Programs Needed.
		Component Sealing	Automatic Machine Placement	By Product Drawing and Specification	Visual Inspection	1st Article	Every Run	QC First Article Inspection	Stop The Line and Report To Supervisor and Engineer. Segregate Suspect Units For Inspection. Modify Assembly Programs Needed.
Reflow	Reflow Over	Quality of Solder	Correct Machine Reflow Soldering Profile	IPC-610 Workmanship Standard Correct Reflow Profile Name and Revision Number Work Instruction and Profile Record	Visual Inspection Record and verify against Work Instruction Profile Checker Reflow Soldering Parameters Audit By QC	100%	100% Every Product New Run	Inspection Record and Database SMT set up and release check list record Reflow Soldering Process Monitoring Record	Scrap Defectives Rework Stop line and notify Technician/Engineer Stop The Line and Verify Over Parameters, Separate Suspect Material

ABC Electronics

Record Owner: RA

Reflow Soldering Process Monitoring

Revision: B

☑ Vitronics Machine ☐ Heller Machine

WW : 29
M/C No. : XPM1030

Description	Temp.zone	1	2	3	4	5	6	7	8	9	10	Conveyor Speed
Date: July 02, 2012	Spec.	130.0	150.0	190.0	180.0	180.0	180.0	190.0	195.0	290.0	290.0	34 in/min
Production order TMN087609	Actual	130.0	150.0	190.0	180.0	180.0	180.0	190.0	195.0	290.0	290.0	
Assy Name AZY	Temp. zone	11	12	13	14	15	16	17	18	19	20	
Assy No AZY001	Spec.											
Profile Name/ Rev.: A9357CB/B	Actual											
Auditor: Kam (Kamon) EIN 5569	Result											
	Temp.zone	1	2	3	4	5	6	7	8	9	10	Conveyor Speed
Date: July 03, 2012	Spec.	130.0	150.0	190.0	180.0	180.0	180.0	190.0	195.0	290.0	290.0	34 in/min
Production order TMN087609	Actual	130.0	150.0	190.0	180.0	180.0	180.0	190.0	195.0	290.0	290.0	
Assy Name AZY	Temp. zone	11	12	13	14	15	16	17	18	19	20	
Assy No AZY001	Spec.											
Profile Name/ Rev.: A9357CB/B	Actual											
Auditor: Kam (Kamon) EIN 5569	Result											
	Temp.zone	1	2	3	4	5	6	7	8	9	10	Conveyor Speed
Date: July 04, 2012	Spec.	130.0	150.0	190.0	180.0	180.0	180.0	190.0	195.0	290.0	290.0	34 in/min
Production order TMN087609	Actual	130.0	150.0	190.0	180.0	180.0	180.0	190.0	195.0	290.0	290.0	
Assy Name AZY	Temp. zone	11	12	13	14	15	16	17	18	19	20	
Assy No AZY001	Spec.											
Profile Name/ Rev.: A9357CB/B	Actual											
Auditor: Kam (Kamon) EIN 5569	Result											
	Temp.zone	1	2	3	4	5	6	7	8	9	10	Conveyor Speed
Date: July 05, 2012	Spec.	130.0	150.0	190.0	180.0	180.0	180.0	190.0	195.0	290.0	290.0	34 in/min
Production order TMN087609	Actual	130.0	150.0	190.0	180.0	180.0	180.0	190.0	195.0	290.0	290.0	
Assy Name AZY	Temp. zone	11	12	13	14	15	16	17	18	19	20	
Assy No AZY001	Spec.											
Profile Name/ Rev.: A9357CB/B	Actual											
Auditor: Kam (Kamon) EIN 5569	Result											
	Temp.zone	1	2	3	4	5	6	7	8	9	10	Conveyor Speed
Date: July 06, 2012	Spec.	130.0	150.0	190.0	180.0	180.0	180.0	190.0	195.0	290.0	290.0	34 in/min
Production order TMN087609	Actual	130.0	150.0	190.0	180.0	180.0	180.0	190.0	195.0	290.0	290.0	
Assy Name AZY	Temp. zone	11	12	13	14	15	16	17	18	19	20	
Assy No AZY001	Spec.											
Profile Name/ Rev.: A9357CB/B	Actual											
Auditor: Kam (Kamon) EIN 5569	Result											
	Temp.zone	1	2	3	4	5	6	7	8	9	10	Conveyor Speed
Date: July 09, 2012	Spec.	130.0	150.0	190.0	180.0	180.0	180.0	190.0	195.0	290.0	290.0	34 in/min
Production order TMN087609	Actual	130.0	150.0	190.0	180.0	180.0	180.0	190.0	195.0	290.0	290.0	
Assy Name AZY	Temp. zone	11	12	13	14	15	16	17	18	19	20	
Assy No AZY001	Spec.											
Profile Name/ Rev.: A9357CB/B	Actual											
Auditor: Kam (Kamon) EIN 5569	Result											

Appendix I SMT Machine Set up and Release Line Check List

ABC Electronics — **SMT Machine Set up and Release Line Check Sheet**

Record Owner: Manufacturing Department — Revision: B

Work Order : _____ Rev : _____ Q'ty : _____
Assy No. : _____
Assy Name : _____ Rev. _____
Requestor : _____
Completed loading parts (Date/ Time) : _____
Stencil ID no._____-_____ Stencil Thickness : _____ Mils
Start machine set up (Date/ Time) : _____ (ME)
Start machine set up (Date/ Time) : _____ (SE)

Date : _____ Shift : _____
Program Name : _____ Rev : _____
SMT Line # : _____
Profile Name : _____
Supv./ Leader : _____
Program Name (screen print) : _____
Eng. / Tech : _____ (ME)
Eng. / Tech : _____ (SE)

Item	Description	By whom	Result OK	Result Not OK	Action / Remark
1	Load the right program to machine per requestor	ME			
2	Check Mounting Revision& Program Name	MFG			
3	Check& compare Feeder Check Sheet of production and component feeder assignment in machine	MFG QA			
	3.1 Check Part Skip per Feeder Check Sheet	ME			
4	Set-up X-Y table, Stopper, Push up pins, Location pin, PCB level	ME			Be careful pin bump to component
5	Adjust machine conveyor width	ME			
6	Affixed double side tape on PCB surface& test loading conveyor	ME			
7	Test Mounting Program , X-Y fine tune, Fine tune part library - Check component polarity of IC, capacitor - Check placement accuracy, no side overhang - Check missing part with gold unit or drawing	ME			
8	Submit mounting unit on double side tape to prod sup (when 1st piece insp. Is required)	ME			
9	After QA accept FAS MFG sup. Inform maintenance backup program	MFG/ME			
10	Set up screen printer Solder paste thickness result Solder Paste P/N : _____ ☐clean ☐no clean ☐Pb-Free	SE SE MFG			
11	Measure solder paste thickness : _____mils	MFG			
12	Buy off set up adhesive dispensing program name : _____ and result	QA/MFG			
13	Select program for reflow oven according to MFG Package	ME			
14	Verify reflow profile graph every 3 months ☐Yes ☐No	MFG			
15	Set up reflow profile	SE			
16	Set up AOI machine : - Adjust machine conveyor width , Bar code reader , Load program - Verify AOI Prgram fine tune false call and escape rate	SE			
17	Record set up time, finished time (Chip mounter,Pick&place)/ date :_____ Record screen printing set up time,finished time/date :_____ Record reflow profile set up time,finished time/date :_____ Record AOI machine set up time,finished time/date :_____ Record AOI fine tune time, Start time/date :_____(received first board or gold board) Finished Time/Date :_____ Total set up time :_____ Hours	ME SE SE SE SE			
18	Confirm assembly program by run the PCBA boards (PCB solder paste and/or glue) **5-10 boards**	MFG			
19	Confirm BGA solder ability using X-RAYs tecnique (only PCBA installed BGA) 5 boards	MFG			
	ME Set up team : _____ SE Set up team :_____	Production Supv._____			

Remark for MFG , If item # 18 Not OK:_____
Remark:_____

From item# 18, QA BUY OFF after MFG confirm 5-10 bds (Including X-Rays BGA (if any)

SOL/Glue	Date /Time	Inspection result	Pass/Fail	QA OPTR

Filled by : MFG/ ME/ PE/ SE

ACTION	By whom

Disposition — **Start time if machine is released :** — *Required Signature* _____ *Date* _____

☐ **RELEASE under Normal Condition , QA buy off pass within two hrs.after start running PCBA** — QA Supv./QE :

☐ CONDITIONAL RELEASE, QA buy off FAIL but machine is released with long term action
Long term action/By whom : _____
_____
PE :
ME :
SE :
QE/ QA Supv. :
MFG Supv. :

☐ SHUT DOWN LINE ; buy off result Fail and Problem cannot be fixed or No action
QA Supv./QE :
MFG Supv. :

BIOGRAPHY

Mrs. Kulchalee Naralai completed her undergraduate studies with the Bachelor's Degree in Engineering from Kasetsart University, Bangkok Thailand. After graduated, she started her career in an international well known electronic company in Thailand and extended working services in an Electronic Manufacturing Service (EMS) provider. In 2009, she enrolled in the dual Master's Degree Program at Chulalongkorn University and University of Warwick to expand her knowledge in the engineering business management at the Regional Center for Manufacturing System Engineering at Chulalongkorn University.