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ภาคผนวก ก

การออกแบบและคำนวณหม้อแปลงไฟฟ้าศักดาสูง

แหล่งจ่ายไฟฟ้าศักดาสูงที่ใช้สำหรับหัววัดรังสีไกเกอร์ ซึ่งใช้กระแส 10 ไมโครแอมแปร์ งานวิจัยนี้จึงเลือกใช้หม้อแปลงแกนเฟอร์ไรต์แบบ EP ขนาด 13 ตารางมิลลิเมตร , A_e = 0.195 cm 2 ,ΔB = 1500 และกำหนดการทำงานต่างๆ ดังนี้ คือ ศักดาไฟฟ้าทางด้านเข้า 9 โวลต์ ให้ศักดาไฟฟ้าด้านขาออก 100 โวลต์ ช่วงเวลา t_{on} = 9 ไมโครวินาทีและประสิทธิภาพของหม้อแปลง 80 เปอร์เซ็นต์ ขั้นตอนการออกแบบมีดังนี้

$$T = \frac{1}{f}$$

$$= \frac{1}{16kHz}$$

$$= 62.5\ \mu s$$

$$t_{on(max)} = \frac{(V_O + V_D)(N_P / N_S)(0.8T)}{(V_{in(max)} - V_{CE(sat)}) + (V_O + V_D)(N_P / N_S)}$$

$$31.25\times10^{-6} = \frac{(100+0.7)(N_P / N_S)(0.8\times62.5\times10^{-6})}{9 + (100+0.7)(N_P / N_S)}$$

$$\frac{N_P}{N_S} = 0.1489$$

$$\frac{N_s}{N_p} = 6.713$$

$$L_P = \frac{\eta\left[(v_{in(max)} - V_{CE(sat)})\times t_{on(max)}\right]^2}{2T\times P_{OUT}}$$

$$= \frac{0.8\left[(9-0.7)\times31.25\times10^{-6}\right]^2}{2\times62.5\times10^{-6}\times100\times10\times10^{-6}}$$

$$= 430\ mH$$

$$I_P = \frac{(V_{in(max)} - V_{CE(sat)})\times ton}{L_P}$$

$$= \frac{(9-0.7)\times31.25\times10^{-6}}{430\times10^{-3}}$$

$$= 603\ \mu A$$

$$N_P = \frac{(V_{in(max)} - V_{CE(sat)} \times t_{on(max)} \times 10^8}{\Delta B A_e}$$

$$= \frac{(9-0.7)\times 31.25\times 10^{-6}\times 10^8}{1500\times 0.195}$$

$$= 88 \text{ รอบ}$$

$$N_S = 6.7 \times N_P$$

$$= 595 \text{ รอบ}$$

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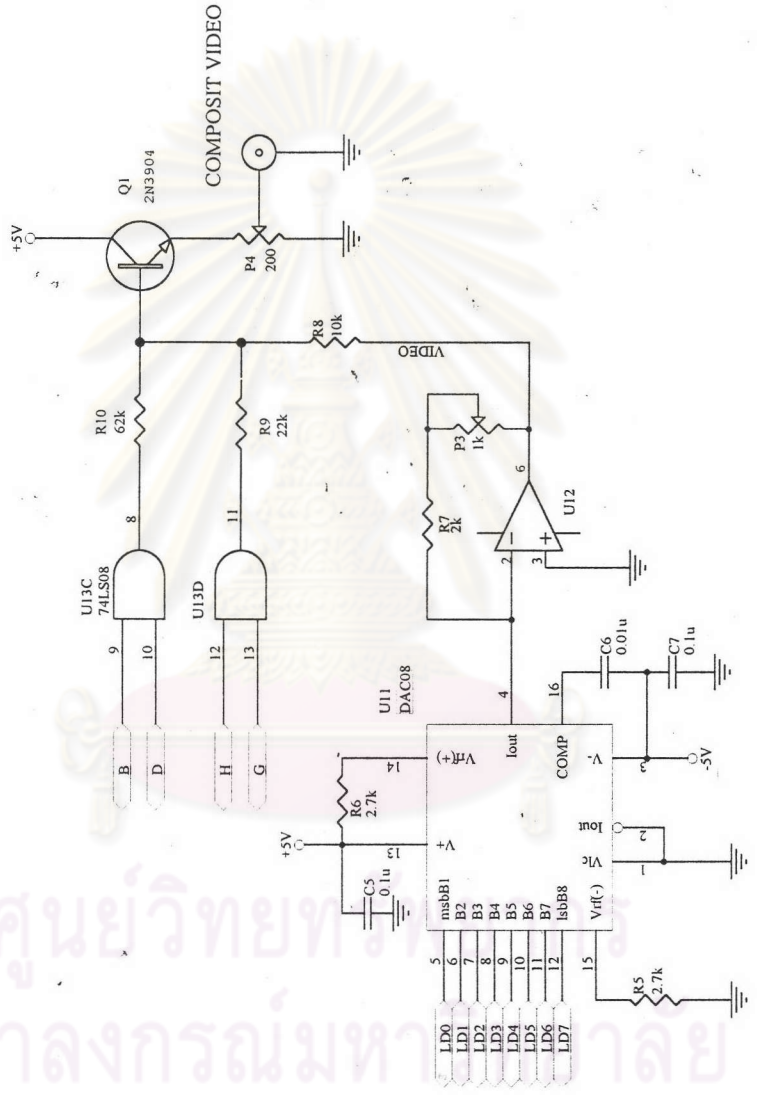
ภาคผนวก ข

วงจรอิเล็กทรอนิกส์ของระบบสแกนรังสีกระเจิงกลับเพื่อแสดงภาพสองมิติ



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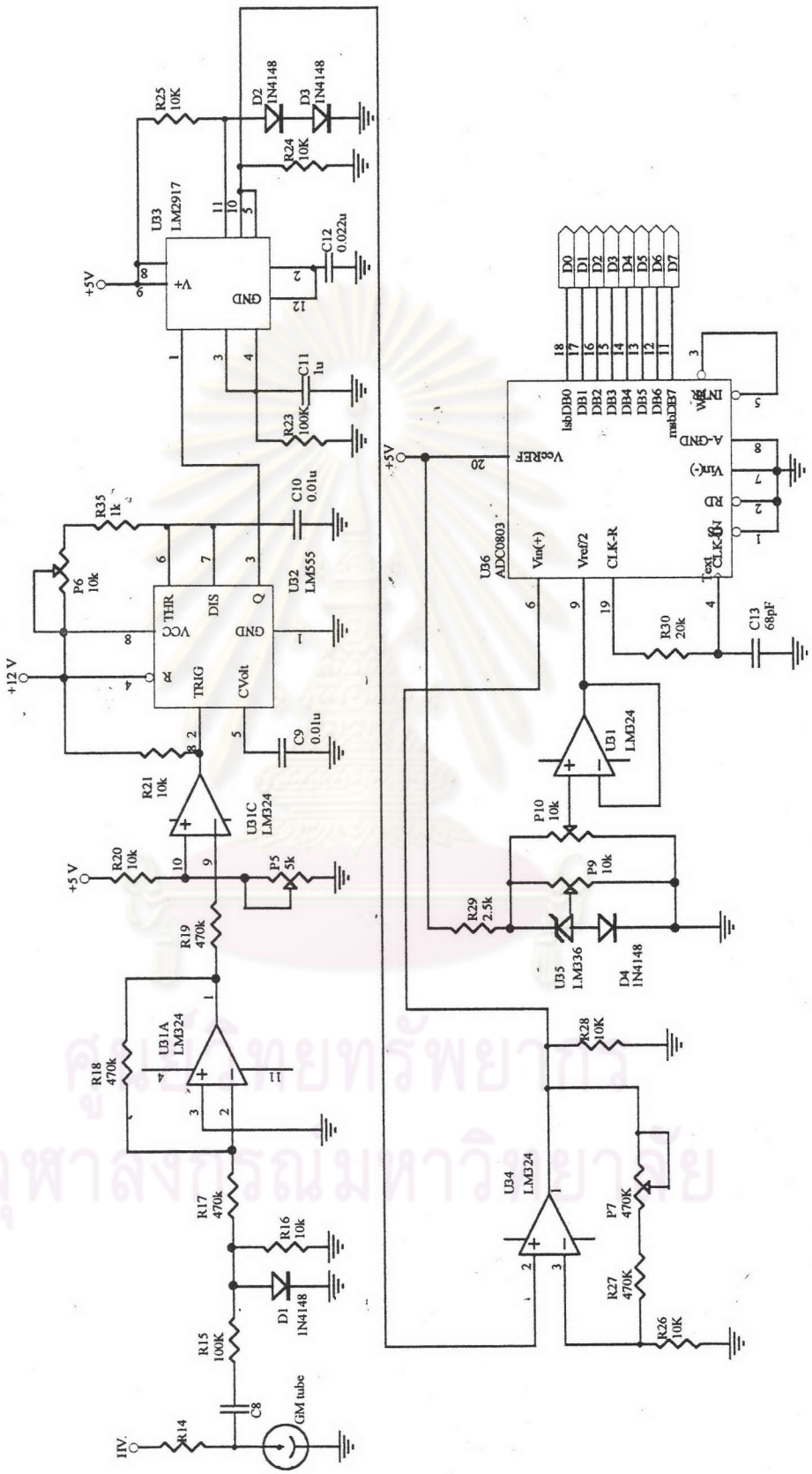
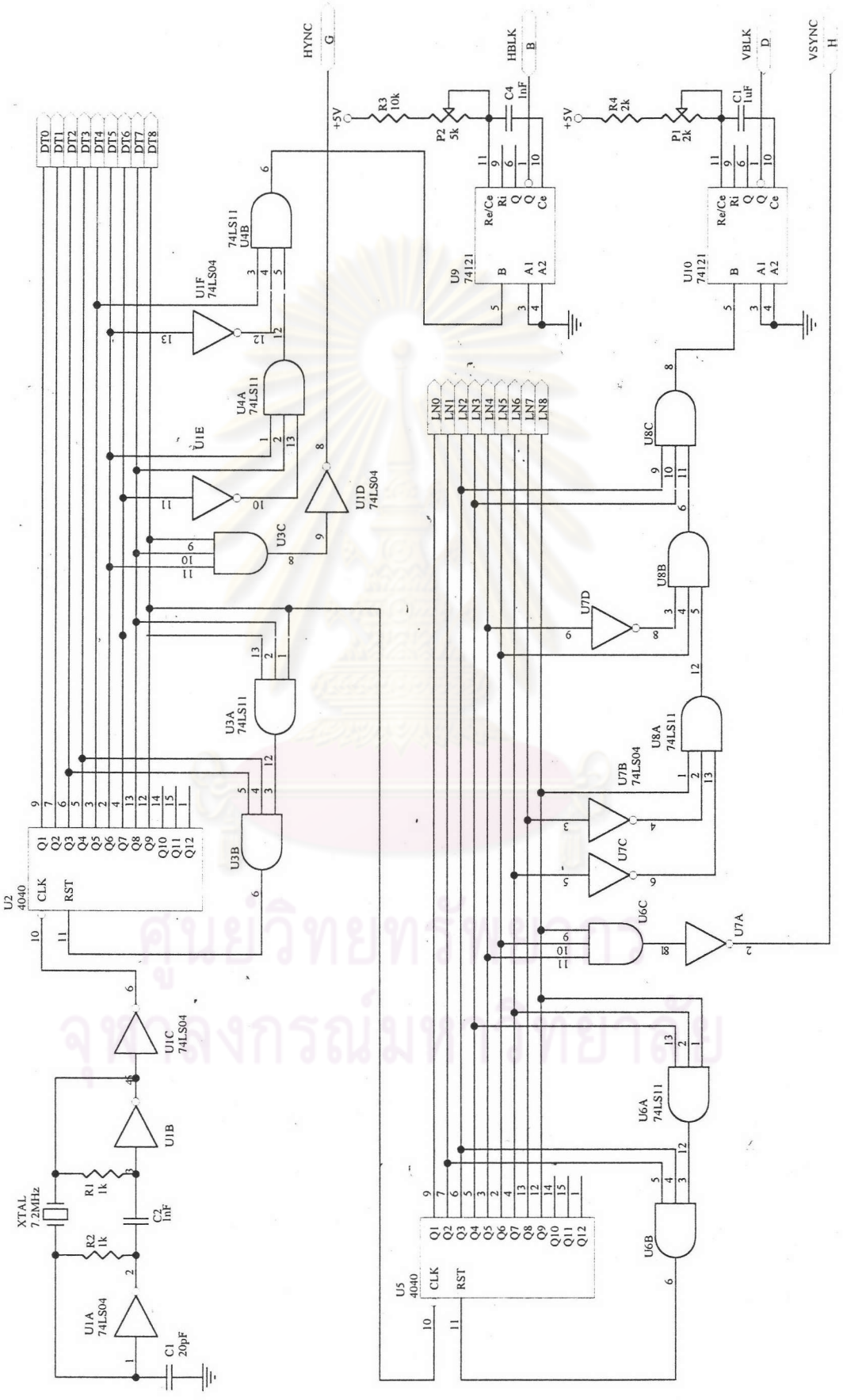


Nuclear measurement & ADC



Video syncronization generator

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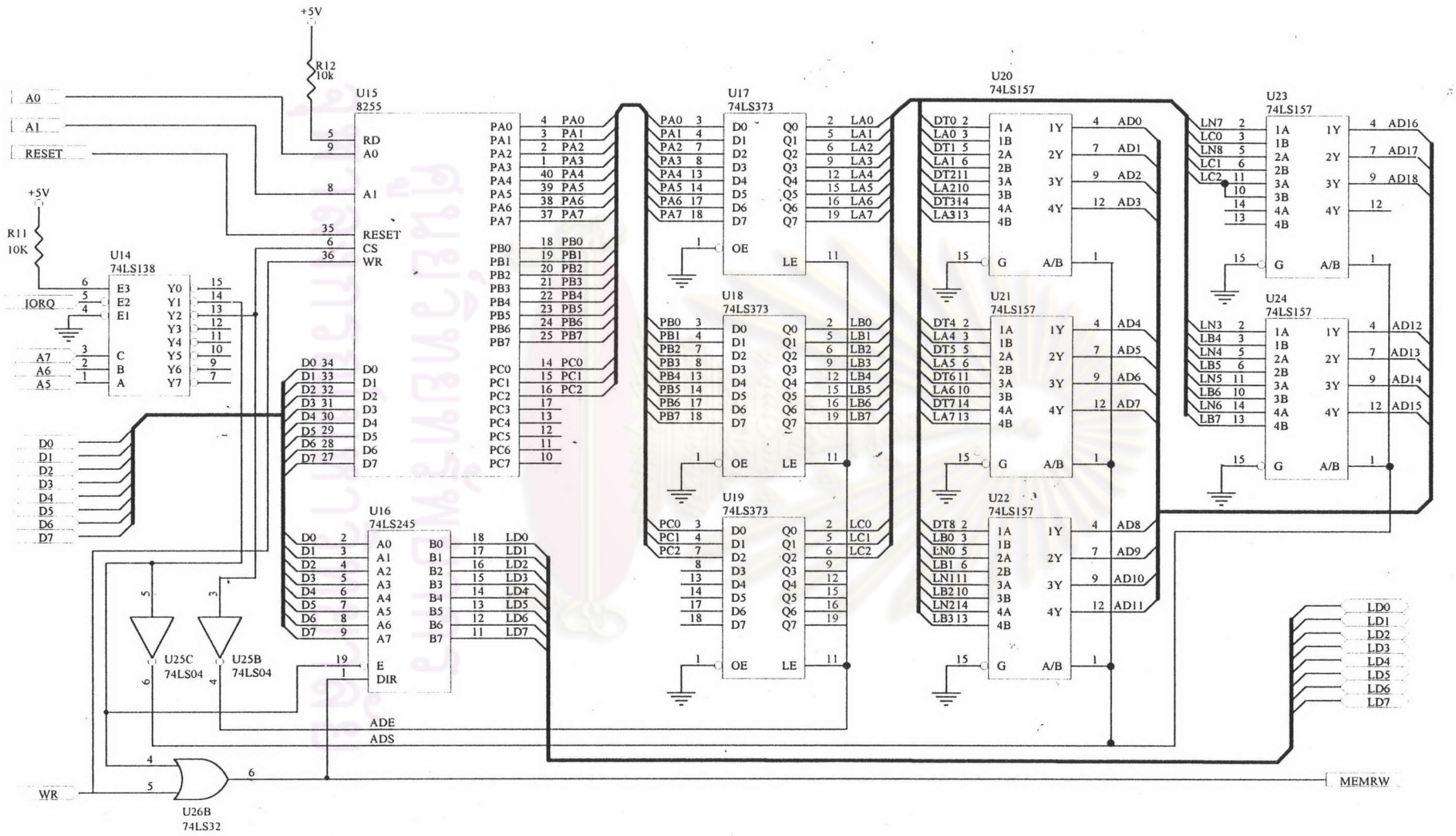
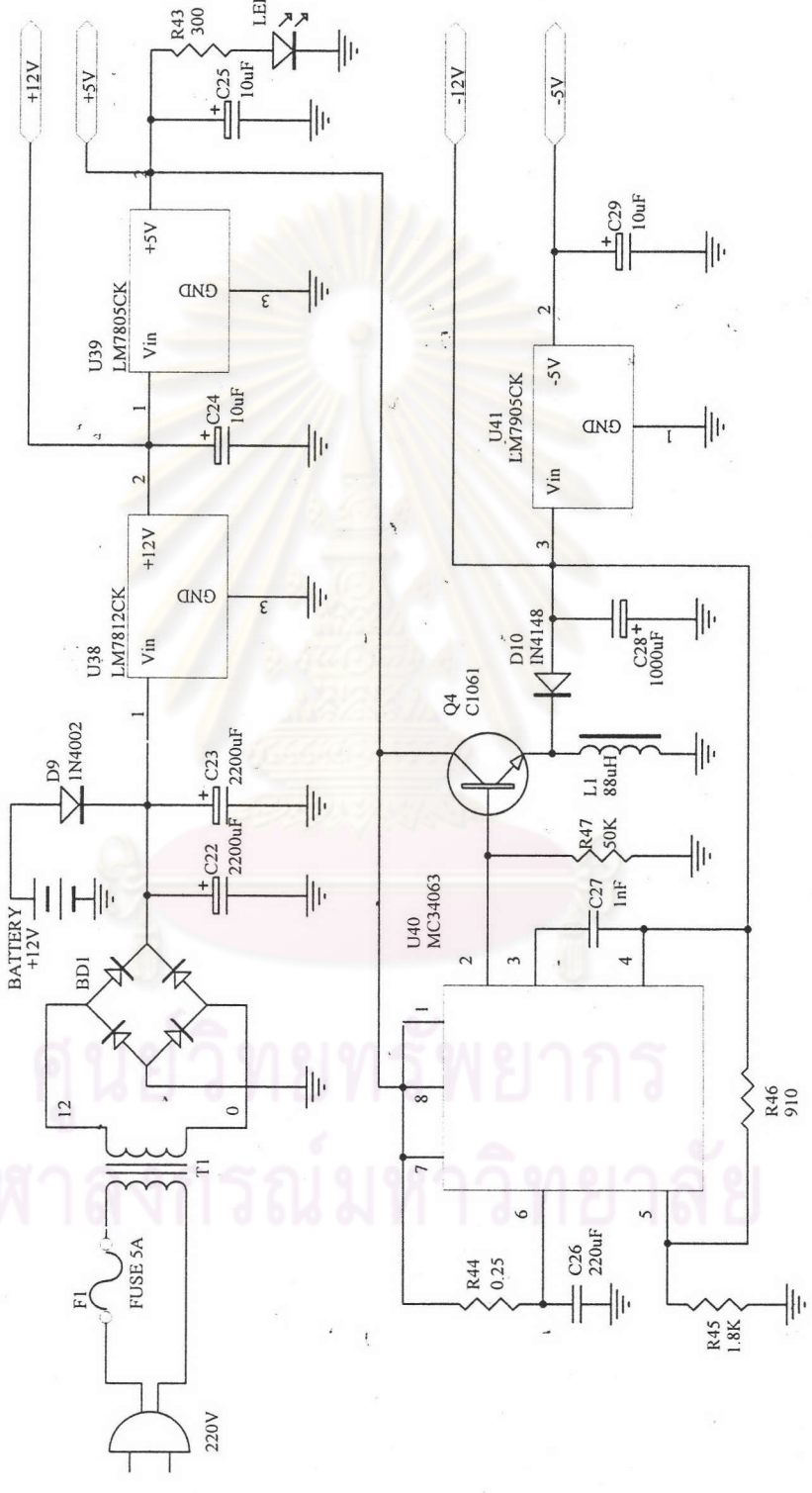
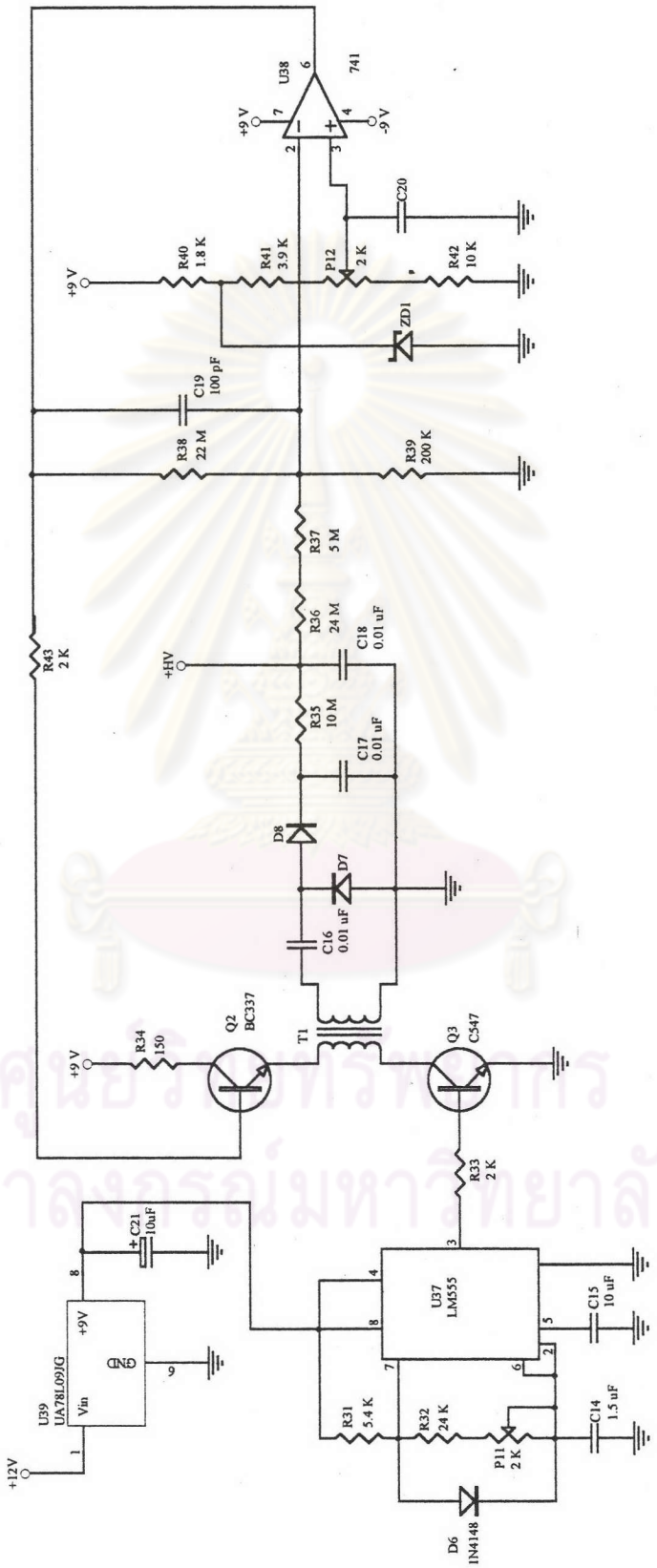


Interface circuit



Power supply



High voltage power supply

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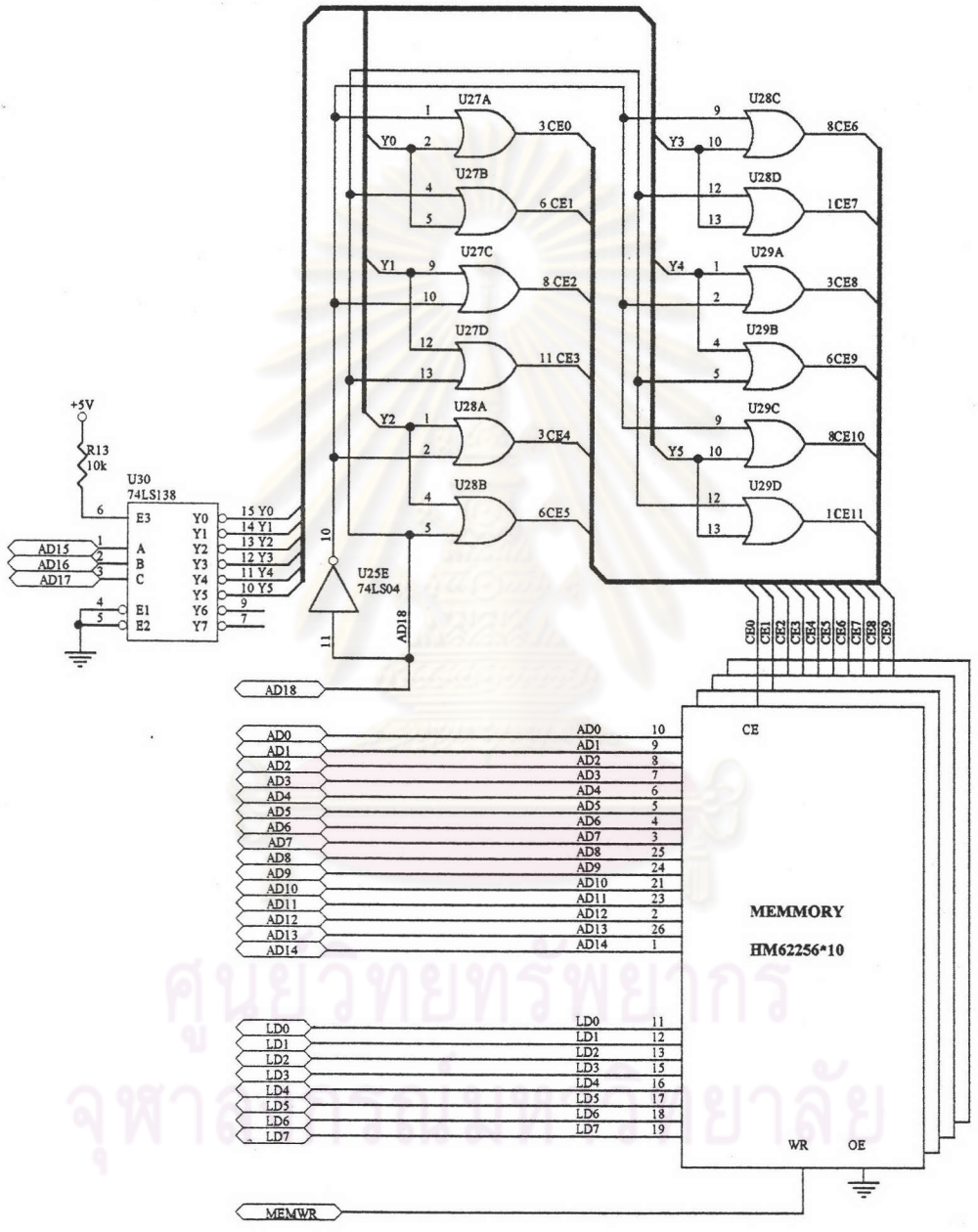
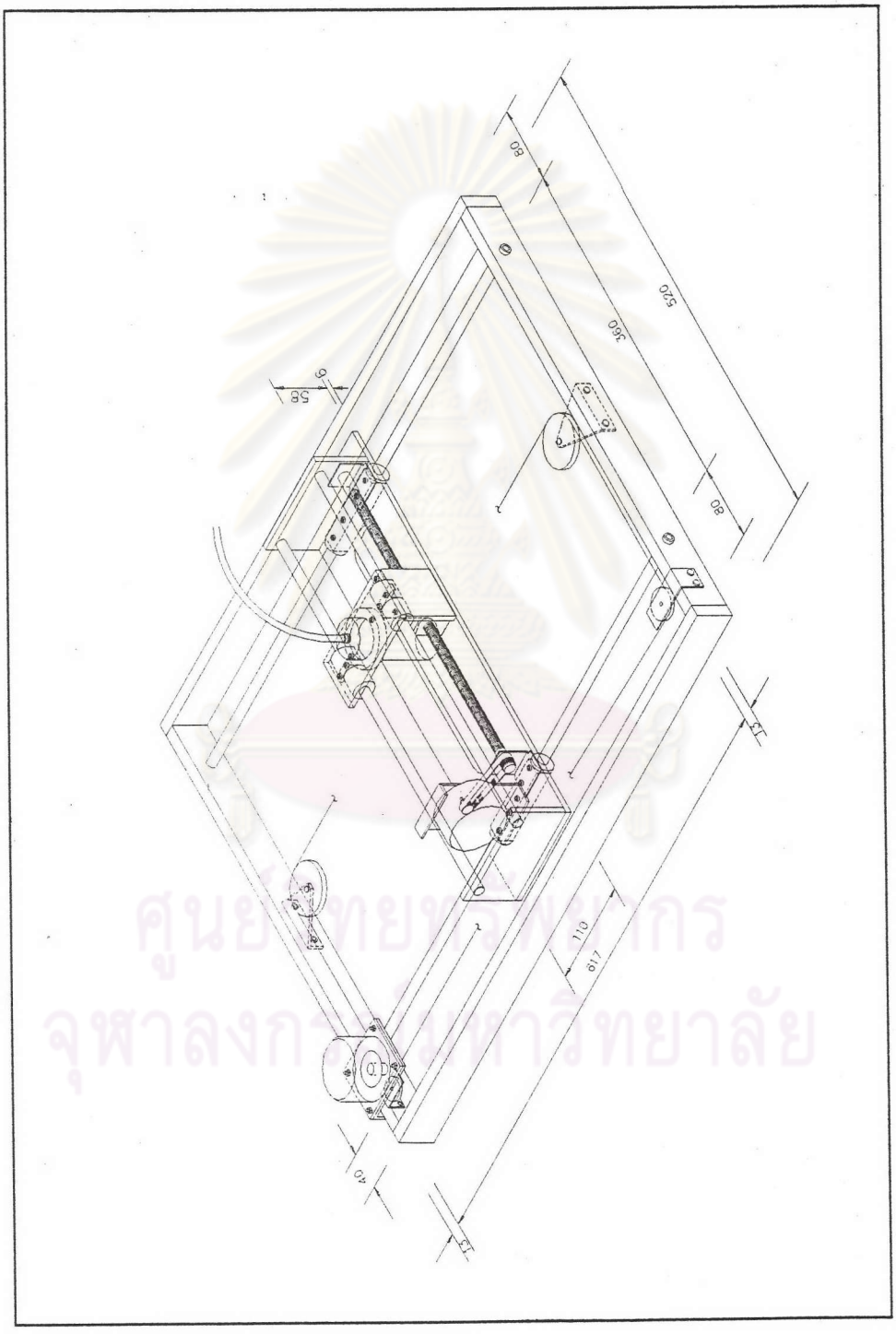


Memmory circuit

ภาคผนวก ค

แบบโครงสร้างอุปกรณ์ขับเคลื่อนทางกล



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ภาคผนวก ง

ข้อมูลทางเทคนิคของไมโครคอนโทรลเลอร์ 83C154

PRELIMINARY

MHS

AUGUST 1988

DATA SHEET 83C154

CMOS SINGLE - CHIP 8 BIT MICROCONTROLLER

- 83C154 – CMOS SINGLE-CHIP 8-BIT MICROCONTROLLER with factory mask-programmable ROM
- 83C154F – The internal ROM code cannot be read or dumped after activation of a special protection
- 80C154 – ROMLESS version
- 83C154-1 – 16 MHz version
- 80C154-1 – 16 MHz ROMless version

FEATURES

- 16K x 8 BIT INTERNAL ROM
- 256 x BIT RAM
- 32 PROGRAMMABLE I/O LINES (PROGRAMMABLE IMPEDANCE)
- THREE 16-BIT TIMER/COUNTERS (INCLUDING WATCH DOG AND 32 BIT TIMER)
- 64K PROGRAM MEMORY SPACE
- FULLY STATIC DESIGN
- POWER CONTROL MODES
- INTERRUPT PRIORITY CONTROL
- 0 TO 16 MHz
- BOOLEAN PROCESSOR
- 6 INTERRUPT SOURCES
- PROGRAMMABLE SERIAL PORT
- 64K DATA MEMORY SPACE
- TEMPERATURE RANGE:
  - COMMERCIAL
  - INDUSTRIAL

DESCRIPTION

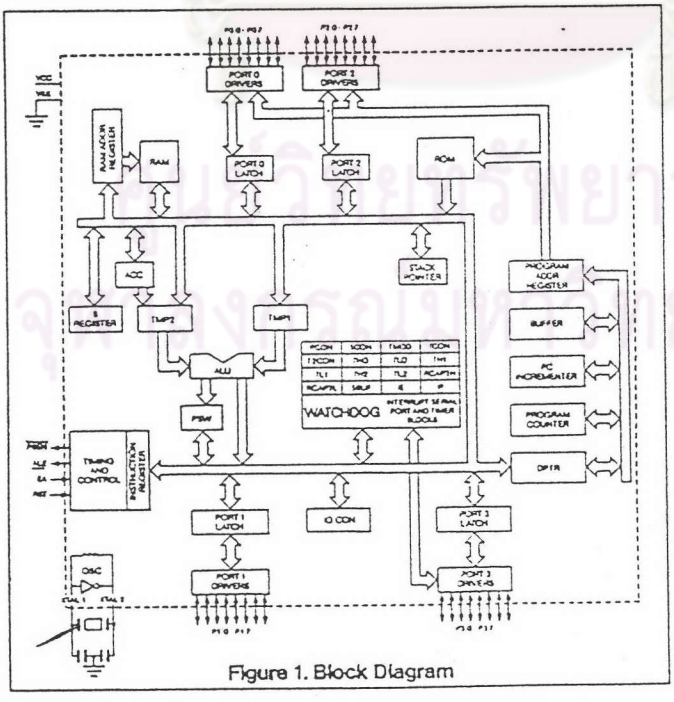


Figure 1. Block Diagram

The 83C154 retains all the features of the MHS 80C52 with extended ROM capacity (16K bytes), 256 bytes of RAM, 32 I/O lines, a 6-source 2-level interrupts, a full duplex serial port, an on-chip oscillator and clock circuits, three 16 bit timers with extra features: 32 bit timer and watch dog functions. Timer 0 and 1 can be configured by program to implement a 32 bit timer. The watch dog function can be activated either with timer 0, or timer 1 or both together (32 bit timer).

In addition, the 83C154 has two software selectable modes of reduced activity for further reduction of power consumption. In the Idle Mode, the CPU is frozen while the RAM is saved, and the timers, the serial port, and the interrupt system continue to function. In the Power Down Mode, the RAM is saved and the timers, serial port and interrupts continue to function when driven by external clocks. In addition as for the MHS 80C51/C52, the stop clock mode is also available.

MHS

C411 / 02 8584

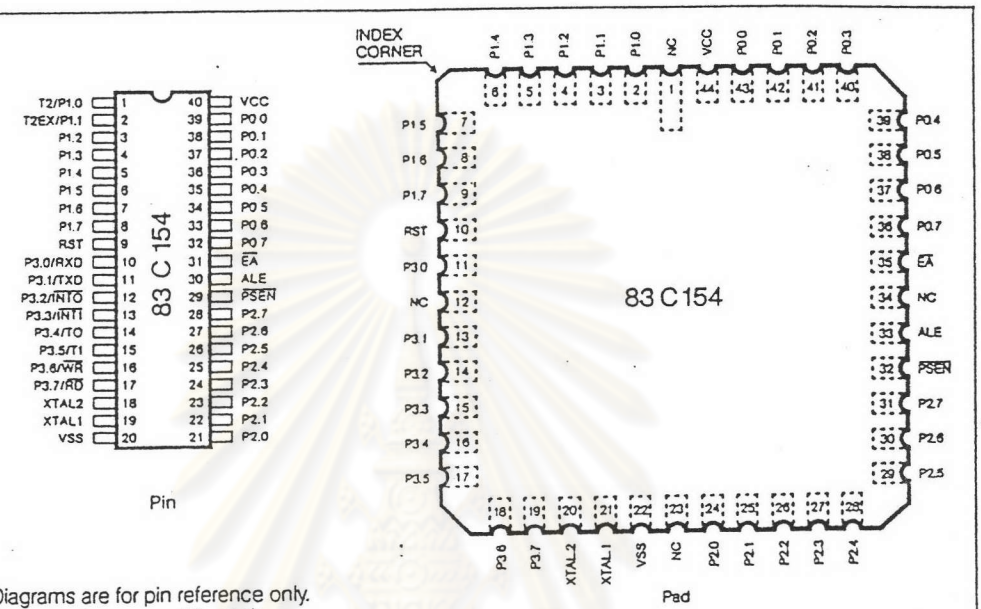


Figure 2. Configurations

IDLE AND POWER DOWN OPERATION

Figure 3 shows the internal Idle and Power Down clock configuration. As illustrated, Power Down operation stops the oscillator. The interrupt, serial port, and timer blocks continue to function only with external clock (INT0, INT1, T0, T1).

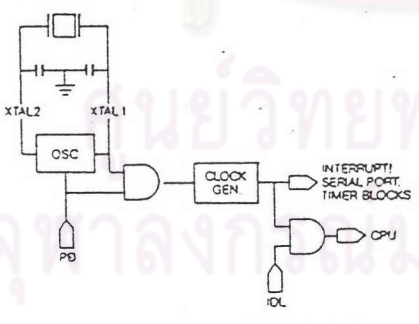


Figure 3. Idle and Power Down Hardware

Idle Mode operation allows the interrupt, serial port, and timer blocks to continue to function with internal or external clocks, while the clock to CPU is gated off. The special modes are activated by software via the Special Function Register, PCON. Its hardware address is 87H. PCON is not bit addressable.

PCON: Power Control Register

(MSB) (LSB)

SMOD	HPD	RPD	–	GF1	GF0	PD	IDL

Symbol	Position	Name and Function
SMOD	PCON.7	Double Baud rate bit. When set to a 1, the baud rate is doubled when the serial port is being used in either modes 1, 2 or 3.
HPD	PCON.6	Hard Power Down bit. Setting this bit allows CPU to enter in Power Down state on an external event (1 to 0 transition) on bit T1 (p. 3-5) the CPU quit the Hard Power Down mode when bit T1 (p. 3-5) go high or when reset is activated.
RPD	PCON.5	Recover from Idle or Power Down bit. When 0 RPD has no effect. When 1, RPD permits to exit from idle or Power Down with any non enabled interrupt source (except timex 2). In this case the program start at the next address. When interrupt is enabled, the appropriate interrupt routine is serviced.
–	PCON.4	(Reserved)
GF1	PCON.3	General-purpose flag bit.
GF0	PCON.2	General-purpose flag bit.
PD	PCON.1	Power Down bit. Setting this bit activates power down operation.
IDL	PCON.0	Ide mode bit. Setting this bit activates idle mode operation.

If 1's are written to PD and IDL at the same time. PD takes, precedence. The reset value of PCON is (000X0000).

IDLE MODE

The instruction that sets PCON.0 is the last instruction executed before the Idle mode is activated. Once in the Idle mode the CPU status is preserved in its entirety: the Stack Pointer, Program Counter, Program Status Word, Accumulator, RAM, and all other registers maintain their data during Idle. In the Idle mode, the internal clock signal is gated off to the CPU, but interrupt, timer and serial port functions are maintained. Table 1 describes the status of the external pins during Idle mode.

There are three ways to terminate the Idle mode. Activation of any enabled interrupt will cause PCON.0 to be cleared by hardware, terminating Idle mode. The interrupt is serviced, and following RETI, the next instruction to be executed will be the one following the instruction that wrote 1 to PCON.0.

The flag bits GF0 and GF1 may be used to determine whether the interrupt was received during normal execution or during the Idle mode. For example, the instruction that writes to PCON.0 can also set or clear one or both flag bits. When Idle mode is terminated by an enabled interrupt, the service routine can examine the status of the flag bits.

The second way of terminating the Idle mode is with a hardware reset. Since the oscillator is still running, the hardware reset needs to be active for only 2 machine cycles (24 oscillator periods) to complete the reset operation.

The third way to terminate the Idle mode is the activation of any disabled interrupt when recover is programmed (RPD=1). This will cause PCON.0 to be cleared. No interrupt is serviced. The next instruction is executed. If interrupt are disabled and RPD=0, only a reset can cancel the Idle mode.

POWER DOWN MODE

The instruction that sets PCON.1 is the last executed prior to entering power down. Once in power down, the oscillator is stopped. The contents of the onchip RAM and the Special Function Register is saved during power down mode. The three ways to terminate the Power Down mode are the same than the Idle mode. But since the onchip oscillator is stopped, the external interrupts, timers and serial port must be sourced by external clocks only, via INT0, INT1, T0, T1.

In the Power Down mode, VCC may be lowered to minimize circuit power consumption. Care must be taken to ensure the voltage is not reduced until the power down mode is entered, and that the voltage is restored before the hardware reset is applied which frees the oscillator. Reset should not be released until the oscillator has restarted and stabilized.

When using voltage reduction: interrupt, timers and serial port functions are guaranteed in the VCC specification limits.

Table 1 describes the status of the external pins while in the power down mode. It should be noted that if the power down mode is activated while in external program memory, the port data that is held in the Special Function Register P2 is restored to Port 2. If the port switches from 0 to 1, the port pin is held high during the power down mode by the strong pullup, T1, shown in Figure 4.

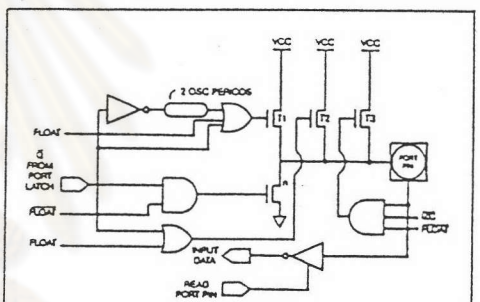


Fig. 4: I/O Buffers in the 83C154 (Ports 1, 2, 3)

STOP CLOCK MODE

Due to static design, the MHS 83C154 clock speed can be reduced until 0 MHz without any data loss in memory or registers. This mode allows step by step utilization, and permits to reduce system power consumption by bringing the clock frequency down to any value. At 0 MHz, the power consumption is the same as in the Power Down Mode.

83C154 I/O PORTS

The I/O drives for P1, P2, P3 of the 83C154 are impedance programmable. The I/O buffers for Ports 1,2 and 3 are implemented as shown in *figure 4*.

When the port latch contains 0, all pFETS in figure 4 are off while the nFET is turned on. When the port latch makes a 0-to-1 transition, the nFET turns off. The strong pullup pFET, T1, turns on for two oscillator periods, pulling the output high very rapidly. As the output line is

Table 1. Status of the external pins during Idle and Power Down modes

Mode	Program Memory	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Port Data	Port Data	Port Data	Port Data
Idle	External	1	1	Floating	Port Data	Address	Port Data
Power Down	Internal	0	0	Port Data	Port Data	Port Data	Port Data
Power Down	External	0	0	Floating	Port Data	Port Data	Port Data

drawn high, pFET T3 turns on through the inverter to supply the IOH source current. This inverter and T3 form a latch which holds the 1 and is supported by T2. When Port 2 is used as an address port, for access to external program of data memory, any address bit that contains a 1 will have his strong pullup turned on for the entire duration of the external memory access.
When an I/O pin on Ports 1, 2 or 3 is used as an input, the user should be aware that the external circuit must sink current during the logical 1-to-0 transition. The maximum sink current is specified as ITL under the D.C. Specifications. When the input goes below approximately 2V, T3 turns off to save ICC current. Note, when returning to a logical 1, T2 is the only internal pullup that is on. This will result in a slow rise time if the user's circuit does not force the input line high.
The input impedance of Port 1, 2, 3 are programmable through the register IOCON. The ALF bit (IOCON0) set all of the Port 1, 2, 3 floating when a Power Down mode occurs. The P1HZ, P2HZ, P3HZ bits (IOCON1, IOCON2, IOCON3) set respectively the Ports P1, P2, P3 in floating state. The IZC (IOCON4) allows to choose input impedance of all ports (P1, P2, P3). When IZC = 0, T2 and T3 pullup of I/O ports are active; the internal input impedance is approximately 10K. When IZC = 1 only T2 pull-up is active. The T3 pull-up is turned off by IZC. The internal impedance is approximately 100K.

PIN DESCRIPTIONS

VSS
Circuit ground potential.

VCC
Supply voltage during normal, Idle, and Power Down operation.

PORT 0
Port 0 is an 8-bit open drain bi-directional I/O port. Port 0 pins that have 1's written to them float, and in that state can be used as high-impedance inputs.
Port 0 is also the multiplexed low-order address and data bus during accesses to external Program and Data Memory. In this application it uses strong internal pullups when emitting 1's. Port 0 also outputs the code bytes during program verification in the 83C154. External pullups are required during program verification. Port 0 can sink eight LS TTL inputs.

PORT 1
Port 1 is an 8-bit bi-directional I/O port with internal pullups. Port 1 pins that have 1's written to them are pulled high by the internal pullups, an in that state can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (IIL, on the data sheet) because of the internal pullups.
Port 1 also receives the low-order address byte during program verification. In the 83C154, Port 1 can sink/source three LS TTL inputs. It can drive CMOS inputs without external pullups.

PORT 2
Port 2 is an 8-bit bi-directional I/O port with internal pullups. Port 2 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (IIL, on the data sheet) because of the internal pullups. Port 2 emits the high-order address byte during fetches from external Program Memory and during accesses to external Data Memory that use 16-bit addresses (MOVX @ DPTR). In this application, it uses strong internal pullups when emitting 1's. During accesses to external Data Memory that use 8-bit addresses (MOVX @Ri), Port 2 emits the contents of the P2 Special Function Register.
It also receives the high-order address bits and control signals during program verification in the 83C154. Port 2 can sink/source three LS TTL inputs. It can drive CMOS inputs without external pullups.

PORT 3
Port 3 is an 8-bit bi-directional I/O port with internal pullups. Port 3 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (IIL, on the data sheet) because of the pullups. It also serves the functions of various special features of the MCS-51 Family, as listed below.

Port Pin	Alternate Function
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	INT0 (external interrupt 0)
P3.3	INT1 (external interrupt 1)
P3.4	T0 (Timer 0 external input)
P3.5	T1 (Timer 1 external input)
P3.6	WR (external Data Memory write strobe)
P3.7	RD (external Data Memory read strobe)

Port 3 can sink/source three LS TTL inputs. It can drive CMOS inputs without external pullups.

RST
A high level on this for two machine cycles while the oscillator is running resets the device. An internal pull-down resistor permits Power-On reset using only a capacitor connected to VCC.

ALE
Address Latch Enable output for latching the low byte of the address during accesses to external memory. ALE is activated as though for this purpose at a constant rate of 1/6 the oscillator frequency except during an external data memory access at which time one ALE pulse is skipped. ALE can sink/source 8 LS TTL inputs. It can drive CMOS inputs without an external pullup.

$\overline{PSEN}$
Program Store Enable output is the read strobe to external Program Memory. PSEN is activated twice each machine cycle during fetches from external Program Memory. (However, when executing out of external Program Memory, two activations of PSEN are skipped during each access to external Data Memory). PSEN is not activated during fetches from internal Program Memory. PSEN can sink/source 8 LS-TTL inputs. It can drive CMOS inputs without an external pullup.

$\overline{EA}$
When EA is held high, the CPU executes out of internal Program Memory (unless the Program Counter

exceeds 3FFFH). When EA is held low, the CPU executes only out of external Program Memory. EA must not be floated.

XTAL1

Input to the inverting amplifier that forms the oscillator. Receives the external oscillator signal when an external oscillator is used.

XTAL2

Output of the inverting amplifier that forms the oscillator. This pin should be floated when an external oscillator is used.

OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output respectively, of an inverting amplifier which is configured for use as an on-chip oscillator, as shown in *figure 5*. Either a quartz crystal or ceramic resonator may be used.

To drive the device from an external clock source, XTAL1 should be driven while XTAL2 is left unconnected as shown in *figure 6*. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum high and low times specified on the Data Sheet must be observed.

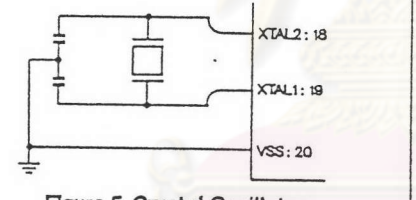


Figure 5. Crystal Oscillator

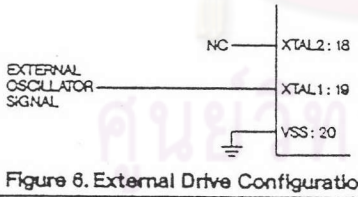


Figure 6. External Drive Configuration

PORT 1 SECONDARY FUNCTIONS

This is a quasi-bidirectional I/O port, internally pulled up when used as input ports. Two of the ports have been allocated a second function which are :

P1.0 [T2]: External clock input for timer/counter 2.

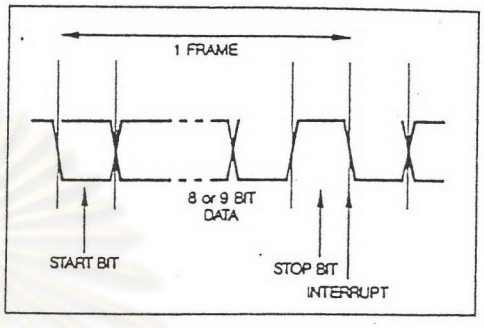
P1.1 [T2EX]: A trigger input for timer/counter 2, to be reloaded or captured causing the timer/counter 2 interrupt.

INTERRUPT MODES

The MHS 80C154/83C154 is capable of handling two external interrupts, three interrupts from the timers, and one interrupt from the serial port, through its incorporated six source, two-level interrupt structure.

SERIAL PORT TIMING

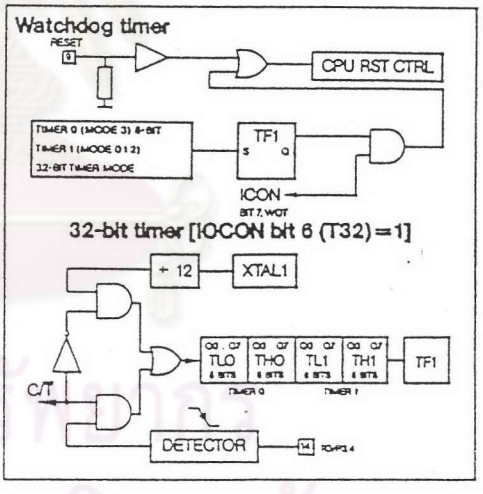
The interrupt is executed after the Stop Bit.



TIMER FUNCTIONS

In fact, timer 0 & 1 can be connected by a software instruction to implement a 32-bit timer function. Timer 0 (mode 3) or timer 1 (mode 0, 1, 2) or a 32-bit timer consisting of timer 0 + timer 1 can be employed in the watchdog mode, in which case a CPU reset is generated upon a TF1 flag.

The internal pull-up resistances at ports 1 ~ 3 can be set to a ten times increased value simply by software.



TIMER/EVENT COUNTER 2

Timer 2 is a 16-bit timer/counter like Timers 0 and 1, it can operate either as a timer or as an event counter. This is selected by bit C/$\overline{T2}$ in the Special Function Register T2CON *(Figure 7)*. It has three operating modes: "capture", "autoload" and "baud rate generator", which are selected by bits in T2CON as shown in *Table 2*.

Table 2. Timer 2 Operating Modes

RCLK+TCLK	CP/RL2	TR2	MODE
0	0	1	16 bit auto-reload
0	1	1	16-bit capture
1	X	1	baud rate generator
X	X	0	(off)

In the capture mode there are two options which are selected by bit EXEN2 in T2CON. If EXEN2 = 0, then Timer 2 is a 16-bit timer or counter which upon overflowing sets bit TF2, the Timer 2 overflow bit, which can be used to generate an interrupt. If EXEN2=1, then Timer 2 still does the above, but with the added feature that a 1-to-0 transition at external input T2EX causes the current value in the Timer 2 registers, TL2 ans TH2, to be captured into registers RCAP2L and RCAP2H, respectively. (RCAP2L and RCAP2H are new Special Function Registers in the 80C52). In addition, the transition at T2EX causes bit EXF2 in T2CON to be set, and EXF2, like TF2, can generate an interrupt.
The capture mode is illustrated in *Figure 8.*
In the auto-reload mode there are again two options, which are selected by bit EXEN2 in T2CON. If EXEN2= 0, then when Timer 2 rolls over it not only sets TF2 but also causes the Timer 2 registers to be reloaded with the 16-bit value in registers RCAP2L and RCAP2H, which are preset by software. If EXEN2=1, then Timer 2 still does the above; but with the added feature that a 1-to-0 transition at external input T2EX will also trigger the 16-bit reload and set EXF2.
The auto-reload mode is illustrated in *Figure 9.*
The baud rate generator mode is selected by: RCLK=1 and/or TCLK=1.

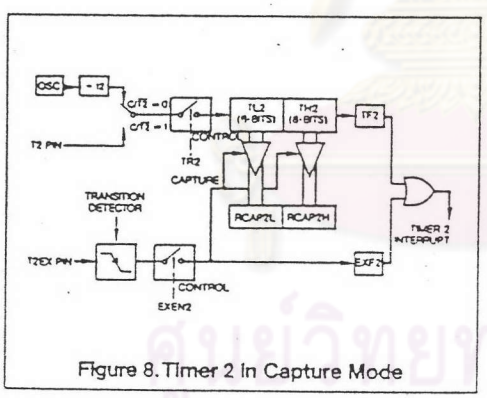


Figure 8. Timer 2 in Capture Mode

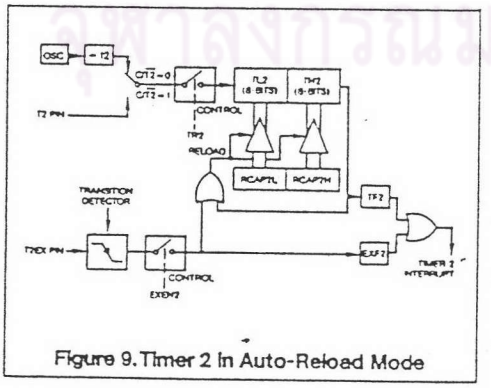


Figure 9. Timer 2 in Auto-Reload Mode

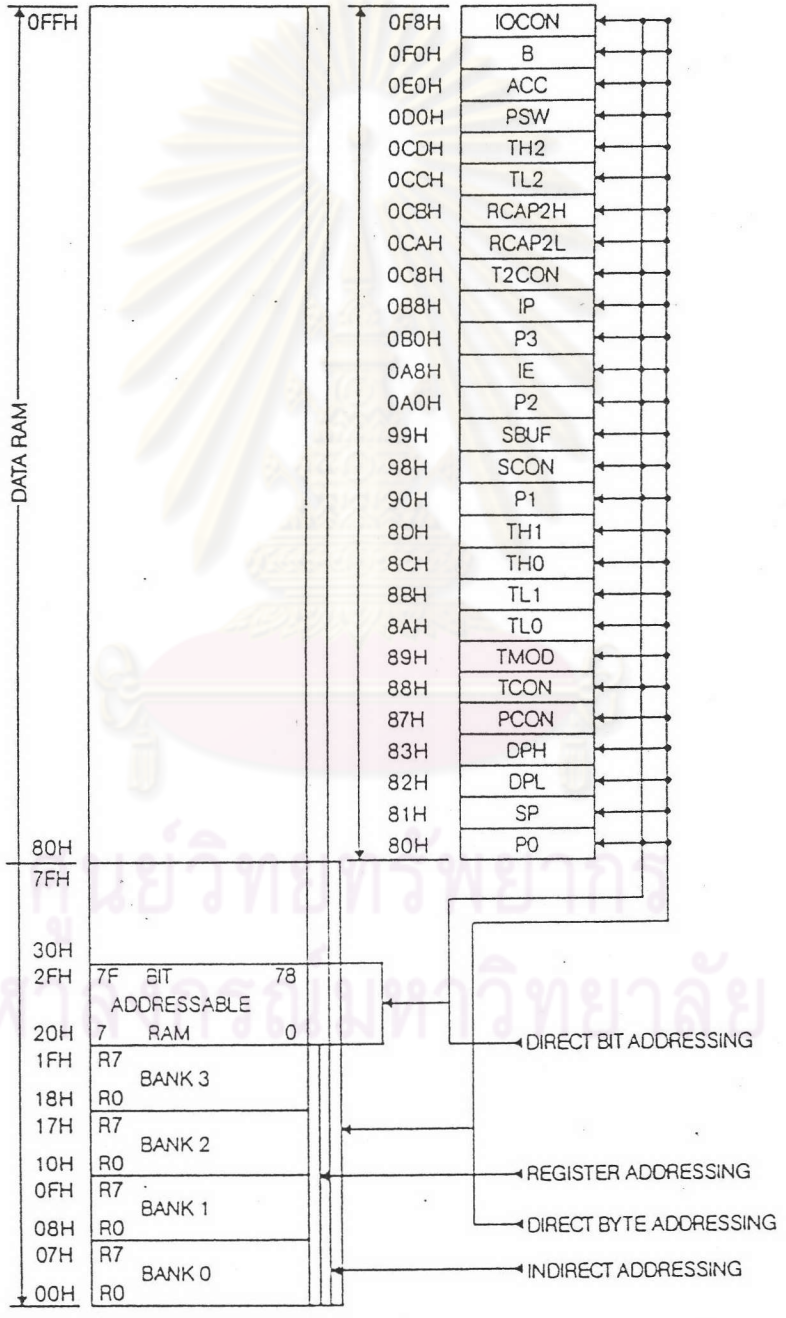
(MSB) (LSB)

TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2	CP/RL2

Symbol	Position	Name and Significance
TF2	T2CON.7	Timer 2 overflow flag set by a Timer 2 overflow and must be cleared by software. TF2 will not be set when either RCLK=1 or TCLK=1.
EXF2	T2CON.6	Timer 2 external flag set when either a capture or reload is caused by a negative transition on T2EX and EXEN2=1. When Timer 2 interrupt is enabled, EXF2=1 will cause the CPU to vector to the Timer 2 interrupt routine. EXF2 must be cleared by software.
RCLK	T2CON.5	Receive clock flag. When set, causes the serial port to use Timer 2 overflow pulses for its receive clock in modes 1 and 3. RCLK=0 causes Timer 1 overflow to be used for the receive clock.
TCLK	T2CON.4	Transmit clock flag. When set, causes the serial port to use Timer 2 overflow pulses for its transmit clock in modes 1 and 3. TCLK=0 causes Timer 1 overflows to be used for the transmit clock.
EXEN2	T2CON.3	Timer 2 external enable flag. When set, allows capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. EXEN2=0 causes Timer 2 to ignore events as T2EX.
TR2	T2CON.2	Start/stop control for Timer 2. A logic 1 starts the timer.
C/T2	T2CON.1	Timer or counter select. (Timer 2) 0 = Internal timer (OSC/12) 1 = External event counter (falling edge triggered).
CP/RL2	T2CON.0	Capture/Reload flag. When set, captures will occur on negative transitions at T2EX if EXEN 2=1. When cleared, auto reloads will occur either with Timer 2 overflows or negative transitions at T2EX when EXEN2 =1. When either RCLK=1 or TCLK=1, this bit is ignored and the timer is forced to auto-reload on Timer 2 overflow.

Figure 7. T2CON:
Timer/Counter 2 Control Register

DATA MEMORY AND SPECIAL FUNCTION REGISTER LAYOUT DIAGRAM



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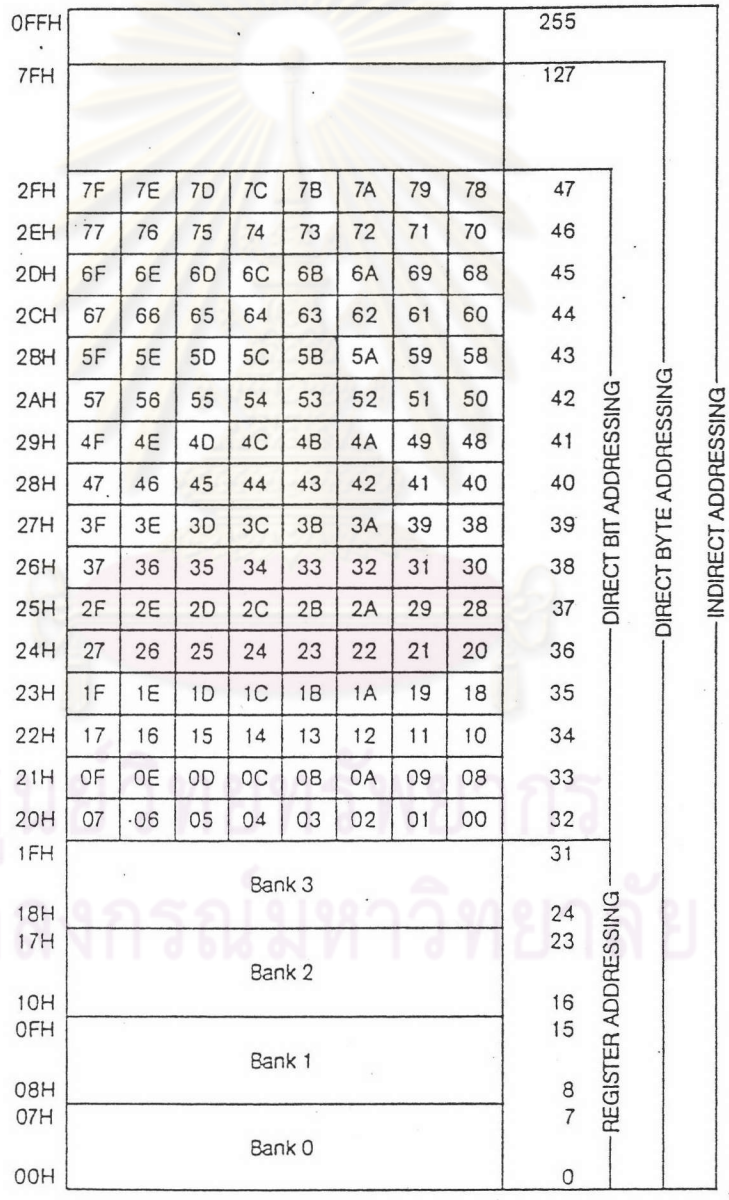
DETAILED DIAGRAM OF DATA MEMORY (RAM)



DETAILED DIAGRAM OF SPECIAL FUNCTION REGISTERS

Direct Byte Address	(MSB) Bit Address (LSB)								Special Function Register Symbol
	WDT	T32	SERR	IZC	P3HZ	P2HZ	P1HZ	ALF	
0F8H	FF	FE	FD	FC	FB	FA	F9	F8	IOCON
0F0H	F7	F6	F5	F4	F3	F2	F1	F0	B
0E0H	E7	E6	E5	E4	E3	E2	E1	E0	ACC
	CY	AC	F0	RS1	RS0	OV	F1	P	
0D0H	D7	D6	D5	D4	D3	D2	D1	D0	PSW
0CDH	Not Bit Addressable								TH2
0CCH	Not Bit Addressable								TL2
0C8H	Not Bit Addressable								RCAP2H
0CAH	Not Bit Addressable								RCAP2L
	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$	
0C8H	CF	CE	CD	CC	CB	CA	C9	C8	T2CON
	PCT		PT2	PS	PT1	PX1	PT0	PX0	
0B8H	BF	–	BD	BC	BB	BA	B9	B8	IP
0B0H	B7	B6	B5	B4	B3	B2	B1	B0	P3
	EA		ET2	ES	ET1	EX1	ET0	EX0	
0A8H	AF	–	AD	AC	AB	AA	A9	A8	IE
0A0H	A7	A6	A5	A4	A3	A2	A1	A0	P2
99H	Not Bit Addressable								SBUF
	SM0	SM1	SM2	REN	TB8	RB8	TI	RI	
98H	9F	9E	9D	9C	9B	9A	99	98	SCON
90H	97	96	95	94	93	92	91	90	P1
8DH	Not Bit Addressable								TH1
8CH	Not Bit Addressable								TH0
8BH	Not Bit Addressable								TL1
8AH	Not Bit Addressable								TL0
89H	Not Bit Addressable								TMOD
	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	
88H	8F	8E	8D	8C	8B	8A	89	88	TCON
87H	Not Bit Addressable								PCON
83H	Not Bit Addressable								DPH
82H	Not Bit Addressable								DPL
81H	Not Bit Addressable								SP
80H	87	86	85	84	83	82	81	80	P0

SPECIAL FUNCTION REGISTERS

TIME MODE REGISTER (TMOD)

NAME	ADDRESS	MSB 7	6	5	4	3	2	1	LSB 0
TMOD	89H	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0
BIT LOCATION	FLAG	FUNCTION							
TMOD.0	M0	M1	M0	Timer/counter 0 mode setting.					
		0	0	8-bit timer/counter with 5-bit prescalar.					
		0	1	16-bit timer/counter.					
		1	0	8-bit timer/counter with 8-bit auto reloading.					
TMOD.1	M1	1	1	Timer/counter 0 separated into TL0 (8-bit) timer/counter and TH0 (8-bit) timer/counter. TF0 is set by TL0 carry, and TF1 is set by TH0 carry.					
TMOD.2	C/$\overline{T}$	Timer/counter 0 count clock designation control bit. XTAL1·2 divided by 12 clocks is the input applied to timer/counter 0 when C/$\overline{T}$ = "0". The external clock applied to the T0 pin is the input applied to timer/counter 0 when C/$\overline{T}$ = "1".							
TMOD.3	GATE	When this bit is "0", the TR0 bit of TCON (timer control register) is used to control the start and stop of timer/counter 0 counting. If this bit is "1", timer/counter 0 starts counting when both the TR0 bit of TCON and $\overline{INT0}$ pin input signal are "1", and stops counting when either is changed to "0".							
TMOD.4	M0	M1	M0	Timer/counter 1 mode setting.					
		0	0	8-bit timer/counter with 5-bit prescalar.					
		0	1	16-bit timer/counter.					
		1	0	8-bit timer/counter with 8-bit auto reloading.					
TMOD.5	M1	1	1	Timer/counter 1 operation stopped.					
TMOD.6	C/$\overline{T}$	Timer/counter 1 count clock designation control bit. XTAL·2 divided by 12 clocks is the input applied to timer/counter 1 when C/$\overline{T}$ = "0". The external clock applied to the T1 pin is the input applied to timer/counter 1 when C/$\overline{T}$ = "1".							
TMOD.7	GATE	When this bit is "0", the TR1 bit of TCON is used to control the start and stop of timer/counter 1 counting. If this bit is "1", timer/counter 1 starts counting when both the TR1 bit of TCON and $\overline{INT1}$ pin input signal are "1", and stops counting when either is changed to "0".							

POWER CONTROL REGISTER (PCON)

NAME	ADDRESS	MSB 7	6	5	4	3	2	1	LSB 0
PCON	87H	SMOD	HPD	RPD	–	GF1	GF0	PD	IDL

BIT LOCATION	FLAG	FUNCTION
PCON.0	IDL	IDLE mode set when this bit is set to "1". CPU operations are stopped when IDLE mode is set, but XTAL1-2, timer/counters 0, 1, and 2, the interrupt circuits, and serial port remain active. IDLE mode is cancelled when the CPU is reset or when an interrupt is generated.
PCON.1	PD	PD mode set when this bit is set to "1". CPU operations and XTAL 1-2 are stopped when PD mode is set. PD mode is cancelled when the CPU is reset or when an interrupt is generated.
PCON.2	GF0	General purpose bit. Testing this flag when IDLE mode is cancelled by an interrupt shows whether the interrupt is a normal interrupt or an IDLE mode release interrupt.
PCON.3	GF1	General purpose bit. Testing this flag when PD mode is cancelled by an interrupt shows whether the interrupt is a normal interrupt or a PD mode release interrupt.
PCON.4	–	Reserved bit. The output data is "1" if the bit is read.
PCON.5	RPD	Bit used to specify cancellation of CPU power down mode (IDLE or PD) by interrupt signal. Power down mode cannot be cancelled by interrupt signal if interrupt is not enabled by IE (interrupt enable register) when this bit is "0". If the interrupt flag is set to "1" by an interrupt request signal when this bit is "1" (even if interrupt is disabled), the program is executed from the next address of the power down mode setting instruction. The flag is reset to "0" by software.

ENABLE	RECOVER	
0	0	PWD not cancelled
1	0	Execute interrupt routine
0	1	Execute next address
1	1	Execute interrupt routine

PCON.6	HPD	The hard power down setting mode is enabled when this bit is set to "1". If the level of the power failure detect signal applied to the HPD1 pin (pin 3.5) is changed from "1" to "0" when this bit is "1", XTAL1-2 oscillation is stopped and the system is put into hard power down mode. HPD mode is cancelled when the CPU is reset, or HPD1 pin go high.
PCON.7	SMOD	When the time/counter 1 carry signal is used as a clock in mode 1, 2 or 3 of the serial port, this bit has the following functions. The serial port operation clock is reduced by 1/2 when the bit is "0" for delayed processing. And when the bit is "1", the serial port operation clock is normal for faster processing.

TIMER CONTROL REGISTER (TCON)

NAME	ADDRESS	MSB 7	6	5	4	3	2	1	LSB 0
TCON	88H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
BIT LOCATION	FLAG	FUNCTION							
TCON.0	IT0	External interrupt 0 signal used in level detect mode when this bit is "0", and in trigger detect mode when "1".							
TCON.1	IE0	Interrupt request flag for external interrupt 0. Bit is reset automatically when interrupt is serviced. Bit can be set and reset by software when IT0 = "1".							
TCON.2	IT1	External interrupt 1 signal used in level detect mode when this bit is "0", and in trigger detect mode when "1".							
TCON.3	IE1	Interrupt request flag for external interrupt 1. Bit is reset automatically when interrupt is serviced. Bit can be set and reset by software when IT1 = "1".							
TCON.4	TR0	Counting start and stop control bit for timer/counter 0. Timer/counter 0 starts counting when this bit is "1", and stops counting when "0".							
TCON.5	TF0	Interrupt request flag for timer interrupt 0. Bit is reset automatically when interrupt is serviced. Bit is set to "1" when carry signal is generated from timer/counter 0.							
TCON.6	TR1	Counting start and stop control bit for timer/counter 1. Timer/counter 1 starts counting when this bit is "1", and stops counting when "0".							
TCON.7	TF1	Interrupt request flag for timer interrupt 1. Bit is reset automatically when interrupt is serviced. Bit is set to "1" when carry signal is generated from timer/counter 1.							

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SERIAL PORT CONTROL REGISTER (SCON)

NAME	ADDRESS	MSB 7	6	5	4	3	2	1	LSB 0
SCON	98H	SM0	SM1	SM2	REN	TB8	RB8	TI	RI

BIT LOCATION	FLAG	FUNCTION
SCON.0	RI	"End of serial port reception" interrupt request flag. This flag must be reset by software during interrupt service routine. This flag is set after the eighth bit of data has been received when in mode 0, or by the STOP bit when in any other mode. In mode 2 or 3, however RI is not set if the RB8 data is "0" with SM2 = "1". RI is set in mode 1 if STOP is received when SM2 = "1".
SCON.1	TI	"End of serial port transmission" interrupt request flag. This flag must be reset by software during interrupt service routine. This flag is set after the eighth bit of data has been sent when in mode 0, or after the last bit of data has been sent when in any other mode.
SCON.2	RB8	The ninth bit of data received in mode 2 or 3 is passed to RB8. The STOP bit is applied to RB8 if SM2 = "0" when in mode 1. RB8 can not be used in mode 0.
SCON.3	TB8	The TB8 data is sent as the ninth data bit when in mode 2 or 3. Any desired data can be set in TB8 by software.
SCON.4	REN	Reception enable control bit. No reception when REN = "0". Reception enabled when REN = "1".
SCON.5	SM2	If the ninth bit of received data is "0" with SM2 = "1" in mode 2 or 3, the "end of reception" signal is not set in the RI flag. Nor is the "end of reception" signal set in the RI flag if the STOP bit is not "1" when SM2 = "1" in mode 1.
SCON.6	SM1	SM0 | SM1 | MODE 0 | 0 | 0 — 8-bit shift register I/O. 0 | 1 | 1 — 8-bit UART variable baud rate.
SCON.7	SM0	1 | 0 | 2 — 9-bit UART 1/32 XTAL1, 1/64 XTAL1 baud rate. 1 | 1 | 3 — 9-bit UART variable baud rate.

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INTERRUPT ENABLE REGISTER (IE)

NAME	ADDRESS	MSB 7	6	5	4	3	2	1	LSB 0
IE	0A8H	EA	–	ET2	ES	ET1	EX1	ET0	EX0

BIT LOCATION	FLAG	FUNCTION
IE.0	EX0	Interrupt control bit for external interrupt 0. Interrupt disabled when bit is "0". Interrupt enabled when bit is "1".
IE.1	ET0	Interrupt control bit for timer interrupt 0. Interrupt disabled when bit is "0". Interrupt enabled when bit is "1".
IE.2	EX1	Interrupt control bit for external interrupt 1. Interrupt disabled when bit is "0". Interrupt enabled when bit is "1".
IE.3	ET1	Interrupt control bit for timer interrupt 1. Interrupt disabled when bit is "0". Interrupt enabled when bit is "1".
IE.4	ES	Interrupt control for serial port. Interrupt disabled when bit is "0". Interrupt enabled when bit is "1".
IE.5	ET2	Interrupt control bit for timer interrupt 2. Interrupt disabled when bit is "0". Interrupt enabled when bit is "1".
IE.6	–	Reserved bit. The output data is "1" if the bit is read.
IE.7	EA	Overall interrupt control bit. All interrupts are disabled when bit is "0". All interrupts are controlled by IE.0 thru IE.5 when bit is "1".

INTERRUPT PRIORITY REGISTER (IP)

NAME	ADDRESS	MSB 7	6	5	4	3	2	1	LSB 0
IP	0B8H	PCT	–	PT2	PS	PT1	PX1	PT0	PX0

BIT LOCATION	FLAG	FUNCTION
IP.0	PX0	Interrupt priority bit for external interrupt 0. Priority is assigned when bit is "1".
IP.1	PT0	Interrupt priority bit for timer interrupt 0. Priority is assigned when bit is "1".
IP.2	PX1	Interrupt priority bit for external interrupt 1. Priority is assigned when bit is "1".
IP.3	PT1	Interrupt priority bit for timer interrupt 1. Priority is assigned when bit is "1".
IP.4	PS	Interrupt priority bit for serial port. Priority is assigned when bit is "1".
IP.5	PT2	Interrupt priority bit for timer interrupt 2. Priority is assigned when bit is "1".
IP.6	–	Reserved bit. The output data is "1" if the bit is read.
IP.7	PCT	Priority interrupt circuit control bit. The priority register contents are valid and priority assigned interrupts can be processed when this bit is "0". When the bit is "1", the priority interrupt circuit is stopped, and interrupts can only be controlled by the interrupt enable register (IE).

PROGRAM STATUS WORD REGISTER (PSW)

NAME	ADDRESS	MSB 7	6	5	4	3	2	1	LSB 0
PSW	0D0H	CY	AC	F0	RS1	RS0	OV	F1	P

BIT LOCATION	FLAG	FUNCTION
PSW.0	P	Accumulator (ACC) parity indicator. "1" when the "1" bit number in the accumulator is an odd number, and "0" when an even number.
PSW.1	F1	User flag which may be set to "0" or "1" as desired by the user.
PSW.2	OV	Overflow flag which is set if the carry C6 from bit 6 of the ALU or CY is "1" as a result of an arithmetic operation. The flag is also set to "1" if the resultant product of executing a multiplication instruction (MUL AB) is greater than 0FFH, but is reset to "0" if the product is less than or equal to 0FFH.
PSW.3	RS0	RAM register bank switch.
PSW.4	RS1	

RS1	RS0	BANK	RAM ADDRESS
0	0	0	00H – 07H
0	1	1	08H – 0FH
1	0	2	10H – 17H
1	1	3	18H – 1FH

PSW.5	F0	User flag which may be set to "0" or "1" as desired by the user.
PSW.6	AC	Auxiliary carry flag. This flag is set to "1" if a carry C_3 is generated from bit 3 of the ALU as a result of executing an arithmetic operation instruction. In all other cases, the flag is reset to "0".
PSW.7	CY	Main carry flag. This flag is set to "1" if a carry C_7 is generated from bit 7 of the ALU as result of executing an arithmetic operation instruction. If a carry C_7 is not generated, the flag is reset to "0".

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TIMER 2 CONTROL REGISTER (T2CON)

NAME	ADDRESS	MSB 7	6	5	4	3	2	1	LSB 0
T2CON	0C8H	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$
BIT LOCATION	FLAG	FUNCTION							
T2CON.0	CP/$\overline{RL2}$	Capture mode is set when TCLK + RCLK = "0" and CP/$\overline{RL2}$ = "1". 16-bit auto reload mode is set when TCLK + RCLK = "0" and CP/$\overline{RL2}$ = "0". CP/$\overline{RL2}$ is ignored when TCLK + RCLK = "1".							
T2CON.1	C/$\overline{T2}$	Timer/counter 2 count clock designation control bit. The internal clocks (XTAL1-2 ÷ 12, XTAL1-2 ÷ 2) are used when this bit is "0", and the external clock applied to the T2 is passed to timer/counter 2 when the bit is "1".							
T2CON.2	TR2	Timer/counter 2 counting start and stop control bit. Timer/counter 2 commences counting when this bit is "1" and stops counting when "0".							
T2CON.3	EXEN2	T2EX timer/counter 2 external control signal control bit. Input of the T2EX signal is disabled when this bit is "0", and enabled when "1".							
T2CON.4	TCLK	Serial port transmit circuit drive clock control bit. Timer/counter 2 is switched to baud rate generator mode when this bit is "1", and the timer/counter 2 carry signal becomes the serial port transmit clock. Note, however, that the serial ports can only use the timer/counter 2 carry signal in serial port modes 1 and 3.							
T2CON.5	RCLK	Serial port receive circuit drive clock control bit. Timer/counter 2 is switched to baud rate generator mode when this bit is "1", and the timer/counter 2 carry signal becomes the serial port receive clock. Note, however, that the serial ports can only use the timer/counter 2 carry signal in serial port modes 1 and 3.							
T2CON.6	EXF2	Timer/counter 2 external flag. This bit is set to "1" when the T2EX timer/counter 2 external control signal level is changed from "1" to "0" while EXEN2 = "1". This flag serves as the timer interrupt 2 request signal. If an interrupt is generated, EXF2 must be reset to "0" by software.							
T2CON.7	TF2	Timer/counter 2 carry flag. This bit is set to "1" by a carry signal when timer/counter 2 is in 16-bit auto reload mode or in capture mode. This flag serves as the timer interrupt 2 request signal. If an interrupt is generated, TF2 must be reset to "0" by software.							

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MHS

AUGUST 1988

APPLICATION NOTE AN1043

DIFFERENCES BETWEEN THE 83C154 AND THE 80C52

The 83C154 is an 8-bit microcontroller belonging to the MHS C51 family of microcontrollers. Its instruction set and the number of functions implemented are fully compatible with this family. The innovations concern the size of RAM available, 16 Kbytes instead of 8 and the new functions listed in table 1.

- TIMER 1 and TIMER 0 :
32-bit TIMER/COUNTER,
WATCH DOG,
Asynchronous counting in POWER-DOWN mode.
- PORTS, 1, 2, 3 :
Choice of output resistance value.
- UART :
Receive error detection.
- POWER-DOWN MODE :
Software and hardware control.
- IDLE MODE :
New possibility for exiting from this mode.
- INTERRUPTS :
New mode.
- BIT TRANSFER :
New instruction for implementing transfers between bits.

IOCON

Figure 1 shows the correspondence between the 83C154's new functions and the different bits of the IOCON register (0F8H) which can only be addressed by bit.

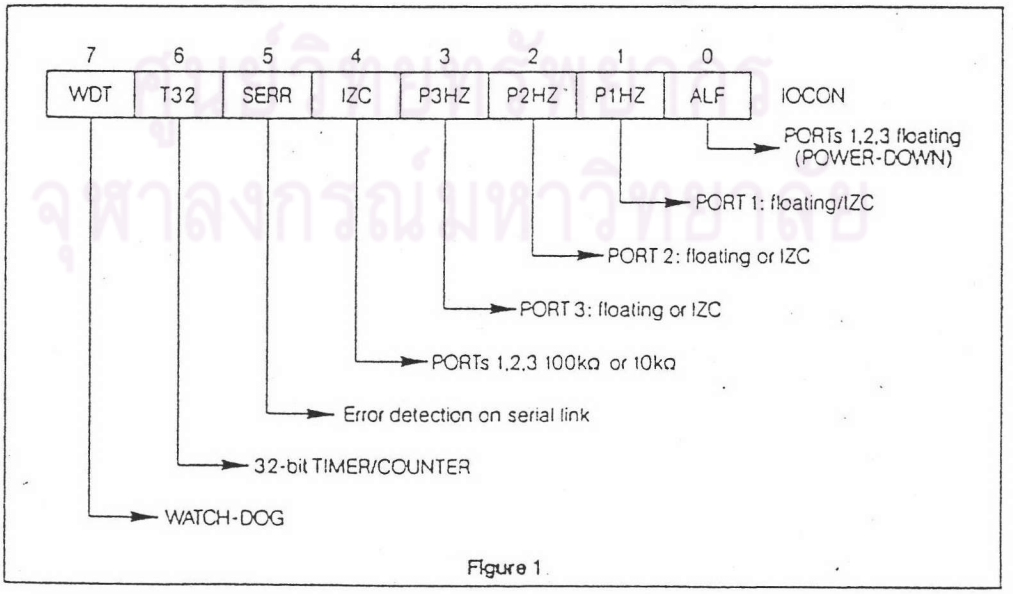

Figure 1

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BITS RPD AND HPD

Two supplementary bits of register PCON, RPD and HPD, are used to provide the additional management functions for the POWER-DOWN and IDLE modes. Figure 2 shows the correspondence between the PCON register bits and the new power saving modes. PCON is not bit-addressable.

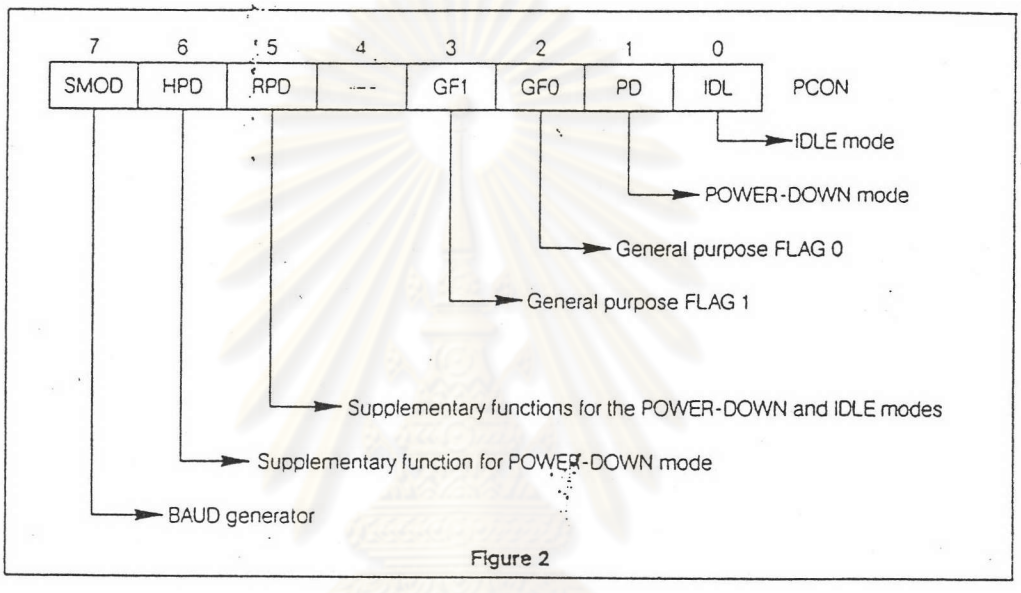


Figure 2

TIMER/COUNTERs 0 AND 1

The 83C154 has three 16-bit TIMER/COUNTERS, TIMER 0, TIMER 1 and TIMER 2. The architecture and instruction set of these three TIMERS are compatible with the MHS C51 family. In addition to the 4 existing modes, 2 other modes have been added for TIMER 1 and TIMER 0 :

- a WATCH-DOG mode,
- A 32-bit TIMER/COUNTER mode.

These new modes are explained in detail below.

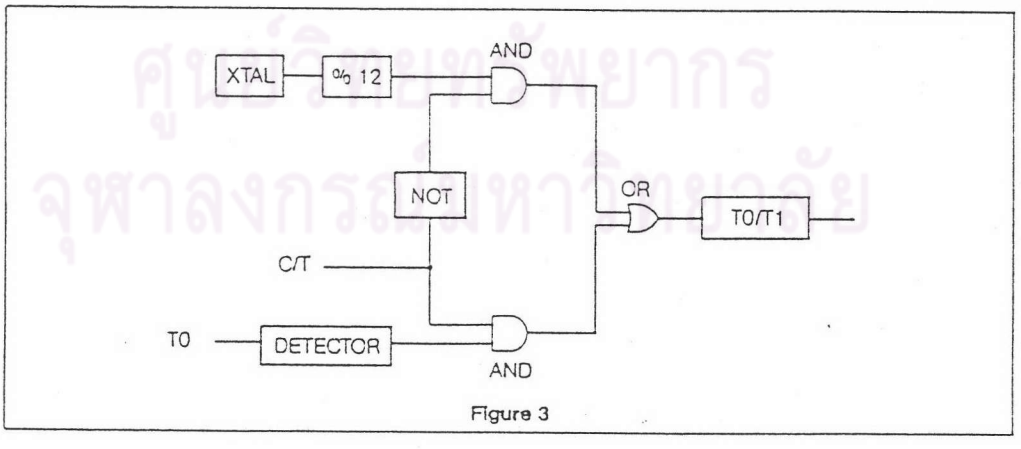
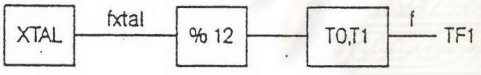


Figure 3

32-BIT MODE:

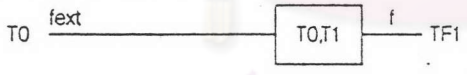
This mode is activated by setting bit T32 of register IOCON (ICON.6=OFEH) to "1". This action causes TIMER 0 and TIMER 1 to be configured as a 32-bit TIMER/COUNTER and this, whatever the value of the configuration register TMOD. TIMER 0 constitutes the LSBs and TIMER 1 the MSBs. Two sources provide control of this 32-bit TIMER/COUNTER, either the 83C154's clock (TIMER mode) or an external clock connected to input T0 (COUNTER mode). This selection is made by programming bit C/T0 of register TMOD (089H). If (C/T0)=0, the 83C154 is in TIMER mode and if (C/T)=1, it is in COUNTER mode.
Counting is started when bit (T32)=1 and is stopped by complementing T32. If the TIMER/COUNTER is to be stopped, when restarted and stopped again, care must be taken to ensure that bits TR0 and TR1 are programmed with the value 0. The contrary would result in the restarting of one of the two TIMER/COUNTERs which would modify the content of the 32-bit TIMER/COUNTER. Bit TF1 enables detection of a TIMER/COUNTER overflow. The following formulae are to be used for calculating the required frequency:

32-bit TIMER MODE



$$f = \frac{fxtal}{12 \times (65\,536 - (T0,T1))}$$

32-bit COUNTER MODE

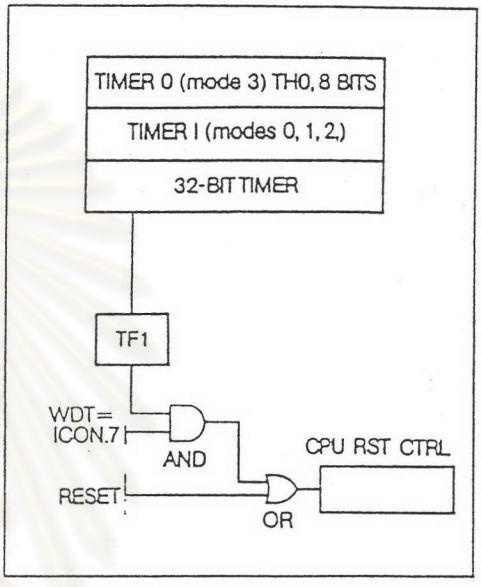


$$f = \frac{fext}{65\,536 - (T0,T1)}$$

$$fext < \frac{fxtal}{24}$$

In order to be able to increment its counter, the 83C154 must detect a complete signal at its input, that is to say a succession of two transitions. On each machine cycle the 83C154 samples its T0 input (fxtal/12). Therefore, to increment its counter, it must read its T0 input at least twice, in other words a minimum time of 24 clock periods. Thus, the maximum frequency of signal fxtal is less than or equal to fxtal/24.

WATCH-DOG MODE



This mode is activated by setting bit WDT of register ICON (ICON.7=OFFH) to "1"
Several configurations are possible, but always based on TIMERs 0 and 1 :
– TIMER 0 : program in mode 3, TH0 is seen as an 8-bit TIMER and is controlled by TR1.
– TIMER 1 : can be programmed in mode 0, 1 and 2.
– TIMER 32 : special 83C154 mode which combines the bits of TIMER 0 and TIMER 1 to form a single 32-bit TIMER.
Whatever the chosen configuration, the WATCH-DOG can be controlled either by an internal source (C/T=0) or by an external source (C/T=1). The TIMER is started by setting bit TR0 or TR1 or TR32 of register TCON or ICON to "1". A timer overflow is detected by flag TF1 (TF1=1) of register TCON (TCON.7=08FH). When an overflow occurs (TF1) = 1, the 83C154 is reset immediately. This action has the same effects as a hardware reset. As there are no precautions for protecting bit WDT, special care must be taken during program writing to avoid accidental manipulation of this bit. In particular, the user should use the IOCON register bit manipulation instructions:
– SETB X and CLR X
in preference to the byte manipulation instructions :
– MOV IOCON, #XXH, ORL IOCON, #XXH,
ANL IOCON, #OXXH,.....

EXTERNAL COUNTING IN POWER-DOWN MODE

In POWER-DOWN mode, the oscillator is stopped and the 83C154's activity is frozen. However, if an external clock is connected to one of the inputs T1 or T0, implementation of the functions of TIMER 0 and TIMER 1 can continue. In this case, counting is asynchronous and the maximum, admissible signal frequency on input T1 or T0 only depends on the counter's intrinsic constants. Overflow of one of the counters, TF0=1 or TF1=1 will either trigger the interrupt or will force a reset if the counter is programmed in the WATCH-DOG mode (COUNTER 1 only). In both cases, the overflow of one of the two counters results in exit from the POWER-DOWN mode.

POWER SAVING MODE IDLE MODE

This mode is 100% compatible with that of the 80C52 and has an additional function. This mode is software-controlled. Entry and execution are implemented by setting the IDL bit to "1". Exit from this mode is controlled by bit RPD of register PCON and the interrupt register IE:

- RPD=0

If no interrupt is enabled, the only possibility of exiting from this mode is a reset of the 83C154.
If the interrupts are enabled, exit from the mode can be made either by interrupt or by reset.

- RPD=1
- Whether enabled or not, an interrupt request causes the 83C154 to exit from the POWER-DOWN mode.
- If no interrupt is present, only a reset will cause the 83C154 to exit from this mode.

Table 2 summarizes the different types of operation of this mode.

Input conditions		Output conditions		
IDLE	IDL	RPD	INTERRUPTS	RST
SOFTWARE	1	0	If authorized	YES
	1	1	Authorized or not	YES

Table 2

POWER-DOWN MODE

This mode is controlled by:
- software by bits PD, RPD and the IE register,
- hardware by bit HPD.

On entry into this mode, the clock is stopped and the 83C154's activity is suspended. However, the UART ant TIMER (0/1) functions continue to work if :
- an external clock is connected to one of the inputs T0 or T1.
- register TMOD is programmed correctly (C/T=1).

HARDWARE CONTROL

Hardware control (HPD=1)

This mode is entirely software-controlled by an external signal connected to input T1. The trailing edge of this signal activates the POWER-DOWN mode (after the current instruction has been executed). The leading edge of this same signal (T1) or a reset enables the 83C154 to quit this mode. Interrupt requests, even if enabled, do not enable exit from this mode.

SOFTWARE CONTROL

- Entry to mode (PD=1)

The POWER-DOWN mode is entered when bit PD of register PCON is at "1".

- Exit from mode

Exit from this mode is controlled by bit RPD.
(RPD=0)
If the interrupts are not enabled, the only means of exit from this mode is to apply a reset to input RST.
(RPD=1)
Whether the interrupts are enabled or not, an interrupt request or a reset causes the 83C154 to quit this mode.
If the interrupt requests are enabled by the IE register, execution of the program continues wiht the servicing of the interrupt sub-routine.
If the interrupt requests are not enabled, the instruction following the POWER-DOWN mode instruction is executed.
Table 3 summarizes the different types of operation in this mode.

Input conditions				Output conditions			
POWER-DOWN	HPD	PD	T1	T1	RPD	INTERRUPTS	RST
SOFTWARE	0	1	X	X	0	If authorized	Yes
	0	1	X	X	1	Authorized or not	Yes
HARDWARE	1	0			X	X	Yes
HARDWARE and SOFTWARE	1	0			0	If authorized	Yes
	1	1			1	Authorized or not	Yes

X = without action

Table 3

COMMENT

In the case of mixed-hardware software working, the POWER-DOWN mode can be entered by means of HPD=1 or PD=1.
When RPD=1, exit from the mode occurs when T1 returns to 1 and when an interrupt request is generated. Otherwise the only way of quitting the mode is to apply a reset to input RST.
It is possible to operate the POWER-DOWN and IDLE modes in parallel. Exit is only possible when exit T1 goes high and if, with RPD 1=1, an interrupt request has been generated. Otherwise the only possibility of exiting is to generate a reset on input RST.

SERIAL LINK

The 83C154 has all four of the 80C52's operating modes, with in addition:
- FRAME and OVERRUN error detection,
- Operation (mode 1, 3) in POWER-DOWN and IDLE mode.

FRAME ERROR

This function enables detection of a transmission error in the format of a received character. Arrival of a character is detected by the trailing edge of the character start bit. All received bits are sampled on the 7th, 8th and 9th bits of the receive clock (16 or 32 times the reception speed). A majority vote is taken on these 3 bits to determine if the received bit is a "1" or a "0". If a "0" is read in place of a stop bit (which is always at "1"), there is an error in the transmission format and bit SERR (SERR) = 1 of register IOCON (IOCON=0F8H) is set at "1". The timing diagram below represents a character with its stop bit missing. A format error is signalled by bit SERR.
Figure 3 gives the timing diagrams for a serial gate presenting this error.

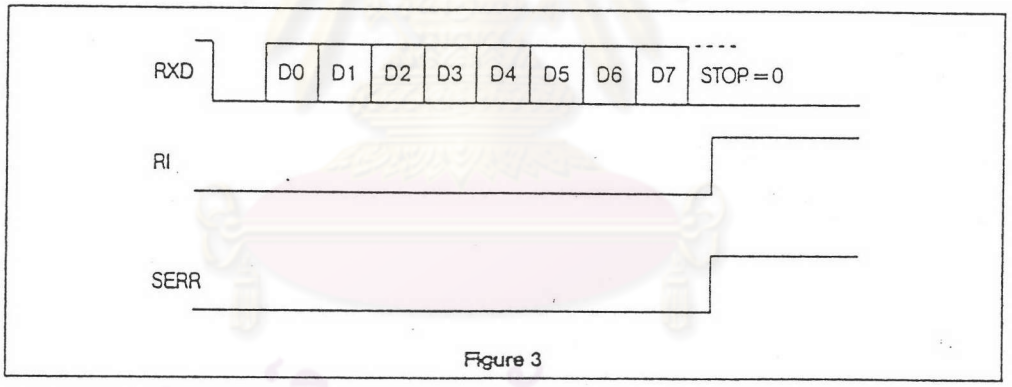


Figure 3

As in the case of the RI flag, the SERR flag is reset to zero by the software.

OVERRUN ERROR

This function detects when a received character has not been read and has been replaced by another character. Reception of a character is signalled to the 83C154 by raising the RI flag to "1". This flag stays at "1" until the user resets it to "0" (CLR RI). If the next character is sent before the previous character has been read, an error is detected and bit SERR of register IOCON (IOCON=0F8H) is set to "1".
Figure 4 shows the timing diagrams of the serial link for this error.

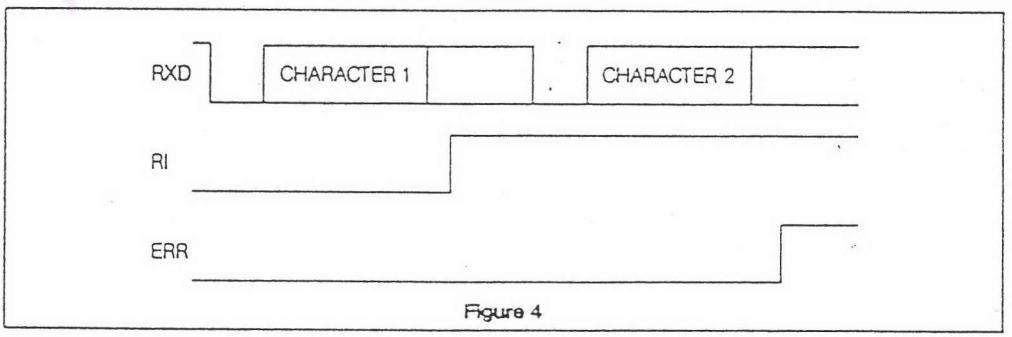


Figure 4

As in the case of the RI flag, the SERR flag is reset to zero by the software.

POWER-DOWN AN IDLE MODE

The serial link is able to run in power down and idle mode. As the CPU clock is frozen, only the UART mode 1 and 3 are operationnal.

The transmission clock has to be generated with Timer 1 and use the external clock ((C/T)=1, ((Gate=0)). Max frequency will be: Fext (Fxtal/24).
Fext ≤ OSC/24

I/O PORT

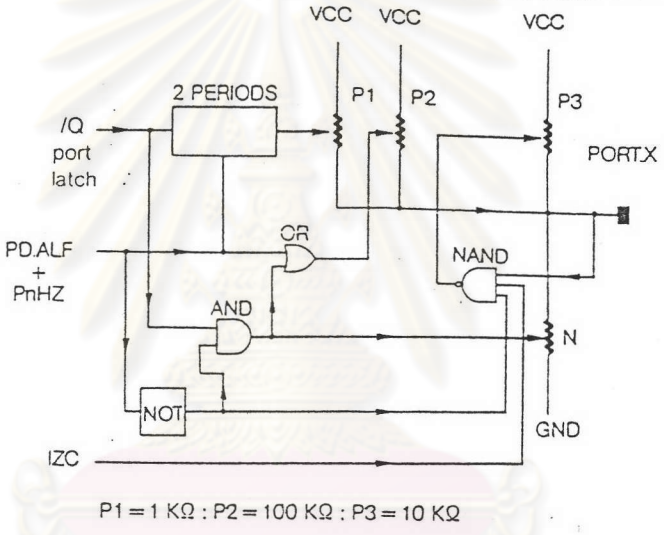


Figure 6

The I/O drives for P1, P2, P3 of the 83C154 are impedance programmable.
The I/O buffers for ports 1, 2 and 3 implemented as shown in *Fig 6*.

The impedance can be programmed through the register IOCON (IOCON = 0F8H).
Table 4 is a detail of register IOCON showing PORT impedance selection.

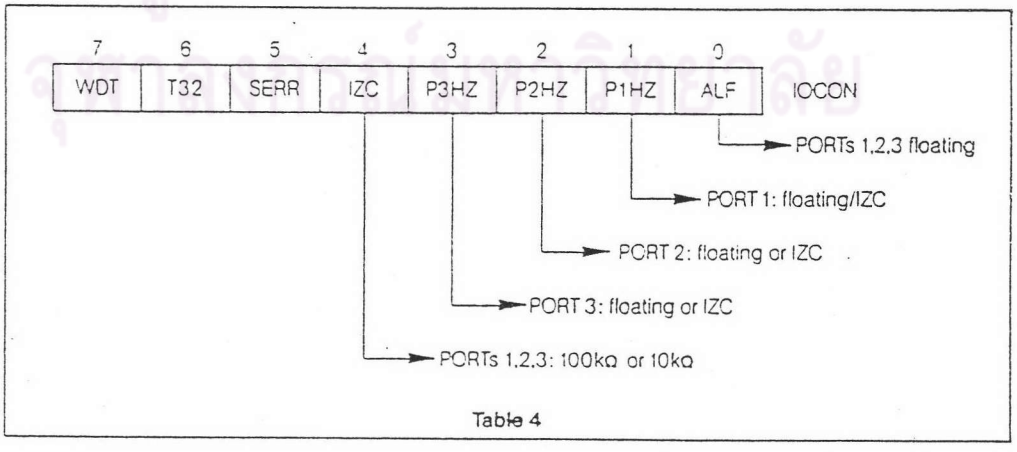


Table 4

There is a choice of three possible resistance values : 10k, 100k, and floating.
ALF = 1, all the PORTS (1, 2 and 3) are floating in POWER-DOWN mode.
P1HZ, P2HZ or P2HZ = 0 the output resistance depends on the choice of IZC.
P1HZ, P2HZ or P3HZ = 1 the PORT is floating.
IZC = 0, the output resistance is 10kΩ.
IZC = 1, the output resistance is 100kΩ.
Table 5 below is a summary of the possibilities offered by register IOCON.

ALF	IZC	PnHZ	Pn
0	0	0	10kΩ
0	0	1	F
0	1	0	100kΩ
0	1	1	F
1	X	X	*F

F = FLOATING; X = 1 or 0; $1 \leqslant n \leqslant 3$
* in POWER-DOWN mode

The 83C154's IP register (088H) has a new function as the possibility of making the interrupt level identical for all types of 83C154 interrupts.

Programming of bit PCT ((PCT)=1, PCT=IP.7) gives all interrupts the same level.
Table 6 is a detail of the IP register.

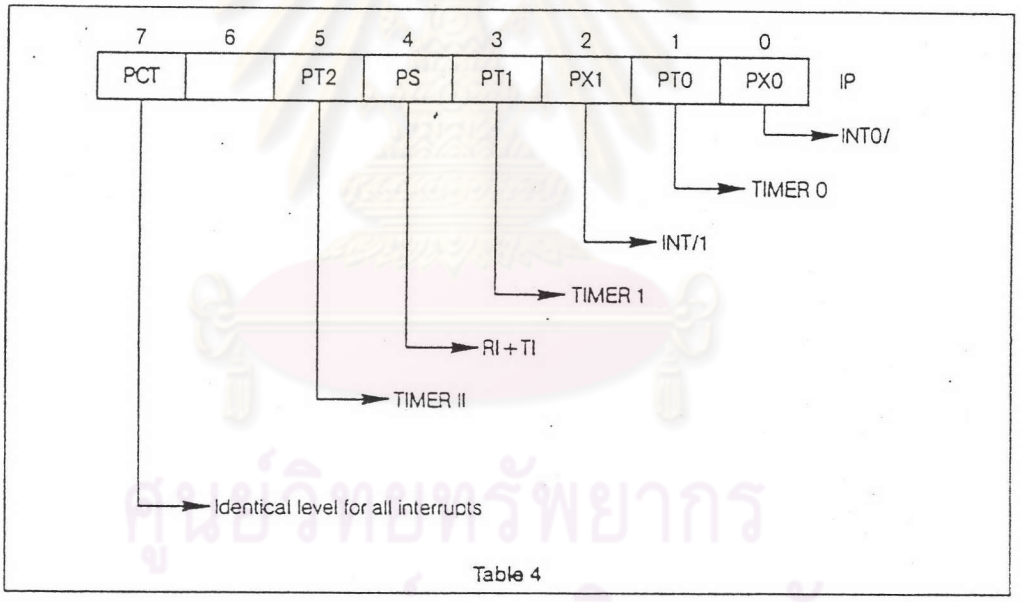


Table 4

All the bits of this register can be addressed directly.

BIT TRANSFER INSTRUCTION

Instruction MOV BIT (code OA5H) enables transfer of a SOURCE BIT value from one register to the DESTINATION BIT of another register. Execution of the MOV BIT instruction is only possible for bit addressable registers.

SYNTAX:

MOVBIT bit ADDR (source), bit ADDR (destination)		
A5H	XX	XX

For example: ACC.2 ← P30.5
MOV P30.5,ACC.2
A5 B5 E2

MHS

AUGUST 1988

APPLICATION NOTE AN1044

DIFFERENCES BETWEEN OKI AND MHS 83C154s

MHS's 83C154 is a development of INTEL's 80C51/52 family of microcontrollers. All the basic mechanisms (interrupts, I/O, etc.) of MHS's 83C154 are 100% compatible with those of the INTEL 80C51/C52 family.

There are several incompatibilities between the basic mechanisms of the OKI 83C154 and the MHS 83C154. In practice, these differences are invisible to the user. They are listed below :

- Division by zero.
- Conditional jump.
- Long jump on a call from a sub-routine.
- Serial port.
- Port writing.
- TIMER interrupt request.

These differences are discussed in the following paragraphs.

DIVISION BY ZERO

Division by zero is performed by putting the numerator in register B and the denominator in register A. The result in the division is stored in register A and the remainder in register B. The difference between MHS and OKI is in the result and is shown below :

A div B → result =A remainder = B

MHS B = FF OKI B = 00

CONDITIONAL JUMP

Conditional jumps JC, JNC, JZ and JNZ are single byte instructions that execute in 2 machine cycles. Before branching to the new address :
- MSH increments the PC twice.
- OKI increments the PC once.

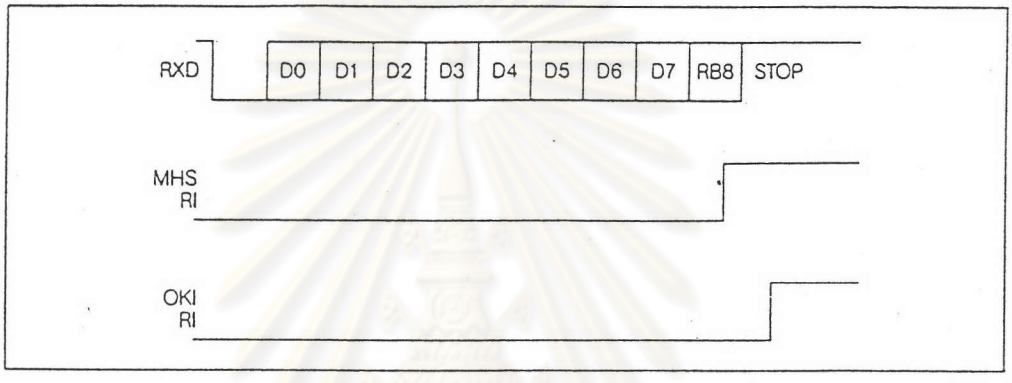
LONG JUMP

The long jumps, LCALL and LJMP are three-byte instructions that execute in 2 machine cycles. Before branching to the new address:
- MHS increments the PC 3 times.
- OKI increments the PC twice.

End of reception in modes 1, 2 and 3

When a received character is complete, an interrupt request (RI) is generated for the microcontroller. Once more, we can see a difference between the manufacturers :

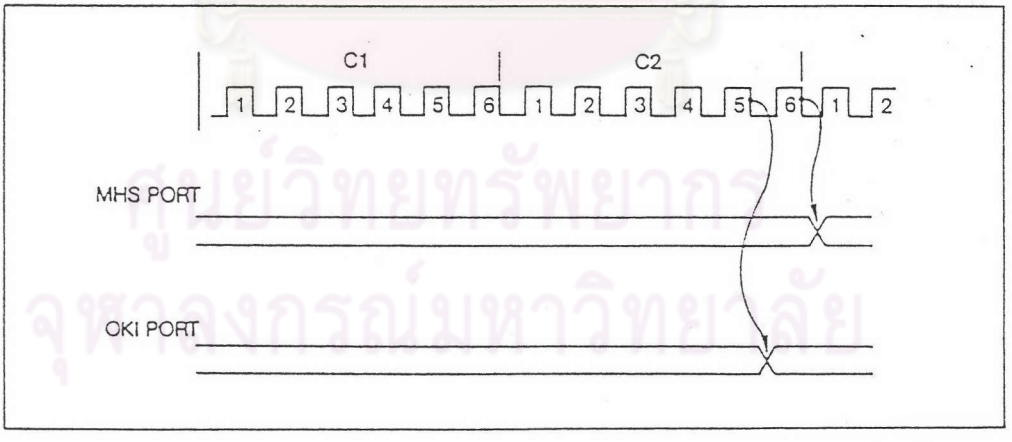
MHS : the interrupt request in the center of the 9th bit received,
OKI : the interrupt request is generated in the center of the stop bit.



INPUT/OUTPUT PORTS

The port write instructions execute in 2 cycles. The data arrives at the gate outputs on the second instruction cycle. The rapidity with which the data arrives at the gates varies with the manufacturer :

MHS : the data arrives in phase with the 1 st clock cycle of the instruction cycle following the write cycle.
OKI : the data arrive in phase with the 6th clock cycle of the 2nd write cycle.



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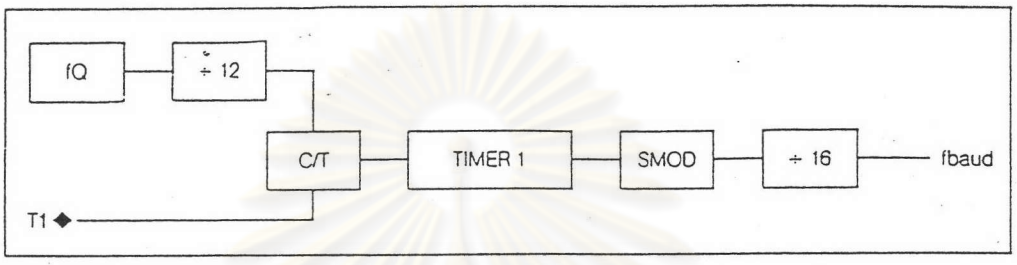
SERIAL PORT

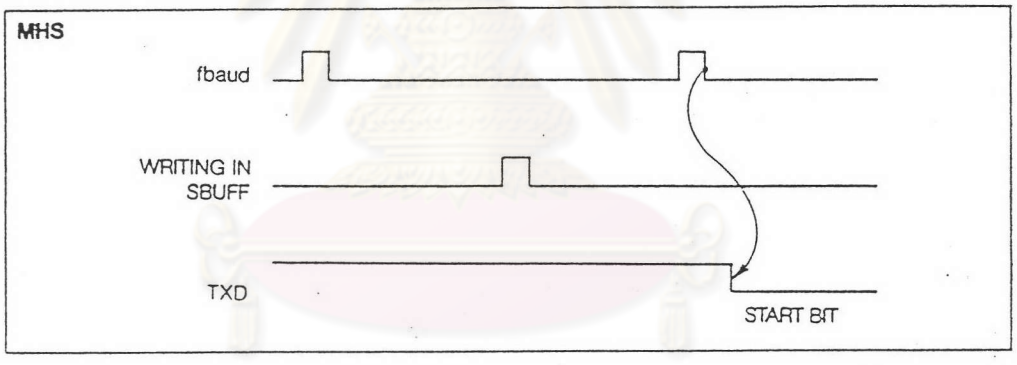
Transmission clock start-up in modes 1, 2 and 3.

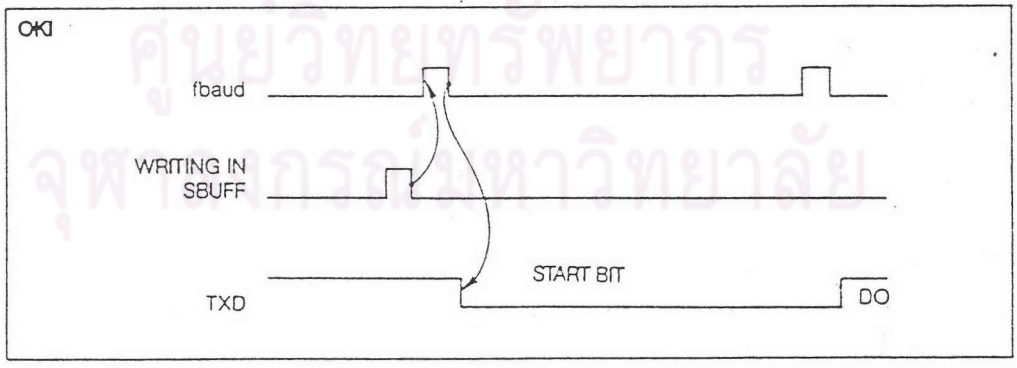


The divider by 16 which, ultimately, generates the clock, is controlled differently according to the manufacturer :

- MHS: the divider starts on completion of RESET,
- OKI: the divider starts after the following instructions :
  - MOV TCON, #XX
  - MOV SCON, #XX
  - MOV SBUF, #XX

The following timing diagrams illustrate the differences :





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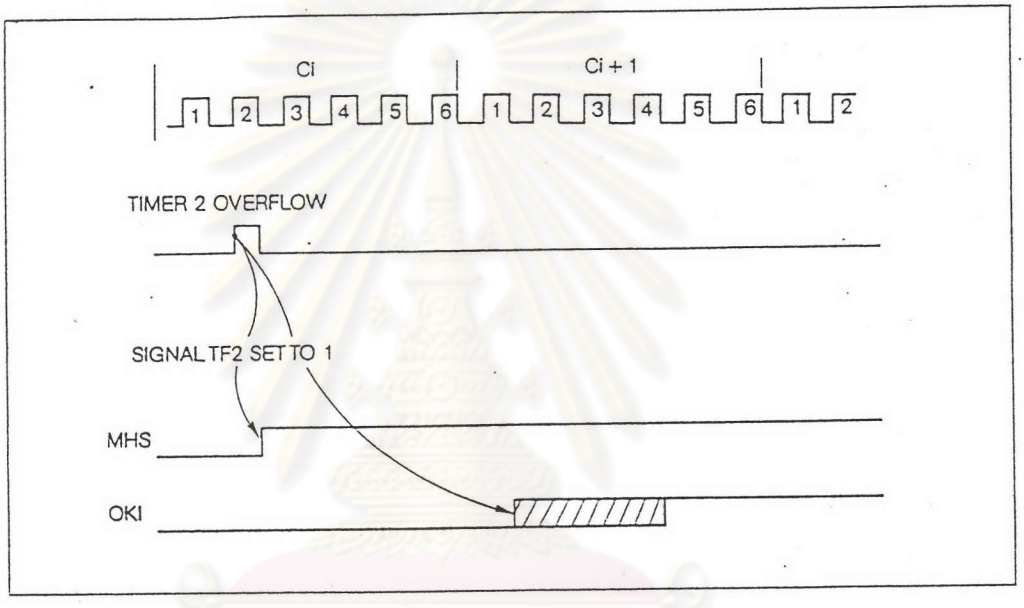
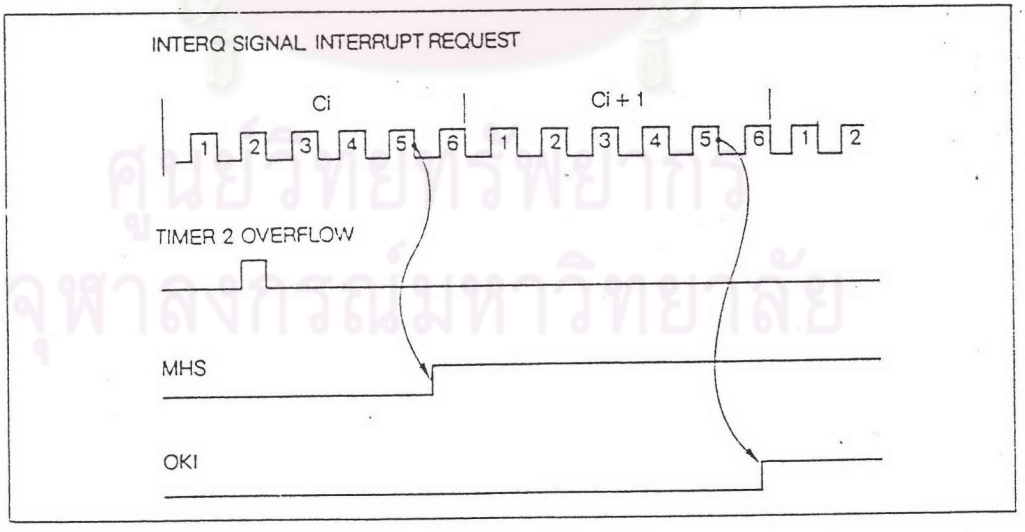
INTERRUPTS

When a TIMER (0, 1 or 2) times out, the interrupt request is generated in the same instruction cycle in the case of the MHS microcontroller and in the next cycle in the case of the OKI.





CONCLUSION

In practice, all these differences are transparent from the User's point of view. Only the differences in the division by zero and the interrupt requests from the TIMERS and the UART are likely to prevent full compatibility between the two circuits.

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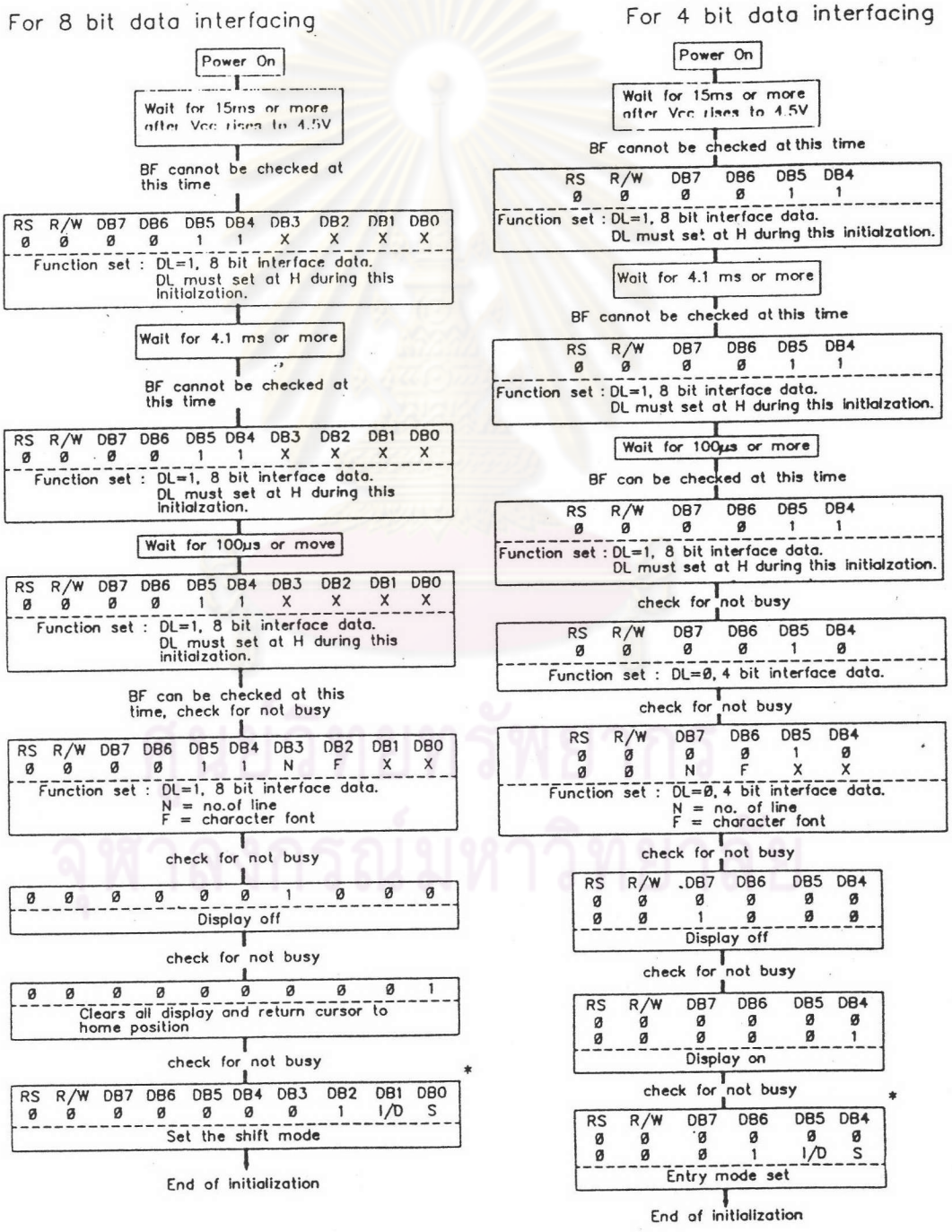
ภาคผนวก จ

ลักษณะพิกัดและคำสั่งของ LCD



■ Instructions

Instruction	Code										Description	Execution Time (max) (when fcp or fosc is 250 kHz)
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Clear Display	0	0	0	0	0	0	0	0	0	1	Clears entire display and sets DD RAM address 0 in address counter.	1.64 ms
Return Home	0	0	0	0	0	0	0	0	1	*	Sets DD RAM address 0 in address counter. Also returns display being shifted to original position. DD RAM contents remain unchanged.	1.64 ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and specifies shift of display. These operations are performed during data write and read.	40μs
Display On/Off Control	0	0	0	0	0	0	1	D	C	B	Sets ON/OFF of entire display (D), cursor ON/OFF (C), and blink of cursor position character (B).	40μs
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	*	*	Moves cursor and shifts display without changing DD RAM contents.	40μs
Function Set	0	0	0	0	1	DL	N	F	*	*	Sets interface data length (DL), number of display lines (L) and character font (F).	40μs
Set CG RAM Address	0	0	0	1	ACG						Sets CG RAM address. CG RAM data is sent and received after this setting.	40μs
Set DD RAM Address	0	0	1	ADD							Sets DD RAM address. DD RAM data is sent and received after this setting.	40μs
Read Busy Flag & Address	0	1	BF	AC							Reads Busy flag (BF) indicating internal operation is being performed and reads address counter contents.	0μs
Write Data to CG or DD RAM	1	0	Write Data								Writes data into DD RAM or CG RAM.	40μs
Read Data from CG or DD RAM	1	1	Read Data								Reads data from DD RAM or CG RAM.	40μs
	I/D=1: Increment I/D=0: Decrement S =1: Accompanies display shift S/C=1: Display shift S/C=0: Cursor move R/L=1: Shift to the right R/L=0: Shift to the left DL=1: 8 bits, DL=0: 4 bits N =1: 2 lines, N=0: 1 line F =1: 5×10 dots, F=0: 5×7 dots BF=1: Internally operating BF=0: Can accept instruction										DD RAM: Display data RAM CG RAM: Character generator RAM ACG: CG RAM address ADD: DD RAM Address: Corresponds to cursor address AC: Address counter used for both DD and CG RAM address.	Execution time changes when frequency changes Example: When fcp or fosc is 270 kHz: $40\mu s \times \frac{250}{270} = 37\mu s$	

* No effect

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DMC164

• Display Format(16chacter ×4line) • Display Fonts(5×8dots) • Driving Method(1/16D)

ABSOLUTE MAXIMUM RATINGS

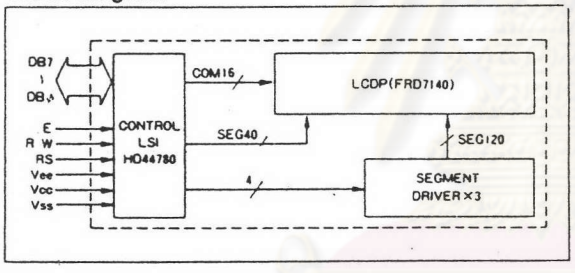
Item	Sym-bol	Test Condition	Standard Value			Unit
			min.	typ.	max.	
Power Supply Voltage for Logic	Vcc~Vss	—	0	—	6.5	V
Power Supply Voltage for LCD Drive	Vcc~Vee	—	0	—	6.0	V
Input Voltage	Vi	—	Vss		Vcc	V
Operating Temperature	Ta	—	0		+50	℃
Storage Temperature	Tstg	—	−20		+70	℃

ELECTRICAL CHARACTERISTICS

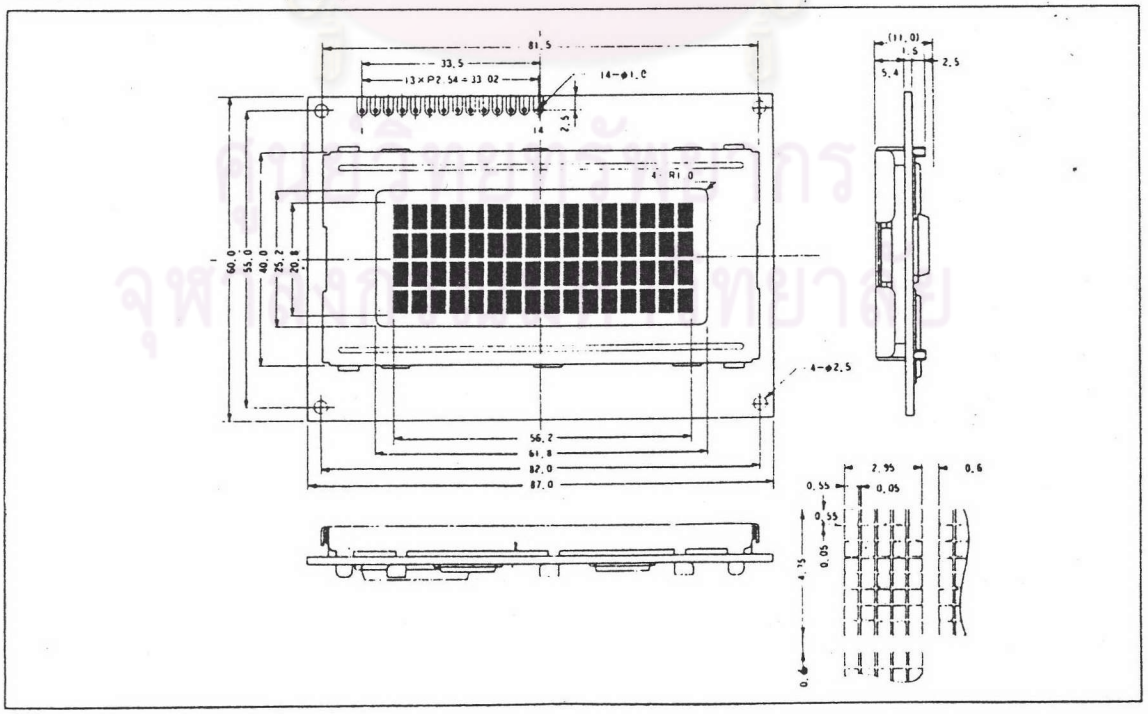
Item	Sym-bol	Test Condition	Standard Value			Unit
			min.	typ.	max.	
Input "High" Voltage	VIH	—	2.2	—	Vcc	V
Input "Low" Voltage	VIL	—	-0.3	—	0.6	V
Output "High" Voltage	VOH	−IOH=0.205mA	2.4			V
Output "Low" Voltage	VOL	IOH=1.2mA			0.4	V
Power Supply Current	Icc	Vcc=5.0V		2.4	4.0	mA

* Vcc=5.0V ± 5%, Ta=25°C

Block diagram



External dimensions / Display pattern



ภาคผนวก ฉ

โปรแกรมควบคุมการทำงานของระบบสแกนข้อมูลภาพ

```
100  STRING 100,16
110  PA=0E060H
120  XBY(PA)=01H
140  PX=80H : N=16 : $(1)="BETA BACKSCATTER" : GOSUB 3950
150  PX=0C3H : N=11 : $(1)="2-D IMAGING" : GOSUB 3950
160  PX=97H : N=2 : $(1)="by" : GOSUB 3950
170  PX=0D3H : N=9 : $(1)="K.Supasit" : GOSUB 3950
180  CALL 9000H
185  PA=0E060H
190  XBY(PA)=01H
200  PX=80H : N=9 : $(1)="Main menu" : GOSUB 3950
210  PX=0C1H : N=11 : $(1)="F1=Clr mode" : GOSUB 3950
220  PX=91H : N=12 : $(1)="F2=Scan mode" : GOSUB 3950
230  PX=0D1H : N=16 : $(1)="F3=Transfer mode" : GOSUB 3950
240  GOSUB 4100
250  IF DA=14 THEN GOTO 5000
260  IF DA=13 THEN GOTO 300
270  IF DA=11 THEN GOTO 290
290  GOTO 240
300  PA=0E060H : XBY(PA)=01H
310  PX=80H : N=9 : $(1)="Scan mode" : GOSUB 3950
320  PX=0C2H : N=12 : $(1)="F1=1st frame" : GOSUB 3950
330  PX=92H : N=12 : $(1)="F2=2nd frame" : GOSUB 3950
340  PX=0D2H : N=6 : $(1)="F3=Ext" : GOSUB 3950
350  GOSUB 4100
360  IF DA=14 THEN GOTO 495
370  IF DA=13 THEN GOTO 5100
380  IF DA=11 THEN GOTO 185
400  GOTO 350
495  PA=0E060H : XBY(PA)=01H
500  PX=80H : N=14 : $(1)="1st frame scan" : GOSUB 3950
510  PX=0C3H : N=8 : $(1)="F1=Start" : GOSUB 3950
530  PX=093H : N=6 : $(1)="F2=Ext" : GOSUB 3950
540  GOSUB 4100
550  IF DA=14 THEN CALL 9100H
560  IF DA=13 THEN GOTO 300
580  GOTO 540
3880 STOP
3890 REM
3900 REM          ********************************
3910 REM          *                              *
3920 REM          *       ini.LCD & display      *
3930 REM          *                              *
3940 REM          ********************************
3945 REM
3950 PA=0E060H : WR=0E062H
3960 XBY(PA)=38H
3970 XBY(PA)=14H : XBY(PA)=0CH
4000 XBY(PA)=PX
4010 FOR I=1 TO N
4020 XBY(WR)=ASC($(1),I)
4030 NEXT
4040 RETURN
```

```
4050  REM             ******************************
4060  REM             *                            *
4070  REM             *        keyboard detect Prog.       *
4080  REM             *                            *
4090  REM             ******************************
4100 XBY(0E0A3H)=92H
4110 DA=XBY(0E0A1H)
4120 DA=DA.AND.0FH
4130  RETURN
5000 PA=0E060H : XBY(PA)=01H
5010 PX=80H : N=10 : $(1)="Clear data" :  GOSUB 3950
5020 PX=0C2H : N=12 : $(1)="F1=1st frame" :  GOSUB 3950
5030 PX=92H : N=12 : $(1)="F2=2nd frame" :  GOSUB 3950
5040 PX=0D2H : N=6 : $(1)="F3=Ext" :  GOSUB 3950
5050  GOSUB 4100
5060  IF DA=14 THEN  CALL 9050H
5070  IF DA=13 THEN  CALL 90C0H
5080  IF DA=11 THEN  GOTO 185
5090  GOTO 5050
5100 PA=0E060H : XBY(PA)=01H
5110 PX=80H : N=14 : $(1)="2nd frame scan" :  GOSUB 3950
5120 PX=0C3H : N=8 : $(1)="F1=Start" :  GOSUB 3950
5130 PX=93H : N=6 : $(1)="F2=Ext" :  GOSUB 3950
5140  GOSUB 4100
5150  IF DA=14 THEN  GOTO 5200
5160  IF DA=13 THEN  GOTO 300
5170  GOTO 5140
5200 PA=0E060H : XBY(PA)=01H
5210 PX=83H : N=9 : $(1)="2nd frame" :  GOSUB 3950
5220 PX=0C3H : N=10 : $(1)="Scanning !" :  GOSUB 3950
5230 PX=93H : N=8 : $(1)="F2=abort" :  GOSUB 3950
5240  GOSUB 4100
5250  IF DA=13 THEN  GOTO 5100
5260  REM   ***** SCAN PROG. *****
5270  GOTO 5240
6000  END
```

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```
        ORG 9000H
        DT EQU 33H
        DELAYX EQU 0FD00H
        DELAYY EQU 0F000H
        PO EQU 0E0C0H
;start
        MOV DPTR,#0E0A3H
        MOV A,#82H
        MOV R0,#DT
        MOVX @DPTR,A
        MOV DPTR,#0E0C3H
        MOV A,#80H
        MOVX @DPTR,A
BACK:
        MOV DPTR,#0E0A1H
        MOVX A,@DPTR
        MOV R1,A
        ANL A,#10H
        CJNE A,#10H,XSTEP
        MOV A,R1
        ANL A,#20H
        CJNE A,#20H,YSTEP
        RET
XSTEP:
        MOV DPTR,#PO
        MOV A,R0
        ANL A,#0FH
        MOVX @DPTR,A
        MOV A,R0
        RR A
        MOV R0,A
        MOV DPTR,#DELAYX
DL1:
        INC DPTR
        MOV R2,DPH
        MOV A,DPL
        ORL A,R2
        JNZ DL1
        SJMP BACK
YSTEP:
        MOV DPTR,#PO
        MOV A,R0
        ANL A,#0F0H
        MOVX @DPTR,A
        MOV A,R0
        RL A
        MOV R0,A
        MOV DPTR,#DELAYY
DL2:
        INC DPTR
        MOV R2,DPH
        MOV A,DPL
        ORL A,R2
        JNZ DL2
        SJMP BACK
; CLR SCREEN 1
        ORG 9000H
        DATA EQU 00H
;
        MOV DPTR,#0000H
        MOV R2,#00H
        SJMP OUTP
NXT:
        INC DPTR
OUTP:
        MOV R0,DPL
        MOV R1,DPH
        MOV DPTR,#0E040H
        MOV A,R0
        MOVX @DPTR,A
        MOV R0,A
        MOV DPTR,#0E041H
        MOV A,R1
        MOVX @DPTR,A
        MOV DPTR,#0E042H
        MOV A,R2
        MOVX @DPTR,A
        MOV DPTR,#0E020H
        MOV A,#DATA
        MOVX @DPTR,A
        MOV DPH,R1
        MOV DPL,R0
        MOV A,#01H
        ANL A,DPH
        CJNE A,#01H,SUB1
        SETB C
BACK1:
        MOV A,DPL
        RRC A
        XRL A,#0E6H
        CJNE A,#00H,NXT
        MOV DPL,#00H
        PUSH DPL
        MOV DPL,DPH
        MOV DPH,R2
        MOV A,DPL
        XRL A,#95H
        MOV R0,A
        MOV A,DPH
        XRL A,#02H
        ORL A,R0
        CJNE A,#00H,SUB2
        RET
SUB1:
        CLR C
        SJMP BACK1
SUB2:
        INC DPTR
        MOV R2,DPH
        MOV DPH,DPL
        POP DPL
        SJMP OUTP
;CLR SCREEN 2
        ORG 90C0H
        DATA EQU 00H
;
        MOV DPTR,#0E043H
        MOV A,#80H
        MOVX @DPTR,A
        MOV DPTR,#0E042H
```

```
        MOV A,#04H
        MOVX @DPTR,A
        MOV DPTR,#0000H
        MOV R2,#04H
        SJMP OUTP
NXT1:
        INC DPTR
OUTP1:
        MOV R0,DPL
        MOV R1,DPH
        MOV DPTR,#0E040H
        MOV A,R0
        MOVX @DPTR,A
        MOV R0,A
        MOV DPTR,#0E041H
        MOV A,R1
        MOVX @DPTR,A
        MOV DPTR,#0E042H
        MOV A,R2
        MOVX @DPTR,A
        MOV DPTR,#0E020H
        MOV A,#DATA
        MOVX @DPTR,A
        MOV DPH,R1
        MOV DPL,R0
        MOV A,#01H
        ANL A,DPH
        CJNE A,#01H,SUB3
        SETB C
BACK2:
        MOV A,DPL
        RRC A
        XRL A,#0E6H
        CJNE A,#00H,NXT
        MOV DPL,#00H
        PUSH DPL
        MOV DPL,DPH
        MOV DPH,R2
        MOV A,DPL
        XRL A,#95H
        MOV R0,A
        MOV A,DPH
        XRL A,#06H
        ORL A,R0
        CJNE A,#00H,SUB4
        RET

SUB3:
        CLR C
        SJMP BACK1
SUB2:
        INC DPTR
        MOV R2,DPH
        MOV DPH,DPL
        POP DPL
        SJMP OUTP
; 1st Prog
        ORG 9100H
        DO EQU 33H
        DELAYX EQU 0C000H
        DELAYY EQU 0F000H
        RESETX EQU 0FF00H
        PO EQU 0E0C0H
;ini
        MOV DPTR,#0E0A3H
        MOV A,#92H
        MOVX @DPTR,A
        MOV DPTR,#0E0C3H
        MOV A,#80H
        MOVX @DPTR,A
        MOVX @DPTR,A
        MOV DPTR,#0E043H
        MOV A,#80H
        MOVX @DPTR,A
        MOV DPTR,#0E042H
        MOV A,#00H
        MOVX @DPTR,A
        MOV DPTR,#0000H
        MOV R2,#00H
        MOV R3,#DO
        MOV R4,#DO
        SJMP OUTP
NXT2:
        INC DPTR
        LCALL XSTEP
OUTP3:
        MOV R0,DPL
        MOV R1,DPH
        MOV DPTR,#0E043H
        MOV A,#80H
        MOVX @DPTR,A
        MOV DPTR,#0E040H
        MOV A,R0
        MOVX @DPTR,A
        MOV R0,A
        MOV DPTR,#0E041H
        MOV A,R1
        MOVX @DPTR,A
        MOV DPTR,#0E042H
        MOV A,R2
        MOVX @DPTR,A
        MOV DPTR,#0E0A0H
        MOVX A,@DPTR
        MOV DPTR,#0E020H
        MOVX @DPTR,A
        MOV DPH,R1
        MOV DPL,R0
        MOV A,#01H
        ANL A,DPH
        CJNE A,#01H,SUB5
        SETB C
BACK3:
        MOV A,DPL
        RRC A
        XRL A,#0C8H
        CJNE A,#00H,NXT
        LCALL XRESET
        MOV DPL,DPH
        MOV DPH,R2
        MOV A,DPL
        XRL A,#59H
        MOV R0,A
```

```
        MOV A,DPH
        XRL A,#02H
        ORL A,R0
        CJNE A,#00H,SUB6
        RET
SUB5:
        CLR C
        LJMP BACK1
SUB6:
        INC DPTR
        MOV R2,DPH
        MOV DPH,DPL
        MOV DPL,#00H
        LJMP OUTP3
ROTX:
        MOV DPTR,#PO
        MOV A,R3
        ANL A,#0FH
        MOV R6,A
        MOV A,R4
        ANL A,#0F0H
        ORL A,R6
        MOVX @DPTR,A
        MOV A,R3
        RR A
        MOV R3,A
        MOV DPTR,#RESETX
DL3:
        INC DPTR
        MOV R7,DPH
        MOV A,DPL
        ORL A,R7
        JNZ DL3
        LJMP GOXRS

LOOPX:
        DEC R5
        SJMP GOX
XSTEP:
        PUSH DPL
        PUSH DPH
        PUSH ACC
        MOV R5,#03H
GOX:
        MOV DPTR,#PO
        MOV A,R3
        ANL A,#0FH
        MOVX @DPTR,A
        MOV A,R3
        RL A
        MOV R3,A
        MOV DPTR,#DELAYX
DL4:
        INC DPTR
        MOV R7,DPH
        MOV A,DPL
        ORL A,R7
        JNZ DL1
        CJNE R5,#00H,LOOPX
        POP ACC
        POP DPH
        POP DPL
        RET

XRESET:
        PUSH DPL
        PUSH DPH
        PUSH ACC
GOXRS:
        MOV DPTR,#0E0A1H
        MOVX A,@DPTR
        ANL A,#10H
        CJNE A,#10H,ROTX
        MOV R5,#2AH
        SJMP YSTEP
LOOPY:
        DEC R5
YSTEP:
        MOV DPTR,#PO
        MOV A,R4
        ANL A,#0F0H
        MOV R7,A
        MOV A,R3
        ANL A,#0FH
        ORL A,R7
        MOVX @DPTR,A
        MOV A,R4
        RR A
        MOV R4,A
        MOV DPTR,#DELAYY
DL5:
        INC DPTR
        MOV R7,DPH
        MOV A,DPL
        ORL A,R7
        JNZ DL2
        CJNE R5,#00H,LOOPY
        MOV DPTR,#PO
        MOVX @DPTR,A
        POP ACC
        POP DPH
        POP DPL
        RET
; 2nd Prog
        ORG 9100H
        DO EQU 33H
        DELAYX EQU 0C000H
        DELAYY EQU 0F000H
        RESETX EQU 0FF00H
        PO EQU 0E0C0H
;ini
        MOV DPTR,#0E0A3H
        MOV A,#92H
        MOVX @DPTR,A
        MOV DPTR,#0E0C3H
        MOV A,#80H
        MOVX @DPTR,A
        MOVX @DPTR,A
        MOV DPTR,#0E043H
        MOV A,#80H
        MOVX @DPTR,A
        MOV DPTR,#0E042H
```

```
        MOV A,#00H
        MOVX @DPTR,A
        MOV DPTR,#0000H
        MOV R2,#04H
        MOV R3,#DO
        MOV R4,#DO
        SJMP OUTP
NXT3:
        INC DPTR
        LCALL XSTEP
OUTP:
        MOV R0,DPL
        MOV R1,DPH
        MOV DPTR,#0E043H
        MOV A,#80H
        MOVX @DPTR,A
        MOV DPTR,#0E040H
        MOV A,R0
        MOVX @DPTR,A
        MOV R0,A
        MOV DPTR,#0E041H
        MOV A,R1
        MOVX @DPTR,A
        MOV DPTR,#0E042H
        MOV A,R2
        MOVX @DPTR,A
        MOV DPTR,#0E0A0H
        MOVX A,@DPTR
        MOV DPTR,#0E020H
        MOVX @DPTR,A
        MOV DPH,R1
        MOV DPL,R0
        MOV A,#01H
        ANL A,DPH
        CJNE A,#01H,SUB7
        SETB C
BACK4:
        MOV A,DPL
        RRC A
        XRL A,#0C8H
        CJNE A,#00H,NXT
        LCALL XRESET
        MOV DPL,DPH
        MOV DPH,R2
        MOV A,DPL
        XRL A,#59H
        MOV R0,A
        MOV A,DPH
        XRL A,#02H
        ORL A,R0
        CJNE A,#00H,SUB8
        RET
SUB7:
        CLR C
        LJMP BACK1
SUB8:
        INC DPTR
        MOV R2,DPH
        MOV DPH,DPL
        MOV DPL,#00H
        LJMP OUTP

ROTX1:
        MOV DPTR,#PO
        MOV A,R3
        ANL A,#0FH
        MOV R6,A
        MOV A,R4
        ANL A,#0F0H
        ORL A,R6
        MOVX @DPTR,A
        MOV A,R3
        RR A
        MOV R3,A
        MOV DPTR,#RESETX1
DL6:
        INC DPTR
        MOV R7,DPH
        MOV A,DPL
        ORL A,R7
        JNZ DL3
        LJMP GOXRS1

LOOPX1:
        DEC R5
        SJMP GOX1
XSTEP1:
        PUSH DPL
        PUSH DPH
        PUSH ACC
        MOV R5,#03H
GOX1:
        MOV DPTR,#PO
        MOV A,R3
        ANL A,#0FH
        MOVX @DPTR,A
        MOV A,R3
        RL A
        MOV R3,A
        MOV DPTR,#DELAYX1
DL7:
        INC DPTR
        MOV R7,DPH
        MOV A,DPL
        ORL A,R7
        JNZ DL1
        CJNE R5,#00H,LOOPX1
        POP ACC
        POP DPH
        POP DPL
        RET

XRESET1:
        PUSH DPL
        PUSH DPH
        PUSH ACC
GOXRS1:
        MOV DPTR,#0E0A1H
        MOVX A,@DPTR
        ANL A,#10H
        CJNE A,#10H,ROTX1
        MOV R5,#2AH
        SJMP YSTEP1
```

```
LOOPY1:
        DEC R5
YSTEP1:
        MOV DPTR,#PO
        MOV A,R4
        ANL A,#0F0H
        MOV R7,A
        MOV A,R3
        ANL A,#0FH
        ORL A,R7
        MOVX @DPTR,A
        MOV A,R4
        RR A
        MOV R4,A
        MOV DPTR,#DELAYY1
DL8:
        INC DPTR
        MOV R7,DPH
        MOV A,DPL
        ORL A,R7
        JNZ DL2
        CJNE R5,#00H,LOOPY1
        MOV DPTR,#PO
        MOVX @DPTR,A
        POP ACC
        POP DPH
        POP DPL
        RET
        END
```

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ประวัติผู้เขียน

นายลุ..สิทธิ์ คะวีรัตน์ เกิดเมื่อวันที่ 19 กุมภาพันธ์ 2512 ที่อำเภอเมือง จังหวัดอุตรดิตถ์ สำเร็จการศึกษาปริญญาบัณฑิตจาก ภาควิชาเทคนิคอุตสาหกรรม สาขาอิเล็กทรอนิกส์ คณะวิศวกรรมศาสตร์ สถาบันเทคโนโลยีพระจอมเกล้าเจ้าคุณทหารลาดกระบัง เมื่อปี พ.ศ. 2535 แล้วเข้าศึกษาต่อในระดับปริญญามหาบัณฑิต สาขาวิชานิวเคลียร์เทคโนโลยี คณะวิศวกรรมศาสตร์ จุฬาลงกรณ์มหาวิทยาลัย ในปี พ.ศ.2536 และระหว่างการศึกษาได้เข้าทำงานที่บริษัท ฟายน์สเปค จำกัด ในตำแหน่งวิศวกร

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