เอกสารอ้างอิง

1. Intel; 8080 Microcomputer system User's Manual. Avenue, Santa Clare, Califonia : Intel Corporation, 1975

2. Douglas V. Hall; Microprocessors and Digital System. New York : Mc Graw-Hill, 1980

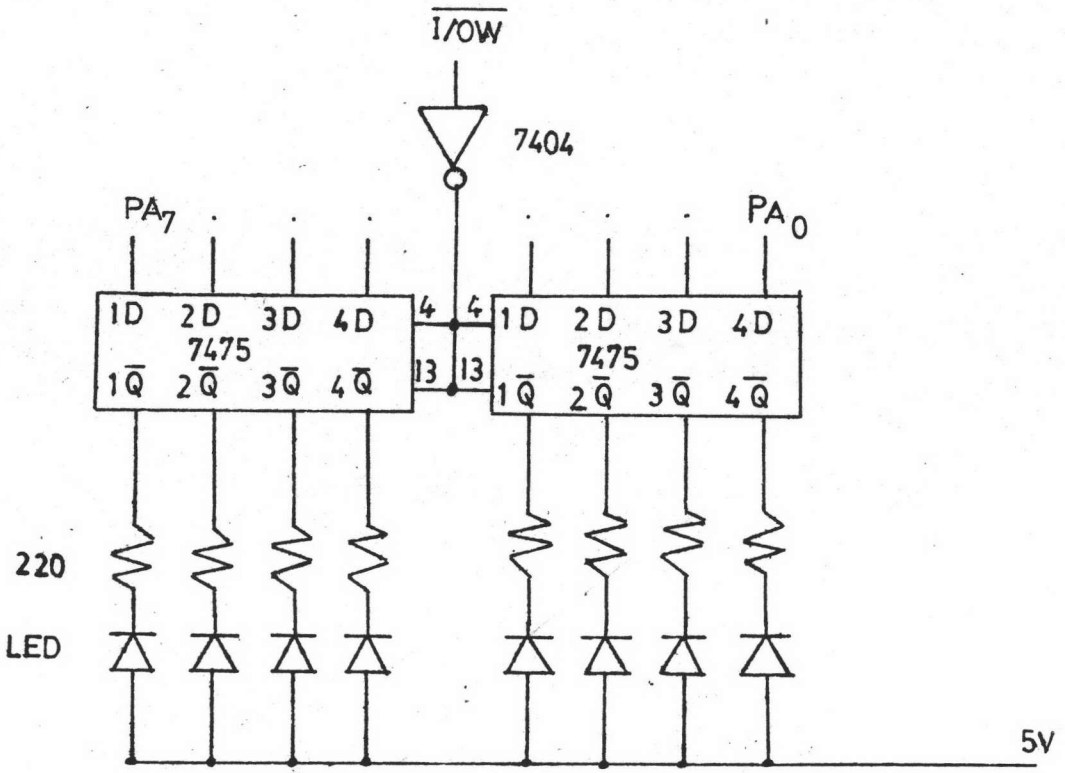
3. A. Lesea, R. Zako; Microprocessor Interface techniques. Sysbex Inc., 1978

4. Intel Corp; Memory design Handbook Intel 1977 .

5. Geny kane; CRT controller Handbook. Mc Graw-Hill, 1978

ภาคผนวก ก

วงจรแสดงผล LED ชนิด 8 บิท


I/OW
7404
PA7
PA0
1D 2D 3D 4D
7475
1Q 2Q 3Q 4Q
4
13
220
LED
5V

ภาคผนวก ข
โปรแกรมโมนิเตอร์ของเทอร์มินอล

```
                        ;
                        ;       MONITOR  CRT  PROGRAM
                        ;         5  SEPTEMBER  1980
                        ;
0000                            ORG     0
0000 3E8A                       MVI     A,8AH
0002 D360                       OUT     ME3
0004 210004                     LXI     H,0400H
0007 31FF0B                     LXI     SP,STACK
000A C33300                     JMP     INA75
0030                            ORG     30H
0030 C3FA01                     JMP     INTSUM
                        ;
                        ;       INITIAL ROUTINE  "8275 CRT"
                        ;
0033 3E00               INA75   MVI     A,00H
0035 D391                       OUT     SUC
0037 3EBF                       MVI     A,0BFH
0039 D390                       OUT     SUP
003B 3E8F                       MVI     A,8FH
003D D390                       OUT     SUP
003F 3E77                       MVI     A,77H
0041 D390                       OUT     SUP
0043 3E09                       MVI     A,09H
0045 D390                       OUT     SUP
0047 3EA0                       MVI     A,0A0H
0049 D391                       OUT     SUC
004B 3E2F                       MVI     A,2FH
004D D391                       OUT     SUC
                        ;
                        ;       POWER  UP
                        ;       CLEAR MEMORY & HOME CURSOR
                        ;
004F 3E20               LOPP    MVI     A,20H
0051 77                         MOV     M,A
0052 7C                         MOV     A,H
0053 FE0B                       CPI     0BH
0055 CA5C00                     JZ      CMMHP
0058 23                 CMMLP   INX     H
0059 C34F00                     JMP     LOPP
005C 7D                 CMMHP   MOV     A,L
005D FEFF                       CPI     0FFH
005F CA6500                     JZ      CHOM1
0062 C35800                     JMP     CMMLP
0065 210004             CHOM1   LXI     H,0400H
0068 010000                     LXI     B,0000H
```

```
                        ;
                        ;       INITIALIZE INTERFACE
                        ;
006B D3F4       PINIT   OUT     PREST
006D D3F5               OUT     PBOUD
006F DBF4               IN      PREG2
0071 E608               ANI     08H
0073 CA7B00             JZ      HALFD
0076 3E04               MVI     A,04H
0078 C37D00             JMP     SFLAG
007B 3E06       HALFD   MVI     A,06H
007D D3F6       SFLAG   OUT     PREG3
007F FB                 EI
                        ;
                        ;       MONITOR  START
                        ;
0080 CD7602     INPUT   CALL    PIST
0083 CDED00             CALL    INKEY
0086 FE0F       PCHK    CPI     0FH
0088 CA8000             JZ      INPUT
008B FE03               CPI     03H     ; CURSOR RIGHT
008D CAC300             JZ      CRT
0090 FE17               CPI     17H     ; CURSOR  LEFT
0092 CAC900             JZ      CLEF
0095 FE04               CPI     04H     ; CLEAR MOMERY
0097 CACF00             JZ      CLR
009A FE18               CPI     18H     ; HOME
009C CAD500             JZ      CHOM
009F FE02               CPI     02H     ; CURSOR DOWN
00A1 CADB00             JZ      CROLD
00A4 FE01               CPI     01H     ; CURSOR UP
00A6 CAE100             JZ      CUP
00A9 FE08               CPI     08H     ; ENTER
00AB CAE700             JZ      ENT
00AE CD1E02             CALL    PSEND
00B1 DBF4               IN      PREG2
00B3 E608               ANI     08H     ;FULL  DUPLEX
00B5 C28000             JNZ     INPUT
00B8 77                 MOV     M,A     ; DATA KB TO MM
00B9 D300               OUT     MEO
00BB CD4901             CALL    CRITE
00BE D3F4               OUT     PREST
00C0 C38000             JMP     INPUT
                        ;
                        ;       CALL SUBROUTINE
                        ;
00C3 CD4901     CRT     CALL    CRITE
00C6 C38000             JMP     INPUT
```

```
                                ;
00C9 CD2001     CLEF    CALL    CLEFT
00CC C38000             JMP     INPUT
                                ;
00CF CDAA01     CLR     CALL    CLEAR
00D2 C38000             JMP     INPUT
                                ;
00D5 CDFC00     CHOM    CALL    HOME
00D8 C38000             JMP     INPUT
                                ;
00DB CD7501     CROLD   CALL    RDOWN
00DE C38000             JMP     INPUT
                                ;
00E1 CD0301     CUP     CALL    CURUP
00E4 C38000             JMP     INPUT
                                ;
00E7 CDCA01     ENT     CALL    ENTER
00EA C38000             JMP     INPUT
                                ;
                                ;
                                ;       INKEY
                                ;
00ED DB20       INKEY   IN      ME1
00EF B7                 ORA     A
00F0 F2ED00     LOPKB   JP      INKEY
00F3 DB20               IN      ME1
00F5 B7                 ORA     A
00F6 FAF000             JM      LOPKB
00F9 DB20               IN      ME1
00FB C9                 RET
                                ;
                                ;       HOME
                                ;
00FC 010000     HOME    LXI     B,0000H
00FF 210004             LXI     H,0400H
0102 C9                 RET
                                ;
                                ;       CURSOR  UP
                                ;
0103 114000     CURUP   LXI     D,0040H
0106 3E00               MVI     A,B
0108 FE00               CPI     00H
010A CA1701             JZ      UPCR
010D 05                 DCR     B
010E 7D                 MOV     A,L
010F 9B                 SBB     E
0110 6F                 MOV     L,A
0111 7C                 MOV     A,H
```

```
0112 9A                 SBB     D
0113 67                 MOV     H,A
0114 C31F01             JMP     UPRET
0117 21C007     UPCR    LXI     H,07C0H
011A 79                 MOV     A,C
011B 85                 ADD     L
011C 6F                 MOV     L,A
011D 060F               MVI     B,0FH
011F C9         UPRET   RET
                ;
                ;       CURSOR  LEFT
                ;
0120 78         CLEFT   MOV     A,B
0121 FE00               CPI     00H
0123 CA3101             JZ      CTEST
0126 79                 MOV     A,C
0127 FE00               CPI     00H
0129 CA4401             JZ      CBCR
012C 0D         CDCR    DCR     C
012D 2B                 DCX     H
012E C34801             JMP     CLRET
0131 79         CTEST   MOV     A,C
0132 FE00               CPI     00H
0134 CA3A01             JZ      CBEGIN
0137 C32C01             JMP     CDCR
013A 060F       CBEGIN  MVI     B,0FH
013C 0E3F               MVI     C,3FH
013E 21FF07             LXI     H,07FFH
0141 C34801             JMP     CLRET
0144 05         CBCR    DCR     B
0145 0E3F               MVI     C,3FH
0147 2B                 DCX     H
0148 C9         CLRET   RET
                ;
                ;       MOVE  CURSOR  RIGHT
                ;
0149 78         CRITE   MOV     A,B
014A FE0F               CPI     0FH
014C CA5A01             JZ      CREND
014F 79                 MOV     A,C
0150 FE3F               CPI     3FH
0152 CA6301             JZ      CRINR
0155 0C         CRNEXT  INR     C
0156 23                 INX     H
0157 C37401             JMP     CRRET
015A 79         CREND   MOV     A,C
015B FE3F               CPI     3FH
015D CA6A01             JZ      CRLRP
```

```
0160 C35501              JMP     CRNEXT
0163 23          CRINR   INX     H
0164 04                  INR     B
0165 0E00                MVI     C,00H
0167 C37401              JMP     CRRET
016A CD9401      CRLRP   CALL    ROLLUP
016D 060F                MVI     B,0FH
016F 0E00                MVI     C,00H
0171 21C007              LXI     H,07C0H
0174 C9          CRRET   RET

                 ;
                 ;       CURSOR  DOWN
                 ;
0175 114000      RDOWN   LXI     D,0040H
0178 78                  MOV     A,B
0179 FE0F                CPI     0FH
017B CA8601              JZ      ROBIN
017E 04                  INR     B
017F 7D                  MOV     A,L
0180 83                  ADD     E
0181 6F                  MOV     L,A
0182 7C                  MOV     A,H
0183 8A                  ADC     D
0184 67                  MOV     H,A
0185 C9          DORET   RET
0186 CD9401      ROBIN   CALL    ROLLUP
0189 21C007              LXI     H,07C0H
018C 79                  MOV     A,C
018D 85                  ADD     L
018E 6F                  MOV     L,A
018F 060F                MVI     B,0FH
0191 C38501              JMP     DORET
                 ;
                 ;       SCROLL  MODE
                 ;
0194 214004      ROLLUP  LXI     H,0440H
0197 110004              LXI     D,0400H

019A 7C          LOPUP   MOV     A,H
019B FE0B                CPI     0BH
019D CAA901              JZ      LOPRET
01A0 7E                  MOV     A,M
01A1 EB                  XCHG
01A2 77                  MOV     M,A
01A3 23                  INX     H
01A4 13                  INX     D
```

```
01A5 EB                 XCHG
01A6 C39A01             JMP     LOPUP
01A9 C9         LOPRET  RET
                ;
                ;       CLEAR   MEMORY
                ;
01AA 210004     CLEAR   LXI     H,0400H
01AD 3E20       LOP     MVI     A,20H
01AF 77                 MOV     M,A
01B0 7C                 MOV     A,H
01B1 FE0B               CPI     0BH

01B3 CABA01     CMML    JZ      CMMH
01B6 23                 INX     H
01B7 C3AD01             JMP     LOP
01BA 7D         CMMH    MOV     A,L
01BB FEFF               CPI     0FFH
01BD CAC301             JZ      BEGIN
01C0 C3B301             JMP     CMML
01C3 210004     BEGIN   LXI     H,0400H
01C6 010000             LXI     B,0000H
01C9 C9                 RET
                ;
                ;       ENTER
                ;
01CA 7D         ENTER   MOV     A,L
01CB 91                 SUB     C
01CC 6F                 MOV     L,A
01CD 0E00               MVI     C,00H
01CF C9                 RET
01D0 FE0D       PCHA    CPI     0DH
01D2 C2DB01             JNZ     PLF
01D5 CDFC00             CALL    HOME
01D8 C3F901             JMP     PRRT
01DB FE0A       PLF     CPI     0AH
01DD C2EA01             JNZ     PBS
01E0 CDFC00             CALL    HOME
01E3 00                 NOP
01E4 CD7501             CALL    RDOWN
01E7 C3F901             JMP     PRRT
01EA FE08       PBS     CPI     08H
01EC C2F501             JNZ     PSAVE
01EF CD2001             CALL    CLEFT
01F2 C3F901             JMP     PRRT
01F5 77         PSAVE   MOV     M,A
01F6 CD4601             CALL    CRITE
01F9 C9         PRRT    RET
```

```
                        ;
                        ;       INTERRUPT ROUTINE "INITIAL 8257 DMA"
                        ;
01FA F5         INTSUM  PUSH    PSW
01FB DB91               IN      SUC
01FD 3E00               MVI     A,00H
01FF D380               OUT     SUA
0201 3E04               MVI     A,04H
0203 D380               OUT     SUA
0205 3E00               MVI     A,00H
0207 D381               OUT     SUT
0209 3E84               MVI     A,84H
020B D381               OUT     SUT
020D 3E41               MVI     A,41H
020F D388               OUT     SUS
0211 3E80               MVI     A,80H
0213 D391               OUT     SUC
0215 79                 MOV     A,C
0216 D390               OUT     SUP
0218 78                 MOV     A,B
0219 D390               OUT     SUP
021B F1                 POP     PSW
021C FB                 EI
021D C9                 RET

                        ;
                        ;       SEND CHARACTER
                        ;
021E F5         PSEND   PUSH    PSW
021F DBF4               IN      PREG2
0221 E608               ANI     08H
0223 C23702             JNZ     PPOUT
0226 3E04               MVI     A,04H
0228 D3F6               OUT     PREG3
022A DBF4               IN      PREG2
022C E640               ANI     40H
022E CA3702             JZ      PPOUT
0231 DBF4       PCTS    IN      PREG2
0233 17                 RAL
0234 D23102             JNC     PCTS
0237 DBF6       PPOUT   IN      PREG1
0239 E604               ANI     04H
023B CA3702             JZ      PPOUT
023E F1                 POP     PSW
023F D3F7               OUT     POUTP
0241 F5                 PUSH    PSW
0242 DBF4               IN      PREG2
0244 E608               ANI     08H
```

```
0246 C25002                JNZ     RETN
0249 F1                    POP     PSW
024A FE0D                  CPI     0DH
024C CA5202                JZ      HREST
024F C9                    RET
0250 F1          RETN      POP     PSW
0251 C9                    RET
0252 DBF5        HREST     IN      PEOC
0254 17                    RAL
0255 D25202                JNC     HREST
0258 D5                    PUSH    D
0259 1E50                  MVI     E,50H
025B 1D          PLOOP     DCR     E
025C 00                    NOP
025D 00                    NOP
025E 00                    NOP
025F 00                    NOP
0260 00                    NOP
0261 00                    NOP
0262 00                    NOP
0263 00                    NOP
0264 00                    NOP
0265 00                    NOP
0266 00                    NOP
0267 00                    NOP
0268 00                    NOP
0269 00                    NOP
026A 00                    NOP
026B 00                    NOP
026C 00                    NOP
026D C25B02                JNZ     PLOOP
0270 D1                    POP     D
0271 3E06                  MVI     A,06H
0273 D3F6                  OUT     PREG3
0275 C9                    RET
                 ;
                 ;         RECEIVE  CHARACTER
                 ;
0276 DBF6        PIST      IN      PREG1
0278 1F                    RAR
0279 D0                    RNC
027A DBF7        PIIN      IN      PINP
027C E67F                  ANI     7FH
027E CDD001                CALL    PCHA
0281 C37602                JMP     PIST
0BFF =           STACK     EQU     0BFFH
0000 =           ME0       EQU     00H
0020 =           ME1       EQU     20H
```

```
0060 =          ME3     EQU     60H
0091 =          SUC     EQU     91H
0090 =          SUP     EQU     90H
0080 =          SUA     EQU     80H
0081 =          SUT     EQU     81H
0088 =          SUS     EQU     88H
00F6 =          PREG1   EQU     0F6H
00F4 =          PREG2   EQU     0F4H
00F6 =          PREG3   EQU     0F6H
00F4 =          PREST   EQU     0F4H
00F5 =          PBOUD   EQU     0F5H
00F5 =          PEOC    EQU     0F5H
00F7 =          PINP    EQU     0F7H
00F7 =          POUTP   EQU     0F7H
0284                    END
```

ภาคผนวก ค
ไอซีเบอร์ที่ใช้วิจัย

intel® Silicon Gate MOS 8080A

SINGLE CHIP 8-BIT N-CHANNEL MICROPROCESSOR

The 8080A is functionally and electrically compatible with the Intel® 8080.

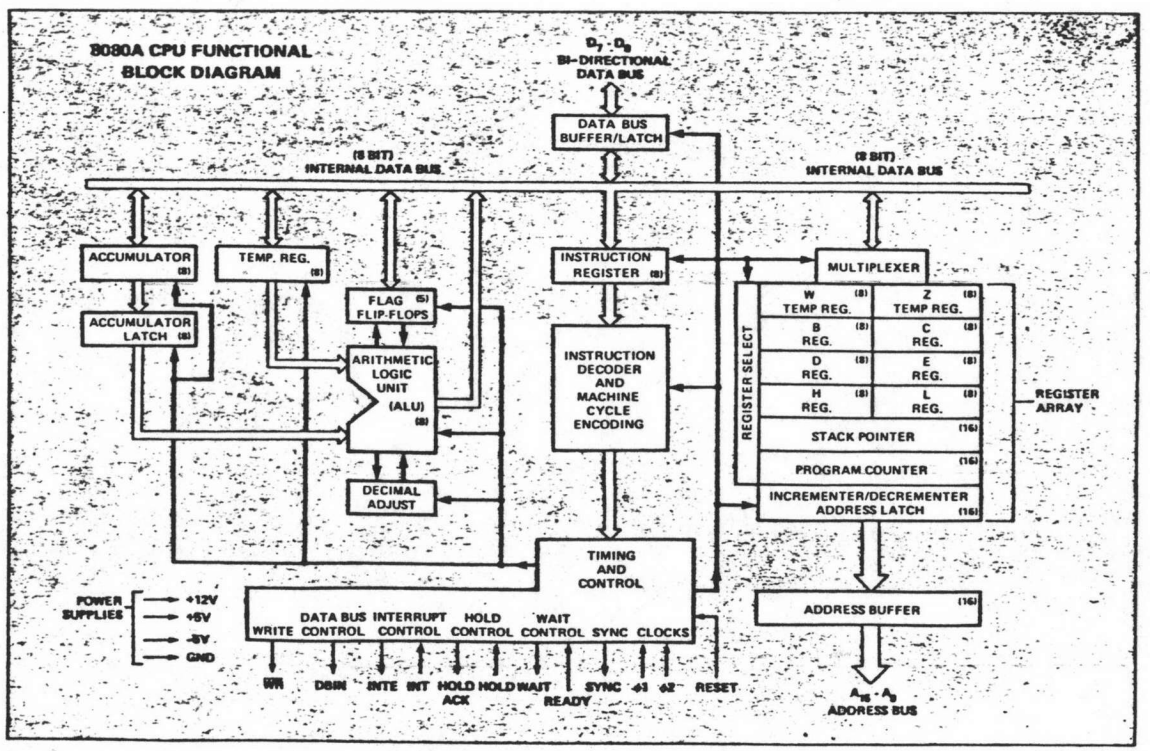
- **TTL Drive Capability**
- **2 μs Instruction Cycle**
- **Powerful Problem Solving Instruction Set**
- **Six General Purpose Registers and an Accumulator**
- **Sixteen Bit Program Counter for Directly Addressing up to 64K Bytes of Memory**
- **Sixteen Bit Stack Pointer and Stack Manipulation Instructions for Rapid Switching of the Program Environment**
- **Decimal, Binary and Double Precision Arithmetic**
- **Ability to Provide Priority Vectored Interrupts**
- **512 Directly Addressed I/O Ports**

The Intel® 8080A is a complete 8-bit parallel central processing unit (CPU). It is fabricated on a single LSI chip using Intel's n-channel silicon gate MOS process. This offers the user a high performance solution to control and processing applications.

The 8080A contains six 8-bit general purpose working registers and an accumulator. The six general purpose registers may be addressed individually or in pairs providing both single and double precision operators. Arithmetic and logical instructions set or reset four testable flags. A fifth flag provides decimal arithmetic operation.

The 8080A has an external stack feature wherein any portion of memory may be used as a last in/first out stack to store/retrieve the contents of the accumulator, flags, program counter and all of the six general purpose registers. The sixteen bit stack pointer controls the addressing of this external stack. This stack gives the 8080A the ability to easily handle multiple level priority interrupts by rapidly storing and restoring processor status. It also provides almost unlimited subroutine nesting.

This microprocessor has been designed to simplify systems design. Separate 16-line address and 8-line bi-directional data busses are used to facilitate easy interface to memory and I/O. Signals to control the interface to memory and I/O are provided directly by the 8080A. Ultimate control of the address and data busses resides with the HOLD signal. It provides the ability to suspend processor operation and force the address and data busses into a high impedance state. This permits OR-tying these busses with other controlling devices for (DMA) direct memory access or multi-processor operation.



8080A FUNCTIONAL PIN DEFINITION

The following describes the function of all of the 8080A I/O pins. Several of the descriptions refer to internal timing periods.

A_{15}-A_0 (output three-state)
ADDRESS BUS; the address bus provides the address to memory (up to 64K 8-bit words) or denotes the I/O device number for up to 256 input and 256 output devices. A_0 is the least significant address bit.

D_7-D_0 (input/output three-state)
DATA BUS; the data bus provides bi-directional communication between the CPU, memory, and I/O devices for instructions and data transfers. Also, during the first clock cycle of each machine cycle, the 8080A outputs a status word on the data bus that describes the current machine cycle. D_0 is the least significant bit.

SYNC (output)
SYNCHRONIZING SIGNAL; the SYNC pin provides a signal to indicate the beginning of each machine cycle.

DBIN (output)
DATA BUS IN; the DBIN signal indicates to external circuits that the data bus is in the input mode. This signal should be used to enable the gating of data onto the 8080A data bus from memory or I/O.

READY (input)
READY; the READY signal indicates to the 8080A that valid memory or input data is available on the 8080A data bus. This signal is used to synchronize the CPU with slower memory or I/O devices. If after sending an address out the 8080A does not receive a READY input, the 8080A will enter a WAIT state for as long as the READY line is low. READY can also be used to single step the CPU.

WAIT (output)
WAIT; the WAIT signal acknowledges that the CPU is in a WAIT state.

$\overline{WR}$ (output)
WRITE; the $\overline{WR}$ signal is used for memory WRITE or I/O output control. The data on the data bus is stable while the $\overline{WR}$ signal is active low ($\overline{WR}$ = 0).

HOLD (input)
HOLD; the HOLD signal requests the CPU to enter the HOLD state. The HOLD state allows an external device to gain control of the 8080A address and data bus as soon as the 8080A has completed its use of these buses for the current machine cycle. It is recognized under the following conditions:

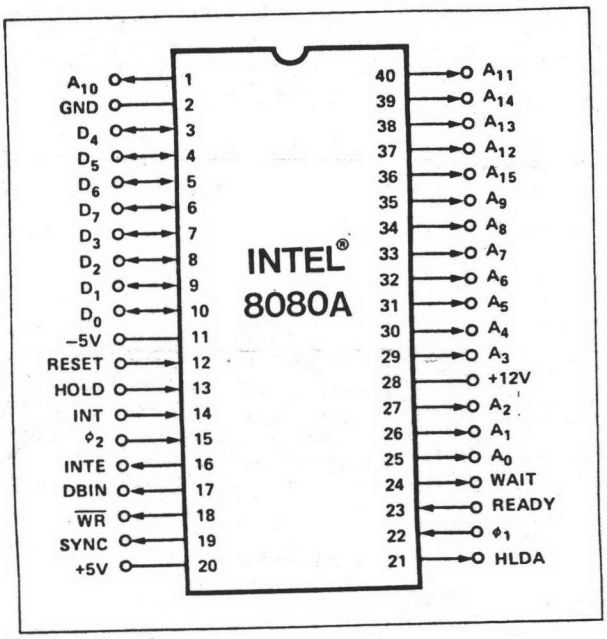
- the CPU is in the HALT state.
- the CPU is in the T2 or TW state and the READY signal is active.

As a result of entering the HOLD state the CPU ADDRESS BUS (A_{15}-A_0) and DATA BUS (D_7-D_0) will be in their high impedance state. The CPU acknowledges its state with the HOLD ACKNOWLEDGE (HLDA) pin.

HLDA (output)
HOLD ACKNOWLEDGE; the HLDA signal appears in response to the HOLD signal and indicates that the data and address bus will go to the high impedance state. The HLDA signal begins at:

- T3 for READ memory or input.
- The Clock Period following T3 for WRITE memory or OUTPUT operation.

In either case, the HLDA signal appears after the rising edge of ϕ_1 and high impedance occurs after the rising edge of ϕ_2.



Pin Configuration

INTE (output)
INTERRUPT ENABLE; indicates the content of the internal interrupt enable flip/flop. This flip/flop may be set or reset by the Enable and Disable Interrupt instructions and inhibits interrupts from being accepted by the CPU when it is reset. It is automatically reset (disabling further interrupts) at time T1 of the instruction fetch cycle (M1) when an interrupt is accepted and is also reset by the RESET signal.

INT (input)
INTERRUPT REQUEST; the CPU recognizes an interrupt request on this line at the end of the current instruction or while halted. If the CPU is in the HOLD state or if the Interrupt Enable flip/flop is reset it will not honor the request.

RESET (input)[1]
RESET; while the RESET signal is activated, the content of the program counter is cleared. After RESET, the program will start at location 0 in memory. The INTE and HLDA flip/flops are also reset. Note that the flags, accumulator, stack pointer, and registers are not cleared.

V_{SS}	Ground Reference.
V_{DD}	+12 ± 5% Volts.
V_{CC}	+5 ± 5% Volts.
V_{BB}	-5 ±5% Volts (substrate bias).
ϕ_1, ϕ_2	2 externally supplied clock phases. (non TTL compatible)

SILICON GATE MOS 8080A

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . . 0°C to +70° C
Storage Temperature . . . . . -65°C to +150°C
All Input or Output Voltages
With Respect to V_{BB} . . . . . -0.3V to +20V
V_{CC}, V_{DD} and V_{SS} With Respect to V_{BB} -0.3V to +20V
Power Dissipation 1.5W

COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS

T_A = 0°C to 70°C, V_{DD} = +12V ± 5%, V_{CC} = +5V ± 5%, V_{BB} = -5V ± 5%, V_{SS} = 0V, Unless Otherwise Noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Condition
V_{ILC}	Clock Input Low Voltage	$V_{SS}-1$		$V_{SS}+0.8$	V	
V_{IHC}	Clock Input High Voltage	9.0		$V_{DD}+1$	V	
V_{IL}	Input Low Voltage	$V_{SS}-1$		$V_{SS}+0.8$	V	
V_{IH}	Input High Voltage	3.3		$V_{CC}+1$	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 1.9mA on all outputs,
V_{OH}	Output High Voltage	3.7			V	I_{OH} = 150μA.
$I_{DD\,(AV)}$	Avg. Power Supply Current (V_{DD})		40	70	mA	Operation
$I_{CC\,(AV)}$	Avg. Power Supply Current (V_{CC})		60	80	mA	T_{CY} = .48 μsec
$I_{BB\,(AV)}$	Avg. Power Supply Current (V_{BB})		.01	1	mA	
I_{IL}	Input Leakage			±10	μA	$V_{SS} \leq V_{IN} \leq V_{CC}$
I_{CL}	Clock Leakage			±10	μA	$V_{SS} \leq V_{CLOCK} \leq V_{DD}$
I_{DL} [2]	Data Bus Leakage in Input Mode			-100 -2.0	μA mA	$V_{SS} \leq V_{IN} \leq V_{SS}+0.8V$ $V_{SS}+0.8V \leq V_{IN} \leq V_{CC}$
I_{FL}	Address and Data Bus Leakage During HOLD			+10 -100	μA	$V_{ADDR/DATA} = V_{CC}$ $V_{ADDR/DATA} = V_{SS} + 0.45V$

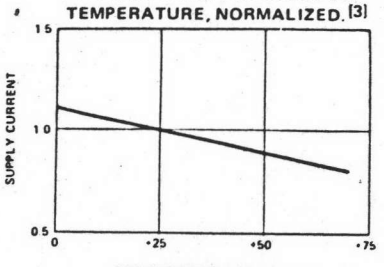
CAPACITANCE

T_A = 25°C $V_{CC} = V_{DD} = V_{SS}$ = 0V, V_{BB} = -5V

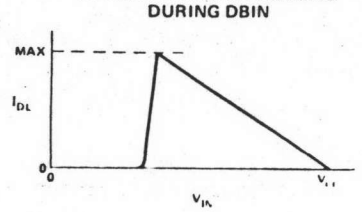
Symbol	Parameter	Typ.	Max.	Unit	Test Condition
C_ϕ	Clock Capacitance	17	25	pf	f_c = 1 MHz
C_{IN}	Input Capacitance	6	10	pf	Unmeasured Pins
C_{OUT}	Output Capacitance	10	20	pf	Returned to V_{SS}

NOTES:
1. The RESET signal must be active for a minimum of 3 clock cycles.
2. When DBIN is high and $V_{IN} > V_{IH}$ an internal active pull up will be switched onto the Data Bus.
3. ΔI supply / ΔT_A = -0.45%/°C.

TYPICAL SUPPLY CURRENT VS. TEMPERATURE, NORMALIZED.[3]



DATA BUS CHARACTERISTIC DURING DBIN



SILICON GATE MOS 8080A

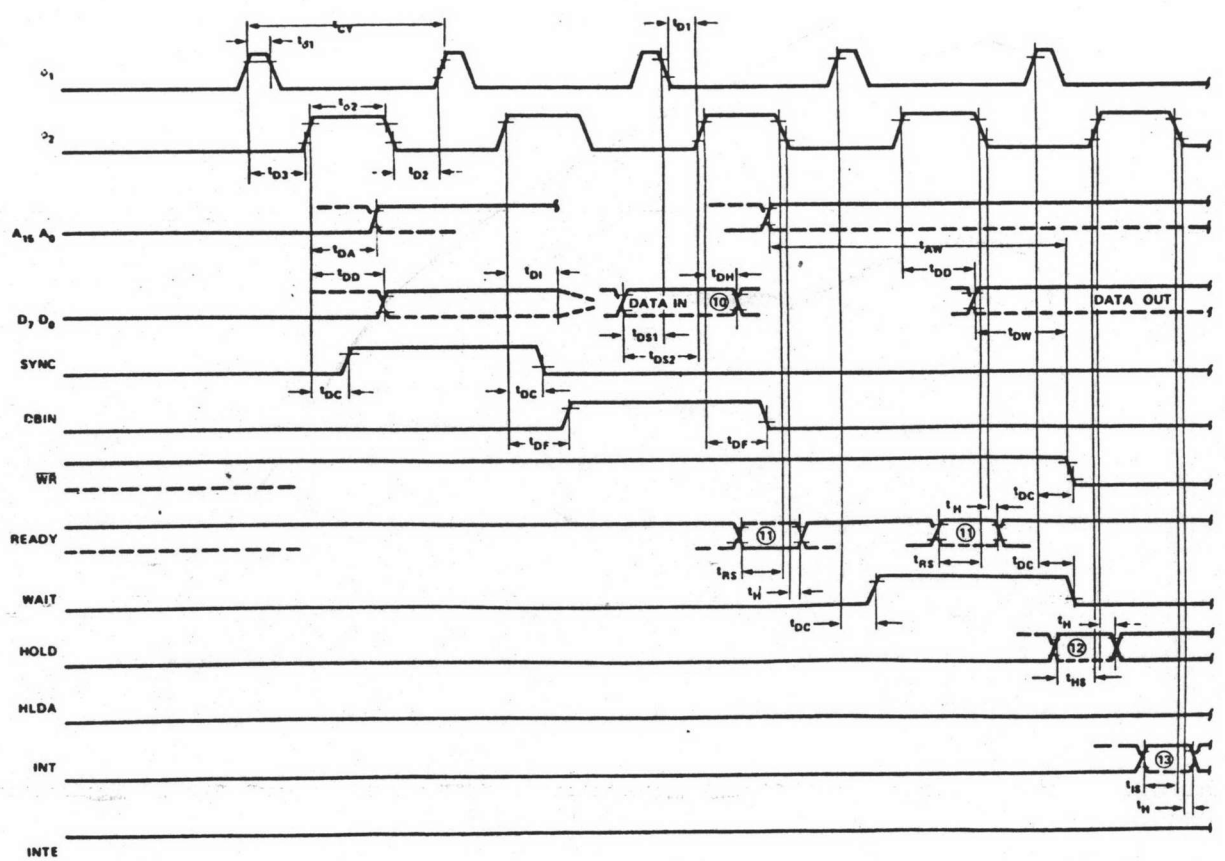
A.C. CHARACTERISTICS

T_A = 0°C to 70°C, V_{DD} = +12V ± 5%, V_{CC} = +5V ± 5%, V_{BB} = -5V ± 5%, V_{SS} = 0V, Unless Otherwise Noted

Symbol	Parameter	Min.	Max.	Unit	Test Condition
t_{CY}[3]	Clock Period	0.48	2.0	μsec	
t_r, t_f	Clock Rise and Fall Time	0	50	nsec	
$t_{\phi 1}$	ϕ_1 Pulse Width	60		nsec	
$t_{\phi 2}$	ϕ_2 Pulse Width	220		nsec	
t_{D1}	Delay ϕ_1 to ϕ_2	0		nsec	
t_{D2}	Delay ϕ_2 to ϕ_1	70		nsec	
t_{D3}	Delay ϕ_1 to ϕ_2 Leading Edges	80		nsec	
t_{DA}[2]	Address Output Delay From ϕ_2		200	nsec	C_L = 100pf
t_{DD}[2]	Data Output Delay From ϕ_2		220	nsec	
t_{DC}[2]	Signal Output Delay From ϕ_1, or ϕ_2 (SYNC, $\overline{WR}$, WAIT, HLDA)		120	nsec	C_L = 50pf
t_{DF}[2]	DBIN Delay From ϕ_2	25	140	nsec	
t_{DI}[1]	Delay for Input Bus to Enter Input Mode		t_{DF}	nsec	
t_{DS1}	Data Setup Time During ϕ_1 and DBIN	30		nsec	

TIMING WAVEFORMS [14]

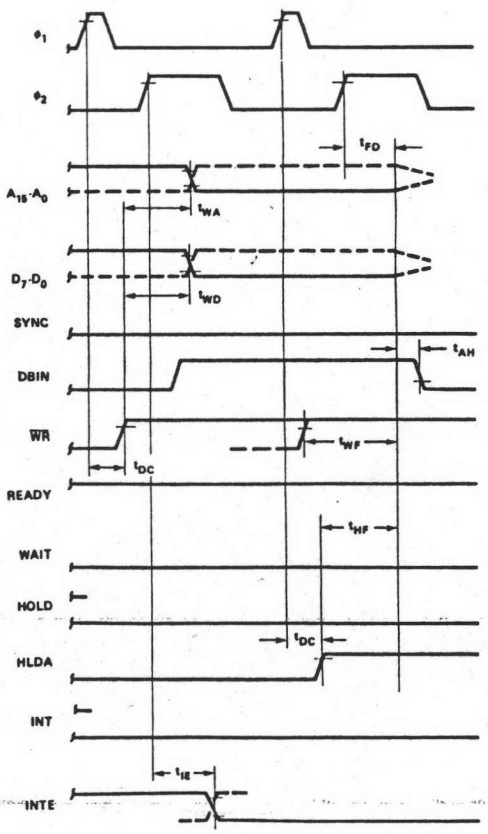
(Note: Timing measurements are made at the following reference voltages: CLOCK "1" = 8.0V "0" = 1.0V; INPUTS "1" = 3.3V, "0" = 0.8V; OUTPUTS "1" = 2.0V, "0" = 0.8V.)



A.C. CHARACTERISTICS (Continued)

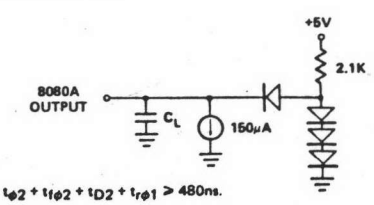
T_A = 0°C to 70°C, V_{DD} = +12V ± 5%, V_{CC} = +5V ± 5%, V_{BB} = -5V ± 5%, V_{SS} = 0V, Unless Otherwise Noted

Symbol	Parameter	Min.	Max.	Unit	Test Condition
t_{DS2}	Data Setup Time to ϕ_2 During DBIN	150		nsec	
t_{DH} [1]	Data Hold Time From ϕ_2 During DBIN	50		nsec	
t_{IE} [2]	INTE Output Delay From ϕ_2		200	nsec	C_L = 50pf
t_{RS}	READY Setup Time During ϕ_2	120		nsec	
t_{HS}	HOLD Setup Time to ϕ_2	140		nsec	
t_{IS}	INT Setup Time During ϕ_2 (During ϕ_1 in Halt Mode)	120		nsec	
t_H	Hold Time From ϕ_2 (READY, INT, HOLD)	0		nsec	
t_{FD}	Delay to Float During Hold (Address and Data Bus)		120	nsec	
t_{AW} [2]	Address Stable Prior to $\overline{WR}$	[5]		nsec	C_L = 100pf: Address, Data C_L = 50pf: WR, HLDA, DBIN
t_{DW} [2]	Output Data Stable Prior to $\overline{WR}$	[6]		nsec	
t_{WD} [2]	Output Data Stable From $\overline{WR}$	[7]		nsec	
t_{WA} [2]	Address Stable From $\overline{WR}$	[7]		nsec	
t_{HF} [2]	HLDA to Float Delay	[8]		nsec	
t_{WF} [2]	$\overline{WR}$ to Float Delay	[9]		nsec	
t_{AH} [2]	Address Hold Time After DBIN During HLDA	-20		nsec	



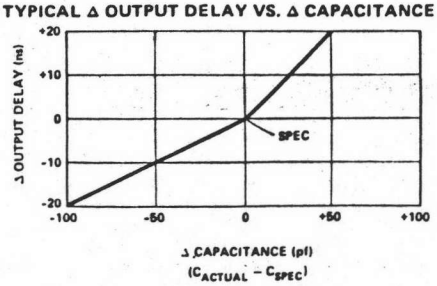
NOTES:

1. Data input should be enabled with DBIN status. No bus conflict can then occur and data hold time is assured. t_{DH} = 50 ns or t_{DF}, whichever is less.
2. Load Circuit.



3. $t_{CY} = t_{D3} + t_{r\phi2} + t_{\phi2} + t_{f\phi2} + t_{D2} + t_{r\phi1} \geq 480$ns.

TYPICAL Δ OUTPUT DELAY VS. Δ CAPACITANCE



4. The following are relevant when interfacing the 8080A to devices having V_{IH} = 3.3V:
   a) Maximum output rise time from .8V to 3.3V = 100ns @ C_L = SPEC.
   b) Output delay when measured to 3.0V = SPEC +60ns @ C_L = SPEC.
   c) If $C_L \neq$ SPEC, add .6ns/pF if $C_L > C_{SPEC}$, subtract .3ns/pF (from modified delay) if $C_L < C_{SPEC}$.
5. $t_{AW} = 2\,t_{CY} - t_{D3} - t_{r\phi2} - 140$nsec.
6. $t_{DW} = t_{CY} - t_{D3} - t_{r\phi2} - 170$nsec.
7. If not HLDA, $t_{WD} = t_{WA} = t_{D3} + t_{r\phi2} + 10$ns. If HLDA, $t_{WD} = t_{WA} = t_{WF}$.
8. $t_{HF} = t_{D3} + t_{r\phi2} - 50$ns.
9. $t_{WF} = t_{D3} + t_{r\phi2} - 10$ns
10. Data in must be stable for this period during DBIN $\cdot T_3$. Both t_{DS1} and t_{DS2} must be satisfied.
11. Ready signal must be stable for this period during T_2 or T_W. (Must be externally synchronized.)
12. Hold signal must be stable for this period during T_2 or T_W when entering hold mode, and during T_3, T_4, T_5 and T_{WH} when in hold mode. (External synchronization is not required.)
13. Interrupt signal must be stable during this period of the last clock cycle of any instruction in order to be recognized on the following instruction. (External synchronization is not required.)
14. This timing diagram shows timing relationships only; it does not represent any specific machine cycle.

INSTRUCTION SET

The accumulator group instructions include arithmetic and logical operators with direct, indirect, and immediate addressing modes.

Move, load, and store instruction groups provide the ability to move either 8 or 16 bits of data between memory, the six working registers and the accumulator using direct, indirect, and immediate addressing modes.

The ability to branch to different portions of the program is provided with jump, jump conditional, and computed jumps. Also the ability to call to and return from subroutines is provided both conditionally and unconditionally. The RESTART (or single byte call instruction) is useful for interrupt vector operation.

Double precision operators such as stack manipulation and double add instructions extend both the arithmetic and interrupt handling capability of the 8080A. The ability to increment and decrement memory, the six general registers and the accumulator is provided as well as extended increment and decrement instructions to operate on the register pairs and stack pointer. Further capability is provided by the ability to rotate the accumulator left or right through or around the carry bit.

Input and output may be accomplished using memory addresses as I/O ports or the directly addressed I/O provided for in the 8080A instruction set.

The following special instruction group completes the 8080A instruction set: the NOP instruction, HALT to stop processor execution and the DAA instructions provide decimal arithmetic capability. STC allows the carry flag to be directly set, and the CMC instruction allows it to be complemented. CMA complements the contents of the accumulator and XCHG exchanges the contents of two 16-bit register pairs directly.

Data and Instruction Formats

Data in the 8080A is stored in the form of 8-bit binary integers. All data transfers to the system data bus will be in the same format.

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

DATA WORD

The program instructions may be one, two, or three bytes in length. Multiple byte instructions must be stored in successive words in program memory. The instruction formats then depend on the particular operation executed.

One Byte Instructions

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	OP CODE

TYPICAL INSTRUCTIONS

Register to register, memory reference, arithmetic or logical, rotate, return, push, pop, enable or disable Interrupt instructions

Two Byte Instructions

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	OP CODE
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	OPERAND

Immediate mode or I/O instructions

Three Byte Instructions

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	OP CODE
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	LOW ADDRESS OR OPERAND 1
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	HIGH ADDRESS OR OPERAND 2

Jump, call or direct load and store instructions

For the 8080A a logic "1" is defined as a high level and a logic "0" is defined as a low level.

SILICON GATE MOS 8080A

INSTRUCTION SET

Summary of Processor Instructions

Mnemonic	Description	Instruction Code[1] D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Clock[2] Cycles
$MOV_{r1,r2}$	Move register to register	0	1	D	D	D	S	S	S	5
MOV M, r	Move register to memory	0	1	1	1	0	S	S	S	7
MOV r, M	Move memory to register	0	1	D	D	D	1	1	0	7
HLT	Halt	0	1	1	1	0	1	1	0	7
MVI r	Move immediate register	0	0	D	D	D	1	1	0	7
MVI M	Move immediate memory	0	0	1	1	0	1	1	0	10
INR r	Increment register	0	0	D	D	D	1	0	0	5
DCR r	Decrement register	0	0	D	D	D	1	0	1	5
INR M	Increment memory	0	0	1	1	0	1	0	0	10
DCR M	Decrement memory	0	0	1	1	0	1	0	1	10
ADD r	Add register to A	1	0	0	0	0	S	S	S	4
ADC r	Add register to A with carry	1	0	0	0	1	S	S	S	4
SUB r	Subtract register from A	1	0	0	1	0	S	S	S	4
SBB r	Subtract register from A with borrow	1	0	0	1	1	S	S	S	4
ANA r	And register with A	1	0	1	0	0	S	S	S	4
XRA r	Exclusive Or register with A	1	0	1	0	1	S	S	S	4
ORA r	Or register with A	1	0	1	1	0	S	S	S	4
CMP r	Compare register with A	1	0	1	1	1	S	S	S	4
ADD M	Add memory to A	1	0	0	0	0	1	1	0	7
ADC M	Add memory to A with carry	1	0	0	0	1	1	1	0	7
SUB M	Subtract memory from A	1	0	0	1	0	1	1	0	7
SBB M	Subtract memory from A with borrow	1	0	0	1	1	1	1	0	7
ANA M	And memory with A	1	0	1	0	0	1	1	0	7
XRA M	Exclusive Or memory with A	1	0	1	0	1	1	1	0	7
ORA M	Or memory with A	1	0	1	1	0	1	1	0	7
CMP M	Compare memory with A	1	0	1	1	1	1	1	0	7
ADI	Add immediate to A	1	1	0	0	0	1	1	0	7
ACI	Add immediate to A with carry	1	1	0	0	1	1	1	0	7
SUI	Subtract immediate from A	1	1	0	1	0	1	1	0	7
SBI	Subtract immediate from A with borrow	1	1	0	1	1	1	1	0	7
ANI	And immediate with A	1	1	1	0	0	1	1	0	7
XRI	Exclusive Or immediate with A	1	1	1	0	1	1	1	0	7
ORI	Or immediate with A	1	1	1	1	0	1	1	0	7
CPI	Compare immediate with A	1	1	1	1	1	1	1	0	7
RLC	Rotate A left	0	0	0	0	0	1	1	1	4
RRC	Rotate A right	0	0	0	0	1	1	1	1	4
RAL	Rotate A left through carry	0	0	0	1	0	1	1	1	4
RAR	Rotate A right through carry	0	0	0	1	1	1	1	1	4
JMP	Jump unconditional	1	1	0	0	0	0	1	1	10
JC	Jump on carry	1	1	0	1	1	0	1	0	10
JNC	Jump on no carry	1	1	0	1	0	0	1	0	10
JZ	Jump on zero	1	1	0	0	1	0	1	0	10
JNZ	Jump on no zero	1	1	0	0	0	0	1	0	10
JP	Jump on positive	1	1	1	1	0	0	1	0	10
JM	Jump on minus	1	1	1	1	1	0	1	0	10
JPE	Jump on parity even	1	1	1	0	1	0	1	0	10
JPO	Jump on parity odd	1	1	1	0	0	0	1	0	10
CALL	Call unconditional	1	1	0	0	1	1	0	1	17
CC	Call on carry	1	1	0	1	1	1	0	0	11/17
CNC	Call on no carry	1	1	0	1	0	1	0	0	11/17
CZ	Call on zero	1	1	0	0	1	1	0	0	11/17
CNZ	Call on no zero	1	1	0	0	0	1	0	0	11/17
CP	Call on positive	1	1	1	1	0	1	0	0	11/17
CM	Call on minus	1	1	1	1	1	1	0	0	11/17
CPE	Call on parity even	1	1	1	0	1	1	0	0	11/17
CPO	Call on parity odd	1	1	1	0	0	1	0	0	11/17
RET	Return	1	1	0	0	1	0	0	1	10
RC	Return on carry	1	1	0	1	1	0	0	0	5/11
RNC	Return on no carry	1	1	0	1	0	0	0	0	5/11

Mnemonic	Description	Instruction Code[1] D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Clock[2] Cycles
RZ	Return on zero	1	1	0	0	1	0	0	0	5/11
RNZ	Return on no zero	1	1	0	0	0	0	0	0	5/11
RP	Return on positive	1	1	1	1	0	0	0	0	5/11
RM	Return on minus	1	1	1	1	1	0	0	0	5/11
RPE	Return on parity even	1	1	1	0	1	0	0	0	5/11
RPO	Return on parity odd	1	1	1	0	0	0	0	0	5/11
RST	Restart	1	1	A	A	A	1	1	1	11
IN	Input	1	1	0	1	1	0	1	1	10
OUT	Output	1	1	0	1	0	0	1	1	10
LXI B	Load immediate register Pair B & C	0	0	0	0	0	0	0	1	10
LXI D	Load immediate register Pair D & E	0	0	0	1	0	0	0	1	10
LXI H	Load immediate register Pair H & L	0	0	1	0	0	0	0	1	10
LXI SP	Load immediate stack pointer	0	0	1	1	0	0	0	1	10
PUSH B	Push register Pair B & C on stack	1	1	0	0	0	1	0	1	11
PUSH D	Push register Pair D & E on stack	1	1	0	1	0	1	0	1	11
PUSH H	Push register Pair H & L on stack	1	1	1	0	0	1	0	1	11
PUSH PSW	Push A and Flags on stack	1	1	1	1	0	1	0	1	11
POP B	Pop register pair B & C off stack	1	1	0	0	0	0	0	1	10
POP D	Pop register pair D & E off stack	1	1	0	1	0	0	0	1	10
POP H	Pop register pair H & L off stack	1	1	1	0	0	0	0	1	10
POP PSW	Pop A and Flags off stack	1	1	1	1	0	0	0	1	10
STA	Store A direct	0	0	1	1	0	0	1	0	13
LDA	Load A direct	0	0	1	1	1	0	1	0	13
XCHG	Exchange D & E, H & L Registers	1	1	1	0	1	0	1	1	4
XTHL	Exchange top of stack, H & L	1	1	1	0	0	0	1	1	18
SPHL	H & L to stack pointer	1	1	1	1	1	0	0	1	5
PCHL	H & L to program counter	1	1	1	0	1	0	0	1	5
DAD B	Add B & C to H & L	0	0	0	0	1	0	0	1	10
DAD D	Add D & E to H & L	0	0	0	1	1	0	0	1	10
DAD H	Add H & L to H & L	0	0	1	0	1	0	0	1	10
DAD SP	Add stack pointer to H & L	0	0	1	1	1	0	0	1	10
STAX B	Store A indirect	0	0	0	0	0	0	1	0	7
STAX D	Store A indirect	0	0	0	1	0	0	1	0	7
LDAX B	Load A indirect	0	0	0	0	1	0	1	0	7
LDAX D	Load A indirect	0	0	0	1	1	0	1	0	7
INX B	Increment B & C registers	0	0	0	0	0	0	1	1	5
INX D	Increment D & E registers	0	0	0	1	0	0	1	1	5
INX H	Increment H & L registers	0	0	1	0	0	0	1	1	5
INX SP	Increment stack pointer	0	0	1	1	0	0	1	1	5
DCX B	Decrement B & C	0	0	0	0	1	0	1	1	5
DCX D	Decrement D & E	0	0	0	1	1	0	1	1	5
DCX H	Decrement H & L	0	0	1	0	1	0	1	1	5
DCX SP	Decrement stack pointer	0	0	1	1	1	0	1	1	5
CMA	Complement A	0	0	1	0	1	1	1	1	4
STC	Set carry	0	0	1	1	0	1	1	1	4
CMC	Complement carry	0	0	1	1	1	1	1	1	4
DAA	Decimal adjust A	0	0	1	0	0	1	1	1	4
SHLD	Store H & L direct	0	0	1	0	0	0	1	0	16
LHLD	Load H & L direct	0	0	1	0	1	0	1	0	16
EI	Enable Interrupts	1	1	1	1	1	0	1	1	4
DI	Disable interrupt	1	1	1	1	0	0	1	1	4
NOP	No-operation	0	0	0	0	0	0	0	0	4

NOTES: 1. DDD or SSS – 000 B – 001 C – 010 D – 011 E – 100 H – 101 L – 110 Memory – 111 A.
2. Two possible cycle times, (5/11) indicate instruction cycles dependent on condition flags.

intel

Schottky Bipolar 8224

CLOCK GENERATOR AND DRIVER FOR 8080A CPU

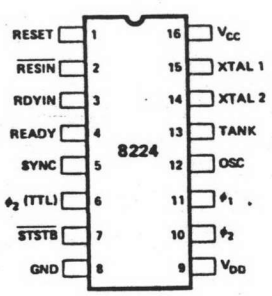
- Single Chip Clock Generator/Driver for 8080A CPU
- Power-Up Reset for CPU
- Ready Synchronizing Flip-Flop
- Advanced Status Strobe
- Oscillator Output for External System Timing
- Crystal Controlled for Stable System Operation
- Reduces System Package Count

The 8224 is a single chip clock generator/driver for the 8080A CPU. It is controlled by a crystal, selected by the designer, to meet a variety of system speed requirements.

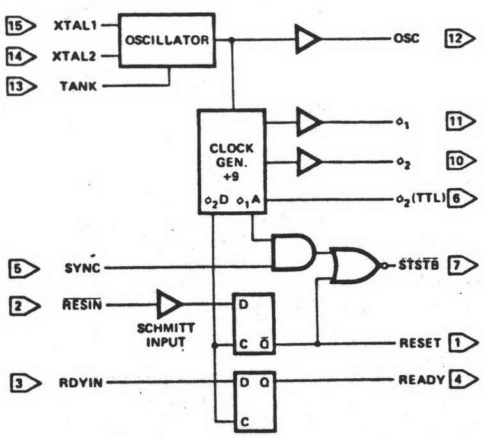
Also included are circuits to provide power-up reset, advance status strobe and synchronization of ready.

The 8224 provides the designer with a significant reduction of packages used to generate clocks and timing for 8080A.

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

$\overline{\text{RESIN}}$	RESET INPUT
RESET	RESET OUTPUT
RDYIN	READY INPUT
READY	READY OUTPUT
SYNC	SYNC INPUT
$\overline{\text{STSTB}}$	STATUS STB (ACTIVE LOW)
ϕ_1	8080 CLOCKS
ϕ_2	8080 CLOCKS

XTAL 1	CONNECTIONS FOR CRYSTAL
XTAL 2	CONNECTIONS FOR CRYSTAL
TANK	USED WITH OVERTONE XTAL
OSC	OSCILLATOR OUTPUT
ϕ_2 (TTL)	ϕ_2 CLK (TTL LEVEL)
V_{CC}	+5V
V_{DD}	+12V
GND	0V

SCHOTTKY BIPOLAR 8224

D.C. Characteristics

T_A = 0°C to 70°C; V_{CC} = +5.0V ±5%; V_{DD} = +12V ±5%.

Symbol	Parameter	Limits Min.	Typ.[1]	Max.	Units	Test Conditions
I_F	Input Current Loading		.15		mA	V_F = .45V
I_R	Input Leakage Current				μA	V_R = 5.25V
V_C	Input Forward Clamp Voltage					I_C = -5mA
V_{IL}	Input "Low" Voltage				V	
V_{IH}	Input "High" Voltage		2.2		V	Reset Input All Other Inputs
V_{IH}-V_{IL}	Ready Input Hysteresis		500		mV	
V_{OL}	Output "Low" Voltage		.3 .3		V	(ϕ_1, ϕ_2), Ready, Reset I_{OL} = 2mA All Other Outputs I_{OL} = 15mA
V_{OH}	Output "High" Voltage ϕ_1 , ϕ_2 READY, RESET All Other Outputs		11V 4V 3V		V V	I_{OH} = -100μA I_{OH} = -100μA I_{OH} = -1mA
I_{SC}	Output Short Circuit Current (All Low Voltage Outputs Only)		40		mA	V_O = 0V V_{CC} = 5.0V
I_{CC}	Power Supply Current		70		mA	
I_{DD}	Power Supply Current		5		mA	

Note 1: Typical values are for T_A = 25°C and nominal supply voltages.

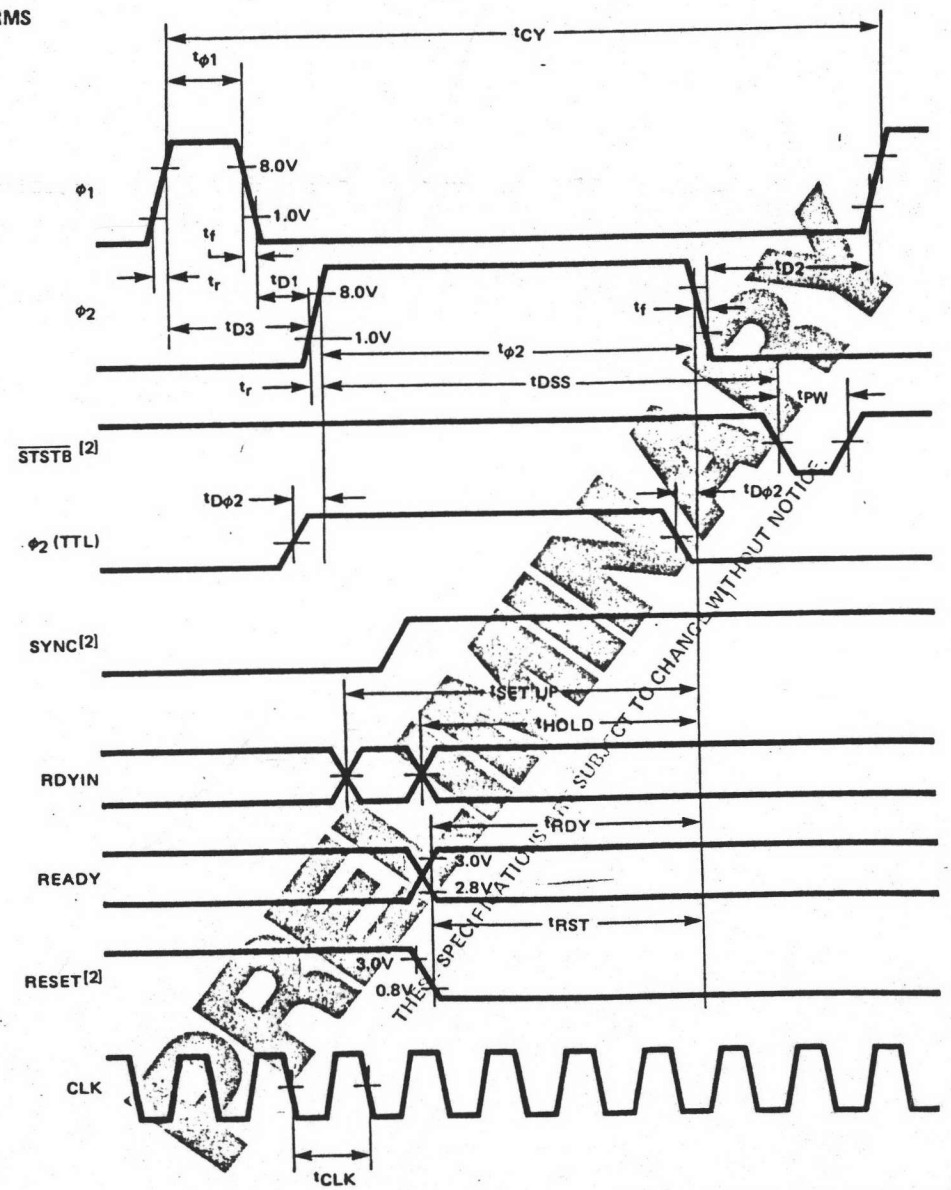
A.C. Characteristics

T_A = 0°C to 70°C; V_{DD} = +5V ±5%; V_{DD} = +12V ±5%.

Symbol	Parameter	Limits Min.	Typ.	Max.	Units	Test Conditions
$t_{\phi 1}$	ϕ_1 Pulse Width		105		ns	t_{CY} = 480ns
$t_{\phi 2}$	ϕ_2 Pulse Width		250		ns	
t_{D1}	Delay ϕ_1 to ϕ_2		5		ns	
t_{D2}	Delay ϕ_2 to ϕ_1		100		ns	ϕ_1 & ϕ_2 Loaded to C_L = 20 to 50pF
t_{D3}	Delay ϕ_1 to ϕ_2 Leading Edges		115		ns	
t_r	Output Rise Time		15		ns	
t_f	Output Fall Time		10		ns	
t_{DSS}	ϕ_2 to $\overline{STSTB}$ Delay		300		ns	ϕ_2 (TTL) & Status Strobe Loaded to 15mA/30pF
$t_{D\phi 2}$	ϕ_2 (TTL) to ϕ_2 Delay		5		ns	
t_{PW}	Status Strobe Pulse Width		55		ns	
t_{SETUP}	RDYIN Setup Time to ϕ_2		250		ns	Ready & Reset Loaded to 2mA/10pF
t_{HOLD}	RDYIN Hold Time to ϕ_2		220		ns	All measurements referenced to 1.5V unless specified otherwise.
t_{RDY}	READY to ϕ_2 Delay		200		ns	
t_{RST}	RESET to ϕ_2 Delay		200		ns	
t_{CLK}	Clock Period =		$t_{CY} \div 9$		ns	

SCHOTTKY BIPOLAR 8224

WAVEFORMS



Note 2. $\overline{\text{STSTB}}$ and SYNC are shown for a typical clock cycle. During RESET, both $\overline{\text{STSTB}}$ and SYNC are normally low.

intel

Schottky Bipolar 8228

SYSTEM CONTROLLER AND BUS DRIVER FOR 8080A CPU

- **Single Chip System Control for MCS™-80 Systems**
- **Built-in Bi-Directional Bus Driver for Data Bus Isolation**
- **Allows the use of Multiple Byte Instructions (e.g. CALL) for Interrupt Acknowledge**
- **User Selected Single Level Interrupt Vector (RST 7)**
- **28 Pin Dual In-Line Package**
- **Reduces System Package Count**

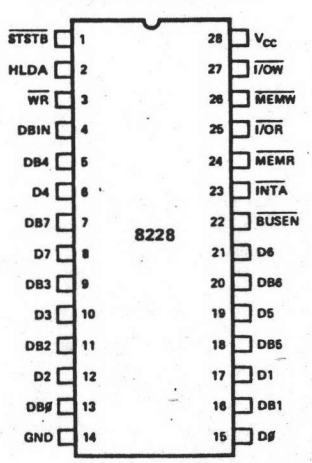
The 8228 is a single chip system controller and bus driver for MCS-80. It generates all signals required to directly interface MCS-80 family RAM, ROM, and I/O components.

A bi-directional bus driver is included to provide high system TTL fan-out. It also provides isolation of the 8080 data bus from memory and I/O. This allows for the optimization of control signals, enabling the systems deisgner to use slower memory and I/O. The isolation of the bus driver also provides for enhanced system noise immunity.

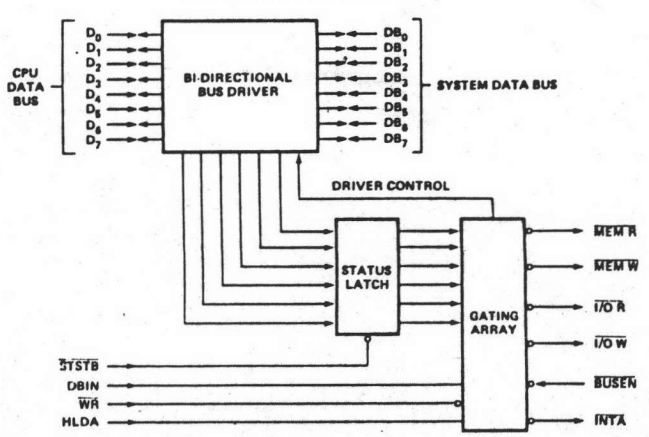
A user selected single level interrupt vector (RST 7) is provided to simplify real time, interrupt driven, small system requirements. The 8228 also generates the correct control signals to allow the use of multiple byte instructions (e.g., CALL) in response to an INTERRUPT ACKNOWLEDGE by the 8080A. This feature permits large, interrupt driven systems to have an unlimited number of interrupt levels.

The 8228 is designed to support a wide variety of system bus structures and also reduce system package count for cost effective, reliable, design of the MCS-80 systems.

PIN CONFIGURATION



8228 BLOCK DIAGRAM

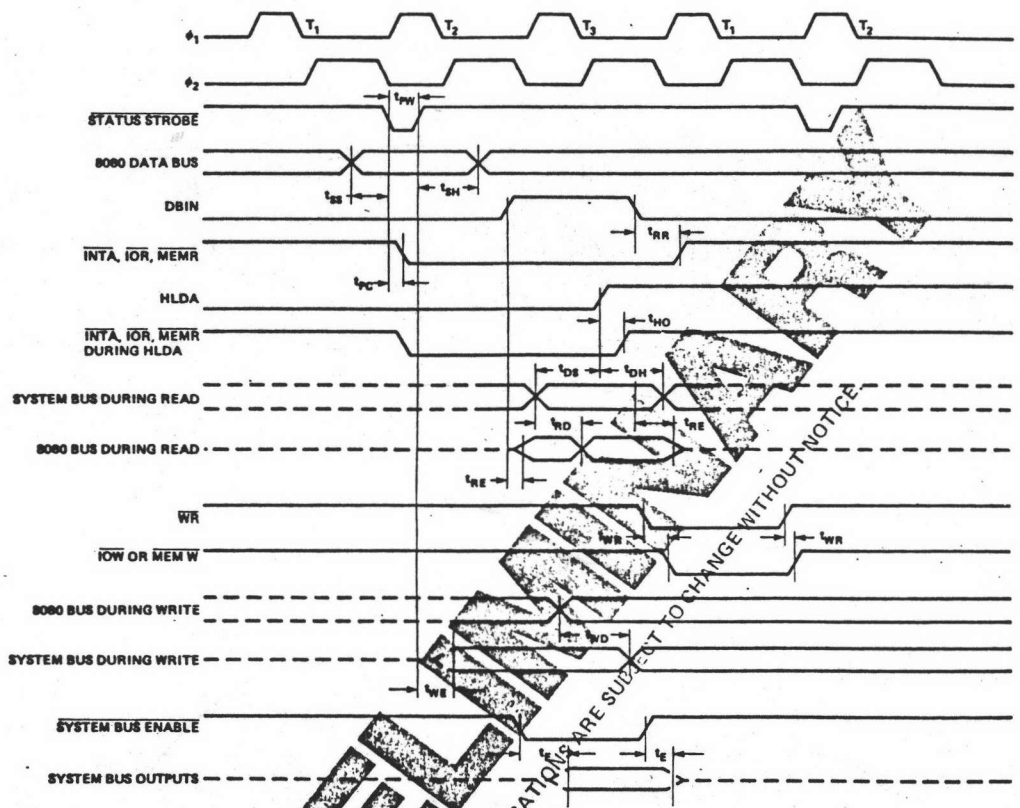


PIN NAMES

D7-D0	DATA BUS (8080 SIDE)	INTA	INTERRUPT ACKNOWLEDGE
DB7-DB0	DATA BUS (SYSTEM SIDE)	HLDA	HLDA (FROM 8080)
I/OR	I/O READ	WR	WR (FROM 8080)
I/OW	I/O WRITE	BUSEN	BUS ENABLE INPUT
MEMR	MEMORY READ	STSTB	STATUS STROBE (FROM 8224)
MEMW	MEMORY WRITE	VCC	+5V
DBIN	DBIN (FROM 8080)	GND	0 VOLTS

SCHOTTKY BIPOLAR 8228

WAVEFORMS



SCHOTTKY BIPOLAR 8228

D.C. Characteristics T_A = 0°C to 70°C; V_{CC} = 5V ±5%.

Symbol	Parameter	Limits Min.	Typ.[1]	Max.	Unit	Test Conditions
V_C	Input Clamp Voltage, All Inputs		.8		V	V_{CC}=4.75V; I_C=-5mA
I_F	Input Load Current, $\overline{STSTB}$				mA	V_{CC} = 5.25V
	D_2 & D_6				mA	V_F = 0.45V
	D_0, D_1, D_4, D_5, & D_7				mA	
	All Other Inputs				mA	
I_R	Input Leakage Current $\overline{STSTB}$				μA	V_{CC} = 5.25V
	DB_0-DB_7				μA	V_R = 5.25V
	All Other Inputs				μA	
V_{TH}*	Input Threshold Voltage, All Inputs	.8		2.0	V	V_{CC} = 5V
I_{CC}	Power Supply Current		150		mA	V_{CC}=5.25V
V_{OL}	Output Low Voltage, D_0-D_7		.3		V	V_{CC}=4.75V; I_{OL}=2mA
	All Other Outputs		.3		V	I_{OL} = 10mA
V_{OH}	Output High Voltage, D_0-D_7		3.7		V	V_{CC}=4.75V; I_{OH}=-100μA
	All Other Outputs		3.0		V	I_{OH} = -1mA
I_{OS}	Short Circuit Current, All Outputs		35		mA	V_{CC}=5V
$I_{O(off)}$	Off State Output Current, All Control Outputs				μA	V_{CC}=5.25V; V_O=5.25
					μA	V_O=.45V

Note 1: Typical values are for T_A = 25°C and nominal supply voltages.

A.C. Characteristics T_A = 0°C to 70°C; V_{CC} = 5V ±5%.

Symbol	Parameter	Limits Min.	Typ.	Max.	Units
t_{PW}	Width of Status Strobe		15		ns
t_{SS}	Setup Time, Status Inputs D_0-D_7		5		ns
t_{SH}	Hold Time, Status Inputs D_0-D_7		5		ns
t_{DC}	Delay from $\overline{STSTB}$ to any Control Signal		25		ns
t_{RR}	Delay from DBIN to Control Outputs		10		ns
t_{RE}	Delay from DBIN to Enable 8080 Bus		25		ns
t_{RD}	Delay from System Bus to 8080 Bus during Read		25		ns
t_{WR}	Delay from $\overline{WR}$ to Control Outputs		20		ns
t_{WE}	Delay to Enable System Bus DB_0-DB_7 after STSTB		25		ns
t_{WD}	Delay from 8080 Bus D_0-D_7 to System Bus DB_0-DB_7 during Write		20		ns
t_E	Delay from System Bus Enable to System Bus DB_0-DB_7		25		ns
t_{HO}	HLDA to Read Status Outputs		10		ns
t_{DS}	Setup Time, System Bus Inputs to HLDA		0		ns
t_{DH}	Hold Time, System Bus Inputs to HLDA		10		ns

intel Silicon Gate MOS 8708/8704 (2708/2704)

8192/4096 BIT ERASABLE AND ELECTRICALLY REPROGRAMMABLE READ ONLY MEMORY

- 8708 1024x8 Organization
- 8704 512x8 Organization

- Fast Programming — Typ. 100 sec. For All 8K Bits
- Low Power During Programming
- Access Time—450 ns
- Standard Power Supplies— +12V, ±5V
- Static—No Clocks Required
- Inputs and Outputs TTL Compatible During Both Read and Program Modes
- Three-State Output—OR-Tie Capability

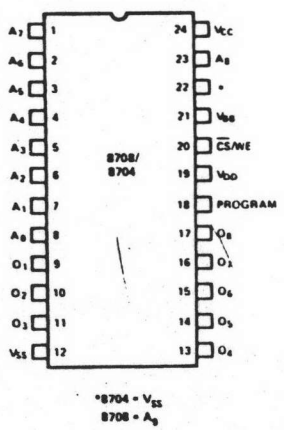
The Intel® 8708/8704 are high speed 8192/4096 bit erasable and electrically reprogrammable ROM's (EPROM) ideally suited where fast turn around and pattern experimentation are important requirements.

The 8708/8704 are packaged in a 24 pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the devices.

A pin for pin mask programmed ROM, the Intel® 8308, is available for large volume production runs of systems initially using the 8708.

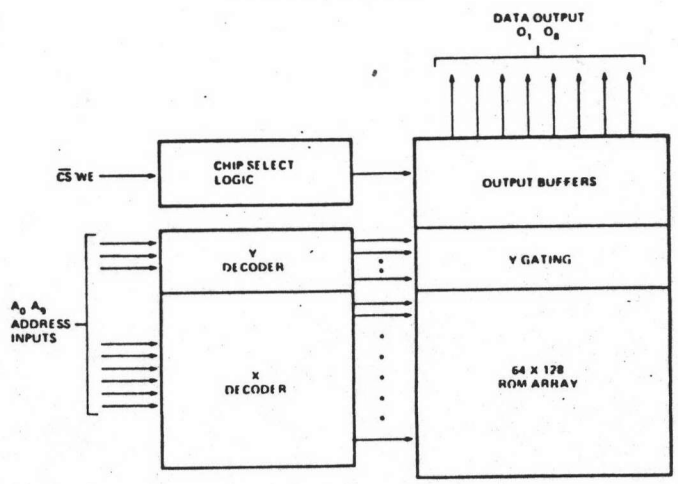
The 8708/8704 is fabricated with the time proven N-channel silicon gate technology.

PIN CONFIGURATIONS



*8704 = V_{SS}
8708 = A_9

BLOCK DIAGRAM



PIN NAMES

A_0-A_9	ADDRESS INPUTS
O_1-O_8	DATA OUTPUTS
$\overline{CS}$/WE	CHIP SELECT/WRITE ENABLE INPUT

Absolute Maximum Ratings*

Temperature Under Bias	-25°C to +85°C
Storage Temperature	-65°C to +125°C
All Input or Output Voltages with Respect to V_{BB} (except Program)	+15V to -0.3V
Program Input to V_{BB}	+35V to -0.3V
Supply Voltages V_{CC} and V_{SS} with Respect to V_{BB}	+15V to -0.3V
V_{DD} with Respect to V_{BB}	+20V to -0.3V
Power Dissipation	1.5W

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

READ OPERATION

D.C. and Operating Characteristics

T_A = 0°C to 70°C, V_{CC} = +5V ±5%, V_{DD} = +12V ±5%, V_{BB} = -5V ±5%, V_{SS} = 0V, Unless Otherwise Noted.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Conditions
I_{LI}	Address and Chip Select Input Load Current			10	μA	V_{IN} = 5.25V
I_{LO}	Output Leakage Current			10	μA	V_{OUT} = 5.25V, $\overline{CS}$/WE = 5V
I_{DD}	V_{DD} Supply Current		50	65	mA	Worst Case Supply Currents: All Inputs High $\overline{CS}$/WE = 5V; T_A = 0°C
I_{CC}	V_{CC} Supply Current		6	10	mA	
I_{BB}	V_{BB} Supply Current		30	45	mA	
V_{IL}	Input Low Voltage	V_{SS}		0.65	V	
V_{IH}	Input High Voltage	3.0		V_{CC}+1	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 1.6mA
V_{OH1}	Output High Voltage	3.7			V	I_{OH} = -100μA
V_{OH2}	Output High Voltage	2.4			V	I_{OH} = -1mA
P_D	Power Dissipation			800	mW	T_A = 70°C

NOTES 1. Typical values are for T_A = 25°C and nominal supply voltages.
2. The program input (Pin 18) may be tied to V_{SS} or V_{CC} during the read mode.

A.C. Characteristics

$T_A = 0°C$ to $70°C$, $V_{CC} = +5V \pm 5\%$, $V_{DD} = +12V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, $V_{SS} = 0V$, Unless Otherwise Noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{ACC}	Address to Output Delay		280	450	ns
$t_{\overline{CO}}$	Chip Select to Output Delay			120	ns
t_{DF}	Chip De-Select to Output Float	0		120	ns
t_{OH}	Address to Output Hold	0			ns

Capacitance[1] $T_A = 25°C$, $f = 1MHz$

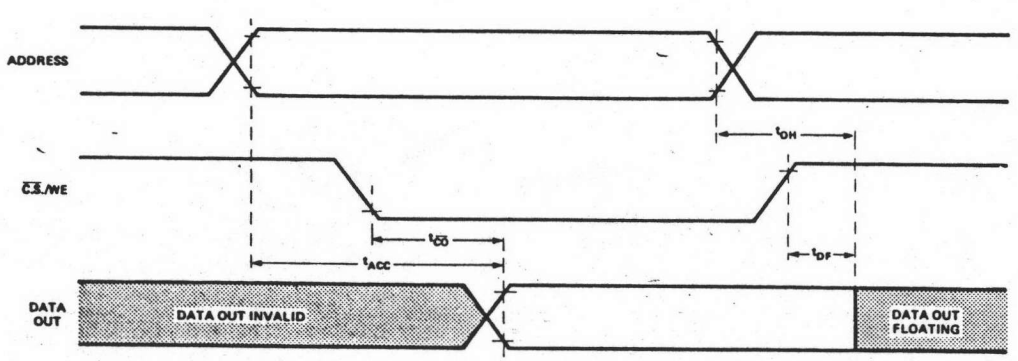
Symbol	Parameter	Typ.	Max.	Unit	Conditions
C_{IN}	Input Capacitance	4	6	pF	$V_{IN}=0V$
C_{OUT}	Output Capacitance	8	12	pF	$V_{OUT}=0V$

Note 1. This parameter is periodically sampled and not 100% tested.

A.C. Test Conditions:

Output Load: 1 TTL gate and $C_L = 100pF$
Input Rise and Fall Times: ≤20ns
Timing Measurement Reference Levels: 0.8V and 2.8V for inputs; 0.8V and 2.4V for outputs
Input Pulse Levels: 0.65V to 3.0V

Waveforms



PROGRAMMING OPERATION

Description

Initially, and after each erasure, all bits of the 8708/8704 are in the "1" state (Output High). Information is introduced by selectively programming "0" into the desired bit locations.

The circuit is set up for programming operation by raising the $\overline{CS}$/WE input (Pin 20) to +12V. The word address is selected in the same manner as in the read mode. Data to be programmed are presented, 8-bits in parallel, to the data output lines (O_1-O_8). Logic levels for address and data lines and the supply voltages are the same as for the read mode. After address and data set up one program pulse (V_P) per address is applied to the program input (Pin 18). One pass through all addresses to be programmed is defined as a program loop. The number of loops (N) required is a function of the program pulse width (t_{PW}) according to $N \times t_{PW} \geq 100$ ms.

For program verification, program loops and read loops may be alternated as shown in waveform B.

Program Characteristics

$T_A = 25°C$, $V_{CC} = +5V \pm 5\%$, $V_{DD} = +12V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, $V_{SS} = 0V$, $\overline{CS}$/WE = +12V, Unless Otherwise Noted.

Symbol	Parameter	Min.	Typ.	Max.	Units
t_{AS}	Address Setup Time	10			μs
t_{CSS}	$\overline{CS}$/WE Setup Time	10			μs
t_{DS}	Data Setup Time	10			μs
t_{AH}	Address Hold Time	1			μs
t_{CH}	$\overline{CS}$/WE Hold Time	.5			μs
t_{DH}	Data Hold Time	1			μs
t_{DF}	Chip Deselect to Output Float Delay	0		120	ns
t_{DPR}	Program To Read Delay			10	μs
t_{PW}	Program Pulse Width	.1		1.0	ms
t_{PR}	Program Pulse Rise Time	.5		2.0	μs
t_{PF}	Program Pulse Fall Time	.5		2.0	μs
I_P	Programming Current		10	20	mA
V_P	Program Pulse Amplitude	25		27	V

NOTE: Intel's standard product warranty applies only to devices programmed to specifications described herein.

Erasing Procedure

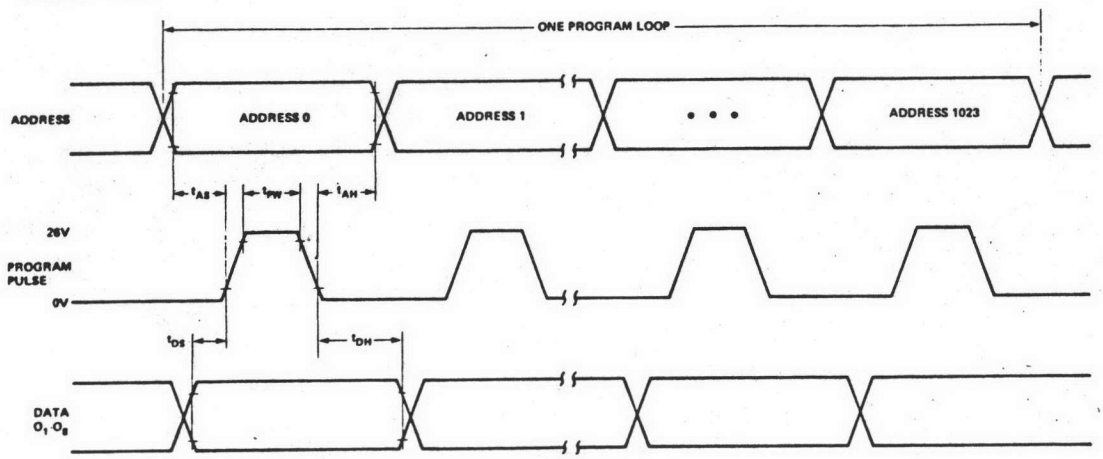
The 8708/8704 may be erased by exposure to high intensity short-wave ultraviolet light at a wavelength of 2537Å. The recommended integrated dose. (i.e., UV intensity x exposure time) is 10W-sec/cm^2. Examples of ultraviolet sources which can erase the 8708/8704 in 20 to 30 minutes are the Model UVS-54 and Model S-52 short-wave ultraviolet lamps manufactured by Ultra-Violet Products, Inc. (5114 Walnut Grove Avenue, San Gabriel, California). The lamps should be used without short-wave filters, and the 8708/8704 to be erased should be placed about one inch away from the lamp tubes.

Waveforms

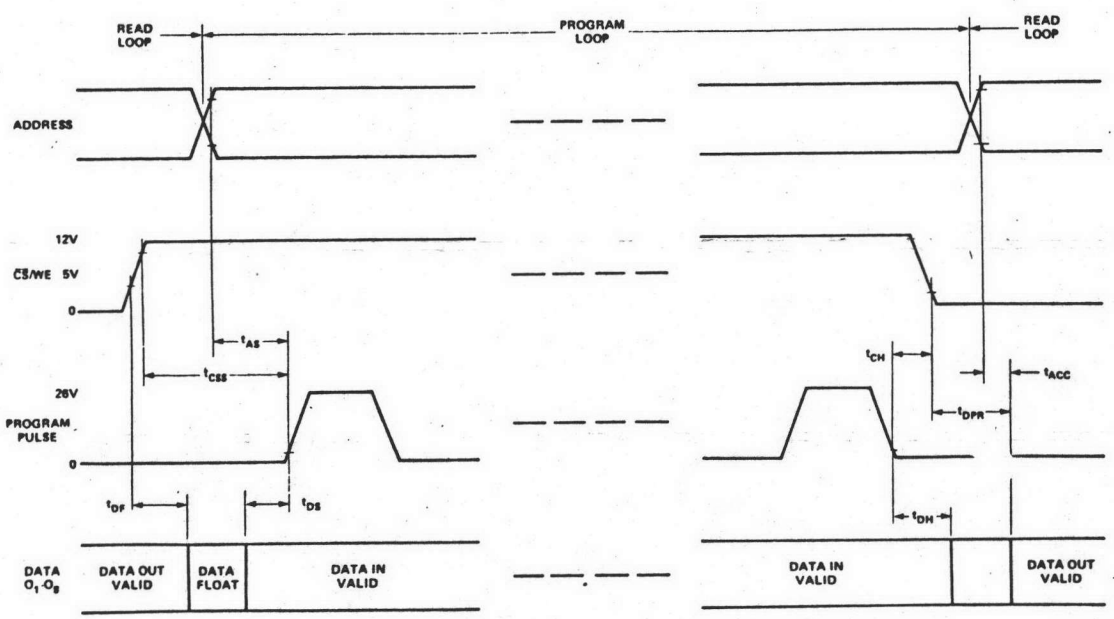
(Logic levels and timing reference levels same as in the Read Mode unless noted otherwise.)

A) Program Mode

$\overline{CS}$/WE = +12V

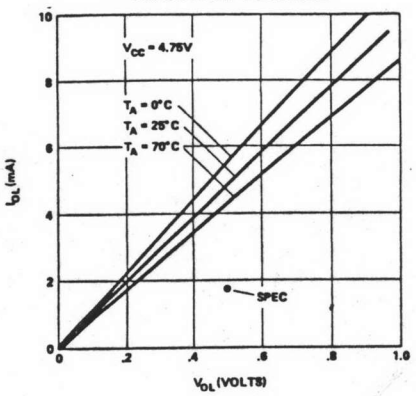


B) Read/Program/Read Transitions

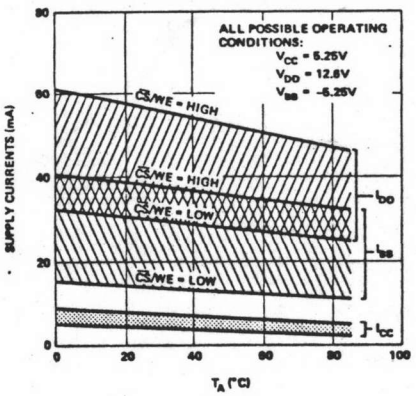


Typical Characteristics (Nominal supply voltages unless otherwise noted):

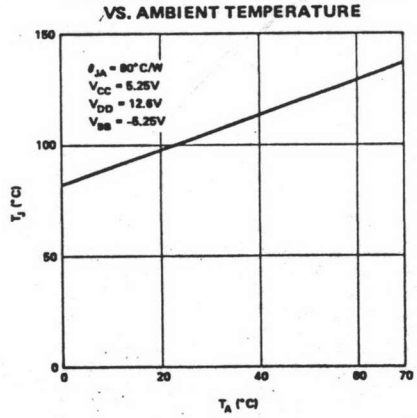
OUTPUT SINK CURRENT
VS. OUTPUT VOLTAGE



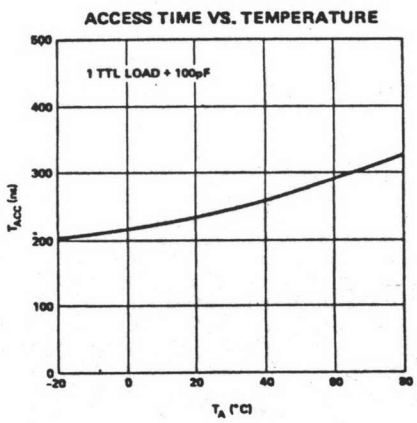
RANGE OF SUPPLY CURRENTS
VS. TEMPERATURE



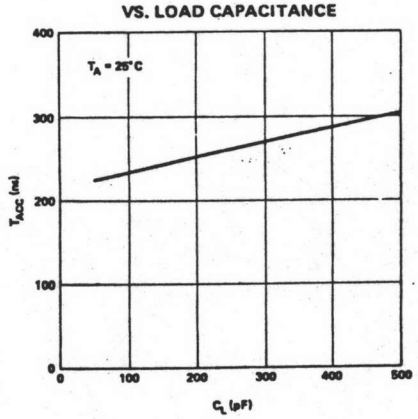
MAXIMUM JUNCTION TEMPERATURE
VS. AMBIENT TEMPERATURE



ACCESS TIME VS. TEMPERATURE



ACCESS TIME
VS. LOAD CAPACITANCE



intel®

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

2114A*
1024 X 4 BIT STATIC RAM

	2114AL-2	2114AL-3	2114AL-4	2114A-4	2114A-5
Max. Access Time (ns)	120	150	200	200	250
Max. Current (mA)	40	40	40	70	70

- HMOS Technology
- Low Power, High Speed
- Identical Cycle and Access Times
- Single +5V Supply ±10%
- High Density 18 Pin Package
- Completely Static Memory - No Clock or Timing Strobe Required
- Directly TTL Compatible: All Inputs and Outputs
- Common Data Input and Output Using Three-State Outputs
- 2114 Upgrade

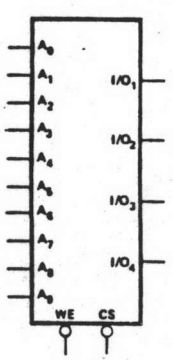
The Intel® 2114A is a 4096-bit static Random Access Memory organized as 1024 words by 4-bits using HMOS, a high performance MOS technology. It uses fully DC stable (static) circuitry throughout, in both the array and the decoding, therefore it requires no clocks or refreshing to operate. Data access is particularly simple since address setup times are not required. The data is read out nondestructively and has the same polarity as the input data. Common input/output pins are provided.

The 2114A is designed for memory applications where the high performance and high reliability of HMOS, low cost, large bit storage, and simple interfacing are important design objectives. The 2114A is placed in an 18-pin package for the highest possible density.

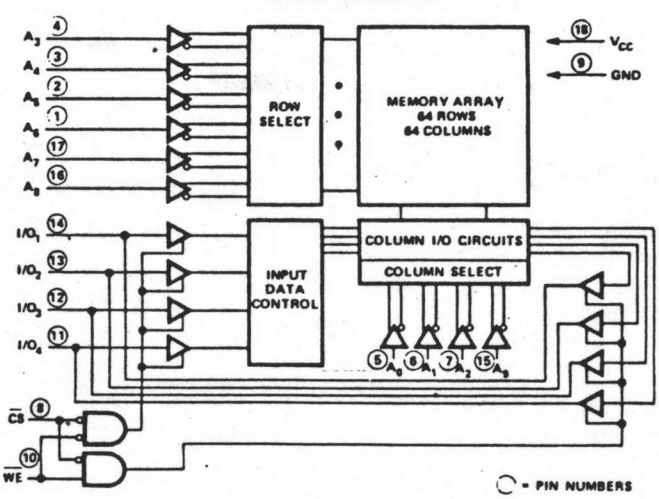
It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. A separate Chip Select ($\overline{CS}$) lead allows easy selection of an individual package when outputs are or-tied.

PIN CONFIGURATION

LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0–A_9	ADDRESS INPUTS	V_{CC}	POWER (+5V)
$\overline{WE}$	WRITE ENABLE	GND	GROUND
$\overline{CS}$	CHIP SELECT		
I/O_1–I/O_4	DATA INPUT/OUTPUT		

*PART ALSO AVAILABLE IN EXTENDED TEMPERATURE RANGE FOR MILITARY GRADE APPLICATIONS.

Intel Corporation, 3065 Bowers Avenue, Santa Clara, California 95051

Schottky Bipolar 8212

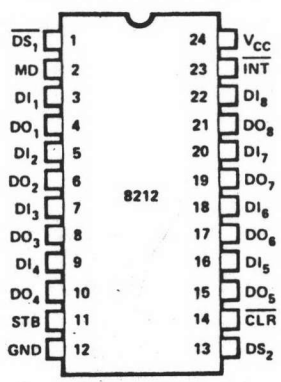
EIGHT-BIT INPUT/OUTPUT PORT

- Fully Parallel 8-Bit Data Register and Buffer
- Service Request Flip-Flop for Interrupt Generation
- Low Input Load Current — .25 mA Max.
- Three State Outputs
- Outputs Sink 15 mA
- 3.65V Output High Voltage for Direct Interface to 8080 CPU or 8008 CPU
- Asynchronous Register Clear
- Replaces Buffers, Latches and Multiplexers in Microcomputer Systems
- Reduces System Package Count

The 8212 input/output port consists of an 8-bit latch with 3-state output buffers along with control and device selection logic. Also included is a service request flip-flop for the generation and control of interrupts to the microprocessor.

The device is multimode in nature. It can be used to implement latches, gated buffers or multiplexers. Thus, all of the principal peripheral and input/output functions of a microcomputer system can be implemented with this device.

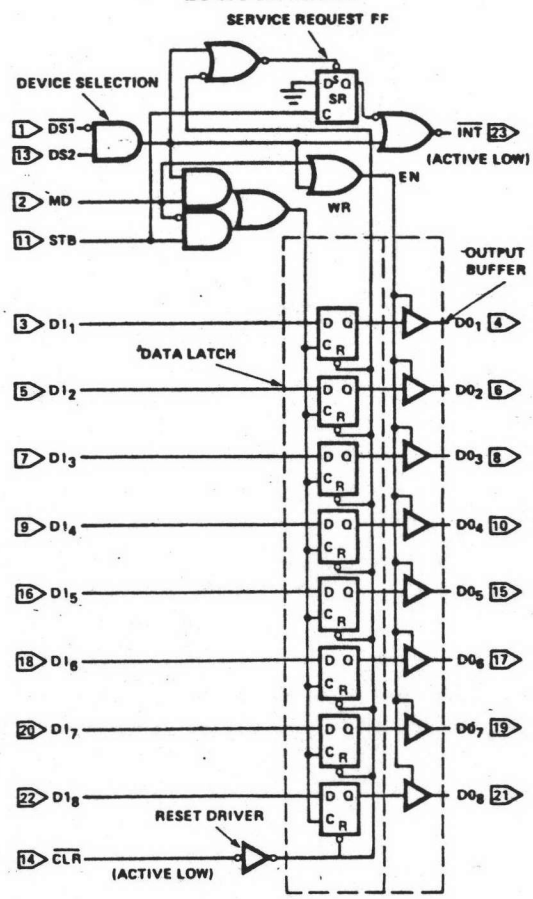
PIN CONFIGURATION



PIN NAMES

DI_1-DI_8	DATA IN
DO_1-DO_8	DATA OUT
$\overline{DS_1}$-DS_2	DEVICE SELECT
MD	MODE
STB	STROBE
$\overline{INT}$	INTERRUPT (ACTIVE LOW)
$\overline{CLR}$	CLEAR (ACTIVE LOW)

LOGIC DIAGRAM



Functional Description

Data Latch

The 8 flip-flops that make up the data latch are of a "D" type design. The output (Q) of the flip-flop will follow the data input (D) while the clock input (C) is high. Latching will occur when the clock (C) returns low.

The data latch is cleared by an asynchronous reset input ($\overline{CLR}$). (Note: Clock (C) Overides Reset ($\overline{CLR}$).)

Output Buffer

The outputs of the data latch (Q) are connected to 3-state, non-inverting output buffers. These buffers have a common control line (EN); this control line either enables the buffer to transmit the data from the outputs of the data latch (Q) or disables the buffer, forcing the output into a high impedance state. (3-state)

This high-impedance state allows the designer to connect the 8212 directly onto the microprocessor bi-directional data bus.

Control Logic

The 8212 has control inputs $\overline{DS1}$, DS2, MD and STB. These inputs are used to control device selection, data latching, output buffer state and service request flip-flop.

$\overline{DS1}$, DS2 (Device Select)

These 2 inputs are used for device selection. When $\overline{DS1}$ is low and DS2 is high ($\overline{DS1} \cdot DS2$) the device is selected. In the selected state the output buffer is enabled and the service request flip-flop (SR) is asynchronously set.

MD (Mode)

This input is used to control the state of the output buffer and to determine the source of the clock input (C) to the data latch.

When MD is high (output mode) the output buffers are enabled and the source of clock (C) to the data latch is from the device selection logic ($\overline{DS1} \cdot DS2$)

When MD is low (input mode) the output buffer state is determined by the device selection logic ($\overline{DS1} \cdot DS2$) and the source of clock (C) to the data latch is the STB (Strobe) input.

STB (Strobe)

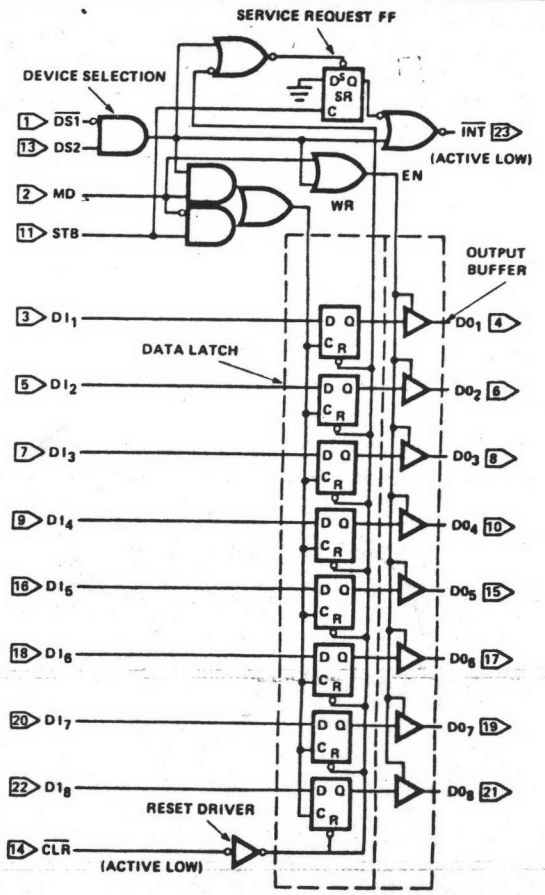
This input is used as the clock (C) to the data latch for the input mode MD = 0) and to synchronously reset the service request flip-flop (SR).

Note that the SR flip-flop is negative edge triggered.

Service Request Flip-Flop

The (SR) flip-flop is used to generate and control interrupts in microcomputer systems. It is asynchronously set by the $\overline{CLR}$ input (active low). When the (SR) flip-flop is set it is in the non-interrupting state.

The output of the (SR) flip-flop (Q) is connected to an inverting input of a "NOR" gate. The other input to the "NOR" gate is non-inverting and is connected to the device selection logic ($\overline{DS1} \cdot DS2$). The output of the "NOR" gate ($\overline{INT}$) is active low (interrupting state) for connection to active low input priority generating circuits.



STB	MD	($\overline{DS_1}$·DS_2)	DATA OUT EQUALS
0	0	0	3-STATE
1	0	0	3-STATE
0	1	0	DATA LATCH
1	1	0	DATA LATCH
0	0	1	DATA LATCH
1	0	1	DATA IN
0	1	1	DATA IN
1	1	1	DATA IN

CLR	($\overline{DS_1}$·DS_2)	STB	*SR	INT
0	0	0	1	1
0	1	0	1	1
1	1	↓	0	0
1	1	0	1	1
1	0	0	1	1
1	1	↓	1	0

*INTERNAL SR FLIP-FLOP

$\overline{CLR}$ – RESETS DATA LATCH
SETS SR FLIP-FLOP
(NO EFFECT ON OUTPUT BUFFER)

Absolute Maximum Ratings*

Temperature Under Bias Plastic . . −65°C to +75°C
Storage Temperature . . . . . −65°C to +160°C
All Output or Supply Voltages . . . . −0.5 to +7 Volts
All Input Voltages . . . . . −1.0 to 5.5 Volts
Output Currents . . . . . 125 mA

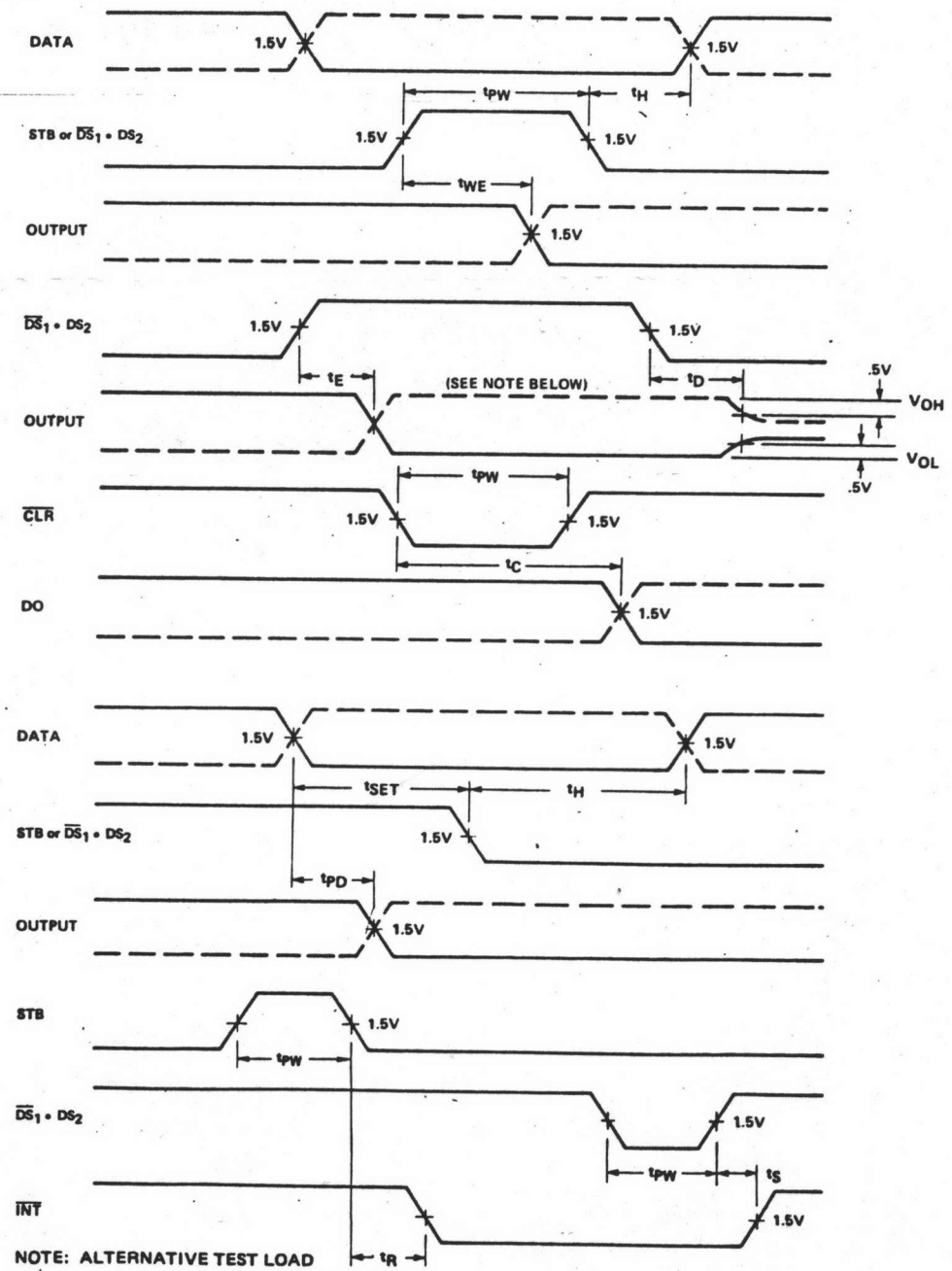
*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

D.C. Characteristics

T_A = 0°C to +75°C V_{CC} = +5V ±5%

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.	Max.		
I_F	Input Load Current ACK, DS_2, CR, DI_1-DI_8 Inputs			−.25	mA	V_F = .45V
I_F	Input Load Current MD Input			−.75	mA	V_F = .45V
I_F	Input Load Current DS_1 Input			−1.0	mA	V_F = .45V
I_R	Input Leakage Current ACK, DS, CR, DI_1-DI_8 Inputs			10	μA	V_R = 5.25V
I_R	Input Leakage Current MO Input			30	μA	V_R = 5.25V
I_R	Input Leakage Current DS_1 Input			40	μA	V_R = 5.25V
V_C	Input Forward Voltage Clamp			−1	V	I_C = −5 mA
V_{IL}	Input "Low" Voltage			.85	V	
V_{IH}	Input "High" Voltage	2.0			V	
V_{OL}	Output "Low" Voltage			.45	V	I_{OL} = 15 mA
V_{OH}	Output "High" Voltage	3.65	4.0		V	I_{OH} = −1 mA
I_{SC}	Short Circuit Output Current	-15		-75	mA	V_O = 0 V
$\|I_O\|$	Output Leakage Current High Impedance State			20	μA	V_O = .45V/5.25V
I_{CC}	Power Supply Current		90	130	mA	

Timing Diagram



intel Silicon Gate MOS 8255

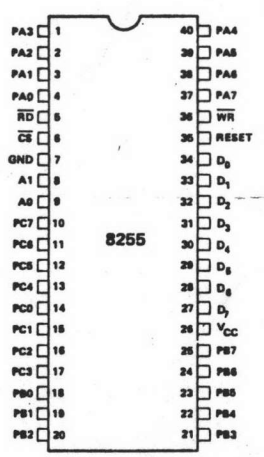
PROGRAMMABLE PERIPHERAL INTERFACE

- 24 Programmable I/O Pins
- Completely TTL Compatible
- Fully Compatible with MCS™-8 and MCS™-80 Microprocessor Families
- Direct Bit Set/Reset Capability Easing Control Application Interface
- 40 Pin Dual In-Line Package
- Reduces System Package Count

The 8255 is a general purpose programmable I/O device designed for use with both the 8008 and 8080 microprocessors. It has 24 I/O pins which may be individually programmed in two groups of twelve and used in three major modes of operation. In the first mode (Mode 0), each group of twelve I/O pins may be programmed in sets of 4 to be input or output. In Mode 1, the second mode, each group may be programmed to have 8 lines of input or output. Of the remaining four pins three are used for handshaking and interrupt control signals. The third mode of operation (Mode 2) is a Bidirectional Bus mode which uses 8 lines for a bidirectional bus, and five lines, borrowing one from the other group, for handshaking.

Other features of the 8255 include bit set and reset capability and the ability to source 1mA of current at 1.5 volts. This allows darlington transistors to be directly driven for applications such as printers and high voltage displays.

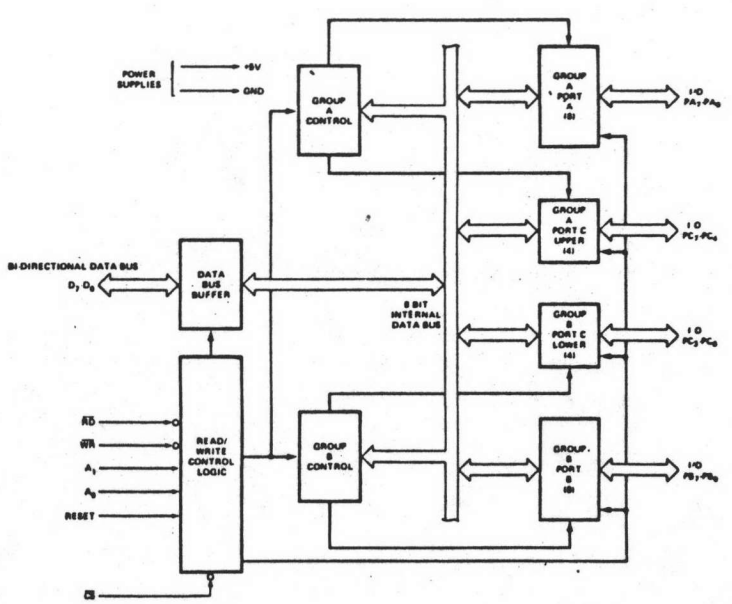
PIN CONFIGURATION



PIN NAMES

D_7–D_0	DATA BUS (BI-DIRECTIONAL)
RESET	RESET INPUT
$\overline{CS}$	CHIP SELECT
$\overline{RD}$	READ INPUT
$\overline{WR}$	WRITE INPUT
A0, A1	PORT ADDRESS
PA7-PA0	PORT A (BIT)
PB7-PB0	PORT B (BIT)
PC7-PC0	PORT C (BIT)
V_{CC}	+5 VOLTS
GND	0 VOLTS

8255 BLOCK DIAGRAM



8255 BASIC FUNCTIONAL DESCRIPTION

General

The 8255 is a Programmable Peripheral Interface (PPI) device designed for use in 8080 Microcomputer Systems. Its function is that of a general purpose I/O component to interface peripheral equipment to the 8080 system bus. The functional configuration of the 8255 is programmed by the system software so that normally no external logic is necessary to interface peripheral devices or structures.

Data Bus Buffer

This 3-state, bi-directional, eight bit buffer is used to interface the 8255 to the 8080 system data bus. Data is transmitted or received by the buffer upon execution of INput or OUTput instructions by the 8080 CPU. Control Words and Status information are also transferred through the Data Bus buffer.

Read/Write and Control Logic

The function of this block is to manage all of the internal and external transfers of both Data and Control or Status words. It accepts inputs from the 8080 CPU Address and Control busses and in turn, issues commands to both of the Control Groups.

($\overline{CS}$)

Chip Select: A "low" on this input pin enables the communication between the 8255 and the 8080 CPU.

($\overline{RD}$)

Read: A "low" on this input pin enables the 8255 to send the Data or Status information to the 8080 CPU on the Data Bus. In essence, it allows the 8080 CPU to "read from" the 8255.

($\overline{WR}$)

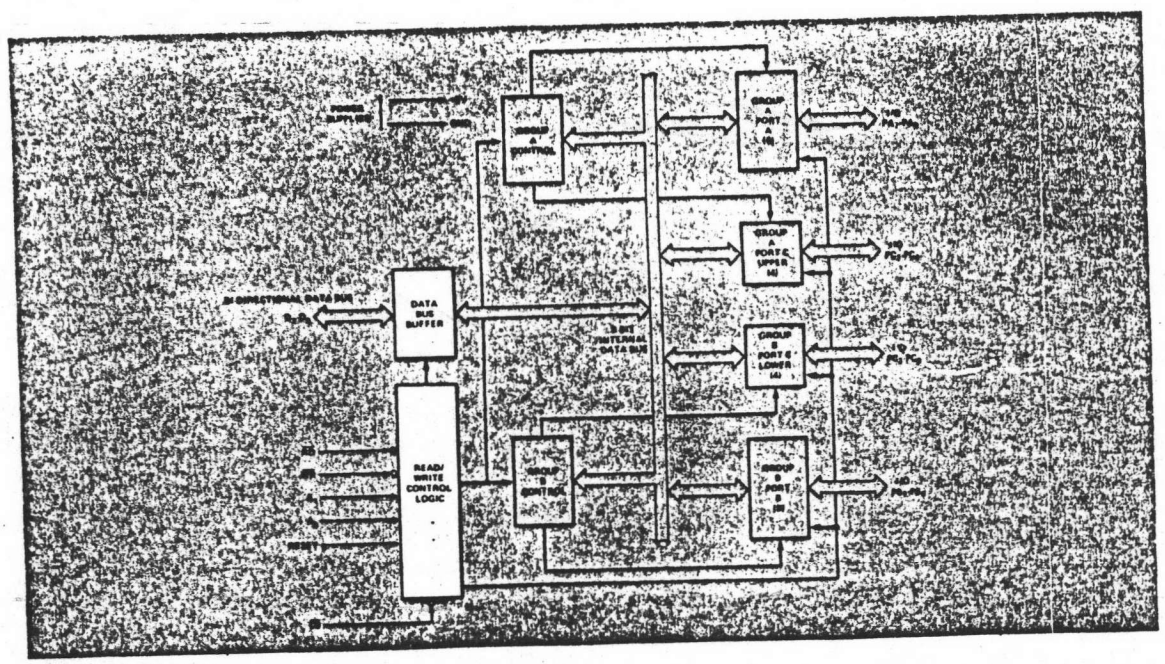
Write: A "low" on this input pin enables the 8080 CPU to write Data or Control words into the 8255.

(A_0 and A_1)

Port Select 0 and Port Select 1: These input signals, in conjunction with the $\overline{RD}$ and $\overline{WR}$ inputs, control the selection of one of the three ports or the Control Word Register. They are normally connected to the least significant bits of the Address Bus (A_0 and A_1).

8255 BASIC OPERATION

A_1	A_0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	INPUT OPERATION (READ)
0	0	0	1	0	PORT A → DATA BUS
0	1	0	1	0	PORT B → DATA BUS
1	0	0	1	0	PORT C → DATA BUS
					OUTPUT OPERATION (WRITE)
0	0	1	0	0	DATA BUS → PORT A
0	1	1	0	0	DATA BUS → PORT B
1	0	1	0	0	DATA BUS → PORT C
1	1	1	0	0	DATA BUS → CONTROL
					DISABLE FUNCTION
X	X	X	X	1	DATA BUS → 3-STATE
1	1	0	1	0	ILLEGAL CONDITION



8255 Block Diagram

SILICON GATE MOS 8255

(RESET)

Reset: A "high" on this input clears all internal registers including the Control Register and all ports (A, B, C) are set to the input mode.

Group A and Group B Controls

The functional configuration of each port is programmed by the systems software. In essence, the 8080 CPU "outputs" a control word to the 8255. The control word contains information such as "mode", "bit set", "bit reset" etc. that initializes the functional configuration of the 8255.

Each of the Control blocks (Group A and Group B) accepts "commands" from the Read/Write Control Logic, receives "control words" from the internal data bus and issues the proper commands to its associated ports.

Control Group A – Port A and Port C upper (C7-C4)
Control Group B – Port B and Port C lower (C3-C0)

The Control Word Register can Only be written into. No Read operation of the Control Word Register is allowed.

Ports A, B, and C

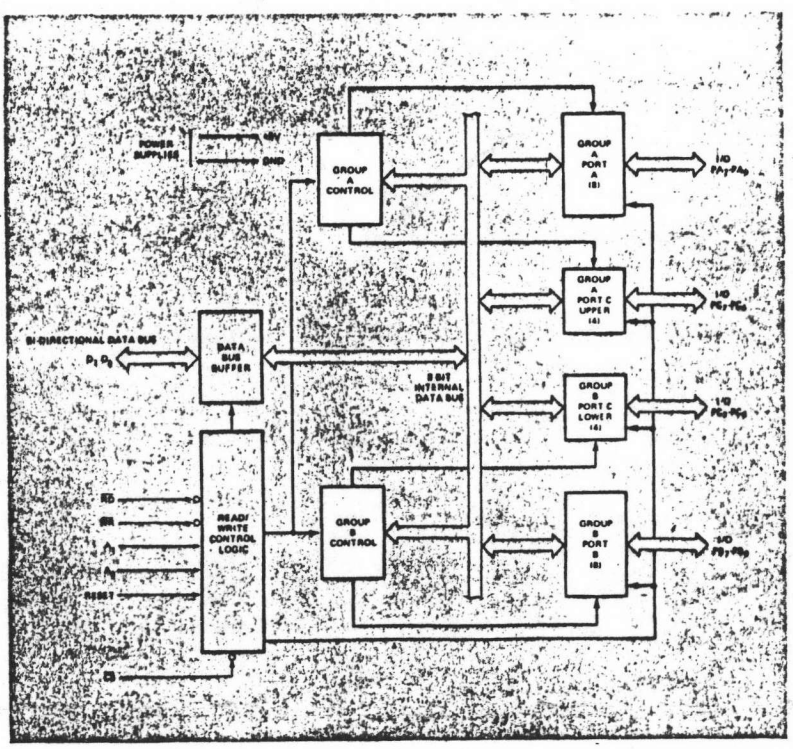
The 8255 contains three 8-bit ports (A, B, and C). All can be configured in a wide variety of functional characteristics by the system software but each has its own special features or "personality" to further enhance the power and flexibility of the 8255.

Port A: One 8-bit data output latch/buffer and one 8-bit data input latch.

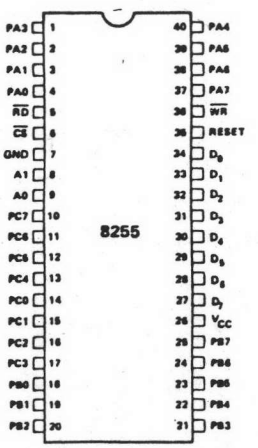
Port B: One 8-bit data input/output latch/buffer and one 8-bit data input buffer.

Port C: One 8-bit data output latch/buffer and one 8-bit data input buffer (no latch for input). This port can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and it can be used for the control signal outputs and status signal inputs in conjunction with Ports A and B.

8255 BLOCK DIAGRAM



PIN CONFIGURATION



PIN NAMES

D_7–D_0	DATA BUS (BI-DIRECTIONAL)
RESET	RESET INPUT
$\overline{CS}$	CHIP SELECT
$\overline{RD}$	READ INPUT
$\overline{WR}$	WRITE INPUT
A0, A1	PORT ADDRESS
PA7-PA0	PORT A (BIT)
PB7-PB0	PORT B (BIT)
PC7-PC0	PORT C (BIT)
V_{CC}	+5 VOLTS
GND	0 VOLTS

8255 DETAILED OPERATIONAL DESCRIPTION

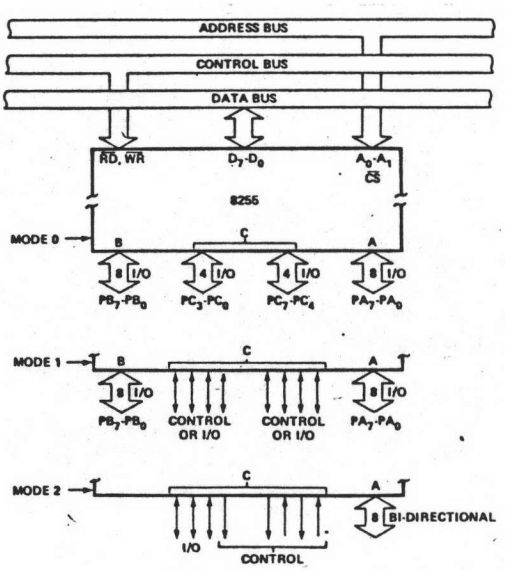
Mode Selection

There are three basic modes of operation that can be selected by the system software:

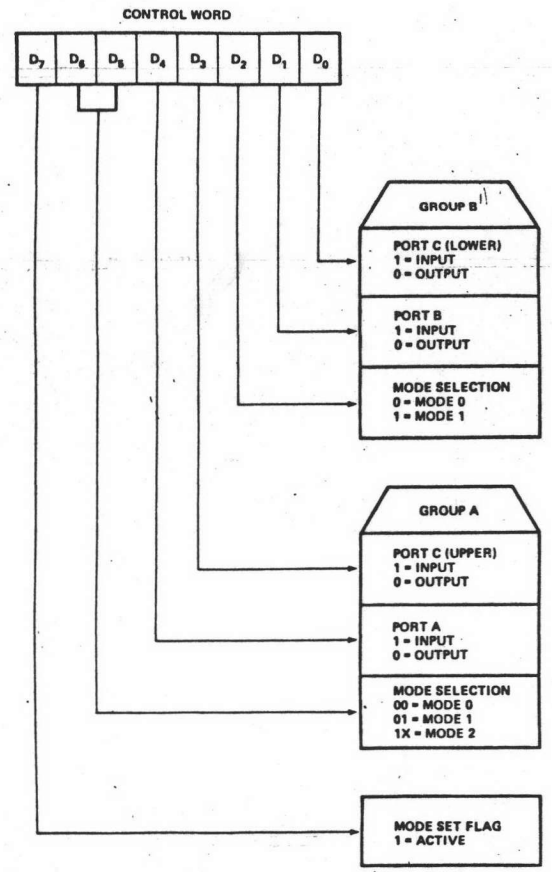
Mode 0 — Basic Input/Output
Mode 1 — Strobed Input/Output
Mode 2 — Bi-Directional Bus

When the RESET input goes "high" all ports will be set to the Input mode (i.e., all 24 lines will be in the high impedance state). After the RESET is removed the 8255 can remain in the Input mode with no additional initialization required. During the execution of the system program any of the other modes may be selected using a single OUTput instruction. This allows a single 8255 to service a variety of peripheral devices with a simple software maintenance routine.

The modes for Port A and Port B can be separately defined, while Port C is divided into two portions as required by the Port A and Port B definitions. All of the output registers, including the status flip-flops, will be reset whenever the mode is changed. Modes may be combined so that their functional definition can be "tailored" to almost any I/O structure. For instance; Group B can be programmed in Mode 0 to monitor simple switch closings or display computational results, Group A could be programmed in Mode 1 to monitor a keyboard or tape reader on an interrupt-driven basis.



Basic Mode Definitions and Bus Interface

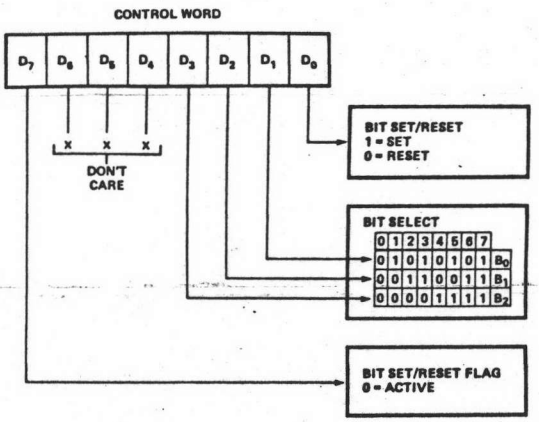


Mode Definition Format

The Mode definitions and possible Mode combinations may seem confusing at first but after a cursory review of the complete device operation a simple, logical I/O approach will surface. The design of the 8255 has taken into account things such as efficient PC board layout, control signal definition vs PC layout and complete functional flexibility to support almost any peripheral device with no external logic. Such design represents the maximum use of the available pins.

Single Bit Set/Reset Feature

Any of the eight bits of Port C can be Set or Reset using a single OUTput instruction. This feature reduces software requirements in Control-based applications.



Bit Set/Reset Format

When Port C is being used as status/control for Port A or B, these bits can be set or reset by using the Bit Set/Reset operation just as if they were data output ports.

Interrupt Control Functions

When the 8255 is programmed to operate in Mode 1 or Mode 2, control signals are provided that can be used as interrupt request inputs to the CPU. The interrupt request signals, generated from Port C, can be inhibited or enabled by setting or resetting the associated INTE flip-flop, using the Bit set/reset function of Port C.

This function allows the Programmer to disallow or allow a specific I/O device to interrupt the CPU without effecting any other device in the interrupt structure.

INTE flip-flop definition:

(BIT-SET) — INTE is SET — Interrupt enable
(BIT-RESET) — INTE is RESET — Interrupt disable

Note: All Mask flip-flops are automatically reset during mode selection and device Reset.

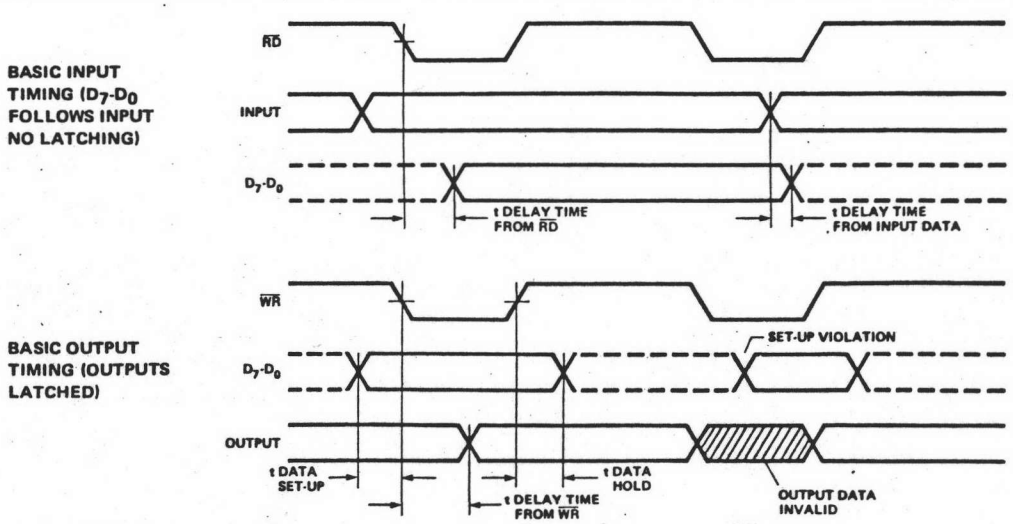
Operating Modes

Mode 0 (Basic Input/Output)

This functional configuration provides simple Input and Output operations for each of the three ports. No "handshaking" is required, data is simply written to or read from a specified port.

Mode 0 Basic Functional Definitions:

- Two 8-bit ports and two 4-bit ports.
- Any port can be input or output.
- Outputs are latched.
- Inputs are not latched.
- 16 different Input/Output configurations are possible in this Mode.



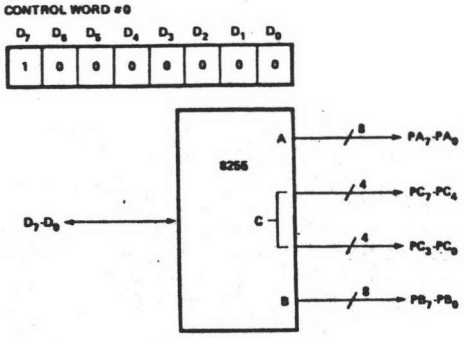
Mode 0 Timing

MODE 0 PORT DEFINITION CHART

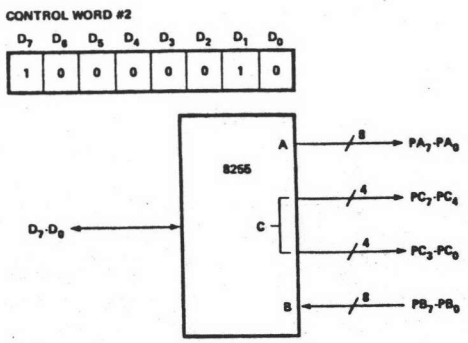
A		B		GROUP A			GROUP B	
D_4	D_3	D_1	D_0	PORT A	PORT C (UPPER)	#	PORT B	PORT C (LOWER)
0	0	0	0	OUTPUT	OUTPUT	0	OUTPUT	OUTPUT
0	0	0	1	OUTPUT	OUTPUT	1	OUTPUT	INPUT
0	0	1	0	OUTPUT	OUTPUT	2	INPUT	OUTPUT
0	0	1	1	OUTPUT	OUTPUT	3	INPUT	INPUT
0	1	0	0	OUTPUT	INPUT	4	OUTPUT	OUTPUT
0	1	0	1	OUTPUT	INPUT	5	OUTPUT	INPUT
0	1	1	0	OUTPUT	INPUT	6	INPUT	OUTPUT
0	1	1	1	OUTPUT	INPUT	7	INPUT	INPUT
1	0	0	0	INPUT	OUTPUT	8	OUTPUT	OUTPUT
1	0	0	1	INPUT	OUTPUT	9	OUTPUT	INPUT
1	0	1	0	INPUT	OUTPUT	10	INPUT	OUTPUT
1	0	1	1	INPUT	OUTPUT	11	INPUT	INPUT
1	1	0	0	INPUT	INPUT	12	OUTPUT	OUTPUT
1	1	0	1	INPUT	INPUT	13	OUTPUT	INPUT
1	1	1	0	INPUT	INPUT	14	INPUT	OUTPUT
1	1	1	1	INPUT	INPUT	15	INPUT	INPUT

MODE 0 CONFIGURATIONS

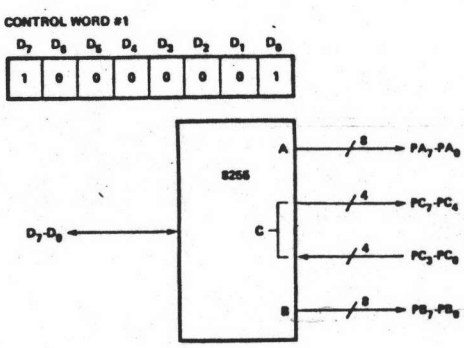
CONTROL WORD #0



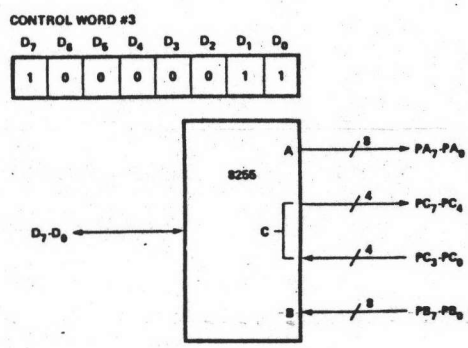
CONTROL WORD #2



CONTROL WORD #1

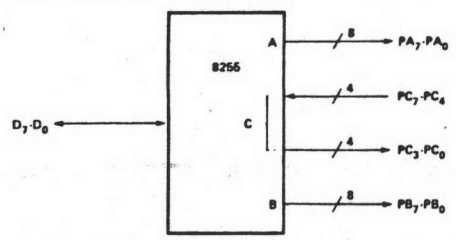


CONTROL WORD #3



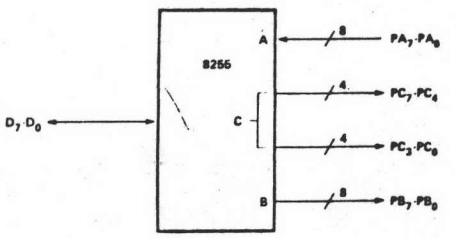
CONTROL WORD #4

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	1	0	0	0



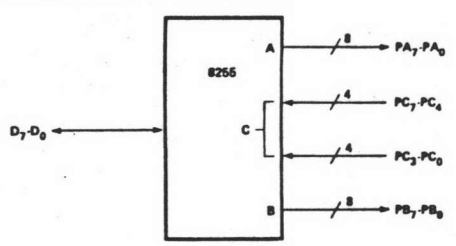
CONTROL WORD #8

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	0	0	0	0



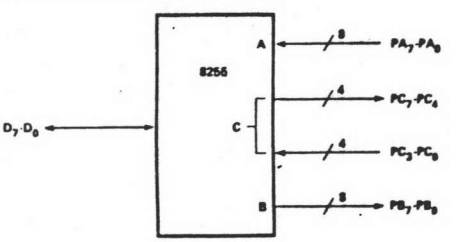
CONTROL WORD #5

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	1	0	0	1



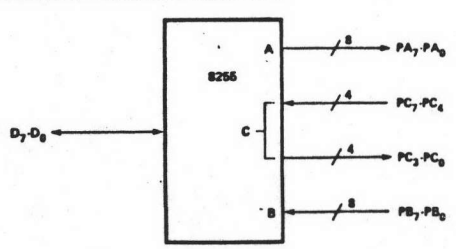
CONTROL WORD #9

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	0	0	0	1



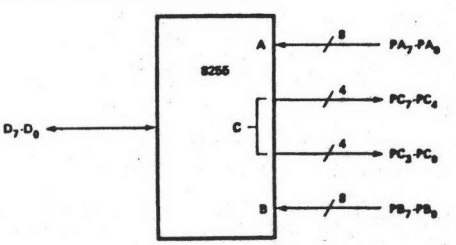
CONTROL WORD #6

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	1	0	1	0



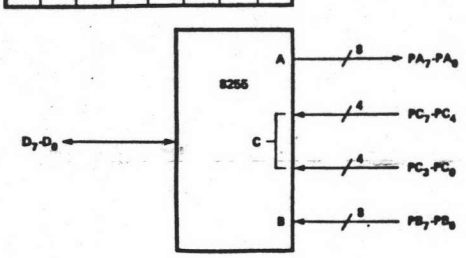
CONTROL WORD #10

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	0	0	1	0



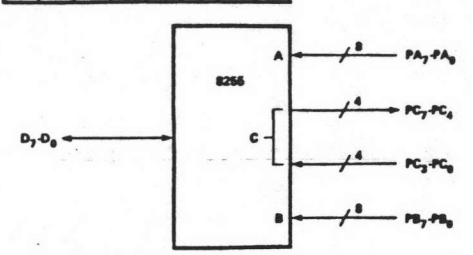
CONTROL WORD #7

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	1	0	1	1



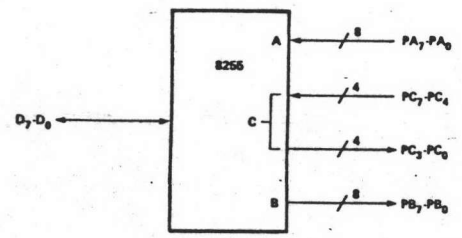
CONTROL WORD #11

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	0	0	1	1



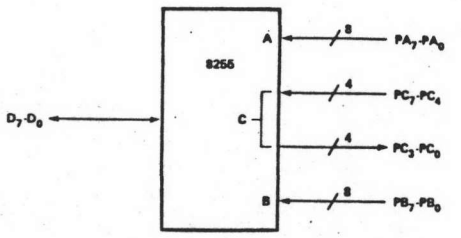
CONTROL WORD #12

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	1	0	0	0



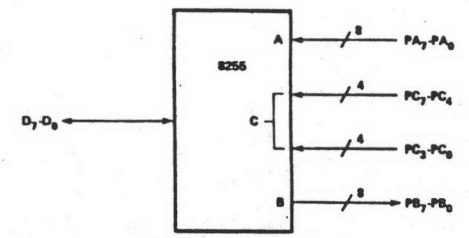
CONTROL WORD #14

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	1	0	1	0



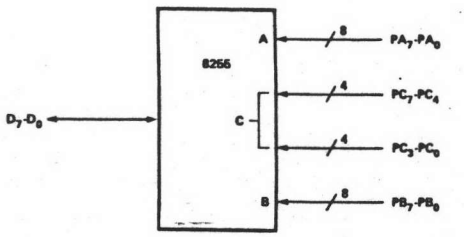
CONTROL WORD #13

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	1	0	0	1



CONTROL WORD #15

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	1	0	1	1



Operating Modes

Mode 1 (Strobed Input/Output)

This functional configuration provides a means for transferring I/O data to or from a specified port in conjunction with strobes or "handshaking" signals. In Mode 1, Port A and Port B use the lines on Port C to generate or accept these "handshaking" signals.

Mode 1 Basic Functional Definitions:

- Two Groups (Group A and Group B)
- Each group contains one 8-bit data port and one 4-bit control/data port.
- The 8-bit data port can be either input or output. Both inputs and outputs are latched.
- The 4-bit port is used for control and status of the 8-bit data port.

Input Control Signal Definition

$\overline{STB}$ (Strobe Input)

A "low" on this input loads data into the input latch.

IBF (Input Buffer Full F/F)

A "high" on this output indicates that the data has been loaded into the input latch; in essence, an acknowledgement. IBF is set by the falling edge of the STB input and is reset by the rising edge of the RD input.

INTR (Interrupt Request)

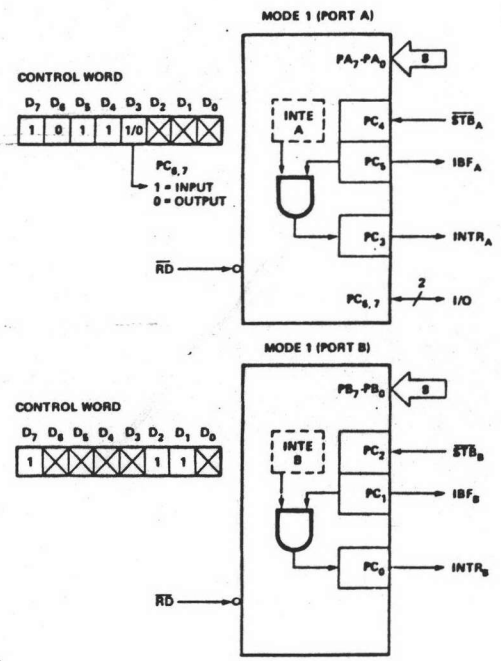
A "high" on this output can be used to interrupt the CPU when an input device is requesting service. INTR is set by the rising edge of $\overline{STB}$ if IBF is a "one" and INTE is a "one". It is reset by the falling edge of $\overline{RD}$. This procedure allows an input device to request service from the CPU by simply strobing its data into the port.

INTE A

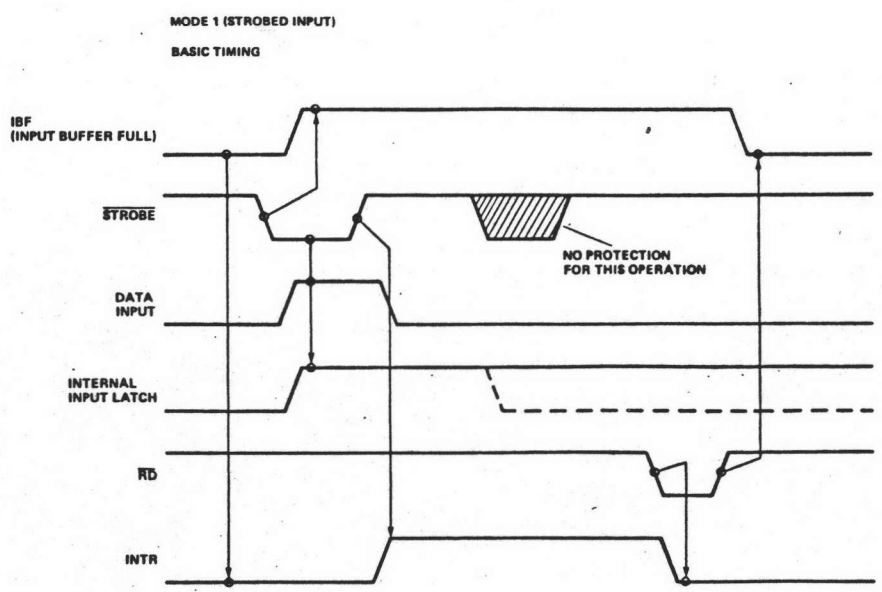
Controlled by bit set/reset of PC_4.

INTE B

Controlled by bit set/reset of PC_2.



Mode 1 Input



Basic Timing Input

Output Control Signal Definition

$\overline{OBF}$ (Output Buffer Full F/F)

The $\overline{OBF}$ output will go "low" to indicate that the CPU has written data out to the specified port. The OBF F/F will be set by the rising edge of the WR input and reset by the falling edge of the $\overline{ACK}$ input signal.

$\overline{ACK}$ (Acknowledge Input)

A "low" on this input informs the 8255 that the data from Port A or Port B has been accepted. In essence, a response from the peripheral device indicating that it has received the data output by the CPU.

INTR (Interrupt Request)

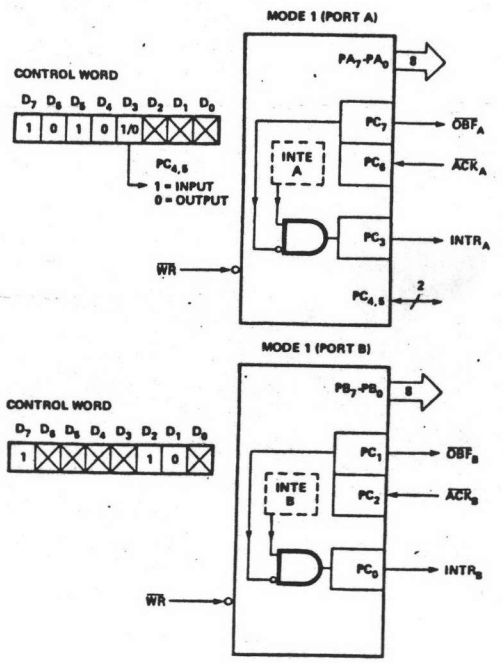
A "high" on this output can be used to interrupt the CPU when an output device has accepted data transmitted by the CPU. INTR is set by the rising edge of $\overline{ACK}$ if $\overline{OBF}$ is a "one" and INTE is a "one". It is reset by the falling edge of $\overline{WR}$.

INTE A

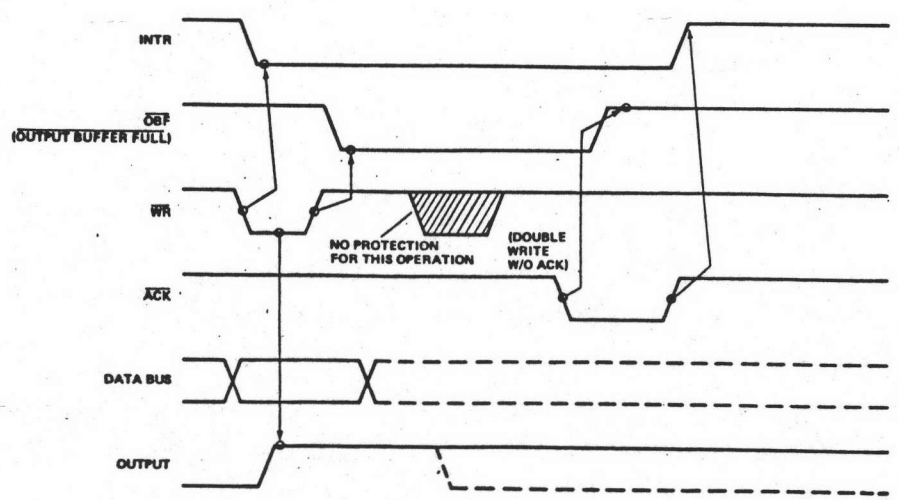
Controlled by bit set/reset of PC_6.

INTE B

Controlled by bit set/reset of PC_2.



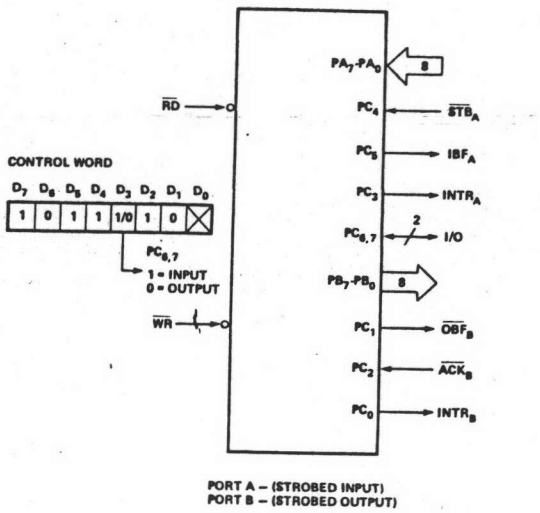
Mode 1 Output

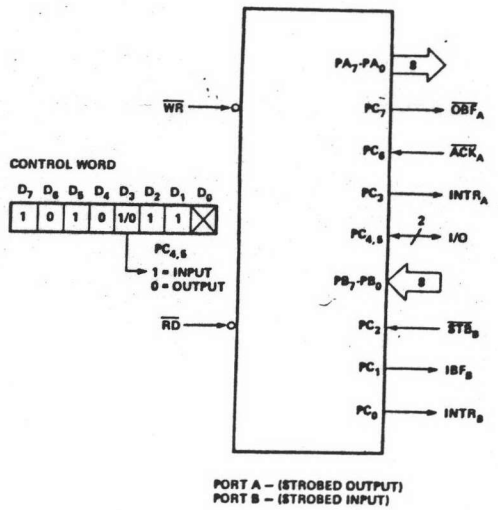


Basic Timing Output

Combinations of Mode 1

Port A and Port B can be individually defined as input or output in Mode 1 to support a wide variety of strobed I/O applications.





Operating Modes

Mode 2 (Strobed Bi-Directional Bus I/O)

This functional configuration provides a means for communicating with a peripheral device or structure on a single 8-bit bus for both transmitting and receiving data (bi-directional bus I/O). "Handshaking" signals are provided to maintain proper bus flow discipline in a similar manner to Mode 1. Interrupt generation and enable/disable functions are also available.

Mode 2 Basic Functional Definitions:

- Used in Group A only.
- One 8-bit, bi-directional bus Port (Port A) and a 5-bit control Port (Port C).
- Both inputs and outputs are latched.
- The 5-bit control port (Port C) is used for control and status for the 8-bit, bi-directional bus port (Port A).

Bi-Directional Bus I/O Control Signal Definition

INTR (Interrupt Request)

A high on this output can be used to interrupt the CPU for both input or output operations.

Output Operations

$\overline{OBF}$ (Output Buffer Full)

The $\overline{OBF}$ output will go "low" to indicate that the CPU has written data out to Port A.

$\overline{ACK}$ (Acknowledge)

A "low" on this input enables the tri-state output buffer of Port A to send out the data. Otherwise, the output buffer will be in the high-impedance state.

INTE 1 (The INTE Flip-Flop associated with $\overline{OBF}$)

Controlled by bit set/reset of PC_6.

Input Operations

$\overline{STB}$ (Strobe Input)

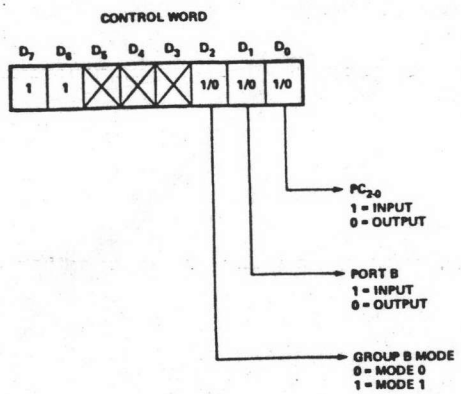
A "low" on this input loads data into the input latch.

IBF (Input Buffer Full F/F)

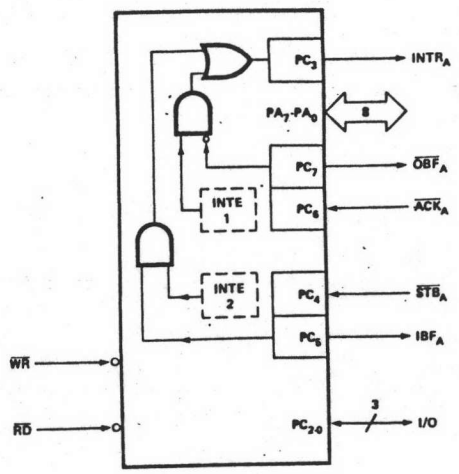
A "high" on this output indicates that data has been loaded into the input latch.

INTE 2 (The INTE Flip-Flop associated with IBF)

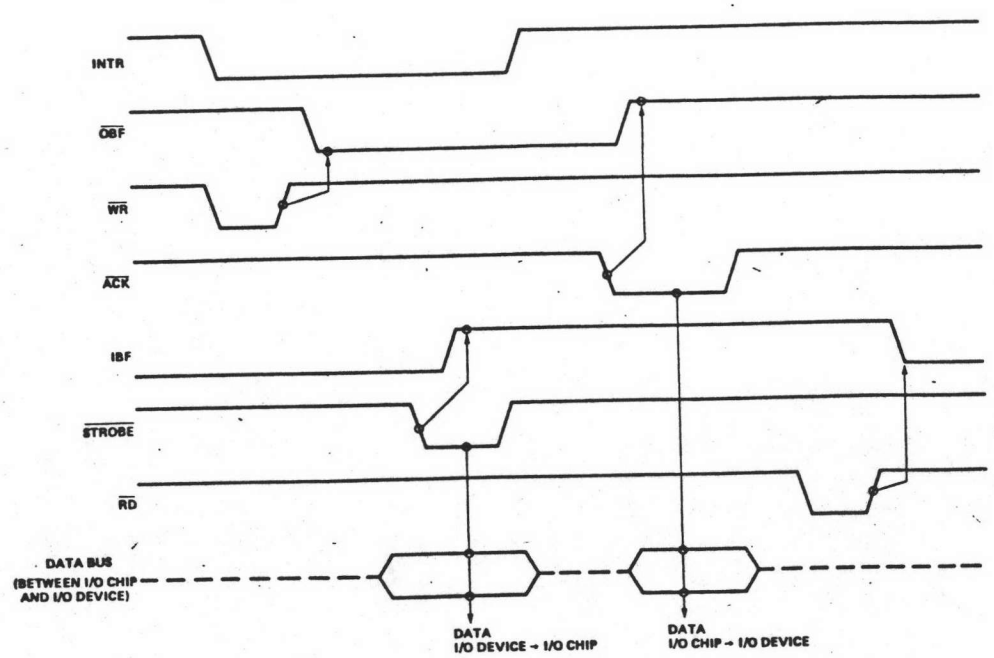
Controlled by bit set/reset of PC_4.



Mode 2 Control Word

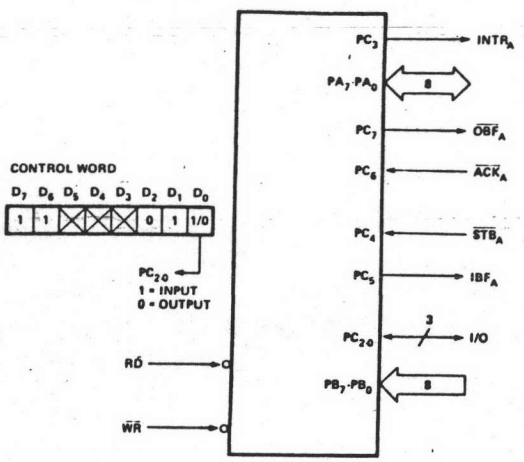


Mode 2

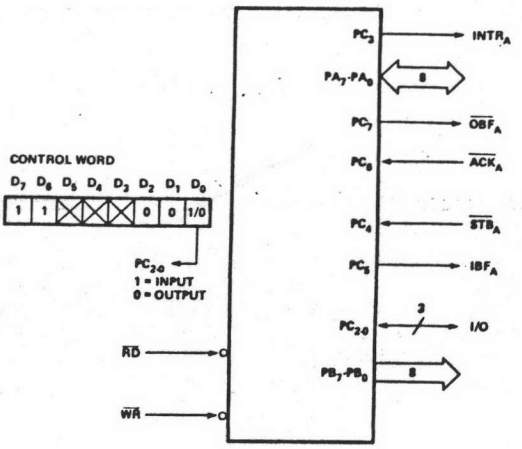


Mode 2 (Bi-directional) Timing

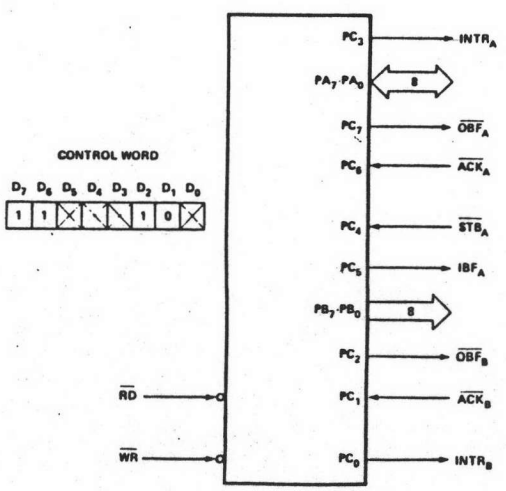
MODE 2 AND MODE 0 (INPUT)



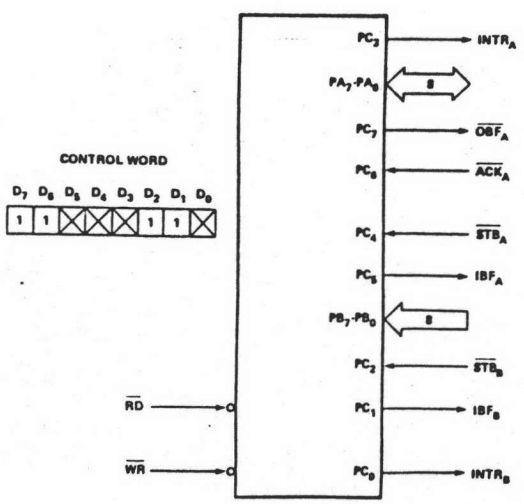
MODE 2 AND MODE 0 (OUTPUT)



MODE 2 AND MODE 1 (OUTPUT)



MODE 2 AND MODE 1 (INPUT)



Mode 2 Combinations

Series 54/74

DM54155/DM74155(SN54155/SN74155)
DM54156/DM74156(SN54156/SN74156)
dual 2:4 demultiplexers

general description

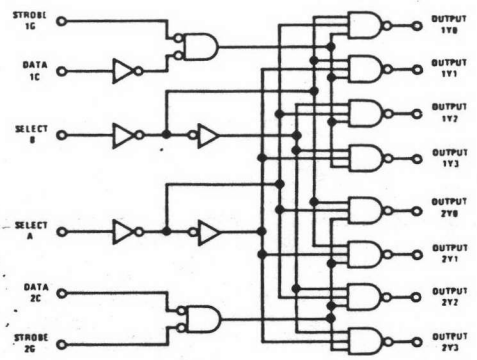
The DM54155/DM74155 and DM54156/DM74156 are monolithic transistor-transistor-logic (TTL) circuits featuring dual 1 line-to-4-line demultiplexers with individual strobes and common binary-address inputs in a single 16-pin package. When both sections are enabled by the strobes, the common binary-address inputs sequentially select and route associated input data to the appropriate output of each section. The individual strobes permit activating or inhibiting each of the 4-bit sections as desired. Data applied to input 1C is inverted at its outputs and data applied at 2C is not inverted through its outputs. The inverter following the 1C data input permits use as a 3-to-8 line decoder or 1-to-8-line demultiplexer without external gating. See the truth tables for more details.

The DM54155/DM74155 has normal TTL "totem-pole" outputs. The DM54156/DM74156 has open collector outputs, but is otherwise identical to the DM54155/DM74155.

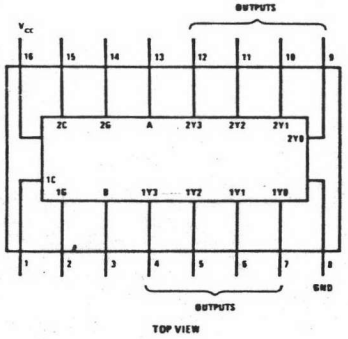
features

- 125 mW typical power dissipation
- 17 ns typical propagation delay for the DM54155/DM74155, 18 ns for the DM54156/DM74156
- Pin compatible with SN54155/SN74155 and SN54156/SN74156

logic and connection diagrams



Dual-In-Line and Flat Package



truth tables

2-LINE-TO-4-LINE DECODER OR 1-LINE-TO-4-LINE DEMULTIPLEXER

INPUTS				OUTPUTS			
SELECT		STROBE	DATA				
B	A	1G	1C	1Y0	1Y1	1Y2	1Y3
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

INPUTS				OUTPUTS			
SELECT		STROBE	DATA				
B	A	2G	2C	2Y0	2Y1	2Y2	2Y3
X	X	H	X	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

3-LINE-TO-8-LINE DECODER TO 1-LINE-TO-8-LINE DEMULTIPLEXER

INPUTS				OUTPUTS							
SELECT			STROBE OR DATA	(0)	(1)	(2)	(3)	(4)	(5)	(6)	(7)
C†	B	A	G‡	2Y0	2Y1	2Y2	2Y3	1Y0	1Y1	1Y2	1Y3
X	X	X	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
H	H	L	L	H	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	H	L

†C = inputs 1C and 2C connected together

‡G = inputs 1G and 2G connected together

Series 54/74

DM5404/DM7404(SN5404/SN7404) hex inverter

general description

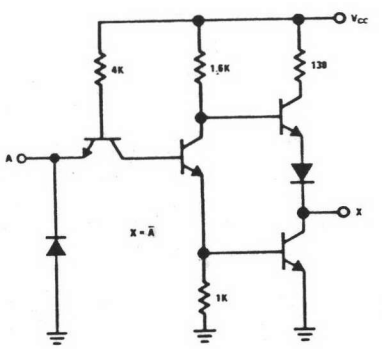
The DM5404/DM7404 is a hex inverter utilizing TTL to achieve high speed at nominal power dissipation. It is totally compatible with other Series 54/74 devices.

features

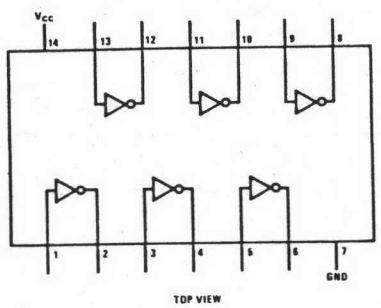
- Input clamping diodes
- Typical Noise Immunity 1V
- Guaranteed Noise Immunity 400 mV
- Fan-out 10
- Allowable Power Supply Variation
  - DM5404 4.5V to 5.5V
  - DM7404 4.75V to 5.25V
- Average Propagation Delay 12 ns (with 50 pF)
- Average Power Dissipation 10 mW per gate

schematic and connection diagrams

DM5404/DM7404

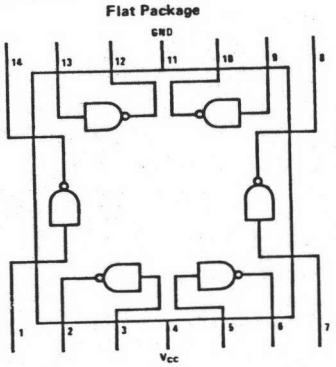


DM5404/DM7404
Dual-In-Line Package



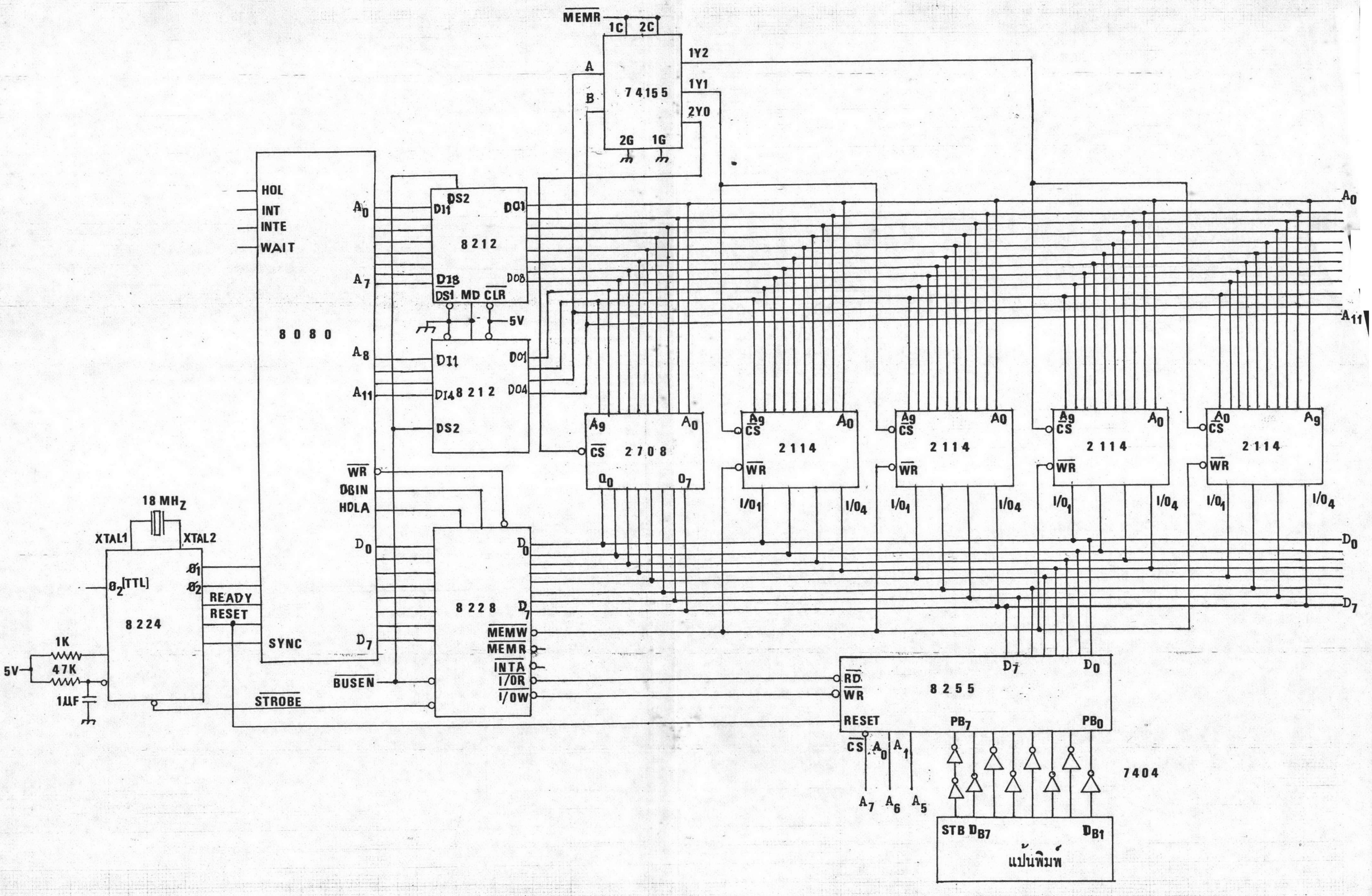
TOP VIEW

DM5404
Flat Package



TOP VIEW

ภาคผนวก ง
วงจรระบบควบคุมข้อมูล


MEMR
1C
2C
1Y2
A
1Y1
B
74155
2Y0
2G
1G
HOL
INT
INTE
WAIT
8080
A0
A7
A8
A11
DS2
DI1
DO1
8212
DI8
DO8
DS1 MD CLR
5V
DI4
DO4
WR
DBIN
HOLA
D0
D7
A9
A0
CS
2708
Q0
Q7
2114
WR
I/O1
I/O4
18 MHz
XTAL1
XTAL2
Ø1
Ø2 [TTL]
8224
READY
RESET
SYNC
1K
47K
5V
1µF
STROBE
BUSEN
8228
MEMW
MEMR
INTA
I/OR
I/OW
RD
8255
RESET
PB7
PB0
CS
A0
A1
A7
A6
A5
7404
STB
DB7
DB1
แป้นพิมพ์

ประวัติผู้เขียน

นายเมธี ศรีสังวาล เกิดวันที่ 15 พฤศจิกายน พ.ศ. 2492 ที่จังหวัดนครปฐม สำเร็จการศึกษาปริญญาครุศาสตร์อุตสาหกรรมบัณฑิต สาขาวิชาไฟฟ้า-อีเล็คโทรนิคส์ จากวิทยาลัยเทคโนโลยีและอาชีวศึกษา ปีการศึกษา 2519 ปัจจุบันรับราชการ เป็นอาจารย์ภาควิชาวิศวกรรมคอมพิวเตอร์ คณะวิศวกรรมศาสตร์ จุฬาลงกรณ์มหาวิทยาลัย