CHAPTER IV

FABRICATION OF GaAlAs / GaAs HETEROJUNCTION BIPOLAR TRANSISTOR

4.1 Epitaxy Growth

Epitaxy growth is the formation of new layers of crystalline solid materials on a well-oriented single crystal in such a manner that the new or epitaxial layer evaluates the crystalline structure of that original structure. This process can be known as in term of Epitaxy Technique. In general, the epitaxy technique can be simplified into two mechanisms such as

(1) Homoepitaxy; which has the same compositions as that of the parent substrate, for example, Si/ Si or GaAs/GaAs

(2) Heteroepitaxy; which has the different compositions as that of the parent substrate, for example, Si/GaAs or InP/InGaAsP

The epitaxial layers of the semiconductor materials can be grown in many techniques which are vapor phase epitaxy (VPE), liquid phase epitaxy (LPE), molecular beam epitaxy (MBE) and etc. Among them, LPE (Liquid Phase Epitaxy) is the simplest or useful technique for the wide variety of III-V compound semiconductor materials that it has been used in the present thesis. LPE is common thin film materials growth technique that has capable of producing reliable semiconductor or magnetic film devices. LPE technique is still popular to grow semiconducting lasers, light emitting diodes, photodetectors and transistors. The technique is quite different compared with other growth technique such as physical vapor deposition, so that it requires the composition of materials for growing formed as liquid at their melting temperature. Epitaxy layers can be thermodynamically grown on a substrate with the same orientation when the substrates meet oversaturated solution.

This LPE technique is utilizing to produce up to100 μm and even thicker high quality, near intrinsic quality, garnets, spinels, and hexaferrite as well as other new materials for planar microwave and magnetic devices. Liquid phase epitaxy (LPE) is also a method to grow semiconductor crystal layers from the melt on solid substrates. This happens at temperatures well below the melting point of the deposited semiconductor.

The semiconductor is dissolved in the melt of another material. At conditions that are close to the equilibrium between dissolution and deposition of the semiconductor crystal on the substrate is slowly and uniform. The equilibrium conditions depend very much on the temperature and on the concentration of the dissolved semiconductor in the melt. The growth of the layer from the liquid phase can be controlled by a forced cooling of the melt. Impurity introduction can be strongly reduced. Doping can be achieved by the addition of dopants.

The method is mainly used for the growth of compound semiconductors. Very thin, uniform and high quality layers can be produced. A typical example for the liquid phase epitaxy method is the growth of ternary and quaternary III-V compounds on Gallium arsenide (GaAs) substrates. As a solvent quite often Gallium is used in this case. Another frequently used substrate is Indium phosphate (InP). However other substrates like glass or ceramic can be applied for special applications. To facilitate nucleation and to avoid tension in the grown layer the thermal expansion coefficient of substrate and grown layer should be similar. TEL Thermo Systems produces equipment for liquid phase epitaxy, based either on a horizontal furnace or on a vertical furnace. The heating of the growth chamber is achieved by Light Gauge Overbend heating element. The chamber can be evacuated and an inert gas or hydrogen gas atmosphere can be established. Special sealed feed-through allow the movement of the samples or of the semiconductor melts in the chamber. In the case of a horizontal tool for liquid phase epitaxy the melt or the melts are brought in contact with the substrate(s) by a sliding boat system. When the dedicated process is finished the next melt can be brought in contact with the next substrate. This way, it is possible to grow multi-layer stacks in an easy way. Depending on the set-up of the system one or several wafer can be processed at the same time. The melt volume to substrate surface area ratio is small, and the melt needs to be refreshed after each growth experiment.

Anyway, the inferior of LPE techniques is that the difficulty to produce the ultra thin layers less than 0.1μm and control the uniformity of the layers in the direction of growth. The optoelectronics or microwave devices application of the III-V compound required that more than one layer to be grown which is using by a multibin boat, a number of solutions come sequentially contact with the substrate. It is therefore possible

to obtain the several semiconductor layers which are doped with different impurities during one growth cycle that is used for the device fabrication. In this research, we used the horizontal LPE system Fig. 4.1 and multibin graphite boat Fig. 4.2. The horizontal LPE apparatus principally consist of

(1) Programmable Temperature Controller: The accuracy of temperature stabilization is within ±0.05°C

(2) Resistance Furnace: The length of the uniform-temperature region is about 200mm and the furnace are movable over the quartz tube.

(3) Quartz Tube: 2400-mm long with inner diameter about 74-mm

(4) Gas System: Hydrogen Purifier (99.99%)

(5) Hygrometer: 0.1-ppm resolution

(6) Nitrogen Hood: This is used to protect the substrates against the effect of environment and the forming of oxides layer on the surface during the growth process.

(7) Thermocouple and Temperature Recorder: checking the temperature

(8) Graphite Boat: allows the sequential deposition of nine semiconductor layer during one growth cycle

(9) Quartz Rod: This is used to slide the substrates sequentially into the bottom of the reservoirs containing the different melting solution of Ga +As +Al

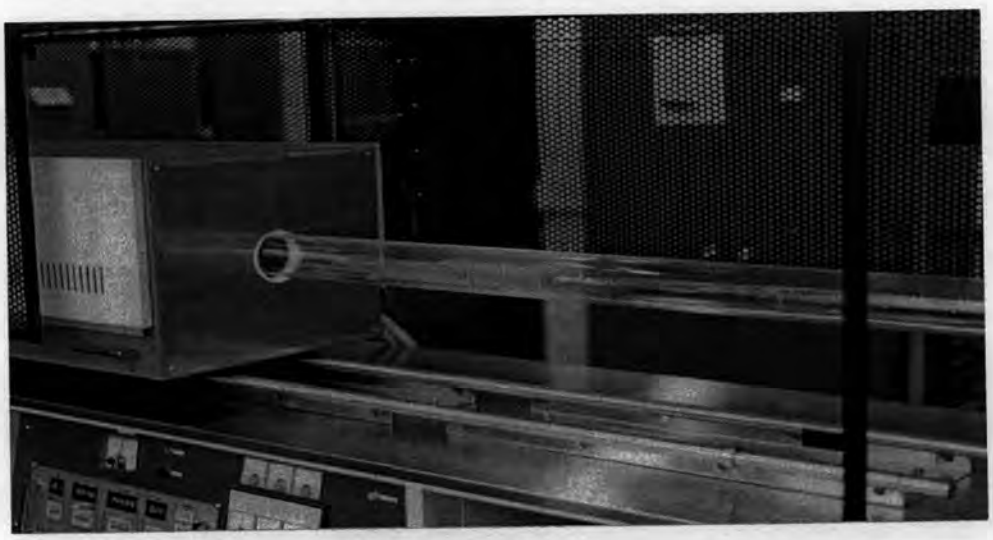

Fig. 4.1 Horizontal LPE system

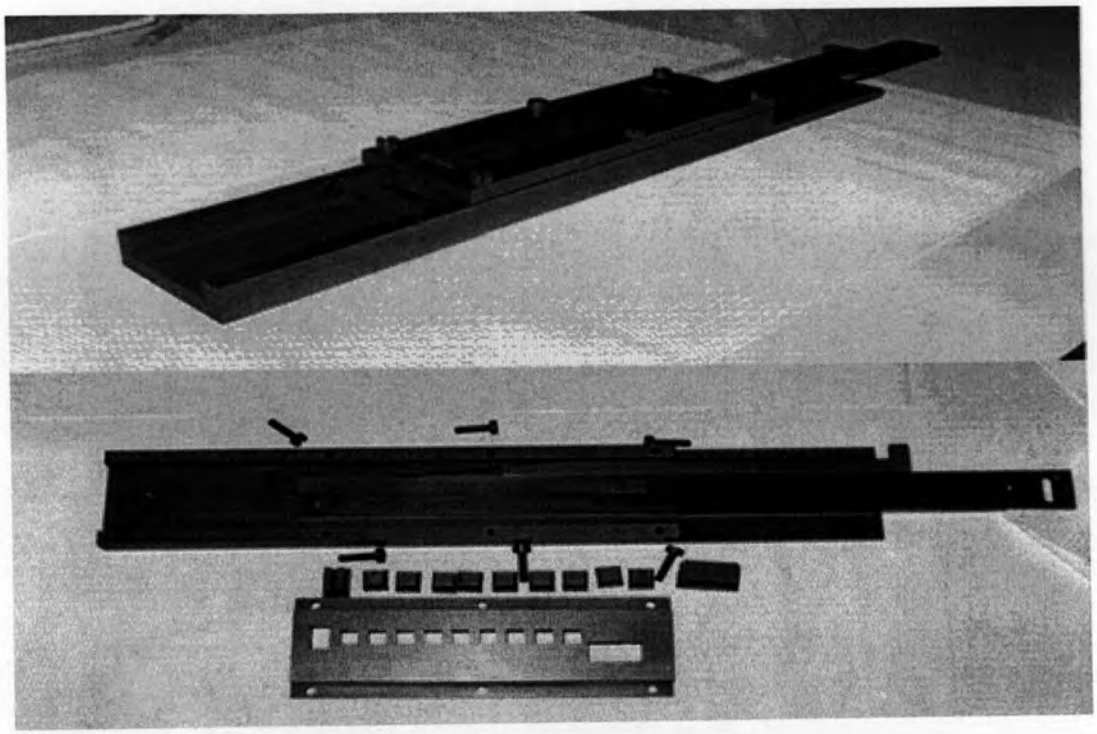

Fig. 4.2 Multibin graphite boat of the LPE system

4.2 Fabrication technique

4.2.1 Preparation of Substrate and Materials

GaAs wafer substrates and other materials such as Ga and also varieties of dopants: Ga, Zn and Sn were used to realize for Heterojunction Bipolar Transistor structure.

GaAs substrate wafers: Two different types of wafer are needed.

(1) Two of (1cm × 1cm) n-type GaAs substrate wafer doped with Si concentration about $3\text{-}5\times10^{18}$ cm^{-3} were used as the underlying substrates or parent substrates for epitaxy growth. One is the dummy and another one is the real sample.

(2) Seven of (0.5cm × 1cm) non-doped GaAs substrate wafer were used as the compensating the solution in each bin (hole) of the graphite boat.

To remove all impurities or defects on the surface of the wafers in the growth processes, the wafers are prepared by the following processes.

-Clean in diluted hydrochloric acid (HCl: H_2O-1:1) about 2-minutes

-Rinse in deionized water (DI-water)

-Blow dries with N_2 gas

Materials: In Liquid Phase Epitaxy super cooling technique, Ga is used as the solvent for As and Al in the growing of GaAs and GaAlAs epitaxial layers. Sn and Te are used as the n-type dopants whereas Ge and Zn are used as the p-type dopants. All of these materials are prepared as solids and the specific amount of materials for each designed layer can be obtained by the mass conservation relation as follow;

$$X_{Ga} + X_{As} + X_{Al} + X_{im} = 1 \tag{4.1}$$

Where, *"X"* is the mole fraction of one of the constituents containing in that compound. The proportional of the weight of Ga (W_{Ga}) and weight of As (W_{As}) can be written as

$$W_{As} = (X_{As} / X_{Ga})\,(M_{As} / M_{Ga}) \times W_{Ga} \tag{4.2}$$

$$W_{AL} = (X_{Al} / X_{Ga})\,(M_{Al} / M_{Ga}) \times W_{Ga} \tag{4.3}$$

Where, *"M" is the atomic weight of each element.* And the weight of impurities dopants (W_{im}) is given by,

$$W_{im} = (X_{im} / X_{Ga})\,(M_{im} / M_{Ga}) \times W_{Ga} \tag{4.4}$$

Since, Arsenic has to be extracted from GaAs substrate, therefore the weight of GaAs (W_{GaAs}) is

$$W_{GaAs} = (X_{As} / X_{Ga})\,(M_{GaAs} / M_{Ga}) \times W_{Ga} \qquad (4.5)$$

Where, $M_{Ga} = 69.72$, $M_{As} = 74.92$

$M_{Al} = 26.98$, $M_{Ge} = 72.59$

$M_{Sn} = 118.69$, $M_{Te} = 127.60$

$M_{GaAs} = M_{Ga} + M_{As} = 144.64$

The atom fractions of the solutes are given by the references data curves in figures 4.3, 4.4, 4.5, 4.6 and 4.7, respectively.

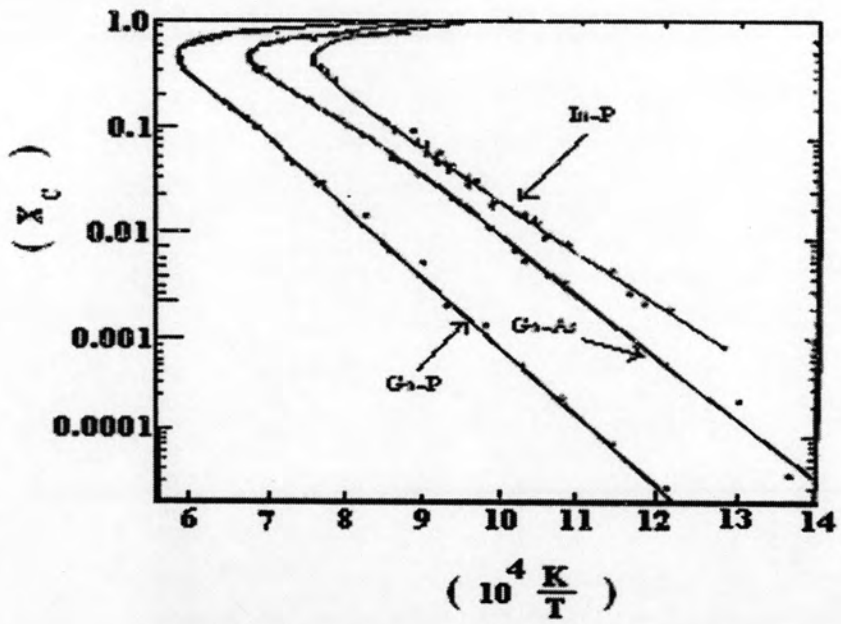

Fig. 4.3 Liquid composition versus reciprocal temperature for Ga-As, Ga-P and In-P

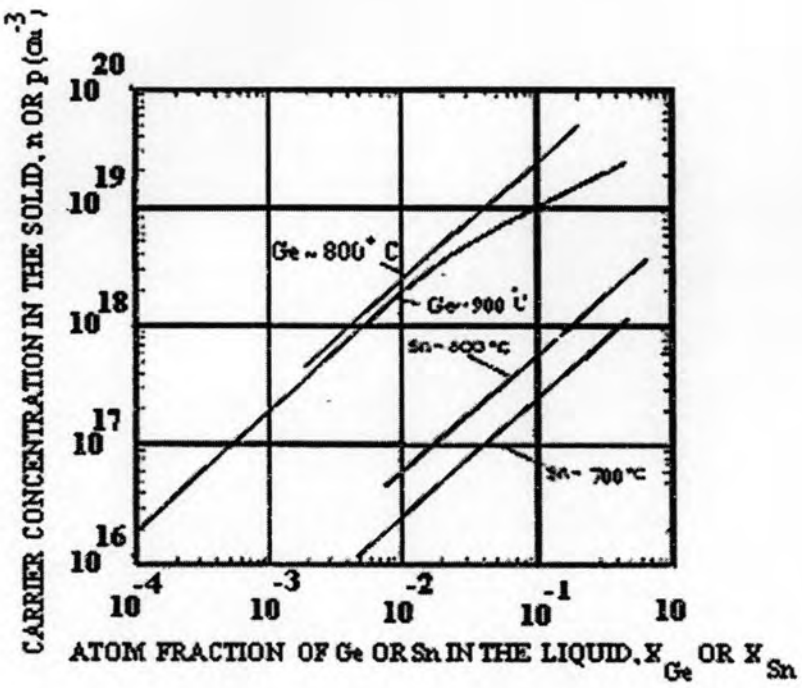

Fig. 4.4 Upper curves are the room-temperature hole concentration in GaAs versus atom fraction of Ge in the liquid along the 800°C, 900°C and the lower curves are the room-temperature electron concentration in GaAs versus atom fraction of Sn in the liquid along the 700°C, 800°C

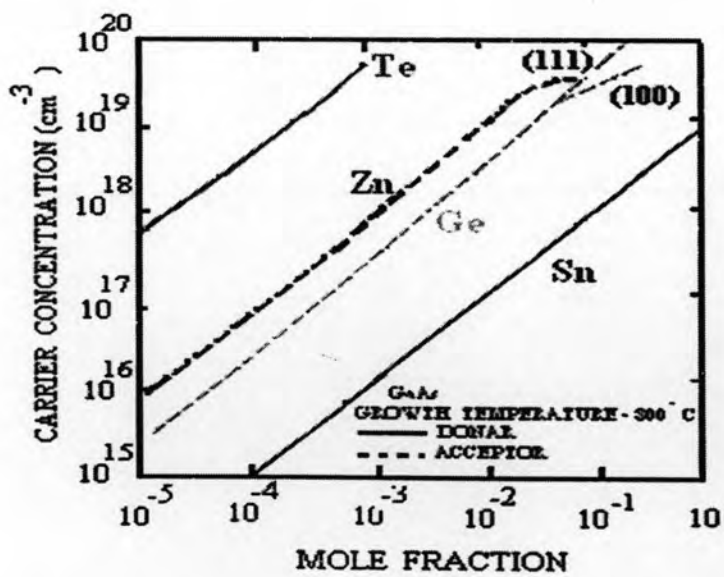

Fig. 4.5 Carrier concentration and atom fraction of Te, Sn, Ge, Zn at 800°C

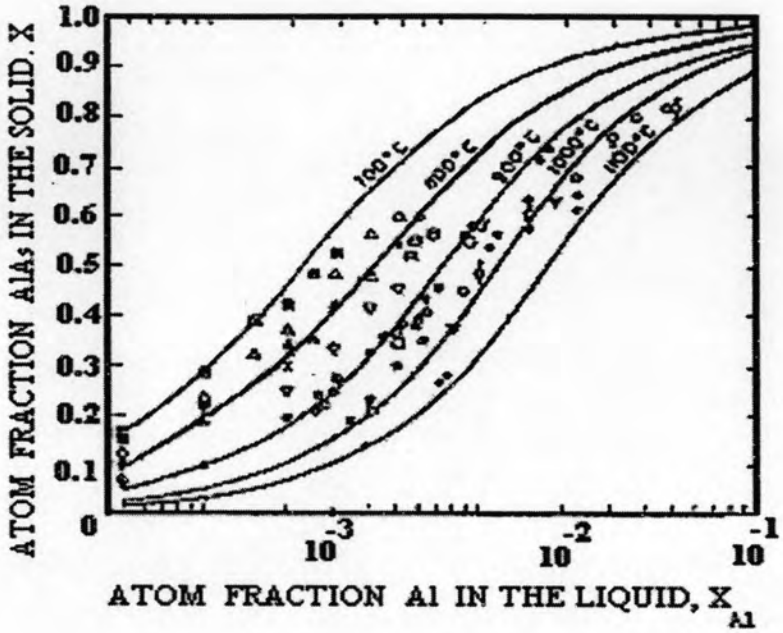

Fig. 4.6 Solidus compositions in $Ga_{1-x}Al_xAs$ as a function of liquidus composition

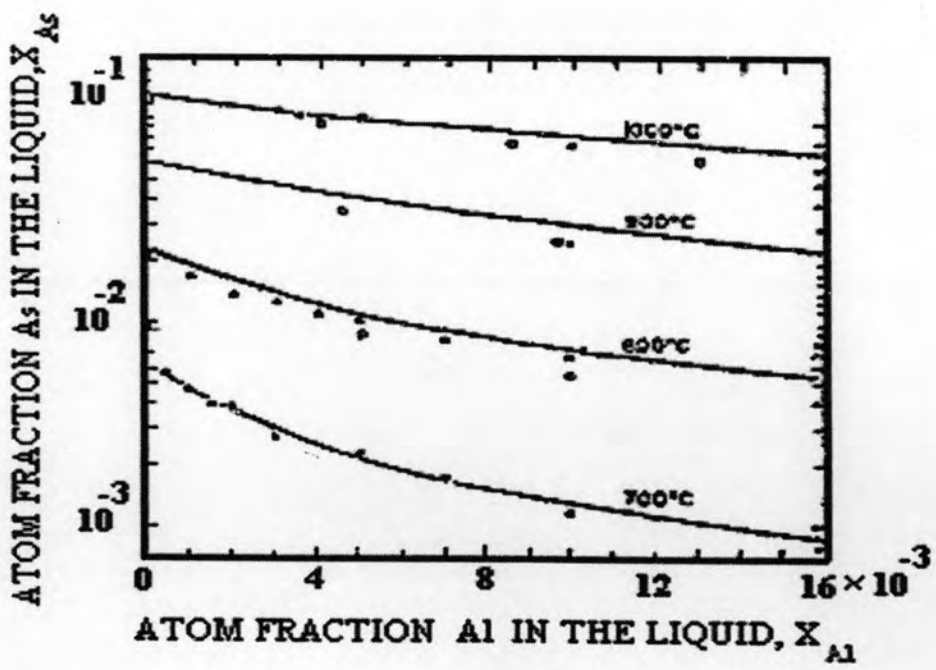

Fig. 4.7 Liquidus isotherms in the Al-Ga-As system

4.2.2 Detail Calculations of the Material Weight

The detail calculations of the weight for the materials in the specific layers of all designed heterojunction bipolar transistors (HBTs) are given as follow;

Heterojunction Bipolar Transistor with GaAs (p^+) - External Base (SYMT-04)

Epitaxial Layers for main structure process

Fig. 4.8 and Fig. 4.9 showed the designed layers of Main structure and epitaxial layers with regrown base of SYMT-04.The calculations of the material weights for all epitaxy layers can be seen in follow.

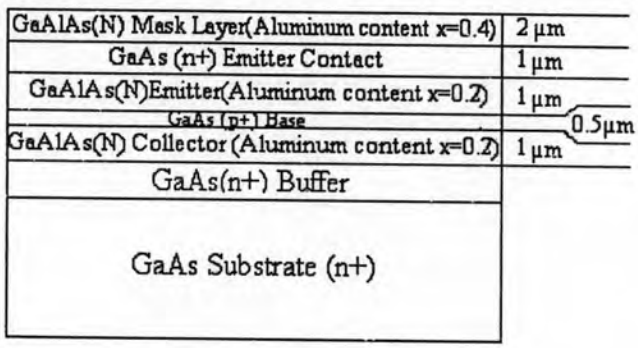

Fig. 4.8 Designed layer descriptions for Main structure of SYMT-04 DHBT

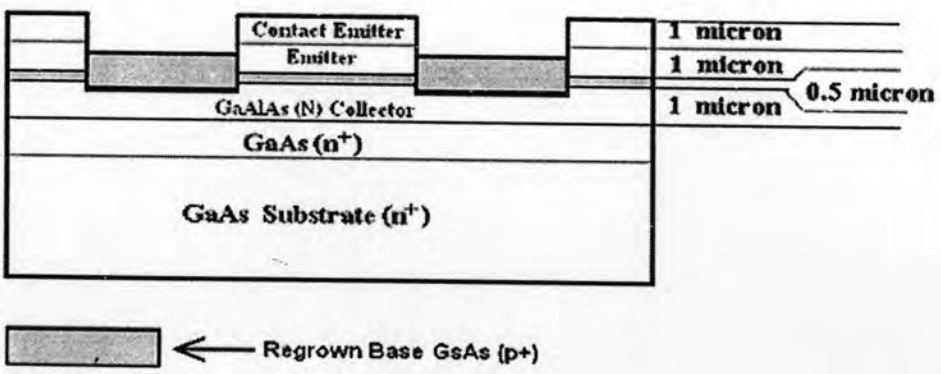

Fig 4.9 Epitaxial layer descriptions with Regrown Base of SYMT-04 DHBT

Buffer Layer: (GaAs -n^+) Te doped with (10^{19} cm^{-3})

From Fig. 4.3, referred to GsAs curve at 800°C,

We have, X_{As} =0.022

From Fig. 4.5, at Te-doped level of $10^{19}cm^{-3}$at 800°C, we have

$$X_{Te}= 0.0002$$

Therefore, $X_{Ga} = 1- X_{As} - X_{Te} =0.9778$

For W_{Ga}=3g, we will have

$$W_{Te} = 1.123mg$$

$$W_{GaAs} = 140.03mg$$

Collector layer: $Ga_{0.8}$ $Al_{0.2}$As (N -type) 5×10^{17} Sn -doped

Referred to Fig. 4.6, with atom fraction of AlAs in the solid x=0.2 at 800°C

We have,

$$X_{Al} = 0.0015$$

From Fig. 4.7, with $X_{Al} = 0.0015$ at 800°C

$$X_{As} = 0.016$$

And from Fig. 4.4, at Sn doped level of (5×10^{17}) cm^{-3} at 800°C, then we have,

$$X_{Sn} = 0.07$$

Therefore, $X_{Ga}= 1- X_{Sn} - X_{As} - X_{Al} = 0.9125$

For Ga =3g, we will have,

$$W_{Al} = 1.91\text{mg}$$

$$W_{Sn} = 391.78\text{mg}$$

$$W_{GaAs} = 109.12\text{mg}$$

Base Layer: GaAs (p^+) 5×10^{18} Ge-doped

From Fig. 4.3, referred to GsAs curve at 800°C,

We have, $X_{As} = 0.022$

From Fig.4.4, at Ge-doped level of 5×10^{18} cm^{-3}at 800°C, we have

$$X_{Ge} = 0.028$$

Therefore, $X_{Ga} = 1 - X_{As} - X_{Ge} = 0.95$

For Ga =3g, we will have,

$$W_{Ge} = 92.06\text{mg}$$

$$W_{GaAs} = 144.12\text{mg}$$

Emitter layer: $Ga_{0.8}$ $Al_{0.2}As$ (N -type) 5×10^{17} Sn –doped

Referred to Fig. 4.6, with atom fraction of AlAs in the solid x=0.2 at 800°C

We have,

$$X_{Al} = 0.0015$$

From Fig. 4.7, with $X_{Al} = 0.0015$ at 800°C

$$X_{As} = 0.016$$

And from Fig. 4.4, at Sn doped level of (5×10^{17}) cm^{-3} at 800°C, then we have,

$$X_{Sn} = 0.07$$

Therefore, $X_{Ga} = 1 - X_{Sn} - X_{As} - X_{Al} = 0.9125$

For Ga =3g, we will have,

$$W_{Al} = 1.91mg$$

$$W_{Sn} = 391.78mg$$

$$W_{GaAs} = 109.12mg$$

Emitter Contact layer: (GaAs -n^+) Te doped with (10^{19} cm^{-3})

From Fig. 4.3, referred to GsAs curve at 800°C,

We have, $X_{As} = 0.022$

From Fig. 4.5, at Te-doped level of $10^{19}cm^{-3}$at 800°C, we have

$$X_{Te} = 0.0002$$

Therefore, $X_{Ga} = 1 - X_{As} - X_{Te} = 0.9778$

For W_{Ga}=3g, we will have

$$W_{Te} = 1.123mg$$

$$W_{GaAs} = 140.03mg$$

Mask layer: $Ga_{0.6}Al_{0.4}As$ (Undoped) with (x=0.4)

Referred to Fig. 4.6, with atom fraction of AlAs in the solid x=0.4 at 800°C

We have,

$$X_{Al} = 0.003$$

From Fig. 4.7, with $X_{Al} = 0.003$ at 800°C

$$X_{As} = 0.015$$

Therefore, $X_{Ga} = 1 - X_{Al} - X_{As} = 0.982$

For W_{Ga}= 3g, we will have

$$W_{Al} = 3.57\text{mg}$$

$$W_{GaAs} = 110.0\text{mg}$$

Epitaxial Layers for Regrown Base process

Buffer Layer: GaAs (Undoped)

From Fig. 4.3, referred to GsAs curve at 800°C,

We have, $X_{As} = 0.022$

Therefore, $X_{Ga} = 1 - X_{As} = 0.978$

For W_{Ga}= 3g, we will have

$$W_{GaAs} = 140.03\text{mg}$$

External Regrown Base layer: $Ga_{1-x}Al_xAs(x=0)$ (P^+ -type) 5×10^{18} cm^{-3} Ge –doped

From Fig. 4.3, referred to GsAs curve at 800°C,

We have, X_{As} =0.022

From Fig. 4.4, at Ge-doped level of 5×10^{18} cm^{-3}at 800°C, we have

$$X_{Ge}= 0.028$$

Therefore, $X_{Ga} = 1- X_{As} - X_{Ge} = 0.95$

For Ga =3g, we will have,

$$W_{Ge} = 92.06\text{mg}$$

$$W_{GaAs} = 144.12\text{mg}$$

The calculated materials of the epitaxial layers both for the main structure and GaAs (p^+) regrown base are shown in tables 4.1 and 4.2.

Layers	**Weight Ga(g)**	**Weight** GaAs(mg)	**Weight** Al(mg)	**Weight** Ge(mg)	**Weight** Sn(mg)	**Weight** Te(mg)	**Contents (x)**	**Thickness (μm)App:**
Buffer(10^{19}) GaAs(n^+)	3	140.03	****	****	****	1.123	0.2	****
Buffer(10^{19}) GaAs(n^+)	3	140.03	****	****	****	1.123	0.2	****
Collector(5×10^{17}) GaAlAs(N)	3	109.12	1.91	****	391.78	****	0.2	1.5
Base(5×10^{18}) GaAs(p^+)	3	144.12	****	92.06	****	****	****	<0.5
Emitter(5×10^{17}) GaAlAs(N)	3	109.12	1.91	****	391.78	****	0.2	3
Emitter contact-10^{19} (GaAs-n^+)	3	140.03	****	****	****	1.123	0.2	2
Mask Layer GaAlAs	3	110.0	3.57	****	****	****	0.4	1

Table 4.1 Caiculated materials which are required for the main structure of SYMT-04

Layers	Weight Ga(g)	Weight GaAs(mg)	Weight Al(mg)	Weight Ge(mg)	Weight Sn(mg)	Weight Te(mg)	Contents (x)	Thickness App:(μm)
GaAs(n) for in situ etching	3	140.03	***	***	***	***	***	***
External Base(p^+)GaAs (5×10^{18})	3	144.12	***	92.06	***	***	***	***

Table 4.2 Calculated materials which are required for GaAs (p^+) regrown base of SYMT-04

Heterojunction Bipolar Transistor with $Ga_{0.8}Al_{0.2}As$ (P^+) Regrown Base (SYMT-07)

Epitaxial Layers for main structure process

Fig. 4.10 and Fig. 4.11 showed the designed layers of Main structure and epitaxial layers of regrown base of SYMT-07 and all calculations of the material weights for main structure epitaxial layers are similar to the ones of sample SYMT-04.

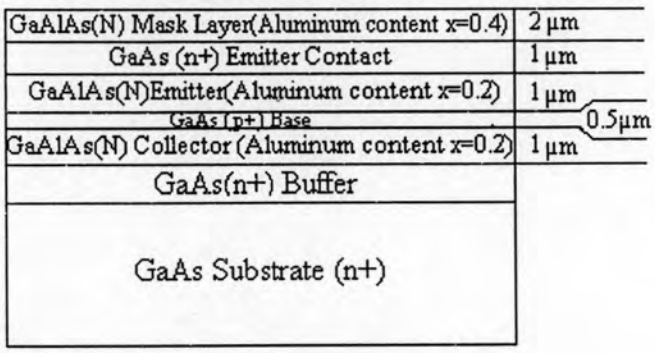

Fig. 4.10 Designed layer descriptions for Main structure of SYMT-07 DHBT

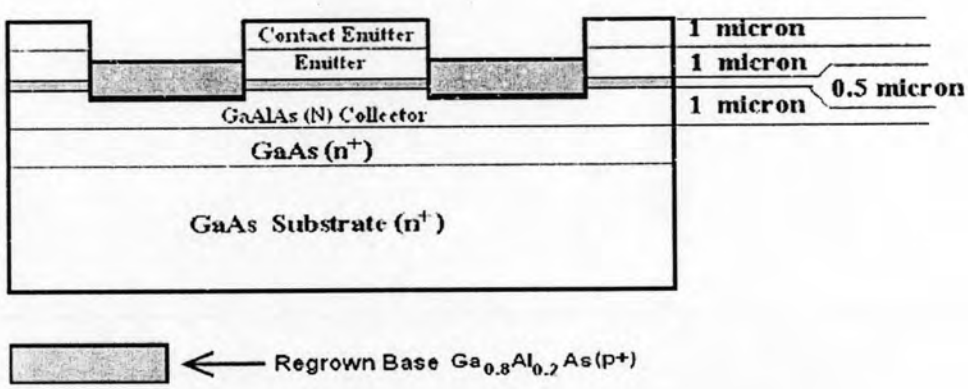

Fig.4.11 Epitaxial layer descriptions with Regrown Base of SYMT-07 DHBT

Epitaxial Layers for Regrown Base process

Buffer Layer: GaAs (Undoped)

The calculation of material weights for this layer is similar to the one of sample SYMT-04.

External Regrown Base layer: $Ga_{0.8}$ $Al_{0.2}As$ (P^+ -type) 5×10^{19} cm^{-3} Ge –doped

Referred to Fig. 4.6, with atom fraction of AlAs in the solid x=0.2 at 800°C

We have,

$$X_{Al} = 0.001$$

From Fig. 4.7, with $X_{Al} = 0.001$ at 800°C

$$X_{As} = 0.018$$

And from Fig. 4.4, at Ge doped level of (5×10^{19}) cm^{-3} at 800°C, then we have,

$$X_{Ge} = 0.04$$

Therefore, $X_{Ga} = 1 - X_{Sn} - X_{As} - X_{Al} = 0.941$

For Ga =3g, we will have,

$$W_{Al} = 1.23\text{mg}$$

$$W_{Ge} = 132.77\text{mg}$$

$$W_{GaAs} = 119.05\text{mg}$$

The calculated materials of the epitaxial layers both for the main structure and $Ga_{0.8}Al_{0.2}$ As (P^+) regrown base are shown in tables 4.3 and 4.4.

Layers	**Weight Ga(g)**	**Weight** GaAs(mg)	**Weight** Al(mg)	**Weight** Ge(mg)	**Weight** Sn(mg)	**Weight** Te(mg)	**Contents (x)**	**Thickness (μm)App:**
Buffer(10^{19}) GaAs(n^+)	3	140.03	****	****	****	1.123	0.2	****
Buffer(10^{19}) GaAs(n^+)	3	140.03	****	****	****	1.123	0.2	****
Collector(5×10^{17}) GaAlAs(N)	3	109.12	1.91	****	391.78	****	0.2	1.5
Base(5×10^{18}) GaAs(p^+)	3	144.12	****	92.06	****	****	****	<0.5
Emitter(5×10^{17}) GaAlAs(N)	3	109.12	1.91	****	391.78	****	0.2	3
Emitter contact-10^{19} (GaAs-n^+)	3	140.03	****	****	****	1.123	0.2	2
Mask Layer GaAlAs	3	110.0	3.57	****	****	****	0.4	1

Table 4.3 Calculated materials which are required for the main structure of SYMT-07

Layers	Weight Ga(g)	Weight GaAs(mg)	Weight Al(mg)	Weight Ge(mg)	Weight Sn(mg)	Weight Te(mg)	Contents (x)	Thickness (μm)App:
GaAs(n) for in situ etching	3	140.03	***	***	***	***	***	***
External Base(P^+)$Ga_{0.8}Al_{0.2}$ As (5×10^{19})	3	119.05	1.23	132.77	***	***	0.2	

Table 4.4 Calculated materials which are required for $Ga_{0.8}$ $Al_{0.2}$ As (P^+) regrown base of SYMT-07

Heterojunction Bipolar Transistor (SYMT-08)

Fig. 4.12 and Fig. 4.13 showed the designed layers of Main structure and epitaxial layers of regrown base of SYMT-08. For this structure, the aluminum content of collector layer is adjusted a little higher to be 0.3 to increase the injection efficiency of inverted mode, whereas the rests of transistor are the same.

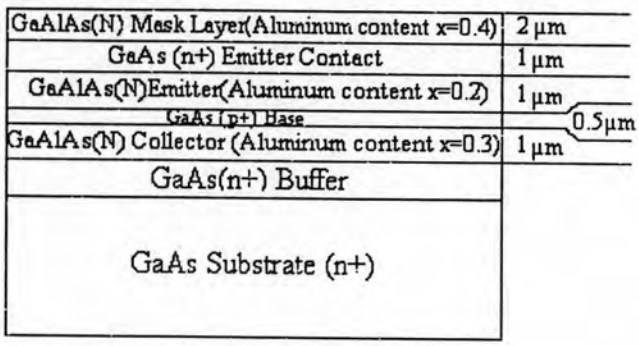

Fig. 4.12 Designed layer descriptions for Main structure of SYMT-08 DHBT

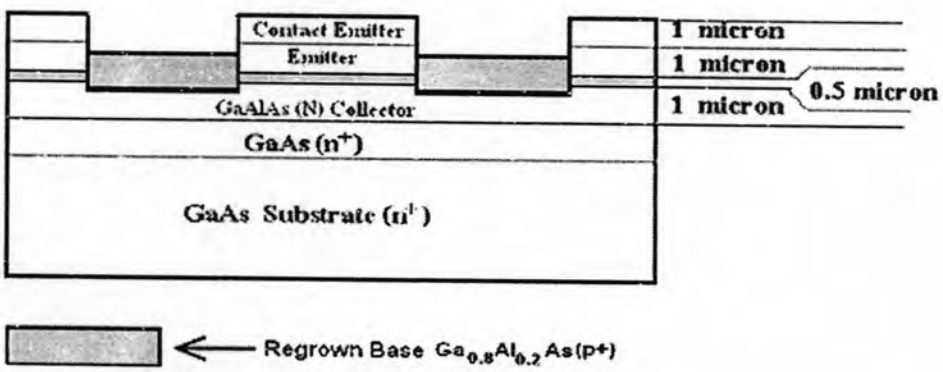

Fig. 4.13 Epitaxial layer descriptions with Regrown Base of SYMT-08 DHBT

The materials needed for 5×10^{17} cm^{-3} $Ga_{0.7}$ $Al_{0.3}As$ (N-type) can be calculated as shown below

Referred to Fig. 4.6, with atom fraction of AlAs in the solid x=0.3 at 800°C

We have,

$$X_{Al} = 0.0019$$

From Fig. 4.7, with $X_{Al} = 0.0015$ at 800°C

$$X_{As} = 0.017$$

And from Fig. 4.4, at Sn doped level of (5×10^{17}) cm^{-3} at 800°C, then we have,

$$X_{Sn} = 0.07$$

Therefore, $X_{Ga} = 1 - X_{Sn} - X_{As} - X_{Al} = 0.9111$

For Ga =3g, we will have,

$$W_{Al} = 2.42\text{mg}$$

$$W_{Sn} = 392.38\text{mg}$$

$$W_{GaAs} = 116.12\text{mg}$$

The calculated materials of the epitaxial layers both for the main structure and $Ga_{0.8}Al_{0.2}$ As (P^+) regrown base are shown in tables 4.5 and 4.6.

Layers	**Weight Ga(g)**	**Weight** GaAs(mg)	**Weight** Al(mg)	**Weight** Ge(mg)	**Weight** Sn(mg)	**Weight** Te(mg)	**Contents (x)**	**Thickness (μm)App:**
Buffer(10^{19}) GaAs(n^+)	3	140.03	****	****	****	1.123	0.2	****
Buffer(10^{19}) GaAs(n^+)	3	140.03	****	****	****	1.123	0.2	****
Collector(5×10^{17}) GaAlAs(N)	3	116.12	2.42	****	392.38	****	0.3	1.5
Base(5×10^{18}) GaAs(p^+)	3	144.12	****	92.06	****	****	****	<0.5
Emitter(5×10^{17}) GaAlAs(N)	3	109.12	1.91	****	391.78	****	0.2	3
Emitter contact-10^{19} (GaAs-n^+)	3	140.03	****	****	****	1.123	0.2	2
Mask Layer GaAlAs	3	95.06	3.54	****	****	****	0.4	1

Table 4.5 Calculated materials which are required for the main structure of SYMT-08

Layers	Weight Ga(g)	Weight GaAs(mg)	Weight Al(mg)	Weight Ge(mg)	Weight Sn(mg)	Weight Te(mg)	Contents (x)	Thickness (μm)App:
GaAs (n) for in situ etching	3	140.03	***	***	***	***	***	***
External Base(P^+)$Ga_{0.8}Al_{0.2}$ As (5×10^{19})	3	119.05	1.23	132.77	***	***	0.2	

Table 4.6 Calculated materials which are required for $Ga_{0.8}$ $Al_{0.2}$ As (P^+) regrown base of SYMT-08

Heterojunction Bipolar Transistor with $Ga_{0.8}$ $Al_{0.2}$ As and GaAs Double Regrown Base (SYMT-10)

For this case, the main structure is similar to SYMT-08 but the regrown base is composed of two p^+ layers. The bottom thinner layer, $Ga_{0.8}$ $Al_{0.2}As$ is for suppressing the injection electrons from collector to the external base area in the inverted mode. The upper thicker layer, GaAs (p^+) is for reducing the base resistance both in the external base region and at the base ohmic contact. Material weights for all epitaxial layers of this structure can be found from the three previous structures except of upper regrown base and tabulated again in tables 4.7 and 4.8. The designed layers of Main structure and epitaxial layers with regrown base of SYMT-10 are shown in Fig. 4.14 and Fig. 4.15.

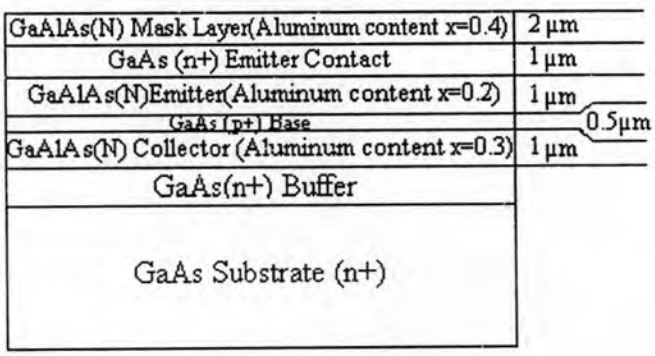

Fig. 4.14 Designed layer descriptions for Main structure of SYMT-10 DHBT

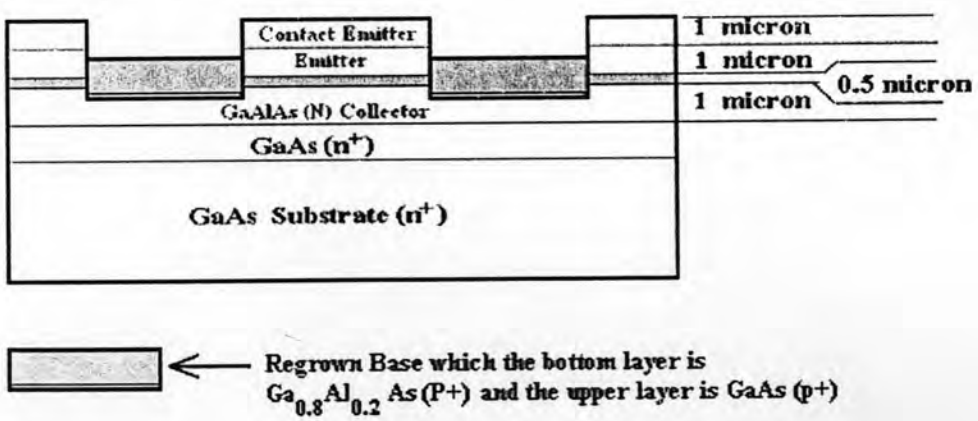

Fig.4.15 Epitaxial layer descriptions with double regrown base of SYMT-10 DHBT

The materials needed for 5×10^{19} cm^{-3} Ga As (p^+) -upper regrown base Layer can be calculated as shown below

From Fig. 4.3, referred to GsAs curve at 800°C,

We have, X_{As} =0.022

From Fig.4.4, at Ge-doped level of 5×10^{19} cm^{-3}at 800°C, we have

$$X_{Ge}= 0.04$$

Therefore, $X_{Ga} = 1- X_{As} - X_{Ge} = 0.938$

For Ga =3g, we will have,

$$W_{Ge} = 133.19\text{mg}$$

$$W_{GaAs} = 265.68\text{mg}$$

The calculated materials of the epitaxial layers both for the main structure and double regrown base are shown in tables 4.7 and 4.8.

Layers	**Weight Ga(g)**	**Weight** GaAs(mg)	**Weight** Al(mg)	**Weight** Ge(mg)	**Weight** Sn(mg)	**Weight** Te(mg)	**Contents (x)**	**Thickness (μm)App:**
Buffer(10^{19}) GaAs(n^+)	3	140.03	****	****	****	1.123	0.2	****
Buffer(10^{19}) GaAs(n^+)	3	140.03	****	****	****	1.123	0.2	****
Collector(5×10^{17}) GaAlAs(N)	3	116.12	2.42	****	392.38	****	0.3	1.5
Base(5×10^{18}) GaAs(p^+)	3	144.12	****	92.06	****	****	****	<0.5
Emitter(5×10^{17}) GaAlAs(N)	3	109.12	1.91	****	391.78	****	0.2	3
Emitter contact-10^{19} (GaAs-n^+)	3	140.03	****	****	****	1.123	0.2	2
Mask Layer GaAlAs	3	95.06	3.54	****	****	****	0.4	1

Table 4.7 Calculated materials which are required for the main structure of SYMT-10

Layers	Weight Ga(g)	Weight GaAs(mg)	Weight Al(mg)	Weight Ge(mg)	Weight Sn(mg)	Weight Te(mg)	Contents (x)	Thick: (μm)App
GaAs (n) for in situ etching	3	140.03	***	***	***	***	***	***
External Base(P^+)$Ga_{0.8}Al_{0.2}$ As (5×10^{19})	3	119.05	1.23	132.77	***	***	0.2	***
External Base (p^+-GaAs) (5×10^{19})	3	265.68	***	133.19	***	***	0	***

Table 4.8 Calculated materials which are required for double regrown base of SYMT-10

Heterojunction Bipolar Transistor with Diffused Base (SYMT-12)

All calculations for material weights are similar to the four previous structures. However, the aluminum content of collector layer was adjusted to be 0.25 to optimize the effective injection efficiency. Hence, it's compositions are again calculated. The designed layers of Main structure and epitaxial layers with diffused base for SYMT-12 are shown in Fig. 4.16 and Fig. 4.17.

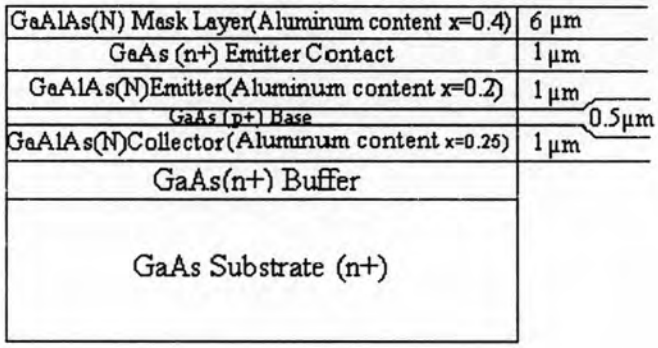

Fig. 4.16 Designed layer descriptions for Main structure of SYMT-12 DHBT

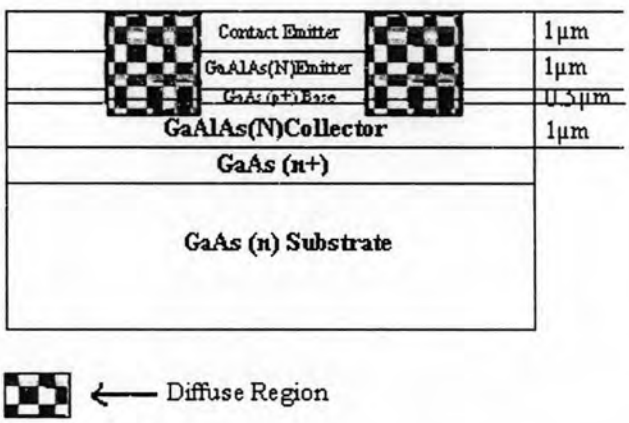

Fig.4.17 Epitaxial layer descriptions with diffused base of SYMT-12 DHBT

The materials needed for 5×10^{17} cm^{-3} $Ga_{0.75}$ $Al_{0.25}As$ (N-type) can be calculated as follows.

Collector layer: $Ga_{0.75}Al_{0.25}As$ (N -type) 5×10^{17} Sn -doped

Referred to Fig. 4.6, with atom fraction of AlAs in the solid x=0.25 at 800°C

We have,

$$X_{Al} = 0.0015$$

From Fig. 4.7, with $X_{Al} = 0.0015$ at 800°C

$$X_{As} = 0.018$$

And from Fig. 4.4, at Sn doped level of (5×10^{17}) cm^{-3} at 800°C, then we have,

$$X_{Sn} = 0.07$$

Therefore, $X_{Ga} = 1 - X_{Sn} - X_{As} - X_{Al} = 0.9105$

For Ga =3g, we will have,

$$W_{Al} = 1.913\text{mg}$$

$$W_{Sn} = 392.64\text{mg}$$

$$W_{GaAs} = 123.04\text{mg}$$

The calculated materials of the epitaxial layers for the main structure of SYMT-12 are shown in table 4.9.

Layers	**Weight Ga(g)**	**Weight** GaAs(mg)	**Weight** Al(mg)	**Weight** Ge(mg)	**Weight** Sn(mg)	**Weight** Te(mg)	**Contents (x)**	**Thickness (μm)App:**
Buffer(10^{19}) GaAs(n^+)	3	140.03	****	****	****	1.123	0.2	****
Buffer(10^{19}) GaAs(n^+)	3	140.03	****	****	****	1.123	0.2	****
Collector(5×10^{17}) GaAlAs(N)	3	123.04	1.913	****	392.64	****	0.25	1
Base(5×10^{18}) GaAs(P^+)	3	144.12	****	92.06	****	****	****	<0.5
Emitter(5×10^{17}) GaAlAs(N)	3	109.12	1.91	****	391.78	****	0.2	1
Emitter contact-10^{19} (GaAs-n^+)	3	140.03	****	****	****	1.123	0.2	1
Mask Layer GaAlAs	3	95.06	3.54	****	****	****	0.4	6

Table 4.9 Calculated materials which are required for the main structure of SYMT-12

4.2.3 Growth process of the Liquid Phase Epitaxy Technique

The epilayer thickness of LPE system depends on the creating mode and relieving super saturation that is also depended on the using temperature program during the growth of epilayer and the growth time at which the substrate contacts the growth solution. LPE system can be used the various mode operations such as super cooling, ramp cooling, steady state and transient mode. In the present thesis, we used the super cooling mode to make the epitaxial layers. Firstly, the solutions are saturated at an initial temperature of 800°C for about 4 hours. The in-situ cleaning can be achieved by rising the temperature to 804°C and the substrate was placed below the solution. During this, the surface layer of the substrate will be dissolved into the solution. The solutions were then super cooled by driving the furnace temperature down to a temperature below that at which the substrate and solutions are in equilibrium at cooling rate of 0.2°C/min. After ΔT~2°C of super cooling growth, the epilayer growth process starts when the substrate and solution contact each other while the temperature program continuously decreases the temperature through the growth period.

The total layer thickness is a function of time at the equilibrium condition of LPE system is given by

$$d = \mathrm{K}\left(\Delta T t^{1/2} + \frac{2}{3}\alpha t^{3/2} \right)$$

Where,

K = the constant which is a function of concentration of As in the liquid

ΔT = the difference between the saturation temperature and growth temperature

α = the cooling rate

The thickness of the grown epilayers were checked by Scanning Electron microscope (SEM) and then we can adjust the growth times for the desired design layers thickness of HBTs. Fig. 4.18 shows the growth times and growth temperatures profile for the main structure of general HBTs. Figures 4.19, 4.20 and 4.21 are temperature profile versus the growth time of the main structures of SYMT-04, SYMT-07, SYMT-08, SYMT-10 and SYMT-12, respectively.

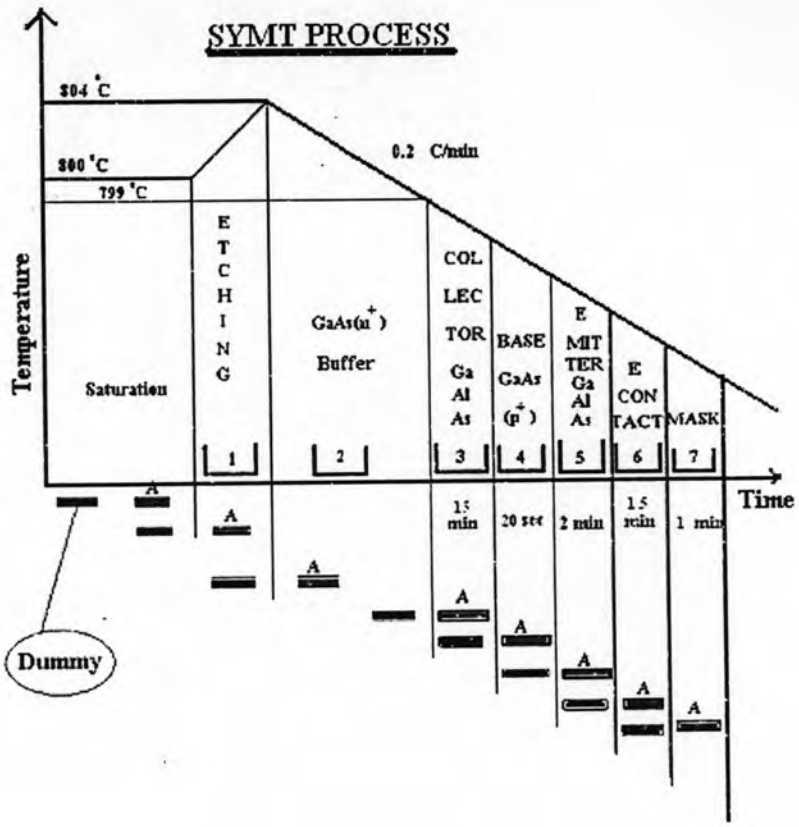

Fig. 4.18 Growth times and growth temperatures for main structure of general Heterojunction Bipolar Transistor

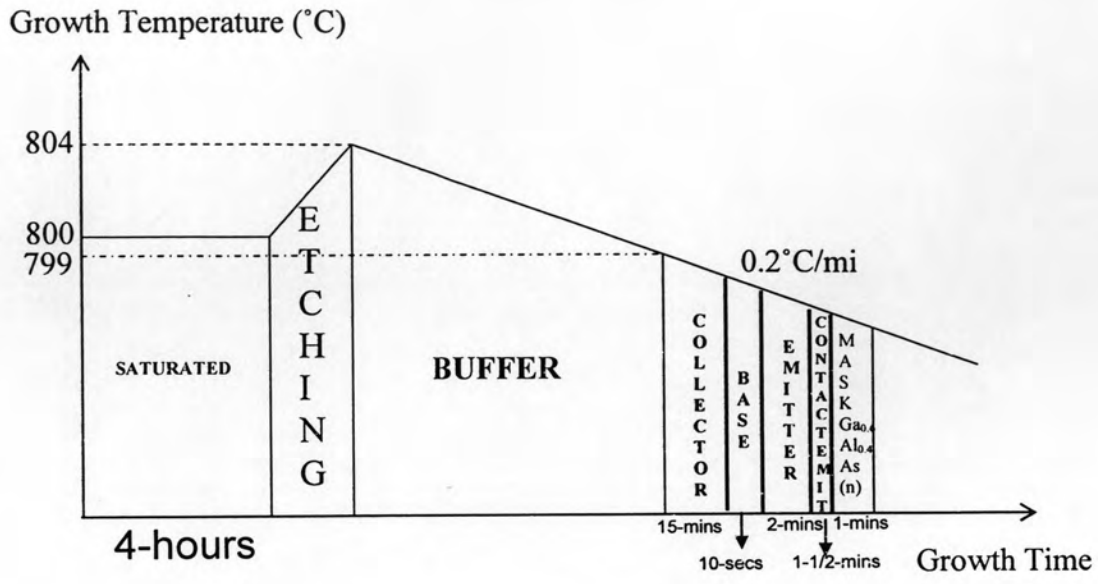

Fig. 4.19 Temperature profile for main structure layers of Heterojunction Bipolar Transistor (SYMT-04)

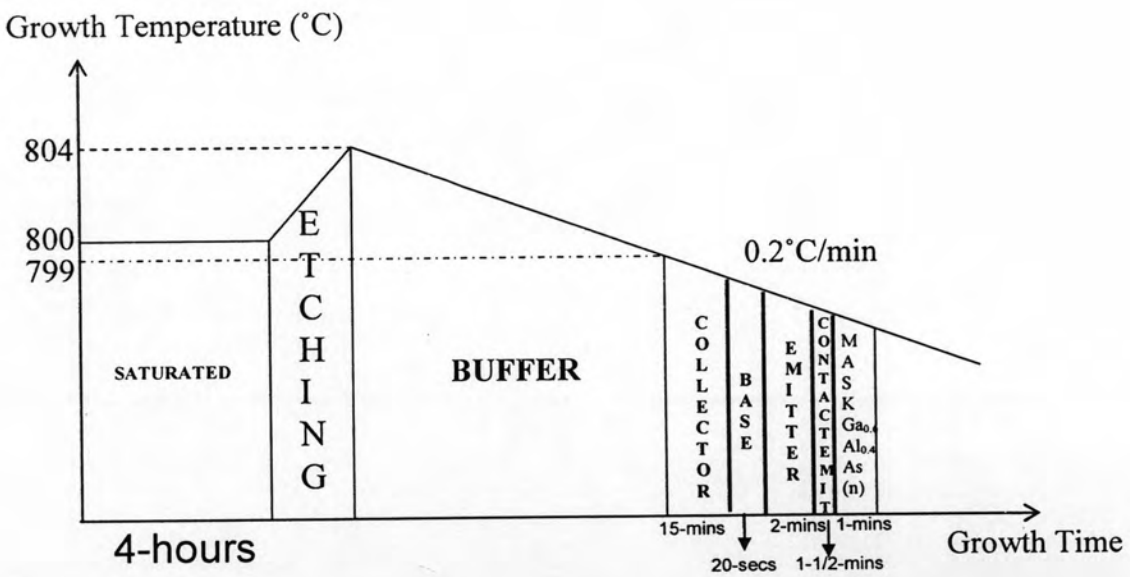

Fig. 4.20 Temperature profile for main structure layer of Heterojunction Bipolar Transistors (SYMT-07, 08, 10)

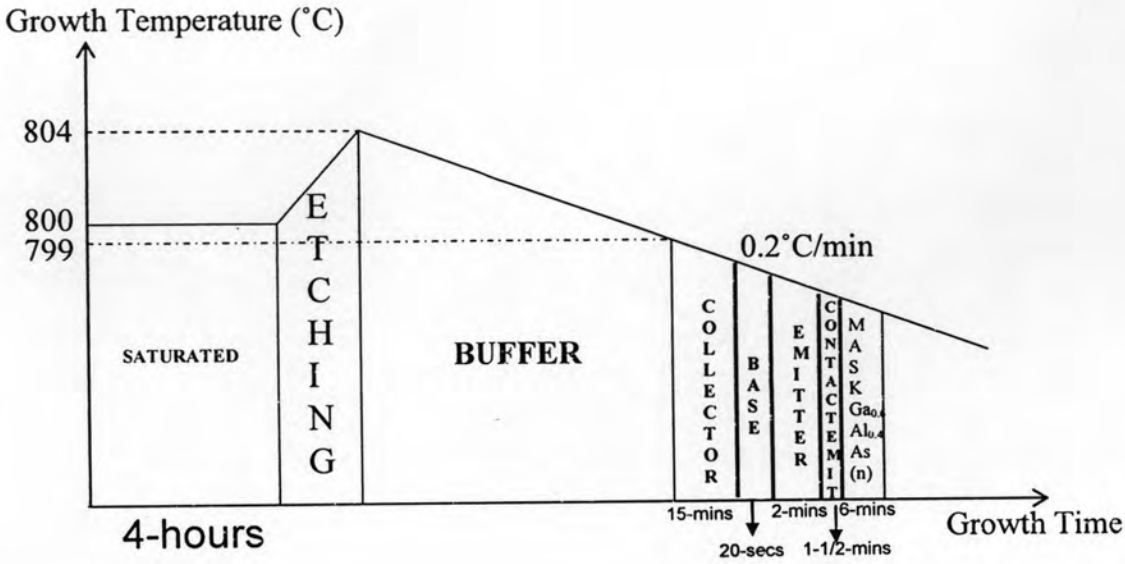

Fig. 4.21 Temperature profile for main structure of Heterojunction Bipolar Transistor (SYMT-12)

Before growing of the epilayers on the substrate (n^+ -GaAs), the graphite boat in the LPE furnace is prebaked at 900°C for about 4-hours in a pure hydrogen atmosphere to remove the moisture and contaminates. The growth layers are checked by the Scanning Electron Microscope (SEM) .The samples are cleaned with HCl +H_2O(1:1) to get rid of the oxide layer and remaining Ga from the surface of the substrate and then the samples are throughly washed with the DI water and dried with the N_2 gas.

4.2.4 Formation of DHBTs with Regrown Base Process

After growing the main structure layers, as shown schematically in Fig. 4.25-a, we used the photolithography technique to define the external base area. The photolithography technique is as follows

- Clean the surface of the samples with $HCl+H_2O$ (1:1) and prebaked (1-min) in oven at (70-80 °C)
- Apply the resist onto the surface of the samples and soft baked again in the oven about (7-minutes) at (70-80 °C)
- Aligned the pattern on the wafers and passed through the UV light (70-second) by the Mask aligner
- Developed the patterns on the wafers by the developer solution at about (1.5 minutes)
- Verify the patterns on the wafer by optical-microscope
- Make the post-baked or hard baked about (31-minutes) at (70-80 °C) and also painted on the back side of samples with the resist or wax to protect the etching.

After that the defined external base area was etched with the solution of $H_2SO_4:H_2O_2:H_2O$ (3:1:15). This etching time can be estimated from the data curve, Fig. 4.22 by considering the etching depth which should be in between the N-GaAlAs collector layer (Fig.4.25-b). Then the samples were carried back into the LPE furnace to regrow the external base layer. This growth may be called second growth. Before this process, LPE furnace was prebaked again at 900°C to remove moistures and contaminates. Then the second growth process is started using the temperature profiles shown in figures 4.23 or 4.24 according to the regrown base designs. However, the growth time should be precisely controlled to ensure that the upper surface of the external regrown base layer is in between the N-GaAlAs emitter layer (Fig. 4.25-c).

Time (Second)	Depth (μ m)
30	0.73
35	0.9
40	0.91
45	1.09
55	1.18
60	1.5
65	1.55

Table 4.10 Experimental data of the Etching depth and Etching time of $NH_4OH:H_2O_2:H_2O$ (3:1:15)

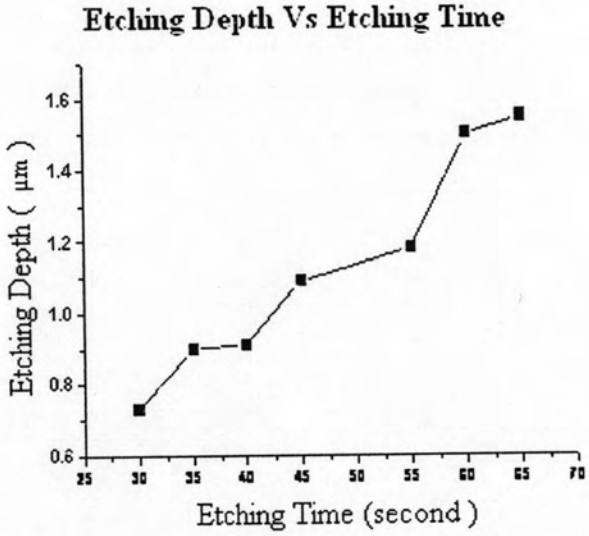

Fig. 4.22 Data curve of the etching depth versus etching time of $NH_4OH:H_2O_2:H_2O$ (3:1:15)

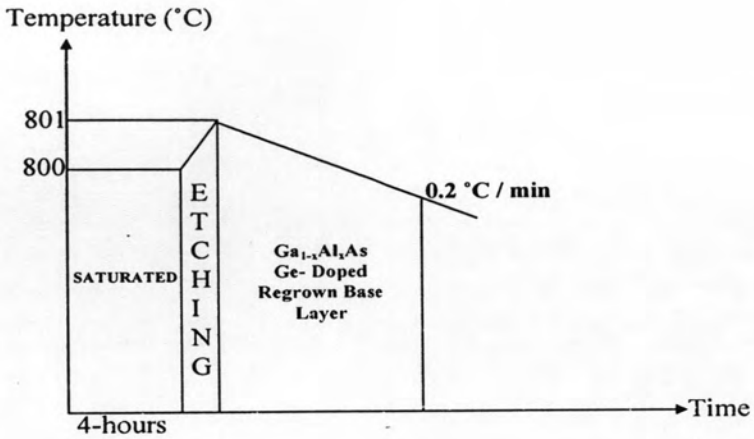

Fig. 4.23 Second growth temperature profile for the single regrown base

(SYMT-04, 07, 08)

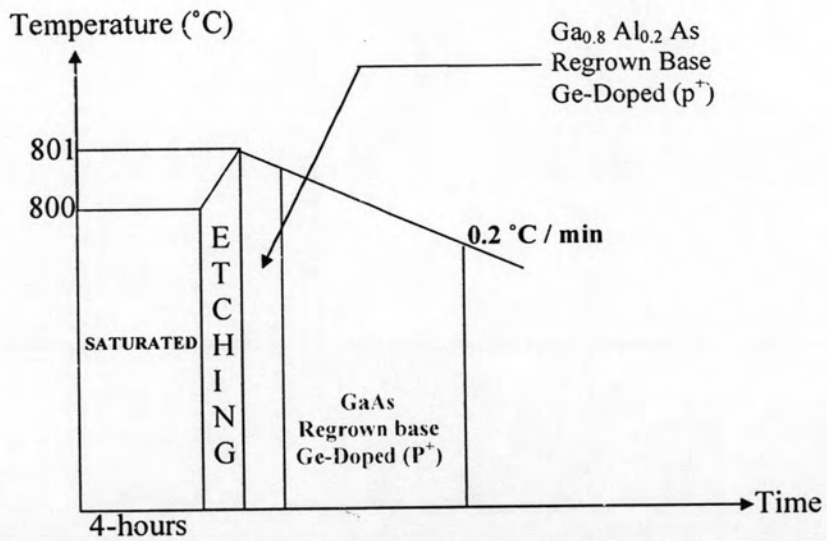

Fig. 4.24 Second growth temperature profile for the double regrown base

(SYMT-10)

After that, the photolithography techniques (already mentioned above) is used to define the internal emitter base area and uncover the contact emitter by etching with the solution of $NH_4OH:H_2O_2:H_2O$ (3:1:15) about 1 minute and 45 seconds (Fig.4.25-d). Then the ohmic contacts were performed on emitter and external base area by the metallization techniques.

The steps to make emitter ohmic contacts are as follow:

- Apply the resist to samples and soft baked about (7-min)
- Mask and align patterned to open the contact emitter with UV-55 second
- Developed the patterns on the sample with deveploper-1min
- Prepared the evaporator to diffuse Au-Ge onto both surfaces (front and back sides) of the samples at (~100°C)
- Continue the Ni evaporation at (~100°C) on the front side of the samples to press Au-Ge or smooth the surface of the samples
- Make the photolithography again (soft baked about 7-minutes and hard baked about 31-minutes at (70-80°C) to protect the etching of (Au-Ge & Ni)
- Ni-etching with HCl about (~1.5 minutes) and Au-Ge etching with (4gm of KI, 1gm of I,40ml of H_2O) about (~30second)
- Patterns of the emitter contact can be seen with the optical microscope
- Make the annealing at (500 °C) about 2-minutes

The steps to make base ohmic contact are as follow:

- Apply the resist to samples and soft baked about (7-min)
- Mask and align patterned to open the contact base with UV-55 second
- Developed the patterns on the sample with deveploper-1min
- Prepared the evaporator to diffuse Au-Zn onto the front surfaces of the samples at (~100°C)
- Make the photolithography again (soft baked about 7-minutes and hard baked about 31-minutes at (70-80°C) to protect the etching of (Au-Zn)
- Au-Zn etching with (4gm of KI, 1gm of I,40ml of H_2O) about (~30second)
- Make the annealing at (400 °C) about 2-minutes

Finally, the mesa etching was used to isolate the devices with the solution of H_2SO_4:H_2O_2:H_2O (4:1:1) and also used CCl_2: CHCl (Trichloroethylene) for wax cleaning, $(CH_3)_2CO$ (Acetone) for photoresit cleaning. All formation steps of the HBTs with Regrown base are shown in figures 4.25-a, b, c, d and 4.26.

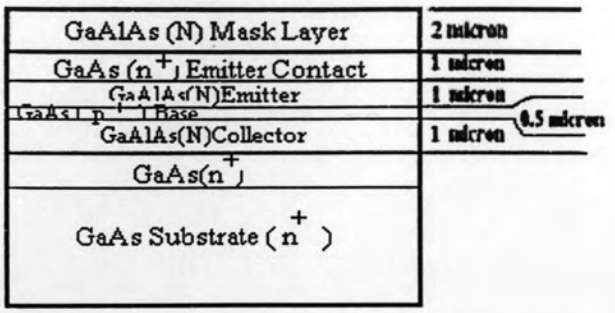

Fig. 4.25-a Epitaxial layers on the substrate by LPE technique

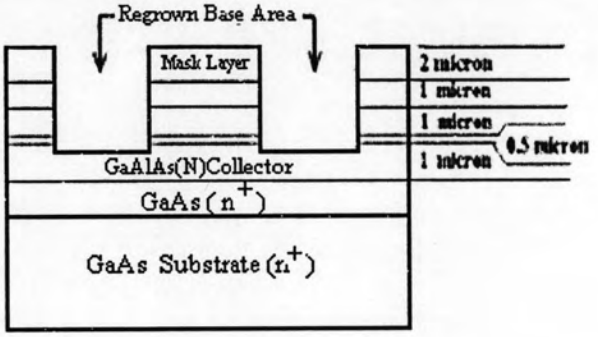

Fig. 4.25-b Defining the regrown base area.

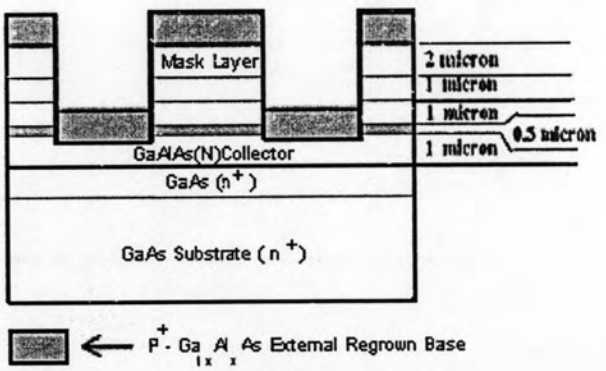

Fig. 4.25-c Regrow the p^+-GaAs base layer.

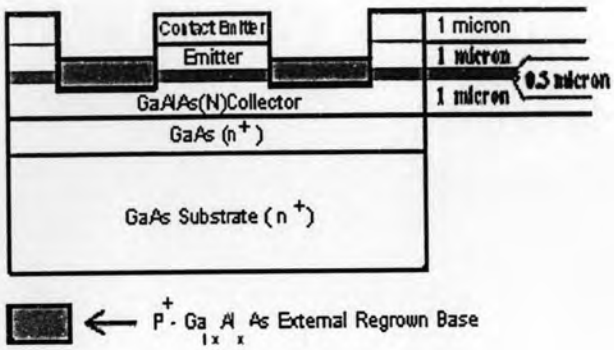

Fig. 4.25-d Define the intrinsic emitter-base area and uncover the contact emitter.

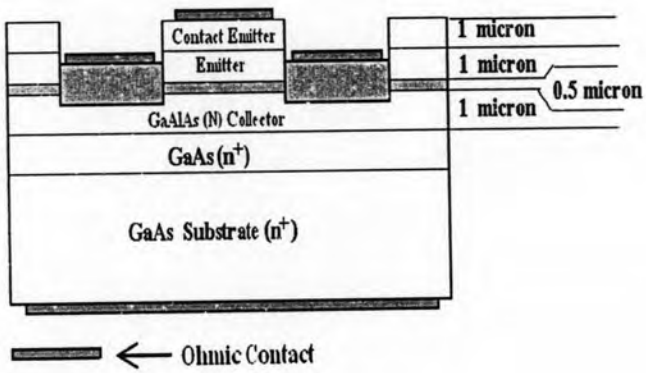

Fig. 4.26 Ohmic contact formation and mesa etching

4.2.5 Formation of DHBTs with Diffused Base Process

After main structure growth, the diffuse area was defined by the etching with the same solution as the one of regrown base, forming the well deep to approximately 0.5 μm over the interface between the mask layer and the emitter contact layer (Fig. 4.28-b). After that, the zinc (Zn) diffusion process can be started by the equipment depicted in Fig.4.27. The vapor phase zinc (Zn) diffusion technique utilizes a confined in LPE graphite boat modified to hold the diffusion source and wafer in close proximity. The Zn is dissolved in a solvent melt such as Ga or Sn as a diffusion charge. The diffusion boat is loaded with the wafer and diffusion charge, and then it is placed in a growth tube of LPE

system, but initially remains outside the furnace. When the furnace temperature reached at 600°C, the furnace center is moved to the position of the boat to heat up for (45-minutes). Due to the very high diffusion coefficient of zinc, all of the surfaces of transistor including the mask layer deep to around 3-4 μm, have been doped to be p-type (Fig. 4.28-c). However, the zinc atoms cannot reach the emitter contact layer outside the exposed base diffusion well because of a 6-μm $Ga_{0.6}Al_{0.4}As$ mask layer barrier. The layer, $Ga_{0.6}Al_{0.4}As$, was then selectively etched by a HF-containing solution at 50°C (Fig. 4.28-d). After that the emitter-ohmic contact and base-ohmic contact are performed by the metallization technique as same as in the regrown base processes. The detail processing steps of the DHBTs with the diffused base are shown in figures (4.28-a, b, c, d, e).

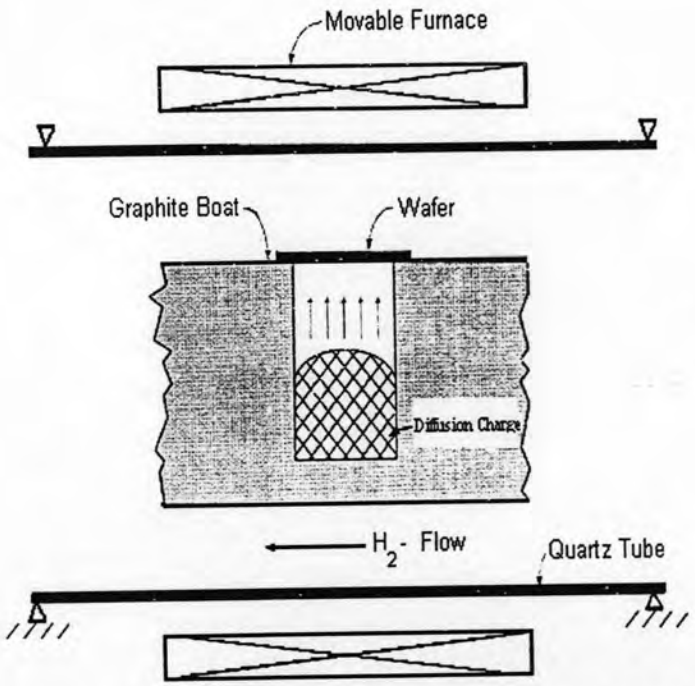

Fig. 4.27 Cross-sectional view of a modified graphite boat showing diffusion charge and confined vapor chamber between the charge and wafer

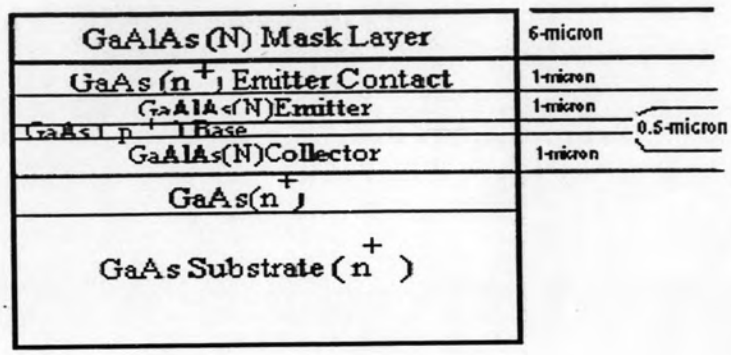

Fig. 4.28-a Epitaxial layers on the substrate by LPE technique

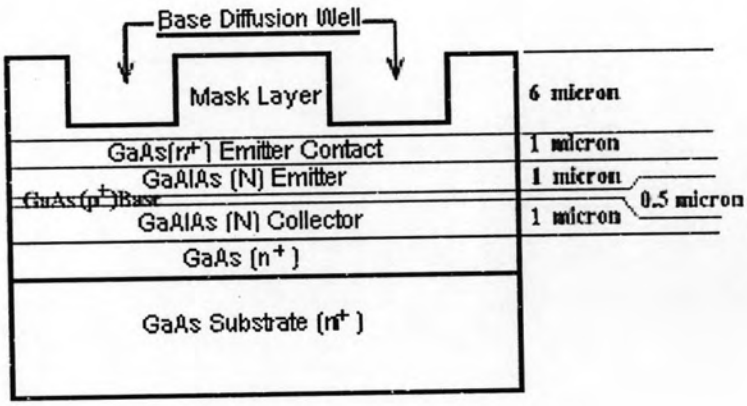

Fig. 4.28-b Selective removal of the mask layer for base contact area.

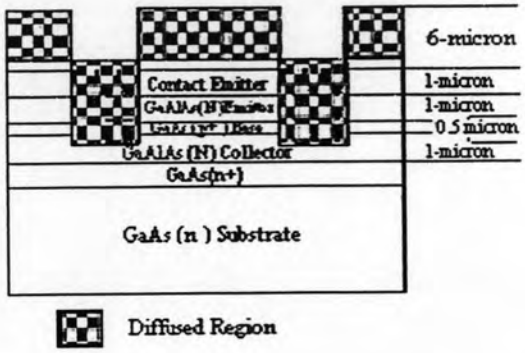

Fig. 4.28-c Zinc diffusion

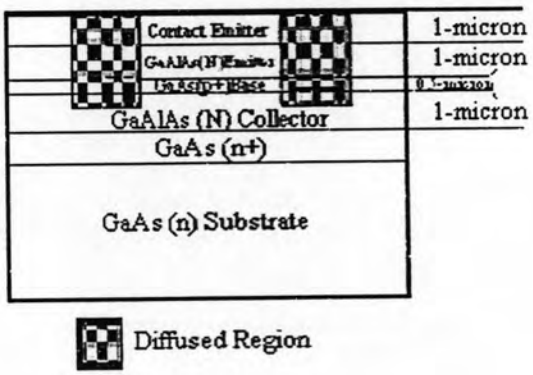

Fig. 4.28-d Etching of Mask layer, $Ga_{0.6}Al_{0.4}As$, by HF.

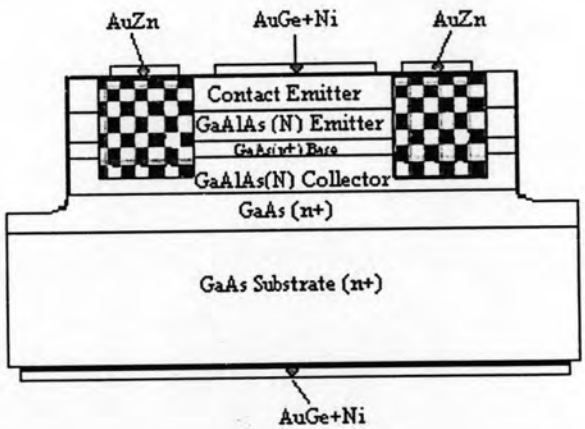

Fig. 4.28-e Ohmic contact metallization and Mesa etching