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10. สุวิทย์ ปุณณชัยยะ "การพัฒนาเครื่องนับรังสีขนาดเบา" วิทยานิพนธ์ปริญญามหาบัณฑิต ภาควิชานิวเคลียร์เทคโนโลยี บัณฑิตวิทยาลัย จุฬาลงกรณ์มหาวิทยาลัย ปี 2525
11. นเรศร์ จันทน์ขาว "ศึกษาการสำรวจยูเรเนียมโดยวิธีแทรค-เอทช์" วิทยานิพนธ์ปริญญามหาบัณฑิต ภาควิชา นิวเคลียร์เทคโนโลยี บัณฑิตวิทยาลัย จุฬาลงกรณ์มหาวิทยาลัย ปี 2522

ภาคผนวก ก

ข้อมูลวงจรรวม

LF155, LF155A, LF255, LF355, LF355A LOW SUPPLY CURRENT
LF156, LF156A, LF256, LF356, LF356A WIDE BAND
LF157, LF157A, LF257, LF357, LF357A WIDE BAND UNCOMPENSATED (Av_{MIN}=5)

LF155
LF156
LF157

COMMON FEATURES
(LF155A, LF156A, LF157A)

- Low input bias current 30 pA
- Low Input Offset Current 3 pA
- High input impedance $10^{12}\Omega$
- Low input offset voltage 1 mV
- Low input offset voltage temperature drift $3\mu V/^{\circ}C$
- Low input noise current 0.01 $pA/\sqrt{Hz}$
- High common-mode rejection ratio 100 dB
- Large dc voltage gain 106 dB

UNCOMMON FEATURES

	LF155A	LF156A	LF157A(Av=5)	UNITS
Extremely fast settling time to 0.01%	4	1.5	1.5	μs
Fast slew rate	5	12	50	V/μs
Wide gain bandwidth	2.5	5	20	MHz
Low input noise voltage	20	12	12	$nV/\sqrt{Hz}$

APPLICATIONS

- Precision high speed integrators
- Fast D/A and A/D converters
- High impedance buffers
- Wideband, low noise, low drift amplifiers
- Logarithmic amplifiers
- Photocell amplifiers
- Sample and Hold circuits

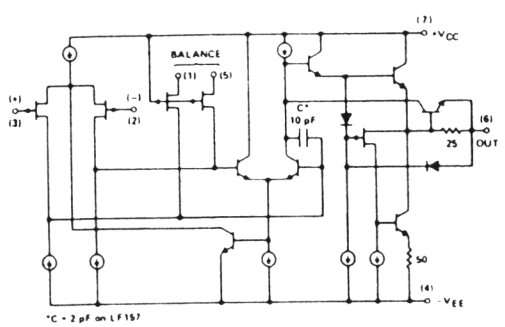
GENERAL DESCRIPTION

These monolithic JFET input operational amplifiers incorporate well matched, high voltage JFETs on the same chip with standard bipolar transistors (BIFET Technology). These amplifiers feature low input bias and offset currents, low offset voltage and offset voltage drift, coupled with offset adjust which does not degrade drift or common-mode rejection. The devices are also designed for high slew rate, wide bandwidth, extremely fast settling time, low voltage and current noise and a low 1/f noise corner.

ADVANTAGES

- Replace expensive hybrid and module FET op amps
- Rugged JFETs allow blow-out free handling compared with MOSFET input devices
- Excellent for low noise applications using either high or low source impedance—very low 1/f corner
- Offset adjust does not degrade drift or common-mode rejection as in most monolithic amplifiers
- New output stage allows use of large capacitive loads (10,000 pF) without stability problems
- Internal compensation and large differential input voltage capability

SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

	LF155A/6A/7A	LF355A/6A/7A	LF155/6/7	LF255/6/7	LF355/6/7
Supply Voltage	±22V	±22V	±22V	±22V	±18V
Power Dissipation TO-99 (H package) (Note 1)	670 mW	500 mW	670 mW	570 mW	500 mW
Operating Temperature Range	−55°C to +125°C	0°C to +70°C	−55°C to +125°C	−25°C to +85°C	0°C to +70°C
$T_{j(MAX)}$	150°C	100°C	150°C	110°C	100°C
Differential Input Voltage	±40V	±40V	±40V	±40V	±30V
Input Voltage Range (Note 2)	±20V	±20V	±20V	±20V	±16V
Output Short Circuit Duration	Continuous	Continuous	Continuous	Continuous	Continuous
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C	300°C	300°C	300°C	300°C

DC ELECTRICAL CHARACTERISTICS (Note 3)

SYMBOL	PARAMETER	CONDITIONS	LF155A/6A/7A			LF355A/6A/7A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	$R_S = 50\Omega$, $T_A = 25°C$		1	2		1	2	mV
		Over Temperature			2.5			2.3	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	$R_S = 50\Omega$		3	5		3	5	mV
$\Delta TC/\Delta V_{OS}$	Change in Average TC with V_{OS} Adjust	$R_S = 50\Omega$, (Note 4)		0.5			0.5		$\mu V/°C$ per mV
I_{OS}	Input Offset Current	$T_j = 25°C$, (Notes 3,5)		3	10		3	10	pA
		$T_j \leq T_{HIGH}$			10			1	nA
I_B	Input Bias Current	$T_J = 25°C$, (Notes 3,5)		30	50		30	50	pA
		$T_J \leq T_{HIGH}$			25			5	nA
R_{IN}	Input Resistance	$T_J = 25°C$		10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	$V_S = \pm15V$, $T_A = 25°C$	50	200		50	200		V/mV
		$V_O = \pm10V$, $R_L = 2k$							
		Over Temperature	25			25			V/mV
V_O	Output Voltage Swing	$V_S = \pm15V$, $R_L = 10k$	±12	±13		±12	±13		V
V_{CM}	Input Common-Mode Voltage Range	$V_S = \pm15V$	±11	+15.1		±11	+15.1		V
				−12			−12		V
CMRR	Common-Mode Rejection Ratio		85	100		85	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 6)	85	100		85	100		dB

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = \pm15V$

SYMBOL	PARAMETER	CONDITIONS	LF155A/355A			LF156A/356A			LF157A/357A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew Rate	LF155A/6A: $A_V = 1$, LF157A: $A_V = 5$	3	5		10	12		40	50		V/μs
GBW	Gain-Bandwidth Product			2.5		4	4.5		15	20		MHz
t_s	Settling Time to 0.01%	(Note 7)		4			1.5			1.5		μs
e_n	Equivalent Input Noise Voltage	$R_S = 100\Omega$										
		f = 100 Hz		25			15			15		$nV/\sqrt{Hz}$
		f = 1000 Hz		20			12			12		$nV/\sqrt{Hz}$
i_n	Equivalent Input Noise Current	f = 100 Hz		0.01			0.01			0.01		$pA/\sqrt{Hz}$
		f = 1000 Hz		0.01			0.01			0.01		$pA/\sqrt{Hz}$
C_{IN}	Input Capacitance			3			3			3		pF

DC ELECTRICAL CHARACTERISTICS (Note 3)

SYMBOL	PARAMETER	CONDITIONS	LF155/6/7			LF255/6/7			LF355/6/7			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	R_S 50Ω, T_A 25°C		3	5		3	5		3	10	mV
		Over Temperature			7			6.5			13	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	R_S 50Ω		5			5			5		μV/°C
$\Delta TC/\Delta V_{OS}$	Change in Average TC with V_{OS} Adjust	R_S 50Ω (Note 4)		0.5			0.5			0.5		μV/°C per mV
I_{OS}	Input Offset Current	T_j 25°C (Notes 3, 5)		3	20		3	20		3	50	pA
		T_j T_{HIGH}			20			1			2	nA
I_B	Input Bias Current	T_J 25°C (Notes 3,5)		30	100		30	100		30	200	pA
		T_J T_{HIGH}			50			5			8	nA
R_{IN}	Input Resistance	T_J 25°C		10^{12}			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	V_S ±15V, T_A 25°C, V_O ±10V, R_L 2k	50	200		50	200		25	200		V/mV
		Over Temperature	25			25			15			V/mV
V_O	Output Voltage Swing	V_S ±15V, R_L 10k	±12	±13		±12	±13		±12	±13		V
V_{CM}	Input Common-Mode Voltage Range	V_S ±15V	±11	+15.1 −12		±11	+15.1 −12		±10	+15.1 −12		V
CMRR	Common-Mode Rejection Ratio		85	100		85	100		80	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 6)	85	100		85	100		80	100		dB

DC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_S = ±15V

PARAMETER	LF155A/355A LF155/255		LF355		LF156A/356A LF156/256		LF356		LF157A/357A LF157/257		LF357		UNITS
	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
Supply Current,	2	4	2	4	5	7	5	10	5	7	5	10	mA

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_S = ±15V

SYMBOL	PARAMETER	CONDITIONS	LF155/LF255/ LF355	LF156/LF256	LF156/LF256/ LF356	LF157/LF257	LF157/LF257/ LF357	UNITS
			TYP	MIN	TYP	MIN	TYP	
SR	Slew Rate	LF155/6 A_V 1, LF157 A_V 5	5	7.5	12	30	50	V/μs
GBW	Gain Bandwidth Product		2.5		5		20	MHz
t_s	Settling Time to 0.01%	(Note 7)	4		1.5		1.5	μs
e_n	Equivalent Input Noise Voltage	R_S 100Ω, f 100 Hz	25		15		15	nV/√Hz
		f 1000 Hz	20		12		12	nV/√Hz
i_n	Equivalent Input Current Noise	f 100 Hz	0.01		0.01		0.01	pA/√Hz
		f 1000 Hz	0.01		0.01		0.01	pA/√Hz
C_{IN}	Input Capacitance		3		3		3	pF

NOTES FOR ELECTRICAL CHARACTERISTICS

NOTE 1: The TO-99 package must be derated based on a thermal resistance of 150°C/W junction to ambient or 45°C/W junction to case.

NOTE 2: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

NOTE 3: These specifications apply for +15V ≤ V_S ≤ +20V, −55°C ≤ T_A ≤ +125°C and T_{HIGH} = +125°C unless otherwise stated for the LF155A/6A/7A and the LF155/6/7. For the LF255/6/7, these specifications apply for +15V ≤ V_S ≤ +20V, −25°C ≤ T_A ≤ +85°C and T_{HIGH} = 85°C unless otherwise stated. For the LF355A/6A/7A, these specifications apply for +15V ≤ V_S ≤ +20V, 0°C ≤ T_A ≤ +70°C and T_{HIGH} = +70°C, and for the LF355/6/7 these specifications apply for V_S = +15V and 0°C ≤ T_A ≤ +70°C. V_{OS}, I_B and I_{OS} are measured at V_{CM} = 0.

NOTE 4: The Temperature Coefficient of the adjusted input offset voltage changes only a small amount (0.5μV/°C typically for each mV of adjustment from its original unadjusted value. Common-mode rejection and open loop voltage gain are also unaffected by offset adjustment.

NOTE 5: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_J. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, Pd. $T_j = T_A + \Theta_{jA} Pd$ where Θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

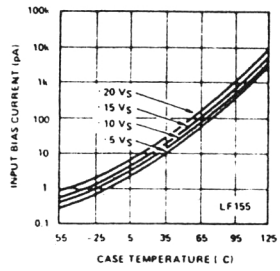
NOTE 6: Supply Voltage Rejection is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.

NOTE 7: Settling time is defined here, for a unity gain inverter connection using 2 kΩ resistors for the LF155/6. It is the time required for error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value from the time a 10V step input is applied to the inverter. For the LF157, A_V = −5, the feedback resistor from output to input is 2 kΩ and the output step is 10V (See Settling Time Test Circuit, page 9).

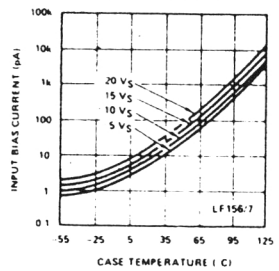
TYPICAL DC PERFORMANCE CHARACTERISTICS

Curves are for LF155, LF156 and LF157 unless otherwise specified.

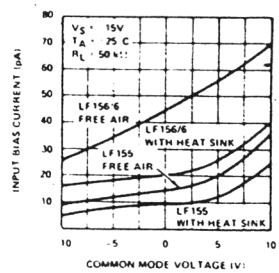
Input Bias Current



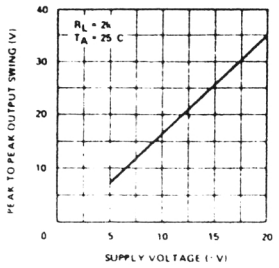
Input Bias Current



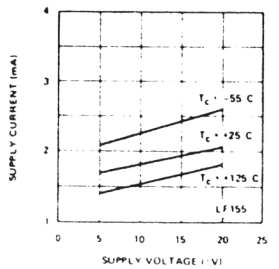
Input Bias Current



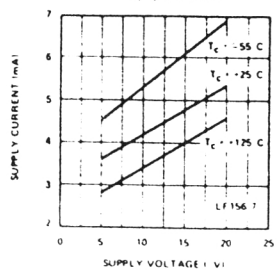
Voltage Swing



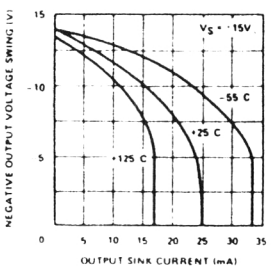
Supply Current



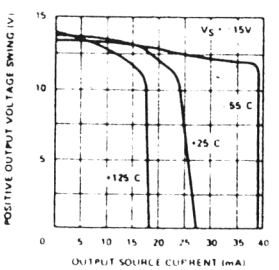
Supply Current



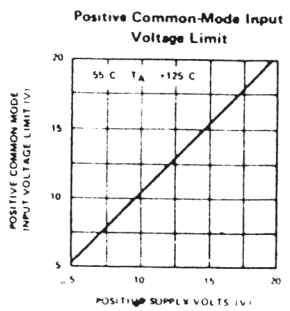
Negative Current Limit



Positive Current Limit

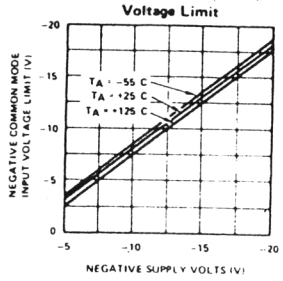


Positive Common-Mode Input Voltage Limit

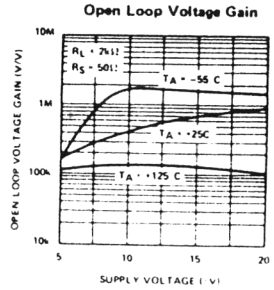


TYPICAL DC PERFORMANCE CHARACTERISTICS (CON'T)

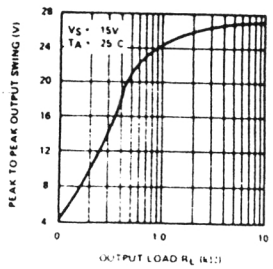
Negative Common-Mode Input Voltage Limit



Open Loop Voltage Gain

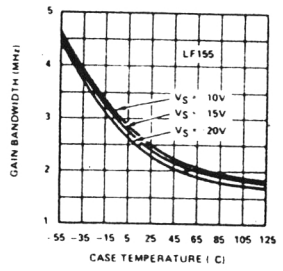


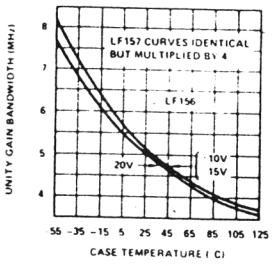
Output Voltage Swing



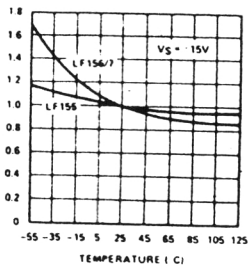
TYPICAL AC PERFORMANCE CHARACTERISTICS

Gain Bandwidth

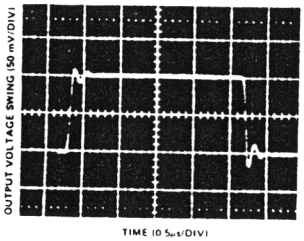




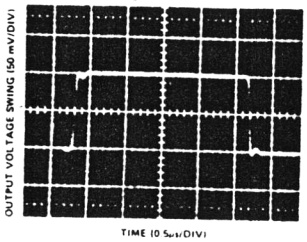
Normalized Slew Rate



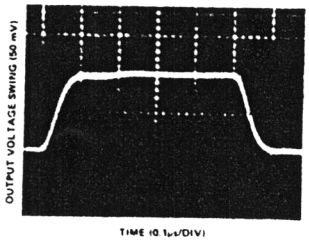
LF155 Small Signal Pulse Response, A_V = +1



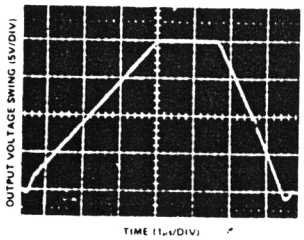
LF156 Small Signal Pulse Response, A_V = +1



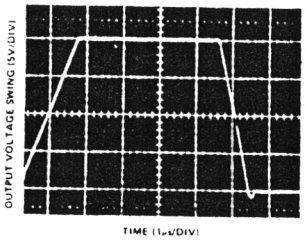
LF157 Small Signal Pulse Response, A_V = +5



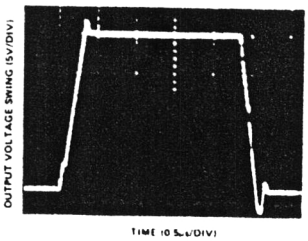
LF155 Large Signal Pulse Response, A_V = +1



LF156 Large Signal Pulse Response, A_V = +1

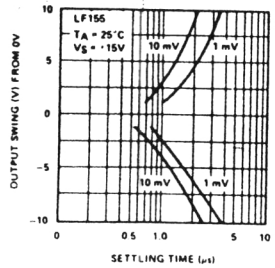


LF157 Large Signal Pulse Response, A_V = +5

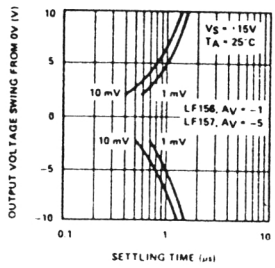


TYPICAL AC PERFORMANCE CHARACTERISTICS (CON'T)

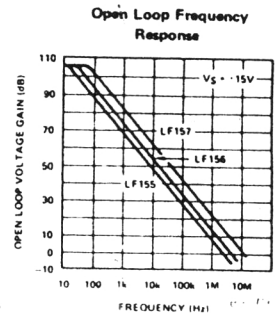
Inverter Settling Time



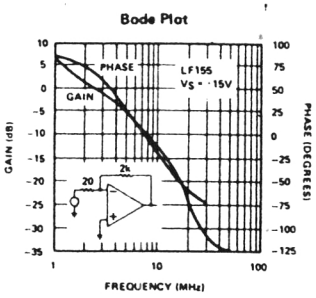
Inverter Settling Time



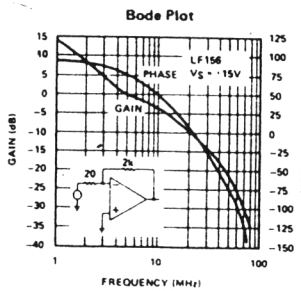
Open Loop Frequency Response



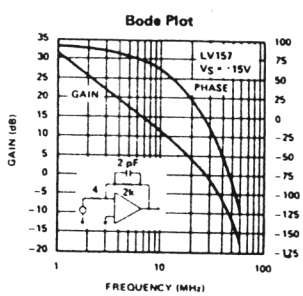
Bode Plot



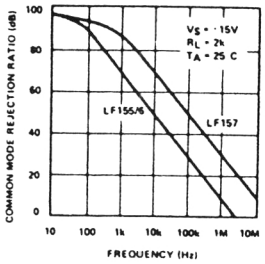
Bode Plot



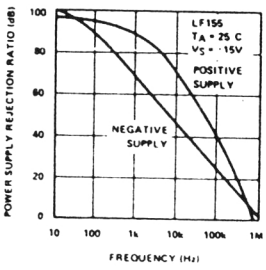
Bode Plot



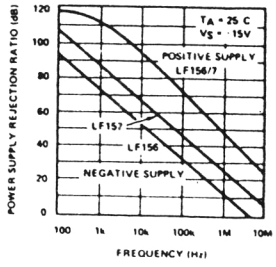
Common-Mode Rejection Ratio



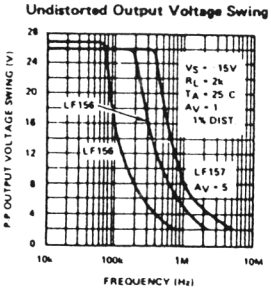
Power Supply Rejection Ratio



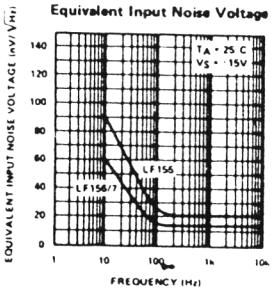
Power Supply Rejection Ratio



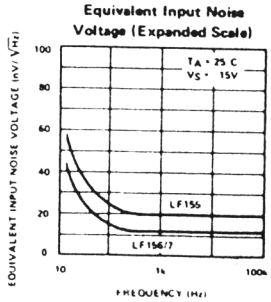
Undistorted Output Voltage Swing



Equivalent Input Noise Voltage

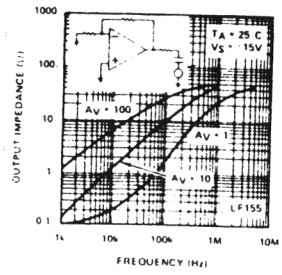


Equivalent Input Noise Voltage (Expanded Scale)

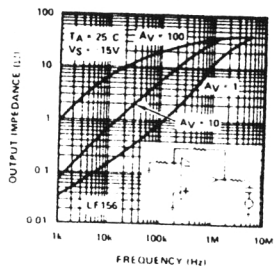


TYPICAL AC PERFORMANCE CHARACTERISTICS (CON'T)

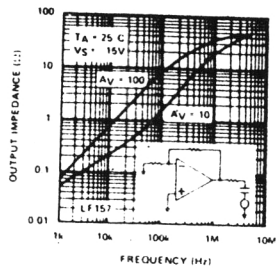
Output Impedance



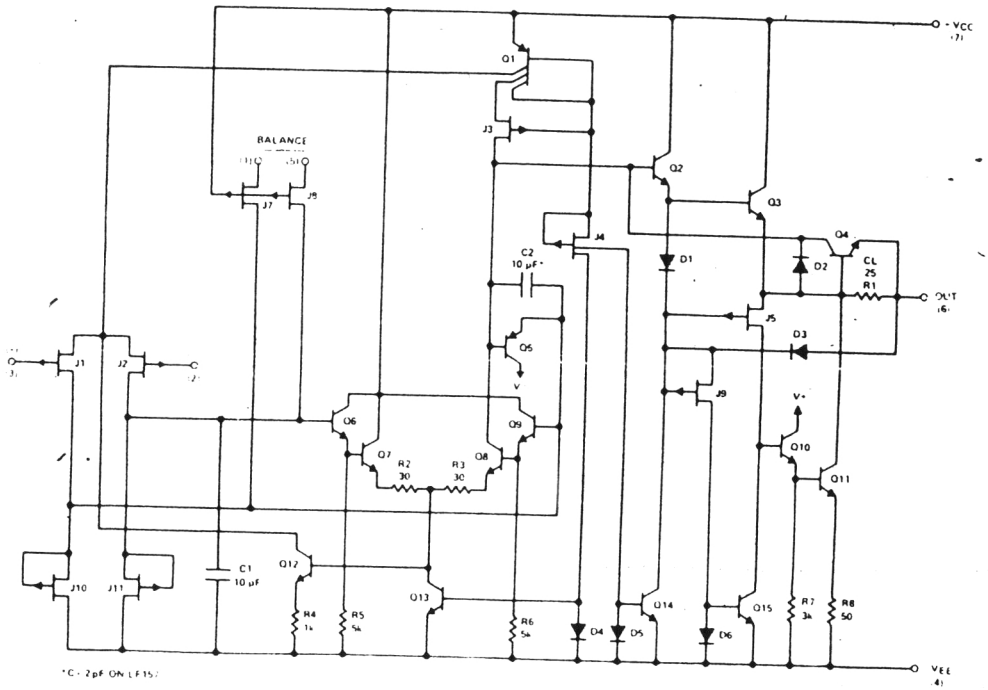
Output Impedance



Output Impedance

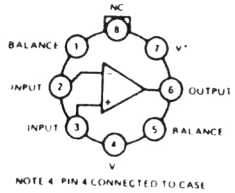


DETAILED SCHEMATIC



CONNECTION DIAGRAM

Metal Can Package



PRECISION VOLTAGE COMPARATORS

111
211
311

FEATURES

- Differential Input Voltage Range – ±30V
- Input Common Mode Voltage Range – ±14V
- Operating Power Supplies +5V to ±18V
- Input Offset Current – 20 nA max
- Input Offset Voltage – 3 mV max
- Output Flexibility – 35V; 50 mA; T^2L Compatible
- Strobed Output & Input Offset Adjustable

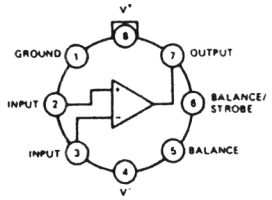
GENERAL DESCRIPTION

The 111 Series comparators are designed for precision applications where the input and output characteristics of 710 and 106 high speed comparators are not adequate for low level signal detection and high level output drive capability. They are designed to operate from supplies up to ±18V and single supplies down to +5V. The output is capable of driving TTL, RTL, DTL as well as MOS and lamps or relays. Input offset voltage balancing and TTL strobe capability are provided. Outputs can be wire OR'ed.

Switching speeds to TTL logic levels are typically 250 ns.

CONNECTION DIAGRAMS*

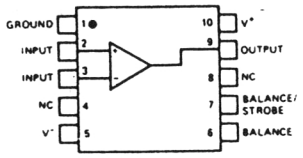
METAL CAN



NOTE Pin 4 connected to case

TOP VIEW

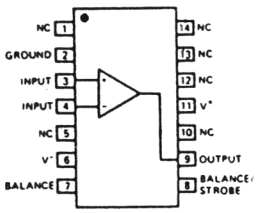
FLAT PACKAGE



NOTE Pin 5 connected to bottom of package

TOP VIEW

DUAL-IN-LINE

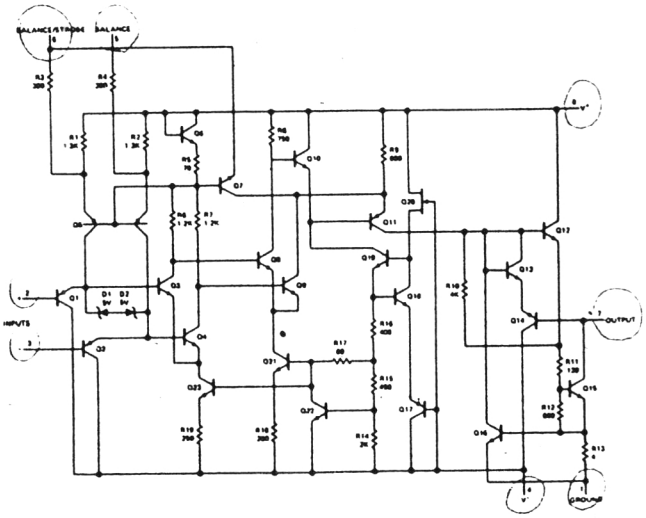


NOTE Pin 6 connected to bottom of package

TOP VIEW

*Pin connections shown on schematic diagram and typical applications are for TO-5 package.

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V_{84})	36V
Output to Negative Supply Voltage (V_{74}) 111, 211	50V
311	40V
Ground to Negative Supply Voltage (V_{14})	30V
Differential Input Voltage	±30V
Input Voltage (Note 1)	±15V
Power Dissipation (Note 2)	500 mW
Output Short Circuit Duration	10 sec
Operating Temperature Range 111	-55°C to +125°C
211	-25°C to +85°C
311	0°C to +70°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

ELECTRICAL CHARACTERISTICS (Note 3)

PARAMETER	CONDITIONS	111/211 MIN	111/211 TYP	111/211 MAX	311 MIN	311 TYP	311 MAX	UNITS
Input Offset Voltage (Note 4)	$T_A = 25°C$, $R_S \leq 50k$		0.7	3.0		2.0	7.5	mV
Input Offset Current (Note 4)	$T_A = 25°C$		4.0	10		6.0	50	nA
Input Bias Current	$T_A = 25°C$		60	100		100	250	nA
Voltage Gain	$T_A = 25°C$		200			200		V/mV
Response Time (Note 5)	$T_A = 25°C$		200			200		ns
Saturation Voltage	$T_A = 25°C$							
	$V_{IN} \leq -5$ mV, $I_{OUT} = 50$ mA		0.75	1.5				
	$V_{IN} < -10$ mV, $I_{OUT} = 50$ mA					0.75	1.5	V
Strobe on Current	$T_A = 25°C$		3.0			3.0		mA
Output Leakage Current (Note 6)	$T_A = 25°C$							
	$V_{IN} \geq 5$ mV, $V_{OUT} = 35V$		0.2	10				
	$V_{IN} \geq 10$ mV, $V_{OUT} = 35V$					0.2	50	nA
Input Offset Voltage (Note 4)	$R_S \leq 50k$			4.0			10	mV
Input Offset Current (Note 4)				20			70	nA
Input Bias Current				150			300	nA
Input Voltage Range			±14			±14		V
Saturation Voltage	$V^+ \geq 4.5V$, $V^- = 0$							
	$V_{IN} \leq -6$ mV, $I_{SINK} \leq 8$ mA		0.23	0.4				
	$V_{IN} \leq -10$ mV, $I_{SINK} \leq 8$ mA					0.23	0.4	V
Output Leakage Current (Note 6)	$V_{IN} \geq 5$ mV, $V_{OUT} = 35V$		0.1	0.5				μA
Positive Supply Current	$T_A = 25°C$		5.1	6.0		5.1	7.5	mA
Negative Supply Current	$T_A = 25°C$		4.1	5.0		4.1	5.0	mA

NOTE 1: This rating applies for ±15V supplies. The positive input voltage limit is 30V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30V below the positive supply, whichever is less.

NOTE 2: The maximum junction temperature of the 111 is 150°C, that of the 211 is 110°C while that of the 311 is 85°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case. For the flat package, the derating is based on a thermal resistance of 185°C/W when mounted on a 1/16-inch-thick epoxy glass board with ten, 0.03-inch-wide, 2-ounce copper conductor. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

NOTE 3: These specifications apply for V_S = ±15V and over the operating temperature range, unless otherwise stated. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5V supply up to ±15V supplies.

NOTE 4: The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1 mA load. Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.

NOTE 5: The response time specified (see definitions) is for a 100 mV input step with 5 mV overdrive.

NOTE 6: This specification applies for Pin 1 @ -15V, Pin 7 @ +20V

MOTOROLA

MC14534B

CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

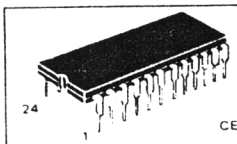
REAL TIME

5-DECADE COUNTER

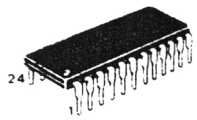
REAL TIME 5-DECADE COUNTER

The MC14534B is a complementary MOS circuit composed of five decade ripple counters that have their respective outputs time multiplexed using an internal scanner. Outputs of each counter are selected by the scanner and appear on four BCD pins. The selected decade is indicated by a logic high on the appropriate digit select pin. Both BCD and digit select outputs have three-state controls providing an "open-circuit" when these controls are high and allowing time multiplexing. Cascading may be accomplished by using the carry-out pin. The counters and scanner can be independently reset by applying a high to the counter master reset (MR) and the scanner reset (SR). The MC14534B was specifically designed for application in real time or event counters where continual updating and multiplexed displays are used.

- Four Operating Modes (See truth table)
- Input Error Detection Circuit
- Clock Conditioning Circuits for Slow Transition Inputs
- Counter Sequences on Positive Transition of Clock A
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range



L SUFFIX
CERAMIC PACKAGE
CASE 623

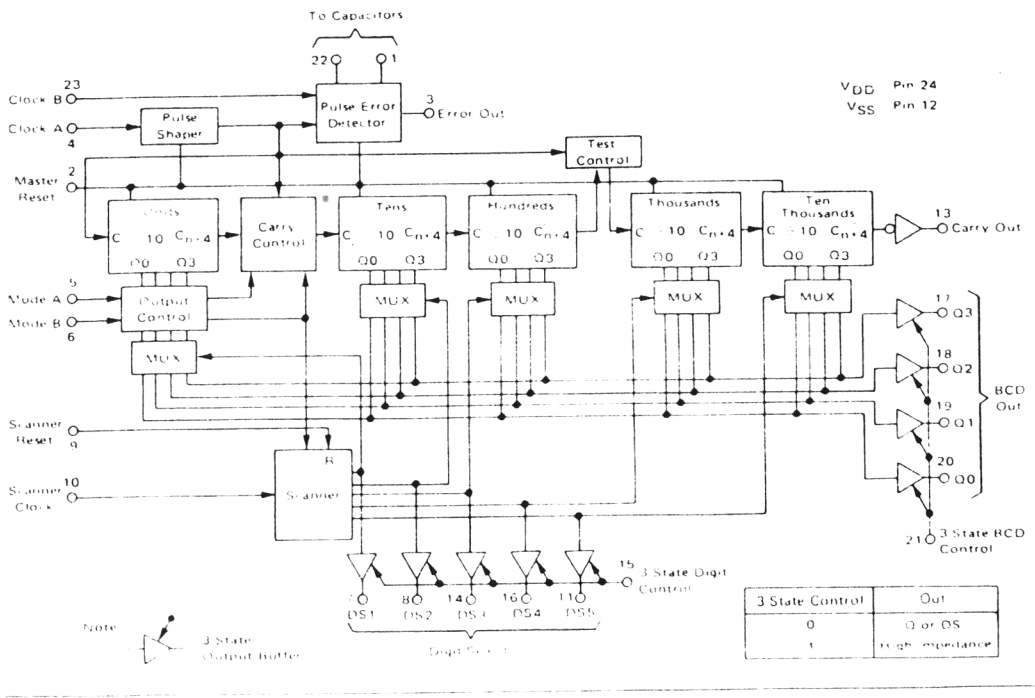


P SUFFIX
PLASTIC PACKAGE
CASE 709

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

BLOCK DIAGRAM



MC14534B

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range AL Device	T_A	-55 to +125	°C
CL/CP Device		-40 to +85	
Storage Temperature Range	T_{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95		
		15	14.95	–	14.95	15	–	14.95		
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	1.0		1.0	1.5		–	1.0	
(V_O = 9.0 or 1.0 Vdc)		10	2.0		2.0	3.0		–	2.0	
(V_O = 13.5 or 1.5 Vdc)		15	3.0		3.0	4.5		–	3.0	
(V_O = 0.5 or 4.5 Vdc) "1" Level	V_{IH}	5.0	4.0		4.0	3.5	–	4.0		Vdc
(V_O = 1.0 or 9.0 Vdc)		10	8.0		8.0	7.0	–	8.0		
(V_O = 1.5 or 13.5 Vdc)		15	12		12	11	–	12		
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-1.2		-1.0	-1.7	–	-0.7		
(V_{OH} = 4.6 Vdc)		5.0	-0.25		-0.2	-0.36	–	-0.14		
(V_{OH} = 9.5 Vdc)		10	-0.62		-0.5	-0.9	–	-0.35		
(V_{OH} = 13.5 Vdc)		15	-1.8		-1.5	-3.5	–	-1.1		
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64		0.51	0.88	–	0.36		mAdc
(V_{OL} = 0.5 Vdc)		10	1.6		1.3	2.25	–	0.9		
(V_{OL} = 1.5 Vdc)		15	4.2		3.4	8.8	–	2.4		
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-1.0		-0.8	-1.7	–	0.6		
(V_{OH} = 4.6 Vdc)		5.0	-0.2		-0.16	-0.36	–	-0.12		
(V_{OH} = 9.5 Vdc)		10	-0.5		-0.4	-0.9	–	-0.3		
(V_{OH} = 13.5 Vdc)		15	-1.4		-1.2	-3.5	–	-1.0		
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52		0.44	0.88	–	0.36		mAdc
(V_{OL} = 0.5 Vdc)		10	1.3		1.1	2.25	–	0.9		
(V_{OL} = 1.5 Vdc)		15	3.6		3.0	8.8	–	2.4		
Output Drive Current Pins 1 and 22 (AL Device)										mAdc
(V_{OH} = 2.5 Vdc) Source	I_{OH}	5.0	-0.31		-0.25	-0.8	–	0.17		
(V_{OH} = 9.5 Vdc)		10	-0.31		-0.25	0.4	–	0.17		
(V_{OH} = 13.5 Vdc)		15	-0.9		-0.75	-1.6	–	-0.51		
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.024		0.02	0.03	–	0.014		mAdc
(V_{OL} = 0.5 Vdc)		10	0.06		0.05	0.09	–	0.035		
(V_{OL} = 1.5 Vdc)		15	1.3		0.25	1.63	–	0.175		
Output Drive Current – Pins 1 and 22 (CL/CP Device)										mAdc
(V_{OH} = 2.5 Vdc) Source	I_{OH}	5.0	-0.11		-0.10	0.8	–	0.08		
(V_{OH} = 9.5 Vdc)		10	-0.11		-0.10	-0.4	–	-0.08		
(V_{OH} = 13.5 Vdc)		15	-0.33		-0.30	-1.6	–	0.24		
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.012		0.01	0.02	–	0.008		mAdc
(V_{OL} = 0.5 Vdc)		10	0.03		0.025	0.05	–	0.02		
(V_{OL} = 1.5 Vdc)		15	0.14		0.12	1.35	–	0.10		
Input Current (AL Device)	I_{in}	15		±0.1		±0.00001	±0.1		±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15		±0.3		±0.00001	±0.3		±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}					5.0	7.5			pF

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device
T_{high} = +125°C for AL Device, +85°C for CL/CP Device

#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level:
1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

MC14534B

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0 10 15	– – –	5.0 10 20	– – –	0.010 0.020 0.030	5.0 10 20	– – –	150 300 600	μAdc
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0 10 15	– – –	50 100 200	– – –	0.010 0.020 0.030	50 100 200	– – –	375 750 1500	μAdc
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0 10 15	$I_T = (0.5\ \mu A/kHz)\ f + I_{DD}$ $I_T = (1.0\ \mu A/kHz)\ f + I_{DD}$ $I_T = (1.5\ \mu A/kHz)\ f + I_{DD}$		Scan Oscillator Frequency = 1 kHz					μAdc
Three State Leakage Current (AL Device)	I_{TL}	15		±0.1		±0.00001	±0.1		±3.0	μAdc
Three State Leakage Current (CL CP Device)	I_{TL}	15		±1.0		±0.00001	±1.0		±7.5	μAdc

†To calculate total supply current at loads other than 50 pF: $I_T(C_L) = I_T(50\ pF) + 1 \times 10^{-3} (C_L - 50) V_{DD} f$ where I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

**The formulas given are for the typical characteristics only at 25°C

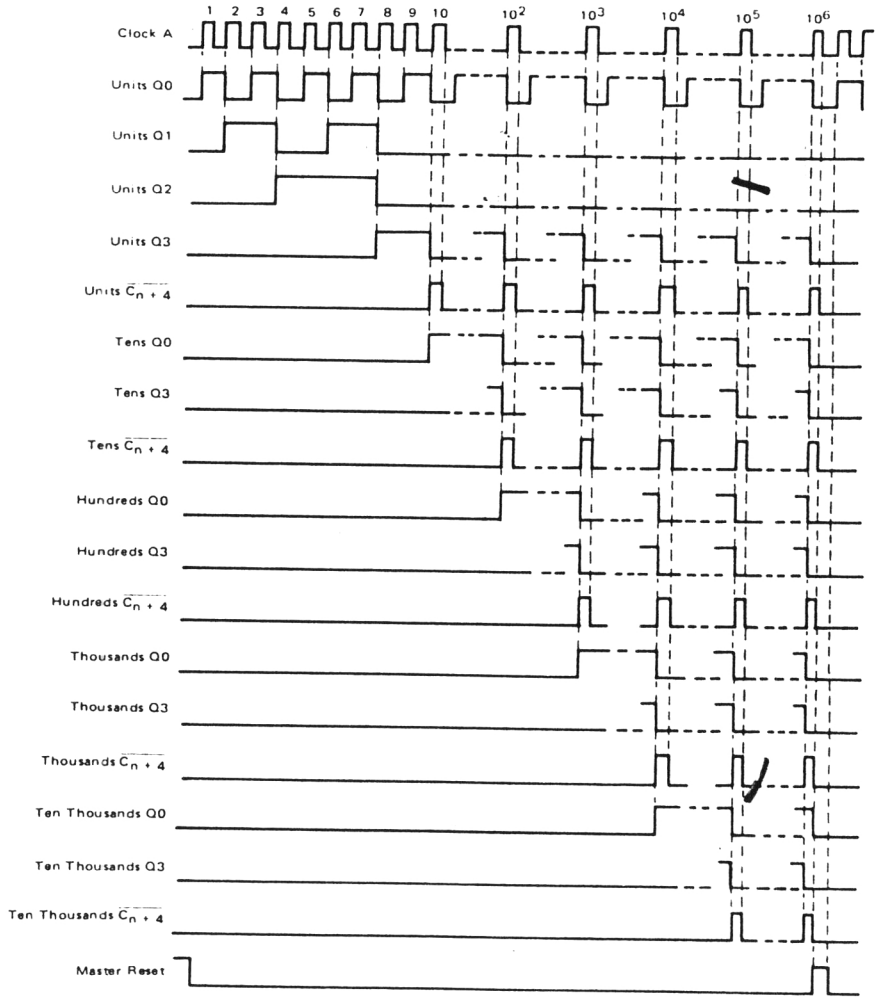
SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 95 ns		5.0	–	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 78 ns		10	–	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 68 ns		15	–	65	130	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 117 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 89 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 67 ns		15	–	40	80	
Propagation Delay Time, Clock to Q	t_{PLH}, t_{PHL}					μs
t_{PLH}, t_{PHL} = (1.8 ns/pF) C_L + 4.0 μs		5.0	–	4.0	8.0	
t_{PLH}, t_{PHL} = (0.8 ns/pF) C_L + 1.5 μs		10	–	1.5	3.0	
t_{PLH}, t_{PHL} = (0.6 ns/pF) C_L + 1.0 μs		15	–	1.0	2.25	
Clock to Carry Out	t_{PLH}					μs
t_{PLH} = (1.8 ns/pF) C_L + 3.3 μs		5.0	–	3.3	6.6	
t_{PLH} = (0.8 ns/pF) C_L + 1.1 μs		10	–	1.1	2.2	
t_{PLH} = (0.6 ns/pF) C_L + 0.8 μs		15	–	0.8	1.7	
Master Reset to Q	t_{PHL}					μs
t_{PHL} = (1.8 ns/pF) C_L + 1.8 μs		5.0	–	1.8	3.6	
t_{PHL} = (0.8 ns/pF) C_L + 0.6 μs		10	–	0.6	1.2	
t_{PHL} = (0.6 ns/pF) C_L + 0.5 μs		15	–	0.5	0.9	
Master Reset to Error Out	t_{PHL}					μs
t_{PHL} = (1.8 ns/pF) C_L + 0.57 μs		5.0	–	0.6	1.5	
t_{PHL} = (0.8 ns/pF) C_L + 0.19 μs		10	–	0.2	.5	
t_{PHL} = (0.6 ns/pF) C_L + 0.11 μs		15	–	0.12	0.38	
Scanner Clock to Q	t_{PLH}, t_{PHL}					μs
t_{PLH}, t_{PHL} = (1.8 ns/pF) C_L + 1.8 μs		5.0	–	1.8	3.6	
t_{PLH}, t_{PHL} = (0.8 ns/pF) C_L + 0.6 μs		10	–	0.6	1.2	
t_{PLH}, t_{PHL} = (0.6 ns/pF) C_L + 0.5 μs		15	–	0.5	0.9	
Scanner Clock to Digit Select	t_{PLH}, t_{PLH},					μs
t_{PHL}, t_{PLH} = (1.8 ns/pF) C_L + 1.5 μs		5.0	–	1.5	3.0	
t_{PHL}, t_{PLH} = (0.8 ns/pF) C_L + 0.5 μs		10	–	0.5	1.0	
t_{PHL}, t_{PLH} = (0.6 ns/pF) C_L + 0.4 μs		15	–	0.4	0.75	
Clock Pulse Frequency	f_{cl}	5.0	–	1.0	0.5	MHz
		10	–	3.0	1.0	
		15	–	5.0	1.2	
Clock or Scanner Clock Pulse Width	t_{WH}	5.0	1000	500	–	ns
		10	500	190	–	
		15	375	125	–	
Master Reset Pulse Width	$t_{WH(R)}$	5.0	2000	900	–	ns
		10	600	300	–	
		15	450	250	–	

*The formula given is for the typical characteristics only.

MC14534B

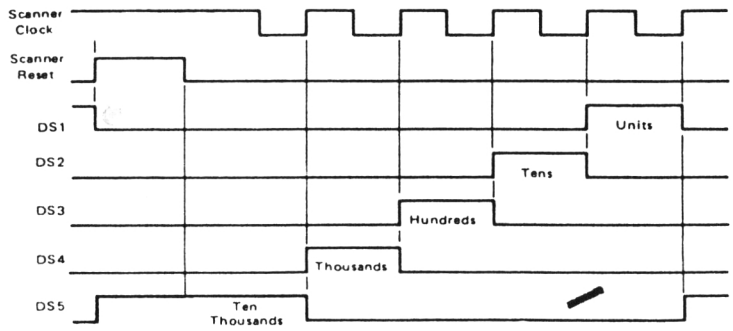
COUNTER TIMING DIAGRAM



MODE CONTROL TRUTH TABLE

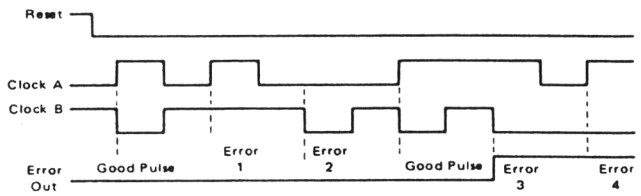
Mode A	Mode B	First Decade Output	Carry to Second Stage	Application
0	0	Normal Count and Display	At 9 to 0 transition of first decade	5 Decade Counter
0	1	Inhibited	Input Clock	Test Mode Clock directly into stages 1, 2, and 4
1	1	Inhibited	At 4 to 5 transition of first decade	ϕ decade counter with ÷ 10 and roundoff at front end
1	0	Counts 3,4,5,6,7 → 5 Counts 8,9,0,1,2 → 0	At 7 to 8 transition of first decade	4 decade counter with 1/2 pence capability

SCANNER TIMING DIAGRAM



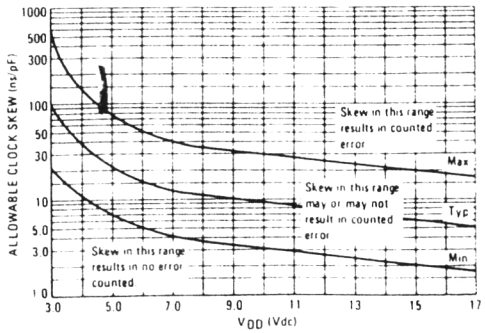
Note If Mode B = 1, the first decade is inhibited and S1 will not go high, and the cycle will be shortened to four stages.
DS5 is selected automatically when Scanner Reset goes high.

ERROR DETECTION TIMING DIAGRAM



Note Error detector looks for inverted pulse on Clock B. Whenever a positive edge at Clock A is not accompanied by a negative pulse at Clock B (or vice-versa) within a time period of the one-shots an error is counted. Three errors result in Error Out to go to a "1". If error detection is not needed, tie Clock B high or low and leave Pins 1 and 22 unconnected.

CLOCK SKEW RANGE

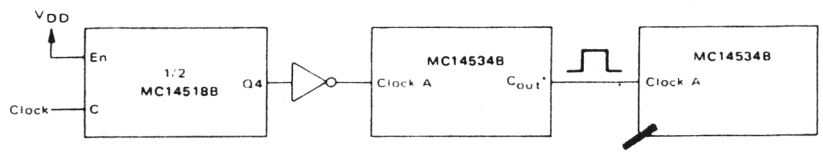


Notes

1. The skew is the time difference between the low-to-high transition of C_A to the high-to-low transition of C_B or vice-versa. Capacitors C1 = C22 tied from pins 1 and 22 to V_{SS}.
2. This graph is accurate for C1 = C22 $\geq$ 100 pF.
3. When the error detection circuitry is not used, pins 1 and 22 are left open.

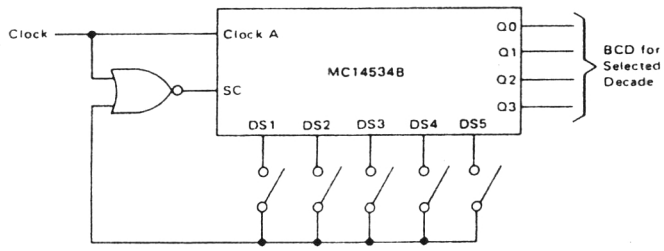
APPLICATIONS INFORMATION

FIGURE 1 – CASCADE OPERATION



*Carry Out is high for a single clock period when all five BCD decades go to zero. (Carry Out also goes high when MR is applied.)

FIGURE 2 – FORCING A DECADE TO THE Q OUTPUTS



When the Q outputs of a given decade are required, this configuration will lock up the selected decade within four clock cycles. The select line feed back may be hardwired or switched.

MOTOROLA

MC14528B

CMOS MSI

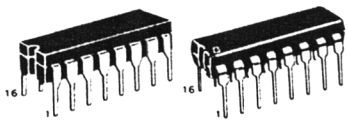
(LOW-POWER COMPLEMENTARY MOS)

DUAL RETRIGGERABLE/RESETTABLE MONOSTABLE MULTIVIBRATOR

DUAL MONOSTABLE MULTIVIBRATOR

The MC14528B is a dual, retriggerable, resettable monostable multivibrator. It may be triggered from either edge of an input pulse, and will produce an accurate output pulse over a wide range of widths, the duration and accuracy of which are determined by the external timing components, C_X and R_X.

- Separate Reset Available
- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Diode Protection on All Inputs
- Triggerable from Leading or Trailing Edge Pulse
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- See MC14538B Data Sheet for Applications Requiring Precise Control of Output Pulse Width



L SUFFIX	P SUFFIX
CERAMIC PACKAGE	PLASTIC PACKAGE
CASE 620	CASE 648

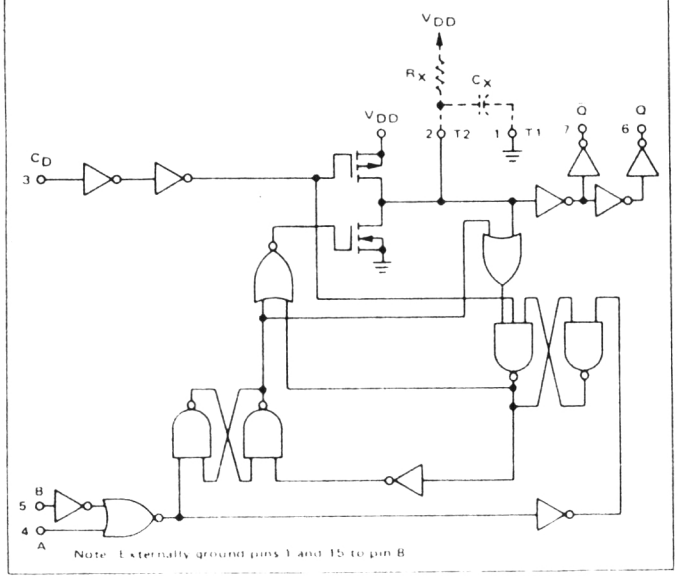
ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

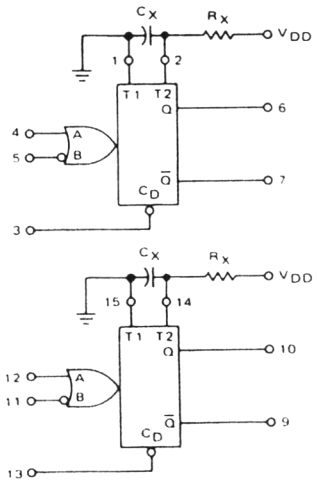
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

LOGIC DIAGRAM
(1/2 of Device Shown)



Note: Externally ground pins 1 and 15 to pin 8.

BLOCK DIAGRAM



R_X and C_X are external components.

V_{DD} = Pin 16
V_{SS} = Pin 8

MC14528B

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0		0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10		0.05	–	0	0.05	–	0.05	
		15		0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−1.2	–	−1.0	−1.7	–	−0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.25	–	−0.2	−0.36	–	−0.14	–	
(V_{OH} = 9.5 Vdc)		10	−0.62	–	−0.5	−0.9	–	−0.35	–	
(V_{OH} = 13.5 Vdc)		15	−1.8	–	−1.5	−3.5	–	−1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−1.0	–	−0.8	−1.7	–	−0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.2	–	−0.16	−0.36	–	−0.12	–	
(V_{OH} = 9.5 Vdc)		10	−0.5	–	−0.4	−0.9	–	−0.3	–	
(V_{OH} = 13.5 Vdc)		15	−1.4	–	−1.2	−3.5	–	−1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
**Total Supply Current at an external load Capacitance (C_L) and at external timing capacitance (C_X), use the formula –	I_T	–	$I_T(C_L, C_X) = [(C_L + 0.36C_X)V_{DD}f + 2\times10^{-8} R_X C_X (V_{DD}-2)^2 f] \times 10^{-3}$ where I_T in μA (per circuit), C_L and C_X in pF, R_X in megohms, V_{DD} in Vdc, f in kHz is input frequency.							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination

Noise Margin for both "1" and "0" level		
1.0 Vdc min @ V_{DD}	5.0 Vdc	
2.0 Vdc min @ V_{DD}	10 Vdc	
2.5 Vdc min @ V_{DD}	15 Vdc	

**The formulas given are for the typical characteristics only at 25°C

SWITCHING CHARACTERISTICS** (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	C_X pF	R_X kΩ	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}	–	–					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns				5.0	–	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns				10	–	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns				15	–	65	130	
Output Fall Time	t_{THL}	–	–					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns				5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns				10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns				15	–	40	80	
Turn-Off, Turn-On Delay Time – A or B to Q or Q̄	t_{PLH}, t_{PHL}	15	5.0					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 240 ns				5.0	–	325	650	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 87 ns				10	–	120	240	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 65 ns				15	–	90	180	
Turn-Off, Turn-On Delay Time – A or B to Q or Q̄	t_{PLH}, t_{PHL}	1000	10					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 620 ns				5.0	–	705	–	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 257 ns				10	–	290	–	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 185 ns				15	–	210	–	
Minimum Input Pulse Width – A or B	t_{WH}	15	5.0	5.0	–	70	150	ns
				10	–	30	75	
				15	–	30	55	
	t_{WL}	1000	10	5.0	–	70	–	ns
				10	–	30	–	
				15	–	30	–	
Output Pulse Width – Q or Q̄	t_W	15	5.0	5.0	–	550	–	ns
(For C_X < 0.01 μF use graph for appropriate V_{DD} level.)				10	–	350	–	
				15	–	300	–	
Output Pulse Width – Q or Q̄	t_W	10,000	10	5.0	–	30	±15	μs
(For C_X > 0.01 μF use formula:				10	–	50	±40	
t_W = 0.2 R_X C_X Ln [V_{DD} – V_{SS}])†				15	–	55	±40	
Pulse Width Match between Circuits in the same package	t1 - t2	10,000	10	5.0	–	6.0	25	%
				10	–	8.0	35	
				15	–	8.0	35	
Reset Propagation Delay – C_D to Q or Q̄	t_{PLH}, t_{PHL}	15	5.0	5.0	–	325	600	ns
				10	–	90	225	
				15	–	60	170	
		1000	10	5.0	–	1000	–	ns
				10	–	300	–	
				15	–	250	–	
Minimum Retrigger Time	t_{rr}	15	5.0	5.0	–	0	–	ns
				10	–	0	–	
				15	–	0	–	
		1000	10	5.0	–	0	–	ns
				10	–	0	–	
				15	–	0	–	
						Min		
External Timing Resistance	R_X	–	–	–	5.0	1000	1000	kΩ
External Timing Capacitance	C_X	–	–	–		No Limits		μF

** The formula given is for the typical characteristics only.

† R_X is in Ohms, C_X is in farads, V_{DD} and V_{SS} in volts, PW_{out} in seconds.

MOTOROLA

MC14511B

BCD-TO-SEVEN SEGMENT LATCH/DECODER/DRIVER

The MC14511B BCD-to-seven segment latch/decoder/driver is constructed with complementary MOS (CMOS) enhancement mode devices and NPN bipolar output drivers in a single monolithic structure. The circuit provides the functions of a 4-bit storage latch, an 8421 BCD-to-seven segment decoder, and an output drive capability. Lamp test ($\overline{LT}$), blanking ($\overline{BI}$), and latch enable (LE) inputs are used to test the display, to turn-off or pulse modulate the brightness of the display, and to store a BCD code, respectively. It can be used with seven-segment light emitting diodes (LED), incandescent, fluorescent, gas discharge, or liquid crystal readouts either directly or indirectly.

Applications include instrument (e.g., counter, DVM, etc.) display driver, computer/calculator display driver, cockpit display driver, and various clock, watch, and timer uses.

- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Low Logic Circuit Power Dissipation
- High-Current Sourcing Outputs (Up to 25 mA)
- Latch Storage of Code
- Blanking Input
- Lamp Test Provision
- Readout Blanking on all Illegal Input Combinations
- Lamp Intensity Modulation Capability
- Time Share (Multiplexing) Facility
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS}).

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Input Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	
Maximum Output Drive Current (Source) per Output	I_{OHmax}	25	mA
Maximum Continuous Output Power (Source) per Output ‡	P_{OHmax}	50	mW

‡ $P_{OHmax} = I_{OH}(V_{DD} - V_{OH})$

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. A destructive high current mode may occure if V_{in} and V_{out} is not constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

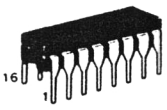
Due to the sourcing capability of this circuit, damage can occur to the device if V_{DD} is applied, and the outputs are shorted to V_{SS} and are at a logical 1. (See Maximum Ratings).

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

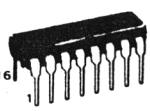
CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

BCD-TO-SEVEN SEGMENT LATCH/DECODER/DRIVER



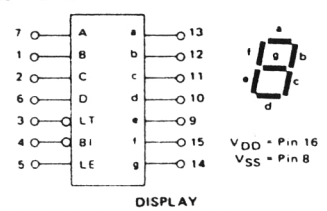
L SUFFIX
CERAMIC PACKAGE
CASE 620



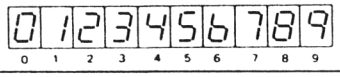
P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range



DISPLAY



TRUTH TABLE

INPUTS							OUTPUTS							
LE	$\overline{BI}$	$\overline{LT}$	D	C	B	A	a	b	c	d	e	f	g	DISPLAY
X	X	0	X	X	X	X	1	1	1	1	1	1	1	8
X	0	1	X	X	X	X	0	0	0	0	0	0	0	Blank
0	1	1	0	0	0	0	1	1	1	1	1	1	0	0
0	1	1	0	0	0	1	0	1	1	0	0	0	0	1
0	1	1	0	0	1	0	1	1	0	1	1	0	1	2
0	1	1	0	0	1	1	1	1	1	1	0	0	1	3
0	1	1	0	1	0	0	0	1	1	0	0	1	1	4
0	1	1	0	1	0	1	1	0	1	1	0	1	1	5
0	1	1	0	1	1	0	0	0	1	1	1	1	1	6
0	1	1	0	1	1	1	1	1	1	0	0	0	0	7
0	1	1	1	0	0	0	1	1	1	1	1	1	1	8
0	1	1	1	0	0	1	1	1	1	0	0	1	1	9
0	1	1	1	0	1	0	0	0	0	0	0	0	0	Blank
0	1	1	1	0	1	1	0	0	0	0	0	0	0	Blank
0	1	1	1	1	0	0	0	0	0	0	0	0	0	Blank
0	1	1	1	1	0	1	0	0	0	0	0	0	0	Blank
0	1	1	1	1	1	0	0	0	0	0	0	0	0	Blank
0	1	1	1	1	1	1	0	0	0	0	0	0	0	Blank
1	1	1	X	X	X	X	*							*

X = Don't Care

*Depends upon the BCD code previously applied when LE = 0

MOTOROLA

MC14518B
MC14520B

CMOS MSI

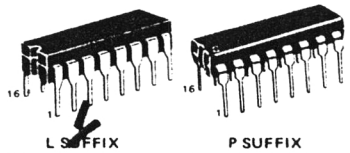
(LOW-POWER COMPLEMENTARY MOS)

DUAL BCD UP COUNTER
(MC14518B)
DUAL BINARY UP COUNTER
(MC14520B)

DUAL UP COUNTERS

The MC14518B dual BCD counter and the MC14520B dual binary counter are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Each consists of two identical, independent, internally synchronous 4-stage counters. The counter stages are type D flip-flops, with interchangeable Clock and Enable lines for incrementing on either the positive-going or negative-going transition as required when cascading multiple stages. Each counter can be cleared by applying a high level on the Reset line. In addition, the MC14518B will count out of all undefined states within two clock periods. These complementary MOS up counters find primary use in multi-stage synchronous or ripple counting applications requiring low power dissipation and/or high noise immunity.

- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Low Input Capacitance = 5.0 pF typical
- Internally Synchronous for High Internal and External Speeds
- Logic Edge-Clocked Design – Incremented on Positive Transition of Clock or Negative Transition on Enable
- 6.0 MHz Counting Rate
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

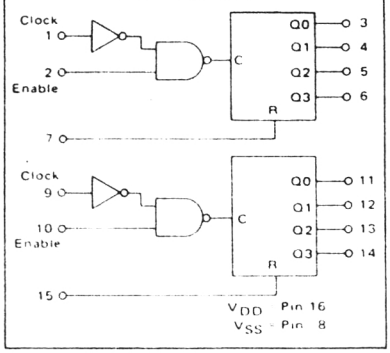
ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

BLOCK DIAGRAM



TRUTH TABLE

CLOCK	ENABLE	RESET	ACTION
⌐¬	1	0	Increment Counter
0	¬⌐	0	Increment Counter
¬⌐	X	0	No Change
X	⌐¬	0	No Change
⌐¬	0	0	No Change
1	¬⌐	0	No Change
X	X	1	Q0 thru Q3 = 0

X = Don't Care

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

MOTOROLA

MC14013B

CMOS SSI

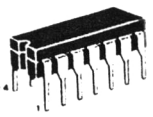
(LOW-POWER COMPLEMENTARY MOS)

DUAL TYPE D FLIP-FLOP

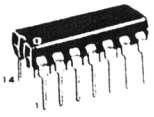
DUAL TYPE D FLIP-FLOP

The MC14013B dual type D flip-flop is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Each flip-flop has independent Data, (D), Direct Set, (S), Direct Reset, (R), and Clock (C) inputs and complementary outputs (Q and $\overline{Q}$). These devices may be used as shift register elements or as type T flip-flops for counter and toggle applications.

- Static Operation
- Quiescent Current = 2.0 nA/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Single Supply Operation
- Toggle Rate = 4 MHz typical @ 5 Vdc
- Logic Edge-Clocked Flip-Flop Design
  Logic state is retained indefinitely with clock level either high or low; information is transferred to the output only on the positive-going edge of the clock pulse
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4013B



L SUFFIX
CERAMIC PACKAGE
CASE 632



P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

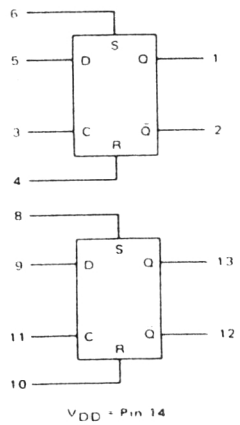
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range AL Device CL CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLE

INPUTS				OUTPUTS		
CLOCK↑	DATA	RESET	SET	Q	$\overline{Q}$	
⌐	0	0	0	0	1	
⌐	1	0	0	1	0	
¬	x	0	0	Q	$\overline{Q}$	No Change
x	x	1	0	0	1	
x	x	0	1	1	0	
x	x	1	1	1	1	

X = Don't Care
↑ = Level Change

BLOCK DIAGRAM



V_{DD} = Pin 14
V_{SS} = Pin 7

MOTOROLA

MC14001B
Quad 2-Input NOR Gate

MC14002B
Dual 4-Input NOR Gate

MC14011B
Quad 2-Input NAND Gate

MC14012B
Dual 4-Input NAND Gate

MC14023B
Triple 3-Input NAND Gate

MC14025B
Triple 3-Input NOR Gate

MC14068B
8-Input NAND Gate

MC14071B
Quad 2-Input OR Gate

MC14072B
Dual 4-Input OR Gate

MC14073B
Triple 3-Input AND Gate

MC14075B
Triple 3-Input OR Gate

MC14078B
8-Input NOR Gate

MC14081B
Quad 2-Input AND Gate

MC14082B
Dual 4-Input AND Gate

B-SUFFIX SERIES CMOS GATES

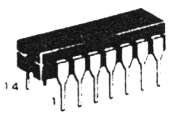
The B Series logic gates are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typ
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacements for Corresponding CD4000 Series B Suffix Devices

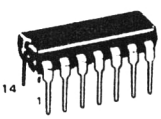
ORDERING INFORMATION

MC14XXXB — Suffix Denotes

- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range



L SUFFIX
CERAMIC PACKAGE
CASE 632



P SUFFIX
PLASTIC PACKAGE
CASE 646

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} +0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range AL Device CL, CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

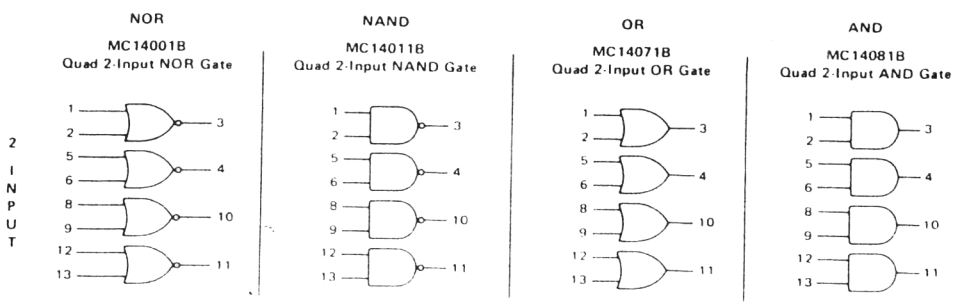
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

B-SERIES GATES

LOGIC DIAGRAMS



ภาคผนวก ข

การอินเวอร์สลาปลาสทรานสฟอร์ม

$$f(t) = \mathcal{L}^{-1}\left[F(S)\right]$$

1. $F(S) = \dfrac{s}{(s-a)(s-b)}$

$$= \frac{b/(b-a)}{s-b} - \frac{a/(b-a)}{s-a}$$

$$f(t) = \frac{be^{bt} - ae^{at}}{b-a}$$

2. $F(S) = \dfrac{1}{(s-a)(s-b)}$

$$= -\frac{1}{b-a}\frac{1}{s-a} + \frac{1}{b-a}\frac{1}{s-b}$$

$$f(t) = \frac{e^{bt} - e^{at}}{b-a}$$

3. $F(S) = \dfrac{s}{(s-a)(s-b)(s-c)}$

$$= \frac{a}{(b-a)(c-a)}\frac{1}{s-a} + \frac{b}{(a-b)(c-b)}\frac{1}{s-b} + \frac{c}{(a-c)(b-c)}\frac{1}{s-c}$$

$$f(t) = \frac{a}{(b-a)(c-a)}e^{at} + \frac{b}{(a-b)(c-b)}e^{bt} + \frac{c}{(a-c)(b-c)}e^{ct}$$

4. $F(S) = \dfrac{s^2}{(s-a)^2(s-b)^2}$

โดยใช้ทฤษฎี Convolution และ $\dfrac{be^{bt} - ae^{at}}{b-a} = \mathcal{L}^{-1}\left[\dfrac{s}{(s-a)(s-b)}\right]$

$$f(t) = \int_0^t \frac{be^{bu} - ae^{au}}{b-a} \cdot \frac{be^{b(t-u)} - ae^{a(t-u)}}{b-a}\, du$$

$$= \frac{1}{(a-b)^2}\left[\left(b^2t + \frac{2ab}{a-b}\right)e^{bt} + \left(a^2t - \frac{2ab}{a-b}\right)e^{at}\right]$$

5. $F(S) = \dfrac{s}{(s-a)^2(s-b)^2}$

$$\mathcal{L}^{-1}\left[\frac{s}{(s-a)(s-b)}\right] = \frac{be^{bt}-ae^{at}}{b-a}$$

$$\mathcal{L}^{-1}\left[\frac{1}{(s-a)(s-b)}\right] = \frac{e^{bt}-e^{at}}{b-a}$$

$$f(t) = \int_0^t \frac{be^{bu}-ae^{au}}{b-a} \cdot \frac{e^{b(t-u)}-e^{a(t-u)}}{b-a}\, du$$

$$\frac{1}{(a-b)^2}\left[(at-\frac{a+b}{a-b})e^{at} + (bt+\frac{a+b}{a-b})e^{bt}\right]$$

6. $F(S) = \dfrac{s^2}{(s-a)^2(s-b)^2(s-c)}$

โดยที่ $$\mathcal{L}^{-1}\left[\frac{s^2}{(s-a)^2(s-b)^2}\right] = \frac{1}{(a-b)^2}\left[(b^2t+\frac{2ab}{a-b})e^{bt} + (a^2t-\frac{2ab}{a-b})e^{at}\right]$$

$$\mathcal{L}^{-1}\left[\frac{1}{s-c}\right] = e^{ct}$$

เมื่อใช้ทฤษฎี Convolution

$$f(t) = \int_0^t \frac{1}{(a-b)^2}\left[(b^2u+\frac{2ab}{a-b})e^{bu} + (a^2u-\frac{2ab}{a-b})e^{au}\right].e^{c(t-u)}\, du$$

$$= \frac{1}{(a-b)^2}\left[\left\{\frac{a^2t}{a-c} - \frac{a^2}{(a-c)^2} - \frac{2ab}{(a-b)(a-c)}\right\} e^{at}\right.$$

$$+ \left\{\frac{b^2t}{b-c} - \frac{b^2}{(b-c)^2} - \frac{2ab}{(a-b)(b-c)}\right\} e^{bt}$$

$$\left. + \left\{\frac{a^2}{(a-c)^2} + \frac{b^2}{(b-c)^2} + \frac{2ab}{(a-b)(a-c)} - \frac{2ab}{(a-b)(b-c)}\right\} e^{ct}\right]$$

ภาคผนวก ค

รายการอุปกรณ์อิเลคทรอนิคส์

ค.1 ภาคขยายและตัดสัญญาณรบกวน (รูป 4.20)

วงจรรวม	IC_1	LF 356	JFET Input Operational Amplifier
	IC_2	LF 356	JFET input Operational Amplifier
	IC_3	LF 356	JFET Input Operational Amplifier
	IC_4	LM 311	Voltage Comparator
ความต้านทาน	R_f	22 MΩ	¼ W 5% Carbon film
	R_1	10 kΩ	
	R_2	100 kΩ	
	R_3	50 kΩ	
	R_4	25 kΩ	
	R_5	68 kΩ	
	R_6	68 kΩ	
	R_7	10 kΩ	
	R_{v1}	50 kΩ	Tenturn pot
ตัวเก็บประจุ	C	.001 μF	Ceramic
	C_f	4.7 pF	NPO
	C_1	.01 μF	Ceramic
	C_2	100 pF	Ceramic
	C_3	100 μF	Electrolyte
	C_4	47 μF	Electrolyte
	C_5	.01 μF	Ceramic
	C_6	.01 μF	Ceramic
	C_7	100 pF	Ceramic

ค.2 ภาคนับรังสี (รูป 4.21)

วงจรรวม

IC_5	MC14528	Dual Retriggerable/Resetable Monostable multivibrator
IC_6	MC14013	Dual Type D Flip-Flop
IC_7	MC14520	Dual Binary Counter
IC_8	MC14520	Dual Binary Counter
IC_9	MC14511	BCD-to Sevent Segment Latch/Decoder/Driver
IC_{10}	MC14534	Real Time 5-Decade Counter
IC_{11}	MC14534	Real Time 5-Decade Counter

ทรานซิสเตอร์ 2SC458

ความต้านทาน

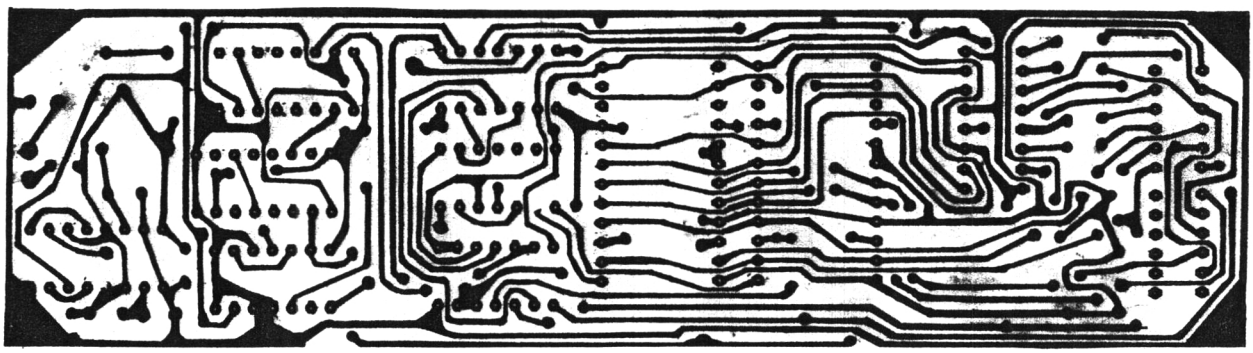
R_8	100 kΩ	¼ W 5% Carbon film
R_9	100 Ω×7	¼ W 5% Carbon film
R_{10}	1 MΩ	¼ W 5% Carbon film
R_{11}	10 kΩ	¼ W 5% Carbon film
R_{12}	10 kΩ	¼ W 5% Carbon film
R_{13}	1 kΩ	¼ W 5% Carbon film
R_{14}	100 Ω	¼ W 5% Carbon film
R_{v2}	50 kΩ	Tenturn pot.

ตัวเก็บประจุ

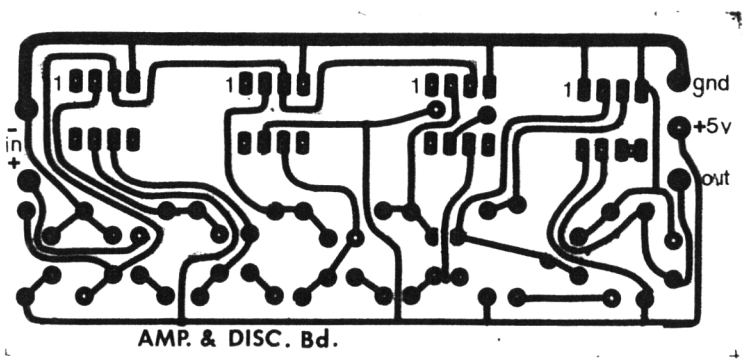
C_8	0.01 μF	Tantalum
C_9	47 μF	Electrolyte

ภาคผนวก ง.

ต้นแบบแผ่นวงจรพิมพ์



รูป ง.1 แผ่นวงจรพิมพ์ของภาคนับรังสี



รูป ง.2 แผ่นวงจรพิมพ์ของภาคขยายและศัดสัญญาณรบกวน

ประวัติผู้เขียน

นาย อุดม วรศรัณย์ เกิดเมื่อวันที่ 9 ตุลาคม พ.ศ. 2500 ณ กรุงเทพมหานคร สำเร็จการศึกษาระดับปริญญาบัณฑิต จากภาควิชาวิศวกรรมไฟฟ้า คณะวิศวกรรมศาสตร์ จุฬาลงกรณ์มหาวิทยาลัย เมื่อปี พ.ศ. 2524 แล้วเข้าศึกษาต่อในระดับปริญญามหาบัณฑิต สาขาวิศวกรรมไฟฟ้า คณะวิศวกรรมศาสตร์ จุฬาลงกรณ์มหาวิทยาลัย