เอกสารอ้างอิง

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ภาคผนวก ก

รายละเอียดเครื่องแปล รหัสจากเพลาหมุน

[illegible]

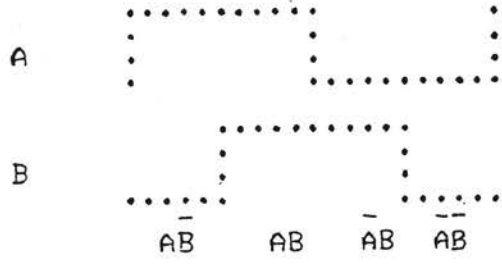
WILMINGTON, MA. U.S.A.

ATE: 10-26-81

ODEL NUMBER: 77L-10-B03-100

ERIAL NUMBER: 30808

INE COUNT: 100



CW ROTATION

QUADRANT WIDTH IN PHASE DEGREES

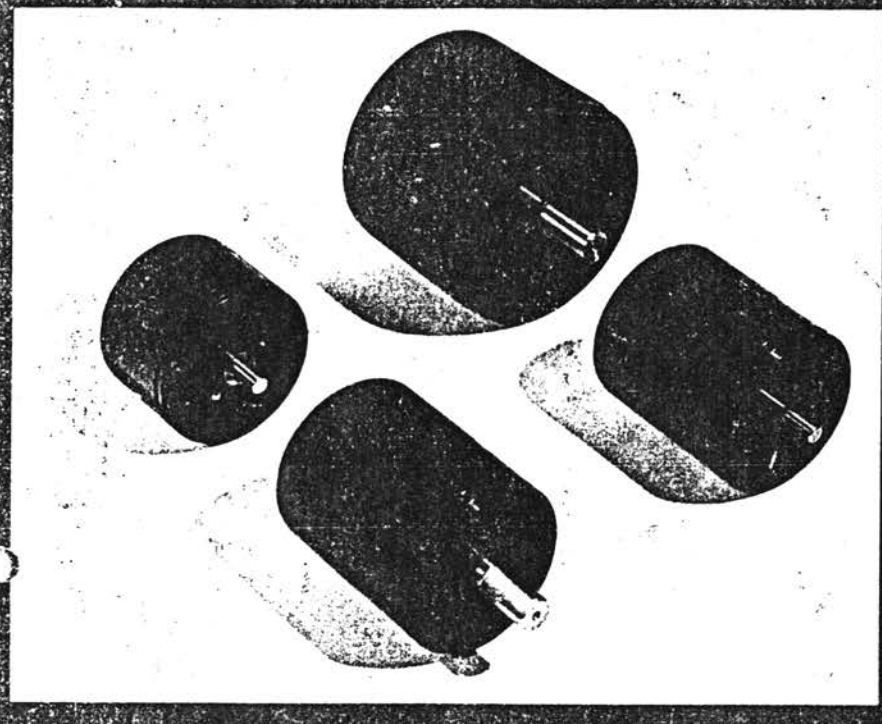
$\overline{AB}$=92.8 AVG.	91.8 MIN	94 MAX.
AB=89.2 AVG.	87.8 MIN.	90.2 MAX.
$\overline{AB}$=91.8 AVG.	90.6 MIN.	93.2 MAX.
$\overline{\overline{AB}}$=86.1 AVG.	84.9 MIN.	87.3 MAX.

CH A TO CH B PHASE =92.3 DEGREES

SYMMETRY CH A =1.02 ON/OFF
SYMMETRY CH B =1.01 ON/OFF

AMPLITUDES (VOLTS)

CH	ONE	ZERO
A	3.3	.2
B	3.2	.2



Data Tech Optecon Series Optical Incremental Shaft Encoders

- Proven reliability for a broad range of shaft measuring applications
- High frequency
- High shaft loading
- Resolutions up to 21,600 pulses per turn
- LED and line driver outputs available
- Backed by strongest warranty

Optecon Series Optical Incremental Shaft Encoders

Compare the Optecon series with any competitive encoder. You'll find an unparalleled range of model variations that let you buy exactly the capabilities you need. You'll find built-in standards that equal or exceed extra cost options on other designs. You'll find proven reliability that's backed up by the strongest warranty in the business. And you'll find all of this at consistently competitive prices.

Design features

- High output frequency (100 kHz) standard on all Optecons allows for simultaneous high resolution and high speed. You don't have to pay a higher price—or sacrifice system performance—when you need both speed and resolution.
- Single light source eliminates errors common on other designs caused by multiple lamp aging effects. Both the incandescent and optional LED light sources are guaranteed—not just rated—for five years' operation.
- The OC25, 0S25 and 0N25 models are the only size 25 encoders offering resolutions up to 5,400 lines with a gated zero marker. This is a conservative operating range and ensures that your application won't come close to straining the limit of their capability.
- Complementary, push-pull photodiodes provide extremely stable output with temperature and power supply fluctuations and in spite of noise and aging effects.
- Optecons are ruggedly constructed with anodized cases and stainless steel shafts. The OS25, ON25 and ON35 models are environmentally protected with shaft seals and sealed MS connectors.
- Sealed duplex bearings pre-loaded to provide high mechanical stability.
- Hysteresis feedback ensures jitter-free operation.
- Single, non-critical voltage requirement and low power consumption enable use of system supply.
- High shock resistance is ensured by a specially designed disc and wide gap spacing between the disc and mask.
- 90° phasing is accomplished physically in the mask ensuring long term stability.
- Low torque magnetic shaft seal in OS25, ON25 and ON35.
- Standard TTL compatible.
- HTL, CMOS compatibility available.
- Advanced integrated circuitry ensures long-term dependability
- Optecons accept high axial and radial forces. There's no need to buy a more expensive encoder when you need high shaft loading.
- Low inertia and torque provide high system performance.

Models to meet every need

The following are standard variations. Data Tech also offers design assistance to meet special requirements.

Mechanical configurations
- Light duty industrial
- Industrial
- General purpose
- Rugged, heavy duty

Resolutions
- From 1 to 5,400 cycles per revolution (increased with X4 logic to 21,600 pulses per turn)
- Over 60 resolutions available standard
- Additional resolutions on special order

Electrical output configurations
- Bi-directional or non-direction sensing
- Square wave, pulse (X1, X2 or X4), or sinusoidal output (buffered)
- With or without gated zero marker

Input voltage
- 5 volts DC
- 12 volts DC
- 15 volts DC

Light source
- Single incandescent lamp
- Single light emitting diode (LED)

Terminals
- Standard connectors (see specifications)
- Screw type terminals
- Hooded screw terminals

Additional output options
- Inverted zero
- Complementary outputs
- I.C. line driver
- Component line driver

The industry's best warranty

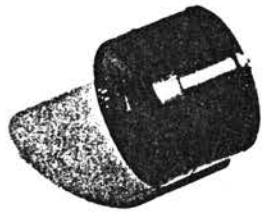
Data Tech backs each Optecon encoder with the industry's longest and strongest equipment warranty. The light source is guaranteed for five years. The rest of the encoder is guaranteed for one year. If anything goes wrong during those period, because of defects in workmanship or materials, we'll fix or replace it free. Extended warranties are also available. See our warranty statement for complete details.

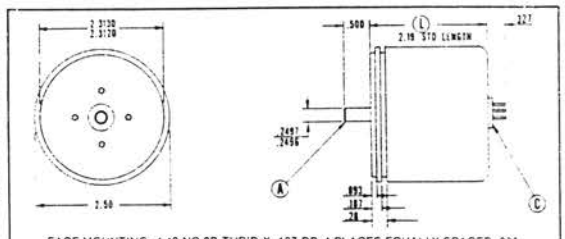
Other Data Tech encoders

Data Tech manufactures a complete family of encoders ranging from the RS-23 series (the industry's lowest cost complete encoders) through the Optecon series to the OP-35 series with resolutions up to 9,000 counts per shaft revolution or 36,000 pulses per turn. Low-cost, modular, kit encoders for adapting to the end of a motor, dual count (English/metric) encoders similar in style to the Optecon Series, and hollow shaft encoders are also available. Ask for individual data sheets.

Model OC25

For light duty industrial applications
- 1 to 5,400 cycles per revolution
- 21,600 pulses per revolution with X4 logic
- 100 kHz standard frequency
- 5 year light source warranty
- All electrical variations
- Connector or terminals





FACE MOUNTING: 4-40 NC-2B THR'D X .187 DP, 4 PLACES EQUALLY SPACED 90°, ON A 1.00 D.B.C.

Ⓐ SHAFT IS CONCENTRIC WITH 2.3130/2.3120 DIA. WITHIN ± .001 T.I.R.

Ⓒ REFER MECHANICAL SPECIFICATION*

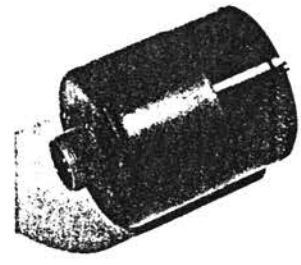
Ⓛ LENGTH VARIES WITH OPTIONS

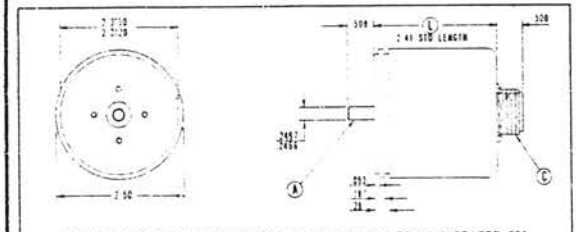
CONNECTIONS	
PIN	FUNCTION
A	DC GROUND
B	VDC
C	ZERO OUTPUT
D	A OUTPUT
E	B OUTPUT
F	NO CONNECTION
H	CASE GROUND

* AVAILABLE WITH SCREW TERMINALS

Model OS25

For industrial applications
- All the features of the OC25 plus . . .
- Magnetically sealed shaft
- Environmentally sealed MS connector





FACE MOUNTING: 4-40 NC-2B THR'D X .187 DP, 4 PLACES EQUALLY SPACED 90°, ON A 1.00 D.B.C.

Ⓐ SHAFT IS CONCENTRIC WITH 2.3130/2.3120 DIA. WITHIN ± .001 T.I.R.

Ⓒ REFER MECHANICAL SPECIFICATION*

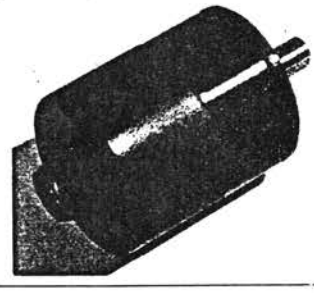
Ⓛ LENGTH VARIES WITH OPTIONS

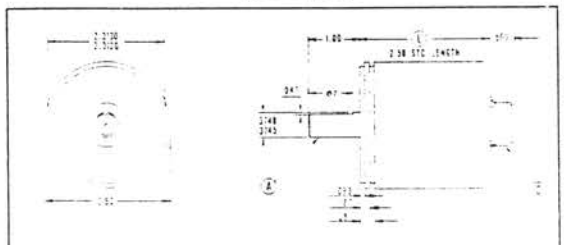
CONNECTIONS	
PIN	FUNCTION
A	DC GROUND
B	VDC
C	ZERO OUTPUT
D	A OUTPUT
E	B OUTPUT
F	CASE GROUND

* AVAILABLE WITH SCREW TERMINALS

Model ON25

For general purpose industrial applications
- All the features of the OS25 plus . . .
- Higher shaft loading
- Longer bearing life
- Larger shaft diameter
- Longer shaft length





Ⓐ SHAFT IS CONCENTRIC WITH 2.3130/2.3120 DIA. WITHIN ± .001 T.I.R.

Ⓒ REFER MECHANICAL SPECIFICATION*

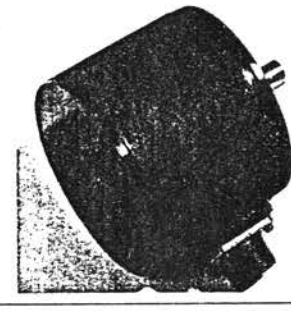
Ⓛ LENGTH VARIES WITH OPTIONS

CONNECTIONS	
PIN	FUNCTION
A	DC GROUND
B	VDC
C	ZERO OUTPUT
D	A OUTPUT
E	B OUTPUT
F	CASE GROUND

* AVAILABLE WITH SCREW TERMINALS

Model ON35

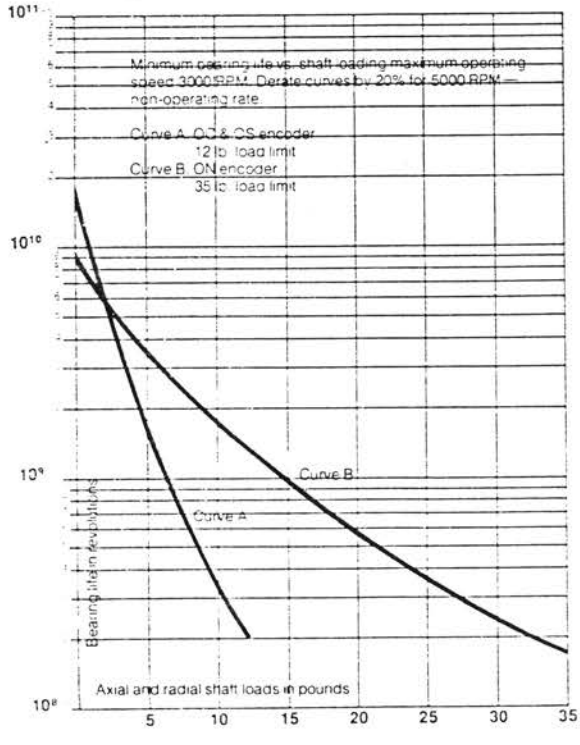
For heavy duty applications
- All the features of the ON25 plus . . .
- Heavy duty case
- Heavy duty mounting
- MS connector only



Mechanical Specifications

	OC25	OS25	ON25	ON35
	Light duty industrial	Industrial	General purpose	Heavy duty
Shaft loading (max) Radial lbs. (kg) Axial lbs. (kg)	12 (5.5) 12 (5.5)		35 (15.9) 35 (15.9)	
Bearing life (Ref. life chart)	CURVE A		CURVE B	
Starting torque Oz-in (gm-cm)	0.05 (3.6)	0.15 (10.8)	0.25 (18.0)	
Inertia Oz-in-sec^2 (gm-cm^2)	0.3×10^{-3} (22)		0.4×10^{-3} (28.4)	
Operating speed RPM max.	Lowest of $\frac{100\ KHz}{resolution} \times 60 \frac{sec}{min}$ or 3000 RPM			
Shaft acceleration rad/sec^2	100,000			
Shaft diameter in (mm)	0.25 (6.35)		0.5 (12.7)	
Sealed shaft and connector	NO	YES		
Connector type mounted	Amphenol 126-197	MS3102E-14S-6P		
Mating connector supplied by D.T.	126-196	MS3108E-14S-6S(C) right angle connector		MS3106E-14S-6S
Shaft rotation	continuous and reversible			
Mounting	servo and face			
Weight oz (gm)	9.0 (255)	13.2 (375)	17.3 (490)	27.4 (780)

Bearing Life Chart



Electrical Specifications

Resolution	1 to 5400 cycles/rev (21,600 pulses/rev. with X4 logic)
Frequency	Lowest of: 100 KHz or $\frac{3000\ RPM}{60 \frac{sec}{min}} \times$ resolution
Light source	Single lamp or single L.E.D. (optional)
Light warranty	5 years (see warranty statement)
Phase relationship	90 ± 22.5 electrical degrees (⅛ cycle worst case)
Input power (square wave output)	5 volt model — +5 VDC ± 5% 200 ma 12 volt model — +12 VDC ± 5% 150 ma
Output characteristics	5 volt model — TTL output source — 400 ua @ +2.4 VDC min. Sink 16 ma @ 0.4 VDC max. 12 volt model — Output source impedance 1 K ohm to 12 VDC. Sink 10 ma @ +0.3 VDC max.
Rise & fall time	5 volt model — 0.1 μsec max. 12 volt model — 1.5 μsec max.
Zero index (optional)	¼ cycle gated pulse
Pulse width (multiplier option only)	2 μ sec ±25%
ENVIRONMENT:	
Operating ambient	0 to 160°F (−18 to +71°C) 0–98% RH (non condensing)
Storage ambient	−65 to 175°F (−54 to 80°C)

DATA TECHnology, Inc.
4 Gill Street, Woburn, Mass. 01801
(617) 935-8820

bulletin 1-604 5 ed 2

ภาคผนวก ข

รายละเอียดของไอซีต่างๆที่ใช้ในวงจร

Absolute Maximum Ratings

Temperature Under Bias	Specified operating range
Storage Temperature	-65°C to +150°C
Voltage On Any Pin with Respect to Ground	-0.3V to +7V
Power Dissipation	1.5 W

*Comment

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note For Z80-CPU all AC and DC characteristics remain the same for the military grade parts except I_{CC}.

I_{CC} = 200 mA

Z80-CPU D.C. Characteristics

T_A = 0°C to 70°C, V_{CC} = 5V ± 5% unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Condition
V_{ILC}	Clock Input Low Voltage	-0.3		0.45	V	
V_{IHC}	Clock Input High Voltage	V_{CC} -.6		V_{CC}+.3	V	
V_{IL}	Input Low Voltage	-0.3		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC}	V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL}=1.8mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -250μA
I_{CC}	Power Supply Current			150	mA	
I_{LI}	Input Leakage Current			10	μA	V_{IN}=0 to V_{CC}
I_{LOH}	Tri-State Output Leakage Current in Float			10	μA	V_{OUT}=2.4 to V_{CC}
I_{LOL}	Tri-State Output Leakage Current in Float			-10	μA	V_{OUT}=0.4V
I_{LD}	Data Bus Leakage Current in Input Mode			±10	μA	$0 \leq V_{IN} \leq V_{CC}$

Capacitance

T_A = 25°C, f = 1 MHz,
unmeasured pins returned to ground

Symbol	Parameter	Max.	Unit
C_Φ	Clock Capacitance	35	pF
C_{IN}	Input Capacitance	5	pF
C_{OUT}	Output Capacitance	10	pF

Z80-CPU Ordering Information

C – Ceramic
P – Plastic
S – Standard 5V ±5% 0° to 70°C
E – Extended 5V ±5% -40° to 85°C
M – Military 5V ±10% -55° to 125°C

Z80A-CPU D.C. Characteristics

T_A = 0°C to 70°C, V_{CC} = 5V ± 5% unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Condition
V_{ILC}	Clock Input Low Voltage	-0.3		0.45	V	
V_{IHC}	Clock Input High Voltage	V_{CC} -.6		V_{CC}+.3	V	
V_{IL}	Input Low Voltage	-0.3		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC}	V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL}=1.8mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -250μA
I_{CC}	Power Supply Current		90	200	mA	
I_{LI}	Input Leakage Current			10	μA	V_{IN}=0 to V_{CC}
I_{LOH}	Tri-State Output Leakage Current in Float			10	μA	V_{OUT}=2.4 to V_{CC}
I_{LOL}	Tri-State Output Leakage Current in Float			-10	μA	V_{OUT}=0.4V
I_{LD}	Data Bus Leakage Current in Input Mode			±10	μA	$0 \leq V_{IN} \leq V_{CC}$

Capacitance

T_A = 25°C, f = 1 MHz,
unmeasured pins returned to ground

Symbol	Parameter	Max.	Unit
C_Φ	Clock Capacitance	35	pF
C_{IN}	Input Capacitance	5	pF
C_{OUT}	Output Capacitance	10	pF

Z80A-CPU Ordering Information

C – Ceramic
P – Plastic
S – Standard 5V ±5% 0° to 70°C

Absolute Maximum Ratings

Temperature Under Bias	Specified operating range.
Storage Temperature	-65° C to +150° C
Voltage On Any Pin With Respect To Ground	-0.3 V to +7 V
Power Dissipation	0.6 W

*Comment

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: All AC and DC characteristics remain the same for the military grade parts except I_{CC}.

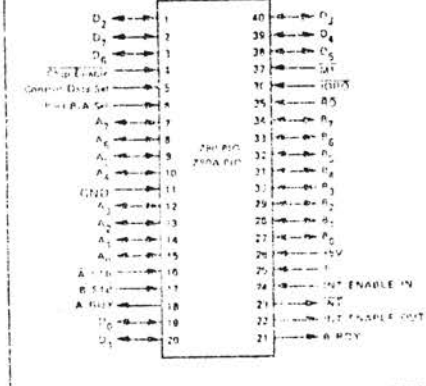
I_{CC} = 130 mA

Z80-PIO and Z80A-PIO D.C. Characteristics

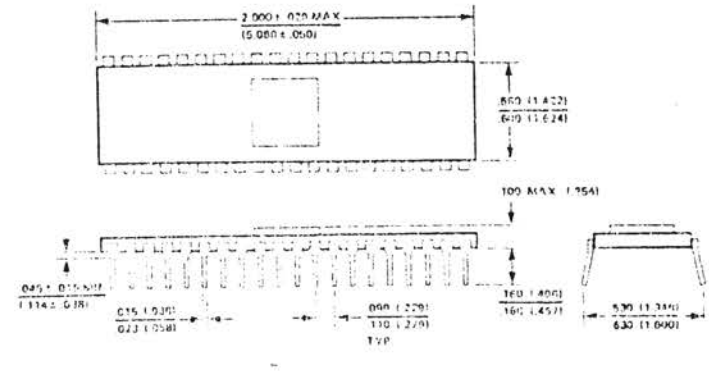
T_A = 0° C to 70° C, V_{CC} = 5 V ± 5% unless otherwise specified

Symbol	Parameter	Min.	Max.	Unit	Test Condition
V_{ILC}	Clock Input Low Voltage	-0.3	.45	V	
V_{IHC}	Clock Input High Voltage	V_{CC}-.6	V_{CC}+.3	V	
V_{IL}	Input Low Voltage	-0.3	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}	V	
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 2.0 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -250 μA
I_{CC}	Power Supply Current		70	mA	
I_{LI}	Input Leakage Current		10	μA	V_{IN} = 0 to V_{CC}
I_{LOH}	Tri-State Output Leakage Current in Float		10	μA	V_{OUT} = 2.4 to V_{CC}
I_{LOL}	Tri-State Output Leakage Current in Float		-10	μA	V_{OUT} = 0.4 V
I_{LD}	Data Bus Leakage Current in Input Mode		±10	μA	$0 \leq V_{IN} \leq V_{CC}$
I_{OHD}	Darlington Drive Current	-1.5	-3.8	mA	V_{OH} = 1.5 V R_{EXT} = 390 Ω Port B Only

Package Configuration



Package Outline



NOTE: Dimensions in parentheses are for metric system (cm).

8251A
PROGRAMMABLE COMMUNICATION INTERFACE

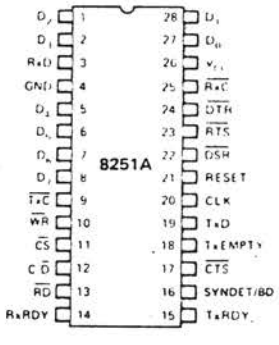
Synchronous and Asynchronous Operation

- **Synchronous:**
  - 5-8 Bit Characters
  - Internal or External Character Synchronization
  - Automatic Sync Insertion
- **Asynchronous:**
  - 5-8 Bit Characters
  - Clock Rate — 1, 16 or 64 Times Baud Rate
  - Break Character Generation
  - 1, 1½, or 2 Stop Bits
  - False Start Bit Detection
  - Automatic Break Detect and Handling

- **Baud Rate —DC to 64k Baud**
- **Full Duplex, Double Buffered, Transmitter and Receiver**
- **Error Detection — Parity, Overrun, and Framing**
- **Fully Compatible with 8080/8085 CPU**
- **28-Pin DIP Package**
- **All Inputs and Outputs Are TTL Compatible**
- **Single 5 Volt Supply**
- **Single TTL Clock**

The 8251A is the enhanced version of the industry standard, Intel® 8251 Universal Synchronous/Asynchronous Receiver/Transmitter (USART), designed for data communications with Intel's new high performance family of microprocessors such as the 3085. The 8251A is used as a peripheral device and is programmed by the CPU to operate using virtually any serial data transmission technique presently in use (including IBM Bi-Sync). The USART accepts data characters from the CPU in parallel format and then converts them into a continuous serial data stream for transmission. Simultaneously, it can receive serial data streams and convert them into parallel data characters for the CPU. The USART will signal the CPU whenever it can accept a new character for transmission or whenever it has received a character for the CPU. The CPU can read the complete status of the USART at any time. These include data transmission errors and control signals such as SYNDET, TxEMPTY. The chip is constructed using N-channel silicon gate technology.

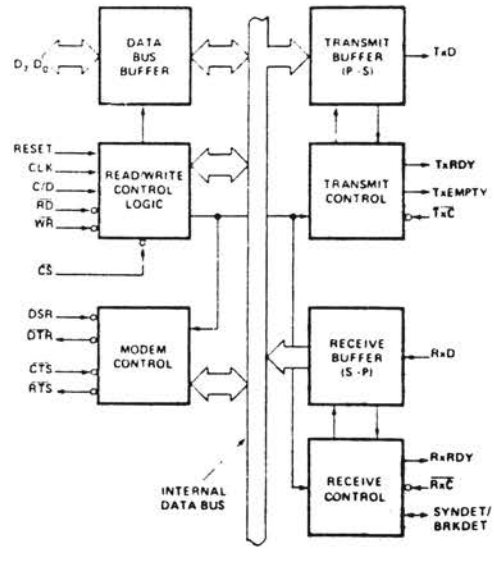
PIN CONFIGURATION



Pin Name	Pin Function
D_7 D_0	Data Bus (8 bits)
C/$\overline{D}$	Control or Data is to be Written or Read
$\overline{RD}$	Read Data Command
$\overline{WR}$	Write Data or Control Command
$\overline{CS}$	Chip Select
CLK	Clock Pulse (TTL)
RESET	Reset
$\overline{TxC}$	Transmitter Clock
TxD	Transmitter Data
$\overline{RxC}$	Receiver Clock
RxD	Receiver Data
RxRDY	Receiver Ready (has character for CPU)

Pin Name	Pin Function
$\overline{DSR}$	Data Set Ready
$\overline{DTR}$	Data Terminal Ready
SYNDET/BD	Sync Detect/ Break Detect
$\overline{RTS}$	Request to Send Data
$\overline{CTS}$	Clear to Send Data
TxEMPTY	Transmitter Empty
V_{CC}	+5 Volt Supply
GND	Ground

BLOCK DIAGRAM



2716
16K (2K×8) UV ERASABLE PROM

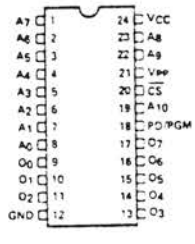
- Single +5V Power Supply
- Simple Programming Requirements
  Single Location Programming
  Programs With One 50ms Pulse
- Low Power Dissipation
  525mW Max. Active Power
  132mW Max. Standby Power
- Pin Compatible To Intel 2316E ROM
- Fast Access Time: 450ns Max.
- Inputs and Outputs TTL
  Compatible During Read
  And Program

The Intel® 2716 is a 16,384-bit ultraviolet erasable and electrically programmable read-only memory (EPROM). The 2716 operates from a single 5-volt power supply, has a static power down mode, and features fast single address location programming. It makes designing with EPROMs faster, easier and more economical. For production quantities, the 2716 user can convert rapidly to Intel's new pin-for-pin compatible 16K ROM, the 2316E.

Since the 450-nsec 2716 operates from a single 5-volt supply, it is ideal for use with the newer high performance +5V microprocessors such as Intel's 8085 and 8048. The 2716 is also the first EPROM with a static power down mode which reduces the power dissipation without increasing access time. The maximum active power dissipation is 525 mW while the maximum standby power dissipation is only 132 mW, a 75% savings.

The 2716 has the simplest and fastest method yet devised for programming EPROMs — single pulse TTL level programming. No need for high voltage pulsing because all programming controls are handled by TTL signals. Now, it is possible to program on-board, in the system, in the field. Program any location at any time — either individually, sequentially or at random, with the 2716's single address location programming. Total programming time for all 16,384 bits is only 100 seconds.

PIN CONFIGURATION



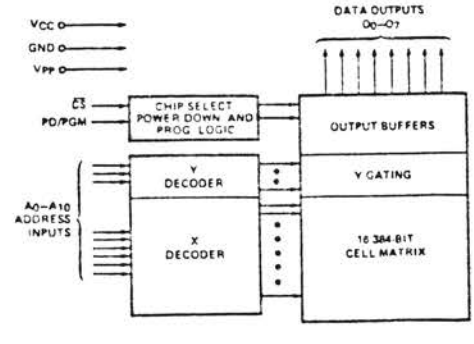
PIN NAMES

A_0–A_{10}	ADDRESSES
PD/PGM	POWER DOWN/PROGRAM
$\overline{CS}$	CHIP SELECT
O_0–O_7	OUTPUTS

MODE SELECTION

PINS / MODE	PD/PGM (18)	$\overline{CS}$ (20)	V_{PP} (21)	V_{CC} (24)	OUTPUTS (9-11, 13-17)
Read	V_{IL}	V_{IL}	+5	+5	D_{OUT}
Deselect	Don't Care	V_{IH}	+5	+5	High Z
Power Down	V_{IH}	Don't Care	+5	+5	High Z
Program	Pulsed V_{IL} to V_{IH}	V_{IH}	+25	+5	D_{IN}
Program Verify	V_{IL}	V_{IL}	+25	+5	D_{OUT}
Program Inhibit	V_{IL}	V_{IH}	+25	+5	High Z

BLOCK DIAGRAM



2114A 1024 X 4 BIT STATIC RAM

	2114AL-1	2114AL-2	2114AL-3	2114AL-4	2114A-4	2114A-5
Max. Access Time (ns)	100	120	150	200	200	250
Max. Current (mA)	40	40	40	40	70	70

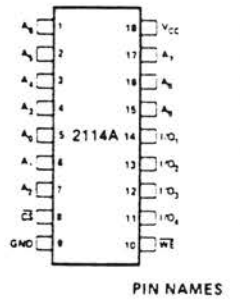
- **HMOS Technology**
- **Low Power, High Speed**
- **Identical Cycle and Access Times**
- **Single +5V Supply ±10%**
- **High Density 18 Pin Package**
- **Completely Static Memory - No Clock or Timing Strobe Required**
- **Directly TTL Compatible: All Inputs and Outputs**
- **Common Data Input and Output Using Three-State Outputs**
- **2114 Upgrade**

The Intel® 2114A is a 4096-bit static Random Access Memory organized as 1024 words by 4-bits using HMOS, a high performance MOS technology. It uses fully DC stable (static) circuitry throughout, in both the array and the decoding, therefore it requires no clocks or refreshing to operate. Data access is particularly simple since address setup times are not required. The data is read out nondestructively and has the same polarity as the input data. Common input/output pins are provided.

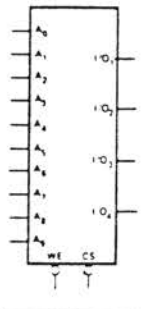
The 2114A is designed for memory applications where the high performance and high reliability of HMOS, low cost, large bit storage, and simple interfacing are important design objectives. The 2114A is placed in an 18-pin package for the highest possible density.

It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. A separate Chip Select ($\overline{CS}$) lead allows easy selection of an individual package when outputs are or-tied.

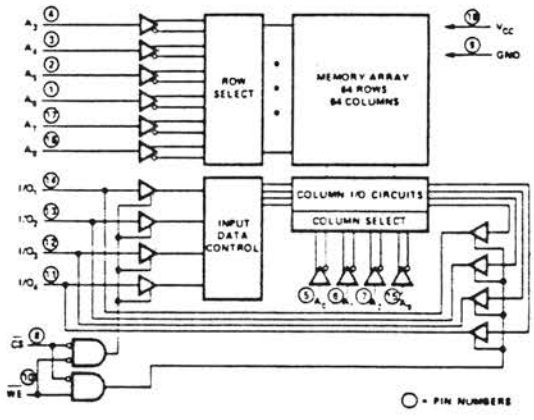
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0–A_9	ADDRESS INPUTS	V_{CC}	POWER (+5V)
$\overline{WE}$	WRITE ENABLE	GND	GROUND
$\overline{CS}$	CHIP SELECT		
I/O_1–I/O_4	DATA INPUT/OUTPUT		

Figure 2.6: A partial data sheet and block diagram for the 2114, 1K × 4, common I/O static RAM.

Line Drivers/Receivers

DS1489/DS1489A quad line receiver

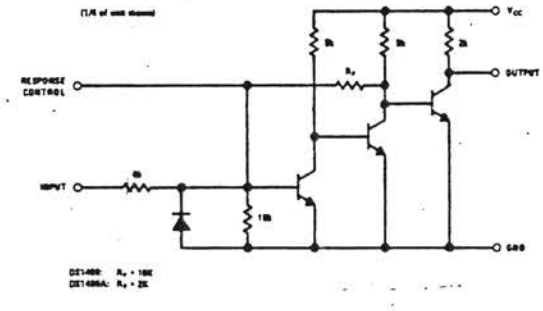
general description

The DS1489/DS1489A are quad line receivers designed to interface data terminal equipment with data communications equipment. They are constructed on a single monolithic silicon chip. These devices satisfy the specifications of EIA standard No. RS232C. The DS1489/DS1489A meet and exceed the specifications of MC1489/MC1489A and are pin-for-pin replacements. The DS1489/DS1489A are available in 14-lead ceramic dual-in-line package.

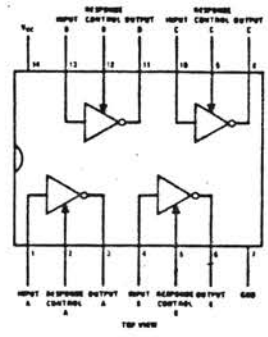
features

- Four totally separate receivers per package
- Programmable threshold
- Built-in input threshold hysteresis
- "Fail safe" operating mode
- Inputs withstand ±30V

schematic and connection diagrams

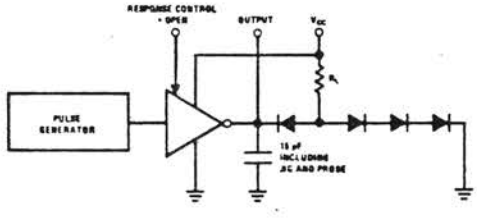


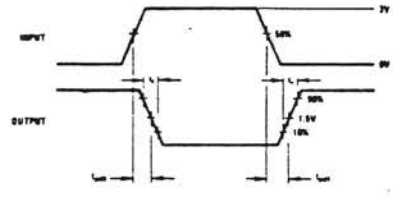
Dual-In-Line Package



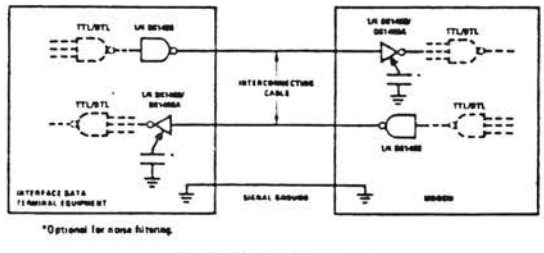
Order Number DS1489J or DS1489AJ

ac test circuit and voltage waveforms

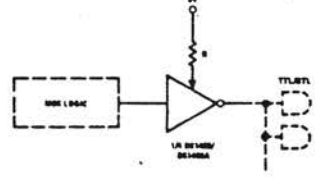




typical applications



RS232C Data Transmission



MOS to TTL/DTL Translator

NATIONAL

Line Drivers/Receivers

DS1488 quad line driver

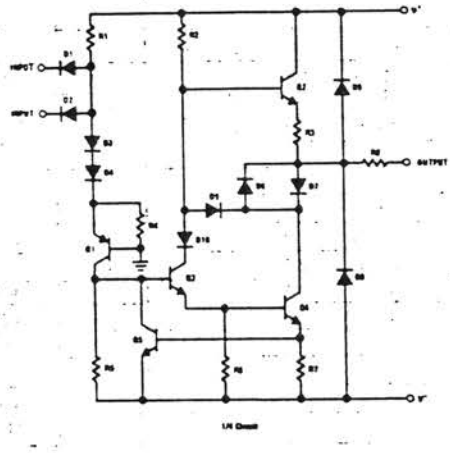
general description

The DS1488 is a quad line driver which converts standard DTL/TTL input logic levels through one stage of inversion to output levels which meet EIA Standard No. RS-232C and CCITT Recommendation V. 24.

features

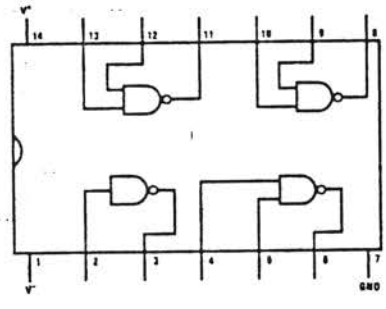
- Current limited output ±10 mA typ
- Power-off source impedance 300Ω min
- Simple slew rate control with external capacitor
- Flexible operating supply range
- Inputs are DTL/TTL compatible

schematic and connection diagrams



1/4 Circuit

Dual-In-Line Package

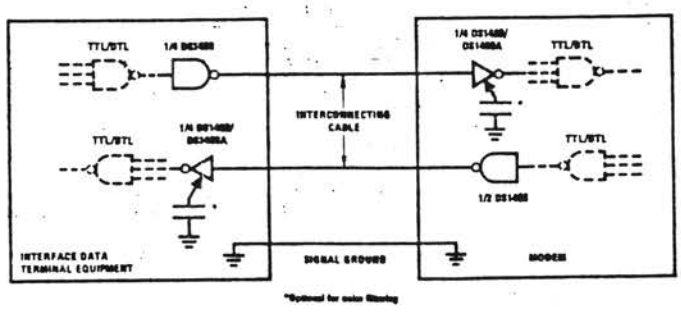


TOP VIEW

Order Number DS1488J

typical applications

RS232C Data Transmission



LM78XX series voltage regulators

general description

The LM78XX series of three terminal regulators is available with several fixed output voltages making them useful in a wide range of applications. One of these is local on card regulation, eliminating the distribution problems associated with single point regulation. The voltages available allow these regulators to be used in logic systems, instrumentation, HiFi, and other solid state electronic equipment. Although designed primarily as fixed voltage regulators these devices can be used with external components to obtain adjustable voltages and currents.

The LM78XX series is available in an aluminum TO-3 package which will allow over 1.0A load current if adequate heat sinking is provided. Current limiting is included to limit the peak output current to a safe value. Safe area protection for the output transistor is provided to limit internal power dissipation. If internal power dissipation becomes too high for the heat sinking provided, the thermal shutdown circuit takes over preventing the IC from overheating.

Considerable effort was expended to make the LM78XX series of regulators easy to use and minimize the number of external components. It is not necessary to bypass the output, although this does improve transient response. Input bypassing is needed only if the regulator is located far from the filter capacitor of the power supply.

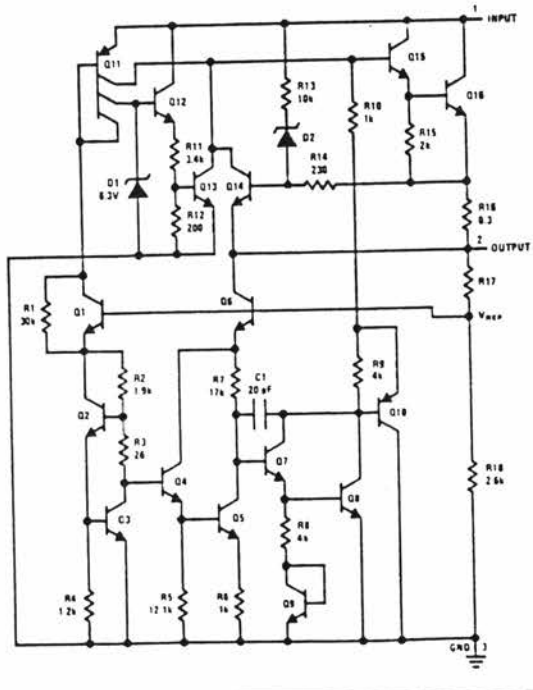
features

- Output current in excess of 1A
- Internal thermal overload protection
- No external components required
- Output transistor safe area protection
- Internal short circuit current limit
- Available in the aluminum TO-3 package

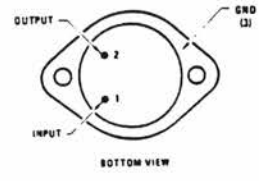
voltage range

LM7805	5V	LM7815	15V
LM7806	6V	LM7818	18V
LM7808	8V	LM7824	24V
LM7812	12V		

schematic and connection diagrams



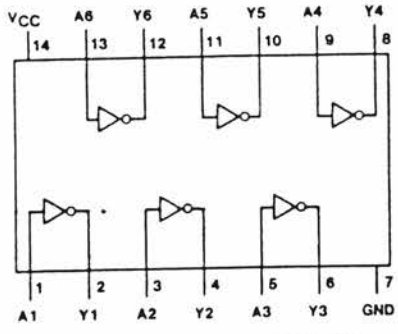
Metal Can Package
TO-3 (KC)



BOTTOM VIEW

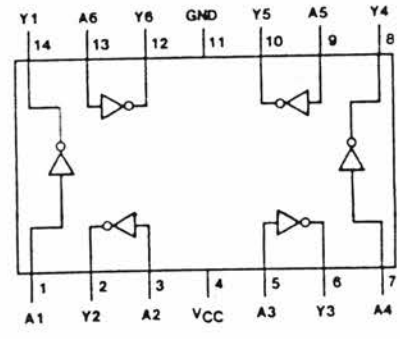
04 Hex Inverters

$Y = \overline{A}$



5404 (J)
54H04 (J)
54L04 (J)
54LS04 (J,W)
54S04 (J,W)

7404 (N)
74H04 (N)
74L04 (N)
74LS04 (N)
74S04 (N)



5404 (W)
54L04 (W)

See page 5-4

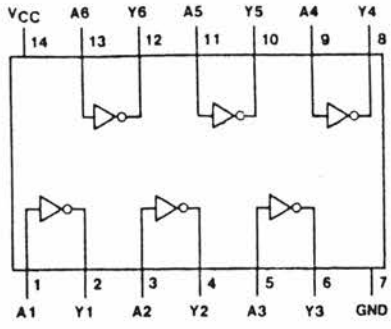
Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted).

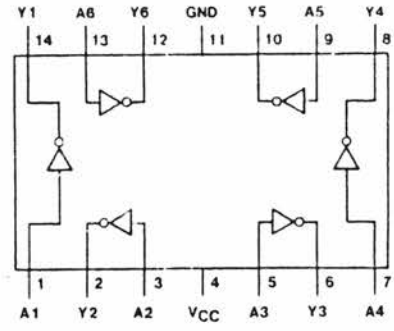
Parameter		Conditions			DM54/74 00, 04 10, 20, 30			DM54/74 H00, H04 H10, H20, H30			DM54/74 L00, L04 L10, L20, L30			DM54/74 LS00, LS04 LS10, LS20, LS30			DM54/74 S00, S04, S10 S20, S30, S133			Units
					Min	Typ(1)	Max	Min	Typ(1)	Max	Min	Typ(1)	Max	Min	Typ(1)	Max	Min	Typ(1)	Max	
V_{IH}	High Level Input Voltage				2			2			2			2			2			V
V_{IL}	Low Level Input Voltage			DM54			0.8			0.8			0.7			0.8			0.8	V
				DM74			0.8			0.8			0.7			0.8			0.8	
V_I	Input Clamp Voltage	V_{CC} = Min	I_I = −8 mA							−1.5			N/A							V
			I_I = −12 mA				−1.5						N/A							
			I_I = −18 mA										N/A			−1.5			−1.2	
I_{OH}	High Level Output Current						−400			−500			−200			−400			−1000	µA
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IL} = Max, I_{OH} = Max		DM54	2.4	3.4		2.4	3.5		2.4	3.3		2.5	3.4		2.5	3.4		V
				DM74	2.4	3.4		2.4	3.5		2.4	3.2		2.7	3.4		2.7	3.4		
I_{OL}	Low Level Output Current			DM54			16			20			2			4			20	mA
				DM74			16			20			3.6			8			20	
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2 V	I_{OL} = Max	DM54		0.2	0.4		0.2	0.4		0.15	0.3		0.25	0.4			0.5	V
				DM74		0.2	0.4		0.2	0.4		0.2	0.4		0.35	0.5			0.5	
			I_{OL} = 4 mA	DM74												0.4				
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max	V_I = 5.5 V				1			1			0.1						1	mA
			V_I = 7 V													0.1				
I_{IH}	High Level Input Current	V_{CC} = Max	V_I = 2.4 V				40			50			10							µA
			V_I = 2.7 V													20			50	
I_{IL}	Low Level Input Current	V_{CC} = Max	V_I = 0.3 V										−0.18							mA
			V_I = 0.4 V	LS30												−0.4				
				Others			−1.6			−2						−0.36				
			V_I = 0.5 V																−2	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (2)		DM54	−20		−55	−40		−100	−3		−15	−20		−100	−40		−100	mA
				DM74	−18		−55	−40		−100	−3		−15	−20		−100	−40		−100	
I_{CC}	Supply Current	V_{CC} = Max			See Table															

Note 1: All typical values are at V_{CC} = 5 V, T_A = 25°C.
Note 2: Not more than one output should be shorted at a time, and for DM54H/DM74H, DM54LS, DM74LS and DM54S/DM74S, duration of short circuit should not exceed one second.

05 Hex Inverters with Open-Collector Outputs

$Y = \overline{A}$





5405 (J)
54L05 (J)
54LS05 (J,W)
54S05 (J,W)

7405 (N)
74L05 (N)
74LS05 (N)
74S05 (N)

5405 (W)
54L05 (W)

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

Parameter		Conditions		DM54/74 01, 03 05			DM54/74 H01			DM54/74 L01, L03 L05			DM54/74 LS01, LS03 LS05, LS12, LS22			DM54/74 S03 S05, S22			Units
				Min	Typ (1)	Max	Min	Typ (1)	Max	Min	Typ (1)	Max	Min	Typ (1)	Max	Min	Typ (1)	Max	
V_{IH}	High Level Input Voltage			2			2			2			2			2			V
V_{IL}	Low Level Input Voltage		DM54			0.8			0.8			0.8			0.8			0.8	V
			DM74			0.8			0.8			0.8			0.8			0.8	
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −8 mA							−1.5			N/A							V
		V_{CC} = Min, I_I = −12 mA				−1.5						N/A							
		V_{CC} = Min, I_I = −18 mA										N/A			−1.5			−1.2	
I_{CEX}	High Level Output Current	V_{CC} = Min, V_{IL} = Max, V_{OH} = 5.5 V				250			250			50			100			250	μA
I_{OL}	Low Level Output Current		DM54			16			20			2			4			20	mA
			DM74			16			20			3.6			8			20	
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2 V, I_{OL} = Max	DM54		0.2	0.4		0.2	0.4		0.15	0.3		0.25	0.4			0.5	V
			DM74		0.2	0.4		0.2	0.4		0.2	0.4		0.35	0.5			0.5	
		I_{OL} = 4 mA	DM74												0.4				
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max	V_I = 5.5 V			1			1			0.1						1	mA
			V_I = 7 V												0.1				
I_{IH}	High Level Input Current	V_{CC} = Max	V_I = 2.4 V			40			50			10							μA
			V_I = 2.7 V												20			50	
I_{IL}	Low Level Input Current	V_{CC} = Max	V_I = 0.3 V									−0.18							mA
			V_I = 0.4 V			−1.6			−2						−0.36				
			V_I = 0.5 V															−2	
I_{CC}	Supply Current	V_{CC} = Max		See Table															

Note 1: All typical values are at V_{CC} = 5 V, T_A = 25°C

Supply Current

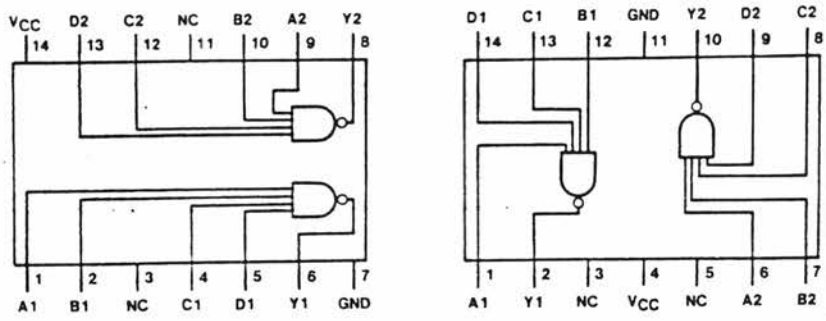
Device	I_{CCH} (mA) Total With Outputs High		I_{CCL} (mA) Total With Outputs Low	
	Typ	Max	Typ	Max
01	4	8	12	22
03	4	8	12	22
05	6	12	18	33
H01	6.8	10	26	40
L01	0.44	0.8	1.16	2.04
L03	0.44	0.8	1.16	2.04
L05	0.66	1.20	1.74	3.06
LS01	0.8	1.6	2.4	4.4
LS03	0.8	1.6	2.4	4.4
LS05	1.2	2.4	3.6	6.6
LS12	0.7	1.4	1.8	3.3
LS22	0.4	0.8	1.2	2.2
S03	6	13.2	20	36
S05	9	19.8	30	54
S22	3	6.6	10	18

Switching Characteristics at V_{CC} = 5 V, T_A = 25°C

Device	Conditions	t_{PLH} (ns) Propagation Delay Time, Low-To-High Output			t_{PHL} (ns) Propagation Delay Time, High-To-Low Output		
		Min	Typ	Max	Min	Typ	Max
01, 03	C_L = 15 pF, R_L = 4 kΩ for t_{PLH}, R_L = 400 Ω for t_{PHL}		35	45		8	15
05			10	55		8	15
H01	C_L = 25 pF, R_L = 280 Ω		10	15		7.5	12
L01, L03, L05	C_L = 50 pF, R_L = 4 kΩ		60	90		33	60
LS01, LS03 LS05 LS12 LS22	C_L = 15 pF, R_L = 2 kΩ	6	12	20	3	7	15
	C_L = 50 pF, R_L = 2 kΩ	20	32	45	4	10	20
S03, S05 S22	C_L = 15 pF, R_L = 280 Ω	2	5	7.5	2	4.5	7
	C_L = 50 pF, R_L = 280 Ω	3	7.5	11	3	7	11

20 Dual 4-Input NAND Gates

$Y = \overline{ABCD}$



5420 (J)
54H20 (J)
54L20 (J)
54LS20 (J,W)

7420 (N)
74H20 (N)
74L20 (N)
74LS20 (N)

5420 (W)
54L20 (W)

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted).

Parameter		Conditions			DM54/74 00, 04 10, 20, 30			DM54/74 H00, H04 H10, H20, H30			DM54/74 L00, L04 L10, L20, L30			DM54/74 LS00, LS04 LS10, LS20, LS30			DM54/74 S00, S04, S10 S20, S30, S133			Units
					Min	Typ(1)	Max	Min	Typ(1)	Max	Min	Typ(1)	Max	Min	Typ(1)	Max	Min	Typ(1)	Max	
V_{IH}	High Level Input Voltage				2			2			2			2			2			V
V_{IL}	Low Level Input Voltage			DM54			0.8			0.8			0.7			0.8			0.8	V
				DM74			0.8			0.8			0.7			0.8			0.8	
V_I	Input Clamp Voltage	V_{CC} = Min	I_I = −8 mA							−1.5			N.A							V
			I_I = −12 mA				−1.5						N.A							
			I_I = −18 mA										N.A			−1.5		−1	−1.2	
I_{OH}	High Level Output Current						−400			−500			−200			−400			−1000	µA
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IL} = Max, I_{OH} = Max		DM54	2.4	3.4		2.4	3.5		2.4	3.3		2.5	3.4		2.5	3.4		V
				DM74	2.4	3.4		2.4	3.5		2.4	3.2		2.7	3.4		2.7	3.4		
I_{OL}	Low Level Output Current			DM54			16			20			2			4			20	mA
				DM74			16			20			3.6			8			20	
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2 V	I_{OL} = Max	DM54		0.2	0.4		0.2	0.4		0.15	0.3		0.25	0.4			0.5	V
				DM74		0.2	0.4		0.2	0.4		0.2	0.4		0.35	0.5			0.5	
			I_{OL} = 4 mA	DM74												0.4				
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max	V_I = 5.5 V				1			1			0.1						1	mA
			V_I = 7 V													0.1				
I_{IH}	High Level Input Current	V_{CC} = Max	V_I = 2.4 V				40			50			10							µA
			V_I = 2.7 V													20			50	
I_{IL}	Low Level Input Current	V_{CC} = Max	V_I = 0.3 V										−0.18							mA
			V_I = 0.4 V	LS30												−0.4				
				Others			−1.6			−2						−0.36				
			V_I = 0.5 V																−2	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (2)		DM54	−20		−55	−40		−100	−3		−15	−20		−100	−40		−100	mA
				DM74	−18		−55	−40		−100	−3		−15	−20		−100	−40		−100	
I_{CC}	Supply Current	V_{CC} = Max			See Table															

Note 1: All typical values are at V_{CC} = 5 V, T_A = 25°C.
Note 2: Not more than one output should be shorted at a time, and for DM54H/DM74H, DM54LS/DM74LS and DM54S/DM74S, duration of short circuit should not exceed one second.

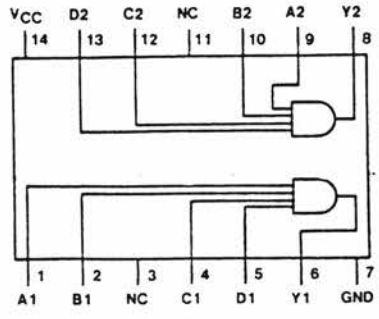
Supply Currents

Device	I_{CCH} (mA) Total With Outputs High		I_{CCL} (mA) Total With Outputs Low	
	Typ	Max	Typ	Max
00	4	8	12	22
04	6	12	18	33
10	3	6	9	16.5
20	2	4	6	11
30	1	2	3	6
H00	10	16.8	26	40
H04	16	26	40	58
H10	7.5	12.6	19.5	30
H20	5	8.4	13	20
H30	2.5	4.2	6.5	10
L00	0.44	0.8	1.16	2.04
L04	0.60	1.2	1.74	3.06
L10	0.33	0.6	0.87	1.53
L20	0.22	0.4	0.58	1.02
L30	0.11	0.2	0.29	0.51
LS00	0.8	1.6	2.4	4.4
LS04	1.2	2.4	3.6	6.6
LS10	0.6	1.2	1.8	3.3
LS20	0.4	0.8	1.2	2.2
LS30	0.35	0.5	0.6	1.1
S00	10	16	20	36
S04	15	24	30	54
S10	7.5	12	15	27
S20	5	8	10	18
S30	3	5	5.5	10
S133	3	5	5.5	10

Switching Characteristics at V_{CC} = 5 V, T_A = 25°C

Device	Conditions	t_{PLH} (ns) Propagation Delay Time, Low-To-High Output			t_{PHL} (ns) Propagation Delay Time, High-To-Low Output		
		Min	Typ	Max	Min	Typ	Max
00, 10	C_L = 15 pF, R_L = 400 Ω		11	22		7	15
04, 20			12	22		8	15
30			13	22		8	15
H00	C_L = 25 pF, R_L = 280 Ω		5.9	10		6.2	10
H04			6	10		6.5	10
H10			5.9	10		6.3	10
H20			6	10		7	10
H30			6.8	10		8.9	12
L00, L04 L10, L20	C_L = 50 pF, R_L = 4 kΩ		35	60		31	60
L30			35	60		70	100
LS00, LS04	C_L = 15 pF, R_L = 2 kΩ	3	5	10	3	5	10
LS10, LS20	C_L = 50 pF, R_L = 2 kΩ	4	8	15	4	8	15
LS30	C_L = 15 pF, R_L = 2 kΩ	4	7	12	4	7	15
	C_L = 50 pF, R_L = 2 kΩ	5	9	18	5	11	20
S00, S04	C_L = 15 pF, R_L = 280 Ω	2	3	4.5	2	3	5
S10, S20	C_L = 50 pF, R_L = 280 Ω	2	4.5	7	2	5	8
S30, S133	C_L = 15 pF, R_L = 280 Ω	2	4	6	2	4.5	7
	C_L = 50 pF, R_L = 280 Ω	2	5.5	8	3	6.5	10

21 Dual 4-Input AND Gates



Y = ABCD

54H21 (J) **74H21 (N)**
54LS21 (J,W) **74LS21 (N)**

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted).

Parameter		Conditions			DM54/74 08, 11			DM54/74 H08, H11, H21			DM54/74 L08, L11			DM54/74 LS08, LS11, LS21			DM54/74 S08, S11			Units
					Min	Typ(1)	Max	Min	Typ(1)	Max	Min	Typ(1)	Max	Min	Typ(1)	Max	Min	Typ(1)	Max	
V_{IH}	High Level Input Voltage				2			2			2			2			2			V
V_{IL}	Low Level Input Voltage			DM54			0.8			0.8			0.7			0.8			0.8	V
				DM74			0.8			0.8			0.7			0.8			0.8	
V_I	Input Clamp Voltage	V_{CC} = Min	I_I = −8 mA							−1.5			N/A							V
			I_I = −12 mA				−1.5						N/A							
			I_I = −18 mA										N/A			−1.5			−1.2	
I_{OH}	High Level Output Current						−800			−500			−200			−400			−1000	µA
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2 V, I_{OH} = Max		DM54	2.4	3.4		2.4	3.4		2.4	3.3		2.5	3.4		2.5	3.4		V
				DM74	2.4	3.4		2.4	3.4		2.4	3.2		2.7	3.4		2.7	3.4		
I_{OL}	Low Level Output Current			DM54			16			20			2			4			20	mA
				DM74			16			20			3.6			8			20	
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IL} = Max	I_{OL} = Max	DM54		0.2	0.4		0.2	0.4		0.15	0.3		0.25	0.4			0.5	V
				DM74		0.2	0.4		0.2	0.4		0.2	0.4		0.35	0.5			0.5	
			I_{OL} = 4 mA	DM74											0.25	0.4				
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max	V_I = 5.5 V				1			1			0.1						1	mA
			V_I = 7 V													0.1				
I_{IH}	High Level Input Current	V_{CC} = Max	V_I = 2.4 V				40			50			10							µA
			V_I = 2.7 V													20			50	
I_{IL}	Low Level Input Current	V_{CC} = Max	V_I = 0.3 V										−0.18							mA
			V_I = 0.4 V				−1.6			−2						−0.36				
			V_I = 0.5 V																−2	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (2)		DM54	−20		−55	−40		−100	−3		−15	−20		−100	−40		−100	mA
				DM74	−18		−55	−40		−100	−3		−15	−20		−100	−40		−100	
I_{CC}	Supply Current	V_{CC} = Max			See Table															

Note 1: All typical values are at V_{CC} = 5 V, T_A = 25°C.
Note 2: Not more than one output should be shorted at a time, and for DM54H/DM74H, DM54LS/DM74LS and DM54S/DM74S, duration of short circuit should not exceed one second.

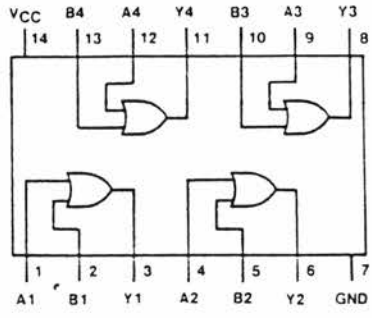
Supply Currents

Device	I_{CCH} (mA) Total With Outputs High		I_{CCL} (mA) Total With Outputs Low	
	Typ	Max	Typ	Max
08	11	21	20	33
11	8	15	14	22
H08	28	40	42	64
H11	18	30	30	48
H21	12	20	20	32
L08	1.1	2.1	2.0	3.3
L11	1.0	1.5	1.6	2.2
LS08	2.4	4.8	4.4	8.8
LS11	1.8	3.6	3.3	6.6
LS21	1.2	2.4	2.2	4.4
S08	18	32	32	57
S11	13.5	24	24	42

Switching Characteristics at V_{CC} = 5 V, T_A = 25°C

Device	Conditions	t_{PLH} (ns) Propagation Delay Time Low-To-High Level Output			t_{PHL} (ns) Propagation Delay Time, High-To-Low Level Output		
		Min	Typ	Max	Min	Typ	Max
08, 11	C_L = 15 pF, R_L = 400 Ω		17.5	27		12	19
H08, H11 H21	C_L = 25 pF, R_L = 280 Ω		7.8	12		8.8	12
L08	C_L = 50 pF		45	90		45	90
L11	R_L = 4 kΩ		40	80		45	90
LS08, LS11	C_L = 15 pF, R_L = 2 kΩ	4	8	13	3	7.5	11
LS21	C_L = 50 pF, R_L = 2 kΩ	6	11	18	5	11	18
S08, S11	C_L = 15 pF, R_L = 280 Ω	2.5	4.5	7	2.5	5	7.5
	C_L = 50 pF, R_L = 280 Ω	3	6	9	3	7.5	11

32 Quad 2-Input OR Gates



$Y = A + B$

5432 (J,W)
54L32 (J,W)
54LS32 (J,W)
54S32 (J,W)

7432 (N)
74L32 (N)
74LS32 (N)
74S32 (N)

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

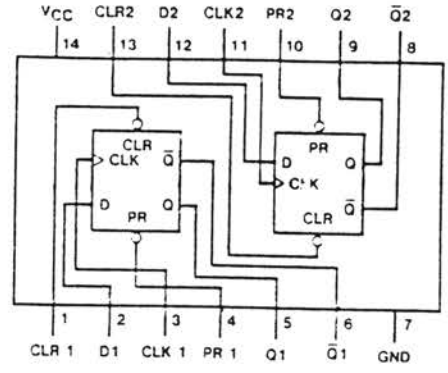
Parameter		Conditions			DM54 74 32 Min	DM54 74 32 Typ (1)	DM54 74 32 Max	DM54 74 L32 Min	DM54 74 L32 Typ (1)	DM54 74 L32 Max	DM54 74 LS32 Min	DM54 74 LS32 Typ (1)	DM54 74 LS32 Max	DM54 74 S32 Min	DM54 74 S32 Typ (1)	DM54 74 S32 Max	Units
V_{IH}	High Level Input Voltage				2			2			2			2			V
V_{IL}	Low Level Input Voltage			DM54			0.8			0.7			0.8			0.8	V
				DM74			0.8			0.7			0.8			0.8	
V_I	Input Clamp Voltage	V_{CC} = Min	I_I = −12 mA				−1.5			N.A.							V
			I_I = −18 mA							N.A.			−1.5			−1.2	
I_{OH}	High Level Output Current						−400			−200			−400			−1000	μA
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2 V, I_{OH} = Max		DM54	2.4	3.4		2.4	2.8		2.5	3.4		2.5	3.4		V
				DM74	2.4	3.4		2.4	2.8		2.7	3.4		2.7	3.4		
I_{OL}	Low Level Output Current			DM54			16			12			4			20	mA
				DM74			16			16			8			20	
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IL} = Max	I_{OL} = Max	DM54		0.2	0.4		0.15	0.3		0.25	0.4			0.5	V
				DM74		0.2	0.4			0.4		0.35	0.5			0.5	
			I_{OL} = 4 mA	DM74								0.25	0.4				
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max	V_I = 5.5 V				1			0.1						1	mA
			V_I = 7 V										0.1				
I_{IH}	High Level Input Current	V_{CC} = Max	V_I = 2.4 V				40			10							μA
			V_I = 2.7 V										20			50	
I_{IL}	Low Level Input Current	V_{CC} = Max	V_I = 0.3 V						−0.12	−0.18							mA
			V_I = 0.4 V				−1.6						−0.36				
			V_I = 0.5 V													−2	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (2)		DM54	−20		−55	−3	−9	−15	−20		−100	−40		−100	mA
				DM74	−18		−55	−3	−9	−15	−20		−100	−40		−100	
I_{CC}	Supply Current	Total Outputs High	V_{CC} = Max			15	22		1.5	2.2		3.1	5.2		18	32	mA
		Total Outputs Low				23	38		2.3	3.8		4.9	9.8		38	68	

Note 1: All typical values are at V_{CC} = 5 V, T_A = 25°C.
Note 2: Not more than one output should be shorted at one time, and for DM54LS/DM74LS and DM54S/74S duration of short circuit should not exceed one second.

Switching Characteristics at V_{CC} = 5 V, T_A = 25°C

Device	Conditions	t_{PLH} (ns) Propagation Delay Time, Low-To-High Level Output			t_{PHL} (ns) Propagation Delay Time, High-To-Low Level Output		
		Min	Typ	Max	Min	Typ	Max
32	C_L = 15 pF, R_L = 400 Ω		10	15		14	22
L32	C_L = 50 pF, R_L = 4 kΩ		40	80		50	100
LS32	C_L = 15 pF, R_L = 2 kΩ	3	7	11	3	7	11
	C_L = 50 pF, R_L = 2 kΩ	4	10	15	4	10	15
S32	C_L = 15 pF, R_L = 280 Ω	2	4	7	2	4	7
	C_L = 50 pF, R_L = 280 Ω	2	5	9	2	5	9

74 Dual D Positive-Edge-Triggered Flip-Flops with Preset and Clear



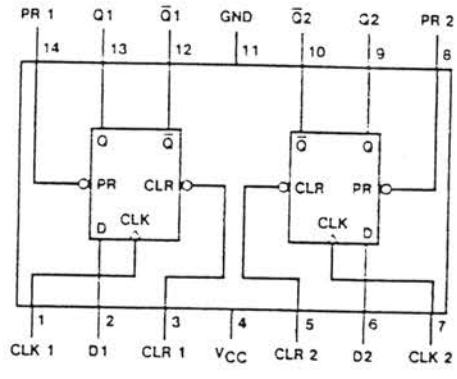
5474 (J)
54H74 (J)
54L74 (J)
54LS74A (J,W)
54S74 (J,W)

7474 (N)
74H74 (N)
74L74 (N)
74LS74A (N)
74S74 (N)

Truth Table

Inputs				Outputs	
PR	CLR	CLK	D	Q	$\bar{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q0	$\bar{Q}$0

Notes: Q0 = the level of Q before the indicated input conditions were established.
*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.



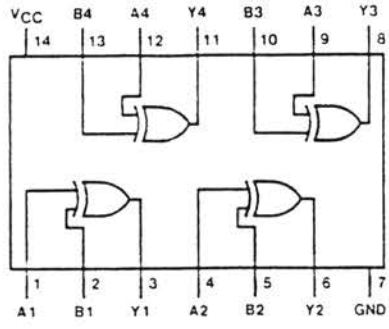
5474 (W); 54L74 (W)

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted).

Parameter			Conditions		DM54/74												Units
					S74			S112			S113			S114			
					Min	Typ (1)	Max	Min	Typ (1)	Max	Min	Typ (1)	Max	Min	Typ (1)	Max	
V_{IH}	High Level Input Voltage				2			2			2			2			V
V_{IL}	Low Level Input Voltage						0.8			0.8			0.8			0.8	V
V_I	Input Clamp Voltage		V_{CC} = Min, I_I = −18 mA				−1.2			−1.2			−1.2			−1.2	V
I_{OH}	High Level Output Current						−1			−1			−1			−1	mA
V_{OH}	High Level Output Voltage		V_{CC} = Min, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −1 mA	DM54	2.5	3.4		2.5	3.4		2.5	3.4		2.5	3.4		V
				DM74	2.7	3.4		2.7	3.4		2.7	3.4		2.7	3.4		
I_{OL}	Low Level Output Current						20			20			20			20	mA
V_{OL}	Low Level Output Voltage		V_{CC} = Min, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 20 mA				0.5			0.5			0.5			0.5	V
I_I	Input Current at Maximum Input Voltage		V_{CC} = Max, V_I = 5.5 V				1			1			1			1	mA
I_{IH}	High Level Input Current	J, K, or D	V_{CC} = Max, V_I = 2.7 V				50			50			50			50	µA
		Clear					150			100			N/A			200	
		Preset					100			100			100			100	
		Clock					100			100			100			200	
I_{IL}	Low Level Input Current	J, K, or D	V_{CC} = Max, V_I = 0.5 V				−2			−1.6			−1.6			−1.6	mA
		Clear (2)					−6			−7			N/A			−14	
		Preset (2)					−4			−7			−7			−7	
		Clock					−4			−4			−4			−8	
I_{OS}	Short Circuit Output Current		V_{CC} = Max (3)		−40		−100	−40		−100	−40		−100	−40		−100	mA
I_{CC}	Supply Current		V_{CC} = Max (4)			30	50		30	50		30	50		30	50	mA

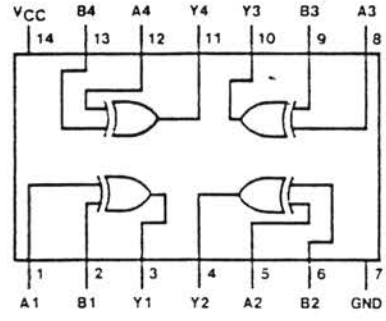
Note 1: All typical values are at V_{CC} = 5 V, T_A = 25°C.
Note 2: Clear tested w/ preset high and preset tested w/ clear high.
Note 3: Not more than one output should be shorted at a time, and duration of short circuit should not exceed one second.
Note 4: With all outputs open, I_{CC} is measured with the Q and Q̄ outputs high in turn. At the time of measurement, the clock input is grounded.

86 Quad 2-Input EXCLUSIVE-OR Gates



5486 (J,W)
54LS86 (J,W)
54S86 (J,W)

7486 (N)
74LS86 (N)
74S86 (N)



54L86 (J); 74L86 (N)

Truth Table
(86,L86, LS86, S86)

Inputs		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

$Y = A \oplus B = \bar{A}B + A\bar{B}$

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted).

Parameter		Conditions			DM54/74 86			DM54/74 L86			DM54/74 LS86, LS386			DM54/74 S86			Units
					Min	Typ (1)	Max	Min	Typ (1)	Max	Min	Typ (1)	Max	Min	Typ (1)	Max	
V_{IH}	High Level Input Voltage				2			2			2			2			V
V_{IL}	Low Level Input Voltage			DM54			0.8			0.7			0.8			0.8	V
				DM74			0.8			0.7			0.8			0.8	
V_I	Input Clamp Voltage	V_{CC} = Min	I_I = −12 mA				−1.5			N.A							V
			I_I = −18 mA							N.A			−1.5			−1.2	
I_{OH}	High Level Output Current						−800			−200			−400			−1000	μA
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2 V, V_{IL} = Max, I_{OH} = Max		DM54	2.4	3.4		2.4	3.3		2.5	3.4		2.5	3.4		V
				DM74	2.4	3.4		2.4	3.2		2.7	3.4		2.7	3.4		
I_{OL}	Low Level Output Current			DM54			16			2			4			20	mA
				DM74			16			3.6			8			20	
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2 V, V_{IL} = Max	I_{OL} = Max	DM54		0.2	0.4		0.15	0.3		0.25	0.4			0.5	V
				DM74		0.2	0.4		0.2	0.4		0.35	0.5			0.5	
			I_{OL} = 4 mA	DM74								0.25	0.4				
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max	V_I = 5.5 V				1			0.2						1	mA
			V_I = 7 V										0.2				
I_{IH}	High Level Input Current	V_{CC} = Max	V_I = 2.4 V				40			20							μA
			V_I = 2.7 V										40			50	
I_{IL}	Low Level Input Current	V_{CC} = Max	V_I = 0.3 V							−0.36							mA
			V_I = 0.4 V				−1.8						−0.8				
			V_I = 0.5 V													−2	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (2)		DM54	−20		−55	−3		−15	−20		−100	−40		−100	mA
				DM74	−18		−55	−3		−15	−20		−100	−40		−100	
I_{CCH}	Supply Current, All Outputs High	V_{CC} = Max (3)		DM54		30	43		22	44		8.1	10		35	50	mA
				DM74		30	50		22	44		8.1	10		35	50	
I_{CCL}	Supply Current, All Outputs Low	V_{CC} = Max (4)				38	57		38	6.68					50	75	mA

Note 1: All typical values are at V_{CC} = 5 V, T_A = 25°C.
Note 2: Not more than one output should be shorted at a time, and for DM54LS, DM74LS and DM54S, DM74S, duration of short circuit should not exceed one second.
Note 3: I_{CCH} is measured with all outputs open, one input of each gate at 4.5 V, and the other inputs grounded.
Note 4: I_{CCL} is measured with all outputs open and all inputs at 4.5 V.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

Device	Conditions		t_{PLH} (ns) Propagation Delay Time, Low-To-High Level Output			t_{PHL} (ns) Propagation Delay Time, High-To-Low Level Output		
			Min	Typ	Max	Min	Typ	Max
86	C_L = 15 pF, R_L = 400 Ω	Other Input Low		15	23		11	17
		Other Input High		18	30		13	22
L86	C_L = 50 pF, R_L = 4 kΩ	Other Input Low		37	60		21	60
		Other Input High		25	60		35	60
LS86	C_L = 15 pF, R_L = 2 kΩ	Other Input Low		12	18		10	17
		Other Input High		7	10		6	12
LS86	C_L = 50 pF, R_L = 2 kΩ	Other Input Low		15	23		14	21
		Other Input High		10	15		10	15

4-Bit Binary Counters

93 Divide-By-Two and Divide-By-Eight

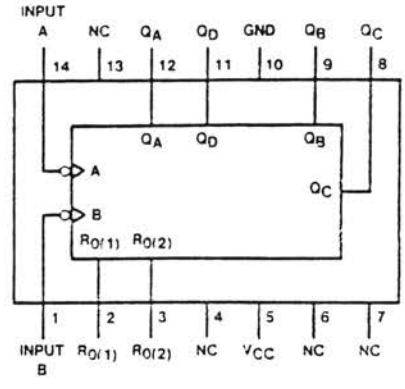
'93A, 'L93, 'LS93
Count Sequence
(See Note C)

Count	Output			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

'93A, 'L93, 'LS93
Reset/Count Function Table

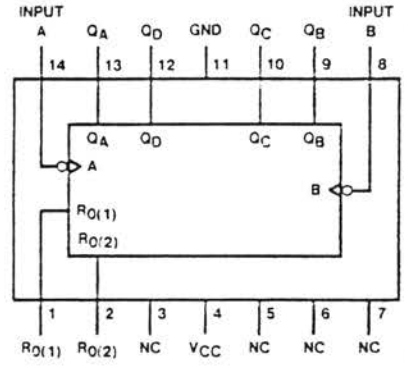
Reset Inputs		Output			
$R_{O(1)}$	$R_{O(2)}$	Q_D	Q_C	Q_B	Q_A
H	H	L	L	L	L
L	X	COUNT			
X	L	COUNT			

C Output Q_A is connected to input B.



5493A (J,W)
54LS93 (J,W)

7493A (N)
74LS93 (N)



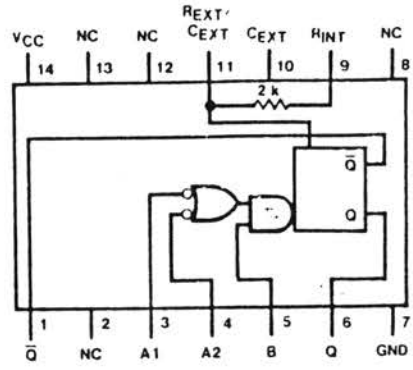
54L93 (J,W); 74L93 (N)

NC—No internal connection (54LS93, 74LS93)
NC—Make no external connection (5493A, 7493A) (54L93, 74L93)

121 One Shots

Truth Table

Inputs			Outputs	
A1	A2	B	Q	$\overline{Q}$
L	X	H	L	H
X	L	H	L	H
X	X	L	L	H
H	H	X	L	H
H	↓	H	⌐¬	¬⌐
↓	H	H	⌐¬	¬⌐
↓	↓	H	⌐¬	¬⌐
L	X	↑	⌐¬	¬⌐
X	L	↑	⌐¬	¬⌐



54121 (J,W); 74121 (N)

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

Parameter		Conditions		DM54/74 121 Min	DM54/74 121 Typ (1)	DM54/74 121 Max	DM54/74 LS221 Min	DM54/74 LS221 Typ (1)	DM54/74 LS221 Max	Units
V_{T+}	Positive-Going Threshold Voltage at A Input	V_{CC} = Min			1.4	2		1.0	2	V
V_{T-}	Negative-Going Threshold Voltage at A Input	V_{CC} = Min	DM54	0.8	1.4		0.8	1.0		V
			DM74	0.8	1.4		0.8	1.0		
V_{T+}	Positive-Going Threshold Voltage at B Input	V_{CC} = Min			1.55	2		1.0	2	V
V_{T-}	Negative-Going Threshold Voltage at B Input	V_{CC} = Min	DM54	0.8	1.35		0.8	0.9		V
			DM74	0.8	1.35		0.8	0.9		
V_I	Input Clamp Voltage	V_{CC} = Min	I_I = −12 mA			−1.5				V
			I_I = −18 mA						−1.5	
I_{OH}	High Level Output Current					−400			−400	μA
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = −400 μA	DM54	2.4	3.4		2.5	3.4		V
			DM74	2.4	3.4		2.7	3.4		
I_{OL}	Low Level Output Current		DM54			16			4	mA
			DM74			16			8	
V_{OL}	Low Level Output Voltage	V_{CC} = Min	I_{OL} = 4 mA					0.25	0.4	V
			I_{OL} = 8 mA DM74					0.35	0.5	
			I_{OL} = 16 mA		0.2	0.4				
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max	V_I = 5.5 V			1				mA
			V_I = 7 V						0.1	
I_{IH}	High Level Input Current	V_{CC} = Max, V_O = 2.4 V	A1 or A2			40				μA
			B			80				
		V_I = 2.7 V	All						20	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4 V	A1 or A2			−1.6			−4	mA
			B			−3.2			−8	
			Clear			N/A			−0.8	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (2)	DM54	−20		−55	−20		−100	mA
			DM74	−18		−55	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max	Quiescent		13	25		4.7	11	mA
			Triggered		23	40		19	27	

Note 1: All typical values are V_{CC} = 5 V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and for DM54LS221/DM74LS221, duration of short circuit should not exceed one second.

Switching Characteristics at V_{CC} = 5 V, T_A = 25°C

Parameter	From (Input)	To (Output)	DM54/74 121 Conditions	DM54/74 121 Min	DM54/74 121 Typ	DM54/74 121 Max	DM54S/74S LS221 Conditions	DM54S/74S LS221 Min	DM54S/74S LS221 Typ	DM54S/74S LS221 Max	Units
t_{PLH} Propagation Delay Time, Low to High Level Output	A1 or A2	Q	C_L = 15 pF, R_L = 400 Ω		45	70	C_{EXT} = 80 pF, R_{EXT} = 2 kΩ		45	70	ns
t_{PHL} Propagation Delay Time, High to Low Level Output	A1 or A2	Q			35	55			35	55	ns
t_{PLH} Propagation Delay Time, Low to High Level Output	B	Q			45	65			45	65	ns
t_{PHL} Propagation Delay Time, High to Low Level Output	B	Q			35	55			35	55	ns
t_{PLH} Propagation Delay Time, Low to High Level Output	Clear	Q			N/A				N/A		ns
t_{PHL} Propagation Delay Time, High to Low Level Output	Clear	Q			50	80			50	80	ns
t_{PHL} Propagation Delay Time, High to Low Level Output	A1 or A2	$\overline{Q}$			40	65			40	65	ns
t_{PLH} Propagation Delay Time, High to Low Level Output	B	$\overline{Q}$			N/A				N/A		ns
t_{PHL} Propagation Delay Time, High to Low Level Output	Clear	$\overline{Q}$			70	110			70	150	ns
$t_{W(OUT)}$ Output Pulse Width	Internal Timing Resistor (1)	Q or $\overline{Q}$	C_{EXT} = 80 pF, R_{INT} to V_{CC}		30	50	C_{EXT} = 80 pF, R_{INT} to V_{CC}		30	50	ns
	Zero Timing Capacitance		C_{EXT} = 0, R_{INT} to V_{CC}		100	800	C_{EXT} = 100 pF, R_{EXT} = 10 kΩ		100	800	ns
	External Timing Resistance		C_{EXT} = 1 μF, R_{EXT} = 10 kΩ		7	8	C_{EXT} = 1 μF, R_{EXT} = 10 kΩ		7	8	ms
$t_{W(H)}$ Input Pulse Width				50				40			ns
$t_{W(CLEAR)}$ Clear Pulse Width				N/A				40			ns
t_r, t_f Rate of Rise or Fall of Input Pulse										1	V/s
R_{ext} External Timing Resistance	Schmitt Input B			1				1			kΩ
	Logic Input A			1				1		30	
				DM54 1.4				DM54 1.4		40	
				DM74 1.6				DM74 1.4		40	
C_{EXT} External Timing Capacitance				0				0		1000	pF
$t_{WC(H)}$ Clear Inactive State Setup Time								15		N-A	ns
Duty Cycle			R_T = 2 kΩ			67				67	%
			R_T = Max R_{ext}			90				90	

Note 1: Use of internal timing resistor applies to DM54/74121 only.

125 TRI-STATE® Quad Buffers

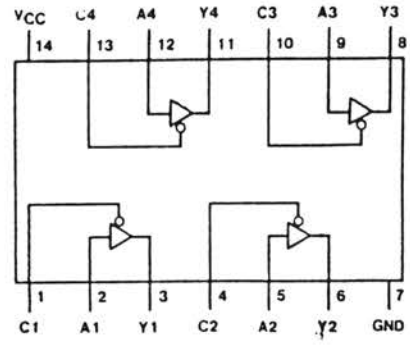
Truth Table

Inputs		Output
A	C	Y
H	L	H
L	L	L
X	H	Hi-Z

Y = A

Supply Currents

Device	Conditions: Data Inputs	Conditions: Output Controls	I_{CC} (mA): Min	Typ (1)	Max
125	0 V	4.5 V		32	54
126	0 V	0 V		38	62
LS125A	0 V	4.5 V		11	20
LS126A	0 V	0 V		12	22
S134	0 V	0 V		7	13
	5 V	0 V		9	16
	5 V	5 V		14	25



54125 (J,W) **74125 (N)**
54LS125A (J,W) **74LS125A (N)**

Notes: ⎍⎍ = one high-level pulse; ⎍⎍ = one low-level pulse
An external timing capacitor may be connected between C_{EXT} and $R_{EXT} \cdot C_{EXT}$ (positive)
For accurate repeatable pulse widths, connect an external resistor between $R_{EXT} \cdot C_{EXT}$ and V_{CC}
To obtain variable pulse widths, connect external variable resistance between $R_{EXT} \cdot C_{EXT}$ and V_{CC}

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

Parameter		Conditions			DM54/74 125, 126 Min	Typ (1)	Max	DM54/74 LS125A, LS126A Min	Typ (1)	Max	DM54/74 S134 Min	Typ (1)	Max	Units
V_{IH}	High Level Input Voltage				2			2			2			V
V_{IL}	Low Level Inut Voltage			DM54			0.8			0.8			0.8	V
				DM74			0.8			0.8			0.8	
V_I	Input Clamp Voltage	V_{CC} = Min	I_I = −12 mA				−1.5							V
			I_I = −18 mA							−1.5			−1.2	
I_{OH}	High Level Output Current			DM54			−2.0			−1.0			−6.5	mA
				DM74			−5.2			−2.6			−6.5	
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2 V, V_{IL} = Max, I_{OH} = Max		DM54	2.4	3.3		2.4	3.4		2.4	3.4		V
				DM74	2.4	3.1		2.4	3.1		2.4	3.2		
I_{OL}	Low Level Output Current			DM54			16			12			20	mA
				DM74			16			24			20	
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2 V, V_{IL} = Max	I_{OL} = Max	DM54			0.4			0.4			0.5	V
				DM74			0.4			0.5			0.5	
			I_{OL} = 12 mA	DM74						0.4				
$I_{O(OFF)}$	Off-State (High Impedance State) Output Current	V_{CC} = Max, V_{IH} = 2 V	V_{IL} = 0.8 V	V_O = 0.4 V						−20				μA
				V_O = 2.4 V						20				
			V_{IL} = 0.8 V	V_O = 0.4 V			−40							
				V_O = 0.5 V									−50	
				V_O = 2.4 V			40						50	
$I_{I(OFF)}$	Off-State (High Impedance State) Input Current	V_{CC} = Max, V_I = 0.4 V (0.5 V for DM54S/74S)					−40			−20			−50	μA
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max	V_I = 5.5 V				1						1	mA
			V_I = 7.0 V							0.1				
I_{IH}	High Level Input Current	V_{CC} = Max	V_I = 2.4 V				40							μA
			V_I = 2.7 V							20			50	
I_{IL}	Low Level Input Current	V_{CC} = Max	V_I = 0.4 V				−1.6			−0.4				mA
			V_I = 0.5 V										−2	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (2)		DM54	−30		−70	−20		−100	−40		−100	mA
				DM74	−28		−70	−20		−100	−40		−100	
I_{CC}	Supply Current	V_{CC} = Max			See Table									

Note 1: All typical values are at V_{CC} = 5 V and T_A = 25°C
Note 2: Not more than one output should be shorted at a time, and for DM54LS/DM74LS and DM54S/74S, duration of short circuit should not exceed one second

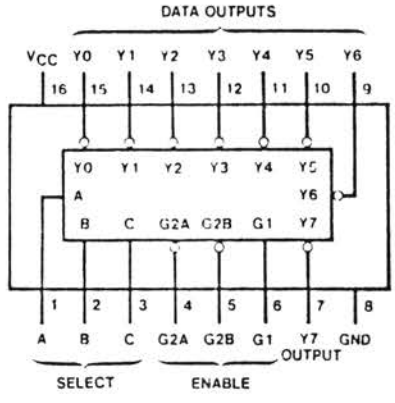
tching Characteristics

:S V_{CC} = 5 V T_A = 25°C

Parameter	Conditions	DM54LS/74LS LS125A Min	Typ	Max	LS126A Min	Typ	Max	Conditions	LS125A Min	Typ	Max	LS126A Min	Typ	Max	Units
Propagation Delay Time Low to High Level Output	C_L = 50 pF, R_L = 667 Ω		10	15		10	15	C_L = 150 pF, R_L = 667 Ω		14	21		14	21	ns
Propagation Delay Time High to Low Level Output			10	18		10	18			15	22		15	22	ns
Output Enable Time to High Level			19	25		22	30			23	35		24	36	ns
Output Enable Time to Low Level			16	25		14	30			24	40		20	42	ns
Output Disable Time From High Level	C_L = 5 pF, R_L = 667 Ω		10	20		10	25								ns
Output Disable Time From Low Level			12	20		14	25								ns

Conditions	DM54/74 125 Min	Typ	Max	126 Min	Typ	Max	Conditions	DM54/74 S134 Min	Typ	Max	Units
C_L = 50 pF, R_L = 400 Ω		10	15		10	15	C_L = 15 pF, R_L = 280 Ω		4	6	ns
							C_L = 50 pF, R_L = 280 Ω		5.5	9	
		12	18		12	18	C_L = 15 pF, R_L = 280 Ω		5	7.5	ns
							C_L = 50 pF, R_L = 280 Ω		7	11	
		12	18		13	19	C_L = 50 pF, R_L = 280 Ω		13	19.5	ns
		8	25		14	25			14	21	ns
C_L = 5 pF, R_L = 400 Ω		5	8		10	16	C_L = 5 pF, R_L = 280 Ω		5.5	8.5	ns
		4	4		14	20			4	14	ns

138 3-to-8 Line Decoders Multiplexers



54LS138 (J,W) 74LS138 (N)
54S138 (J,W) 74S138 (N)

Truth Tables

LS138, S138

Inputs					Outputs							
Enable		Select										
G1	G2*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

LS139, S139

Inputs			Outputs			
Enable	Select					
G	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

H = high level, L = low level, X = don't care

*G2 = G2A + G2B
H = High level, L = low level, X = don't care

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

Parameter		From (Input)	To (Output)	Levels of Delay	Conditions	DM54/74 LS138 Min	LS138 Typ	LS138 Max	DM54/74 LS139 Min	LS139 Typ	LS139 Max	Conditions	DM54/74 S138 Min	S138 Typ	S138 Max	DM54/74 S139 Min	S139 Typ	S139 Max	Units
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Binary Select	Any	2	C_L = 15 pF, R_L = 2 kΩ		13	18		13	18	C_L = 15 pF, R_L = 280 Ω		4.5	7		5	7.5	ns
					C_L = 50 pF, R_L = 2 kΩ		18	27		18	27	C_L = 50 pF, R_L = 280 Ω		6	9		6.5	10	
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				C_L = 15 pF, R_L = 2 kΩ		17	27		17	27	C_L = 15 pF, R_L = 280 Ω		7	10.5		6.5	10	ns
					C_L = 50 pF, R_L = 2 kΩ		23	40		23	40	C_L = 50 pF, R_L = 280 Ω		9	14		8.5	13	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output			3	C_L = 15 pF, R_L = 2 kΩ		13	18		13	18	C_L = 15 pF, R_L = 280 Ω		7.5	12		7	12	ns
					C_L = 50 pF, R_L = 2 kΩ		18	27		18	27	C_L = 50 pF, R_L = 280 Ω		9	14		8.5	13	
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				C_L = 15 pF, R_L = 2 kΩ		17	27		17	27	C_L = 15 pF, R_L = 280 Ω		8	12		8	12	ns
					C_L = 50 pF, R_L = 2 kΩ		23	40		23	40	C_L = 50 pF, R_L = 280 Ω		10	15		10	15	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Enable	Any	2	C_L = 15 pF, R_L = 2 kΩ		13	18		13	18	C_L = 15 pF, R_L = 280 Ω		5	8		5	8	ns
					C_L = 50 pF, R_L = 2 kΩ		18	27		18	27	C_L = 50 pF, R_L = 280 Ω		6.5	10		6.5	10	
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				C_L = 15 pF, R_L = 2 kΩ		16	24		16	24	C_L = 15 pF, R_L = 280 Ω		7	11		6.5	10	ns
					C_L = 50 pF, R_L = 2 kΩ		22	40		22	40	C_L = 50 pF, R_L = 280 Ω		9	14		8.5	13	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output			3	C_L = 15 pF, R_L = 2 kΩ		13	18			N/A	C_L = 15 pF, R_L = 280 Ω		7	11			N/A	ns
					C_L = 50 pF, R_L = 2 kΩ		18	27			N/A	C_L = 50 pF, R_L = 280 Ω		8.5	13			N/A	
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				C_L = 15 pF, R_L = 2 kΩ		19	28			N/A	C_L = 15 pF, R_L = 280 Ω		7	11			N/A	ns
					C_L = 50 pF, R_L = 2 kΩ		24	40			N/A	C_L = 50 pF, R_L = 280 Ω		9	14			N/A	

4-Line to 16-Line Decoders/Demultiplexers

General Description

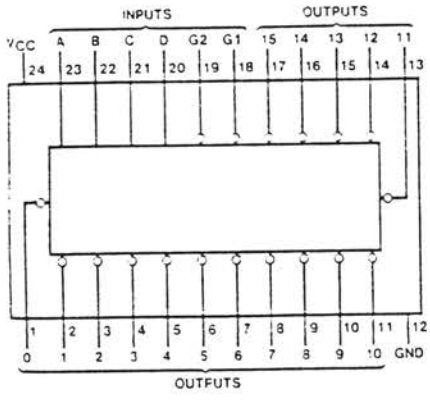
Each of these 4-line-to-16-line decoders utilizes TTL circuitry to decode four binary-coded inputs into one of sixteen mutually exclusive outputs when both the strobe inputs, G1 and G2, are low. The demultiplexing function is performed by using the 4 input lines to address the output line, passing data from one of the strobe inputs with the other strobe input low. When either strobe input is high, all outputs are high. These demultiplexers are ideally suited for implementing high-performance memory decoders. All inputs are buffered and input clamping diodes are provided to minimize transmission-line effects and thereby simplify system design.

Features

- Decodes 4 binary-coded inputs into one of 16 mutually exclusive outputs
- Performs the demultiplexing function by distributing data from one input line to any one of 16 outputs
- Input clamping diodes simplify system design
- High fan-out, low-impedance, totem-pole outputs

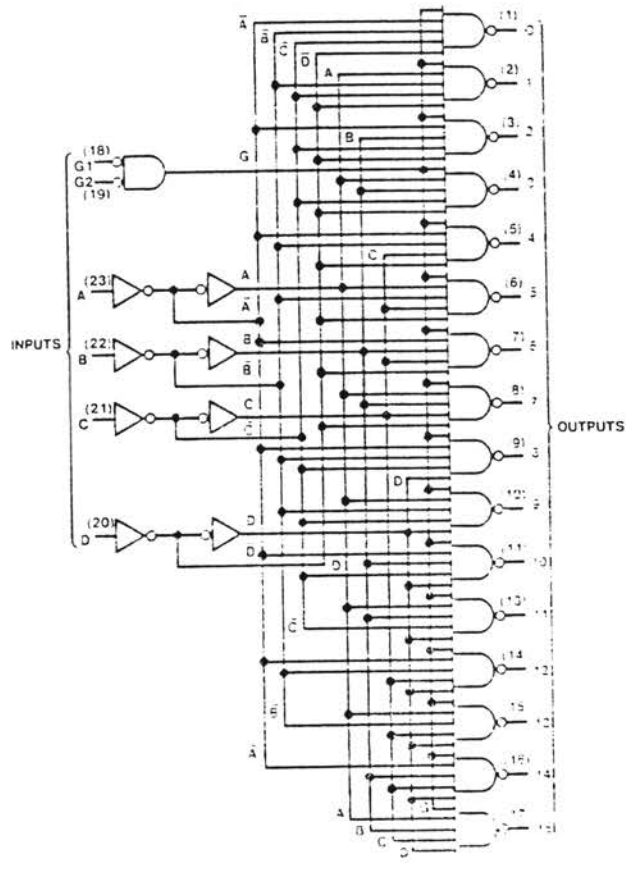
Type	Typical Propagation Delay		Typical Power Dissipation
	3 Levels of Logic	Strobe	
154	19 ns	18 ns	170 mW
L154A	55 ns	45 ns	24 mW
LS154	23 ns	19 ns	45 mW

Connection and Logic Diagrams



54154 (J,F)
54L154A (J,F)
54LS154 (J,F)

74154 (N)
74L154A (N)
74LS154 (N)



Hex / Quad D Flip-Flops with Clear

General Description

These positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic. All have a direct clear input, and the quad (175) versions feature complementary outputs from each flip-flop.

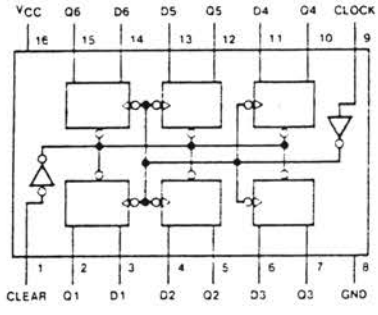
Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

Features

- 174, LS174, S174 contain six flip-flops with single-rail outputs.
- 175, LS175, S175 contain four flip-flops with double-rail outputs.
- Buffered clock and direct clear inputs
- Individual data input to each flip-flop
- Applications include:
  - Buffer storage registers
  - Shift registers
  - Pattern generators

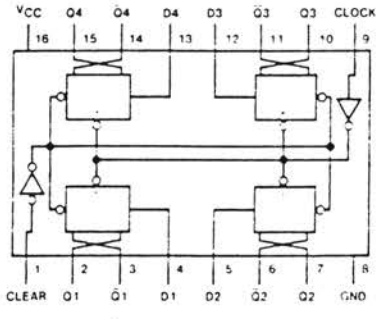
Type	Typical Clock Frequency	Typical Power Dissipation Per Flip-Flop
174, 175	40 MHz	38 mW
LS174, LS175	40 MHz	14 mW
S174, S175	110 MHz	75 mW

Connection Diagrams



54174 (J,W)
54LS174 (J,W)
54S174 (J,W)

74174 (N)
74LS174 (N)
74S174 (N)

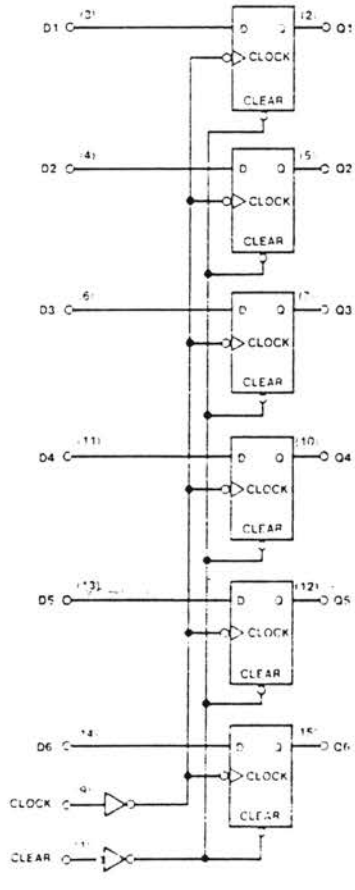


54175 (J,W)
54LS175 (J,W)
54S175 (J,W)

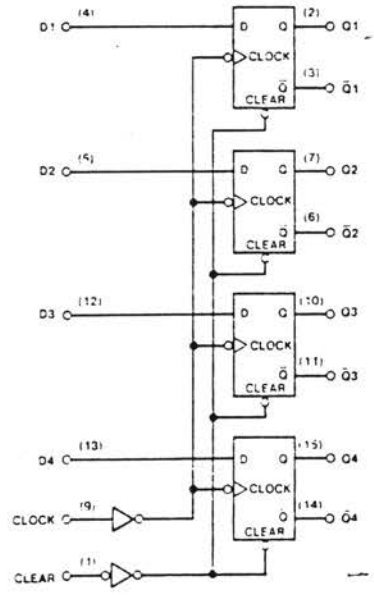
74175 (N)
74LS175 (N)
74S175 (N)

Logic Diagrams

174, LS174, S174



175, LS175, S175



SN54LS192/ SN74LS192

PRESETTABLE BCD/DECADE UP/DOWN COUNTER

SN54LS193/ SN74LS193

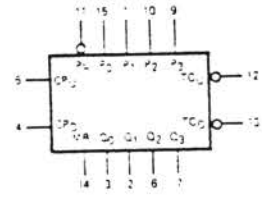
PRESETTABLE 4-BIT BINARY UP/DOWN COUNTER

DESCRIPTION – The SN54LS192/SN74LS192 is an UP/DOWN BCD Decade (8421) Counter and the SN54LS193/SN74LS193 is an UP/DOWN MODULO-16 Binary Counter. Separate Count Up and Count Down Clocks are used and in either counting mode the circuits operate synchronously. The outputs change state synchronous with the LOW-to-HIGH transitions on the clock inputs.

Separate Terminal Count Up and Terminal Count Down outputs are provided which are used as the clocks for a subsequent stages without extra logic, thus simplifying multistage counter designs. Individual preset inputs allow the circuits to be used as programmable counters. Both the Parallel Load ($\overline{PL}$) and the Master Reset (MR) inputs asynchronously override the clocks.

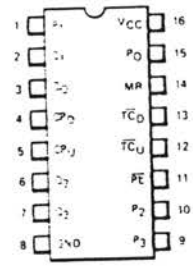
- LOW POWER . . . . 95 mW TYPICAL DISSIPATION
- HIGH SPEED . . . 40 MHz TYPICAL COUNT FREQUENCY
- SYNCHRONOUS COUNTING
- ASYNCHRONOUS MASTER RESET AND PARALLEL LOAD
- INDIVIDUAL PRESET INPUTS
- CASCADING CIRCUITRY INTERNALLY PROVIDED
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM DIP (TOP VIEW)



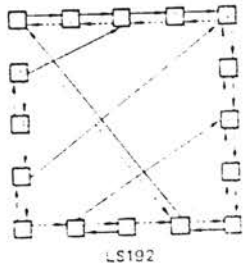
NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES

		LOADING (Note a) HIGH	LOW
CP_U	Count Up Clock Pulse Input	0.5 U.L.	0.25 U.L.
CP_D	Count Down Clock Pulse Input	0.5 U.L.	0.25 U.L.
MR	Asynchronous Master Reset (Clear) Input	0.5 U.L.	0.25 U.L.
$\overline{PL}$	Asynchronous Parallel Load (Active LOW) Input	0.5 U.L.	0.25 U.L.
P_n	Parallel Data Inputs	0.5 U.L.	0.25 U.L.
Q_n	Flip-Flop Outputs (Note b)	10 U.L.	5(2.5) U.L.
$\overline{TC}_D$	Terminal Count Down (Borrow) Output (Note b)	10 U.L.	5(2.5) U.L.
$\overline{TC}_U$	Terminal Count Up (Carry) Output (Note b)	10 U.L.	5(2.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 µA HIGH/1.6 mA LOW
b. The Output LOW drive factor is 2.5 U.L. for MILITARY (54) and 5 U.L. for COMMERCIAL (74) Temperature Ranges.

STATE DIAGRAMS



LS192

LS192 LOGIC EQUATIONS FOR TERMINAL COUNT

$\overline{TC}_U = Q_0 \cdot Q_2 \cdot \overline{CP}_U$

$\overline{TC}_D = \overline{Q_0} \cdot \overline{Q_1} \cdot \overline{Q_2} \cdot \overline{Q_3} \cdot \overline{CP}_D$

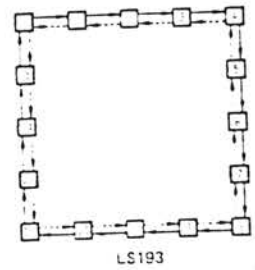
LS193 LOGIC EQUATIONS FOR TERMINAL COUNT

$\overline{TC}_U = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot \overline{CP}_U$

$\overline{TC}_D = \overline{Q_0} \cdot \overline{Q_1} \cdot \overline{Q_2} \cdot \overline{Q_3} \cdot \overline{CP}_D$

COUNT UP ——

COUNT DOWN ·····



LS193

Octal TRI-STATE® Buffers/Line Drivers/Line Receivers

General Description

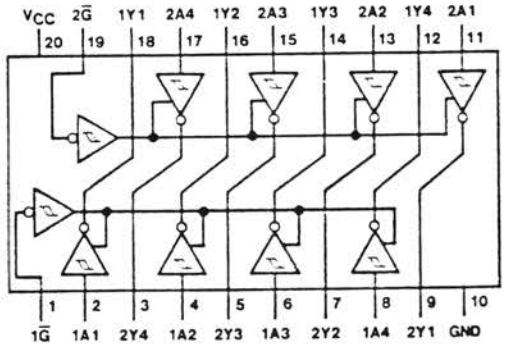
These buffers/line drivers are designed to improve both the performance and PC board density of TRI-STATE® buffers/drivers employed as memory-address drivers, clock drivers, and bus-oriented transmitters/receivers. Featuring 400 mV of hysteresis at each low current PNP data line input, they provide improved noise rejection and high fanout outputs, and can be used to drive terminated lines down to 133 Ω.

Features

- TRI-STATE outputs drive bus lines directly
- PNP inputs reduce DC loading on bus lines
- Hysteresis at inputs improves noise margins

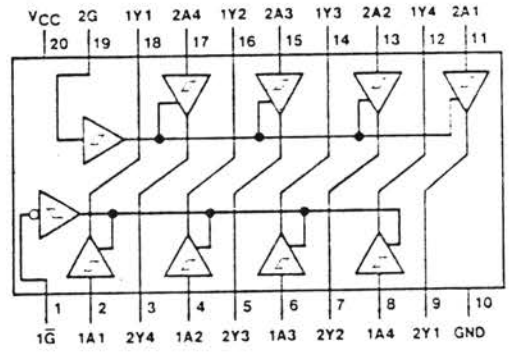
	Typical I_{OL} (Sink Current)	Typical I_{OH} (Source Current)	Typical Propagation Delay Times		Typical Enable/ Disable Times	Typical Power Dissipation (Enabled)	
			Inverting	Noninverting		Inverting	Noninverting
54LS	12 mA	−12 mA	10.5 ns	12 ns	18 ns	130 mW	135 mW
74LS	24 mA	−15 mA	10.5 ns	12 ns	18 ns	130 mW	135 mW
54S	48 mA	−12 mA	4.5 ns	6 ns	9 ns	450 mW	538 mW
74S	64 mA	−15 mA	4.5 ns	6 ns	9 ns	450 mW	538 mW

Connection Diagrams



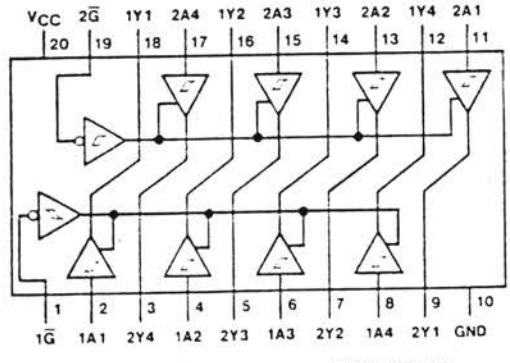
54LS240 (J)
54S240 (J)

74LS240 (N)
74S240 (N)



54LS241 (J)
54S241 (J)

74LS241 (N)
74S241 (N)



54LS244 (J)
54S244 (J)

74LS244 (N)
74S244 (N)

TRI-STATE® Octal Bus Transceiver

General Description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation minimizes external timing requirements.

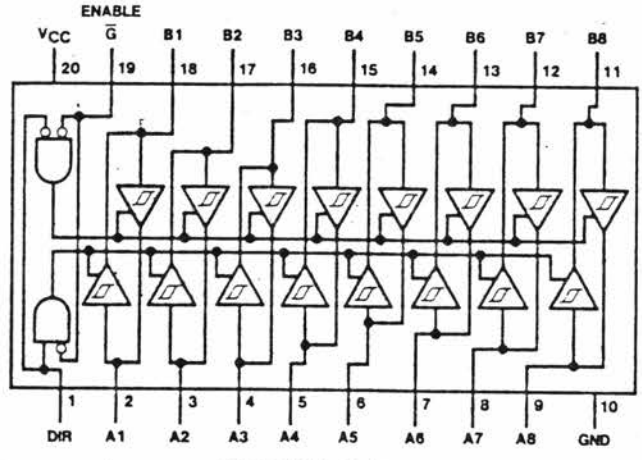
The device allows data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction control (DIR) input. The enable input ($\overline{G}$) can be used to disable the device so that the buses are effectively isolated.

Features

- Bi-directional bus transceiver in a high-density 20-pin package
- Tri-state outputs drive bus lines directly
- P-N-P inputs reduce D-C loading on bus lines
- Hysteresis at bus inputs improve noise margins
- Typical propagation delay times, port-to-port . . . 8 ns
- Typical enable/disable times . . . 17ns

Type	I_{OL} (Sink Current)	I_{OH} (Source Current)
54LS245	12 mA	−12 mA
74LS245	24 mA	−15 mA

Connection Diagram



54LS245 (J); 74LS245 (N)

Truth Table

Enable $\overline{G}$	Direction Control DIR	Operation
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

H = high level, L = low level, X = irrelevant

TRI-STATE® Octal D-Type Transparent Latches and Edge-Triggered Flip-Flops

General Description

These 8-bit registers feature totem-pole TRI-STATE outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

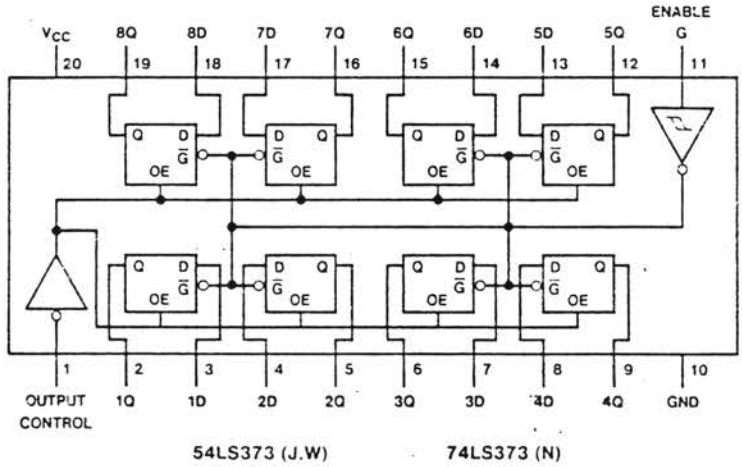
The eight latches of the DM54/74LS373 and DM54/74S373 are transparent D-type latches meaning that while the enable (G) is high the Q outputs will follow the data (D) inputs. When the enable is taken low the output will be latched at the level of the data that was set up.

(Continued next page)

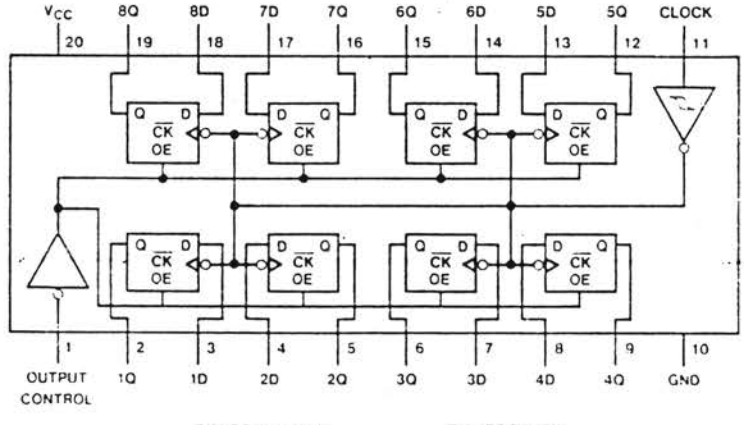
Features

- Choice of 8 Latches or 8 D-Type Flip-Flops in a Single Package
- TRI-STATE Bus-Driving Outputs
- Full Parallel-Access for Loading
- Buffered Control Inputs
- Clock/Enable Input Has Hysteresis to Improve Noise Rejection
- P-N-P Inputs Reduce D-C Loading on Data Lines (DM54/74S373 and DM54/74S374)

Connection Diagrams



54LS373 (J,W) 74LS373 (N)
54S373 (J,W) 74S373 (N)



54LS374 (J,W) 74LS374 (N)
54S374 (J,W) 74S374 (N)

ภาคผนวก ค

โปรแกรมที่ใช้ในการพัฒนา

```
                0001 ;
                0002 ;          OUTPUT PORTS NAME LIST
                0003 ;
(0000)          0004 PIO0       EQU     00H
(0001)          0005 PIO1       EQU     01H
(0002)          0006 PIO2       EQU     02H
(0003)          0007 PIO3       EQU     03H
(0004)          0008 WSCNT      EQU     04H
(0006)          0009 CLRX       EQU     06H
(0007)          0010 CLRY       EQU     07H
(0008)          0011 CLRZ       EQU     08H
(0009)          0012 SETX0      EQU     09H
(000A)          0013 SETX1      EQU     0AH
(000B)          0014 SETX2      EQU     0BH
(000C)          0015 SETX3      EQU     0CH
(000D)          0016 SETY0      EQU     0DH
(000E)          0017 SETY1      EQU     0EH
(000F)          0018 SETY2      EQU     0FH
(0010)          0019 SETY3      EQU     10H
(0011)          0020 SETZ0      EQU     11H
(0012)          0021 SETZ1      EQU     12H
(0013)          0022 SETZ2      EQU     13H
(0014)          0023 SETZ3      EQU     14H
(0015)          0024 OUTKL      EQU     15H
(0018)          0025 OCTC0      EQU     18H
(0019)          0026 OCTC1      EQU     19H
(001A)          0027 OCTC2      EQU     1AH
(001B)          0028 OTC3       EQU     1BH
(001E)          0029 WDSIO      EQU     1EH
(001F)          0030 WCSIO      EQU     1FH
                0031 ;          INPUT PORTS NAME LIST
                0032 ;
                0033 ;
(0000)          0034 INX0       EQU     00H
(0001)          0035 INX1       EQU     01H
(0002)          0036 INX2       EQU     02H
(0003)          0037 INX3       EQU     03H
(0004)          0038 INY0       EQU     04H
(0005)          0039 INY1       EQU     05H
(0006)          0040 INY2       EQU     06H
(0007)          0041 INY3       EQU     07H
(0008)          0042 INZ0       EQU     08H
(0009)          0043 INZ1       EQU     09H
(000A)          0044 INZ2       EQU     0AH
(000B)          0045 INZ3       EQU     0BH
(000C)          0046 INKB       EQU     0CH
(000E)          0047 RDSIO      EQU     0EH
(000F)          0048 RCSIO      EQU     0FH
                0049 ;
                0050 ;          1-BYTE BUFFER NAME LIST
                0051 ;
(3000)          0052 DISMEM     EQU     3000H   ;ST.ADDR DISPLAY AREA
(2BFF)          0053 ASTACK     EQU     2BFFH   ;ST.ADDR STACK AREA
(2000)          0054 SEGBUF     EQU     2000H   ;ST.ADDR 7-SEG BUFF.AREA
(20E0)          0055 NBCDBF     EQU     20E0H   ;ST.ADDR N-NUMBER BCD CODE
(2400)          0056 BUF.MAX    EQU     2400H   ;MAX.ADDR OF BCD-BUF
(2100)          0057 BCDBUF     EQU     2100H   ;ST.ADDR BCD-BUF (BCD VALUE)
```

```
(20A0)   BNXIN   EQU   20A0H   ;ADDR OF WORD TO RECORD ADDR.
                               ;OF NEXT ENTRY IN BCDBUF-↑IN
(20A1)   BNXOUT  EQU   20A1H   ;ADDR OF WORD TO RECORD ADDR.
                               ;OF NEXT ENTRY IN BCDBUF-↑OUT
(20A2)   BUFCNT  EQU   20A2H   ;ADDR. OF WORD TO RECORD NO.
                               ;OF WORDS WAITING FOR OUT.
(20B0)   FLAG    EQU   20B0H   ;FLAG WORD ADDRESS.
(20B1)   MWSIO   EQU   20B1H   ;MODE WORD OF SIO
(20B2)   CWSIO   EQU   20B2H   ;COMMAND WORD OF SIO
(20B3)   STSIO   EQU   20B3H   ;STATUS WORD OF SIO
(20B4)   CWPIO   EQU   20B4H   ;COMMAND WORD OF PIO
(20B5)   BCTPIO  EQU   20B5H   ;BYTE COUNTER OF PIO
(20B6)   BCTSIO  EQU   20B6H   ;BYTE COUNTER OF SIO
         ;
(20C0)   WKAREA  EQU   20C0H   ;WORK AREA
         ;                     SEGBUF ENTRY ADDRESS
(201F)   NADDR   EQU   201FH
(2017)   ZADDR   EQU   2017H
(200F)   YADDR   EQU   200FH
(2007)   XADDR   EQU   2007H
         ;
(20C1)   WORK1   EQU   20C1H
         ;
         ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
         ;               KEY CODE
         ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
(0000)   K0      EQU   00H
(0001)   K1      EQU   01H
(0002)   K4      EQU   02H
(0003)   K7      EQU   03H
(0004)   KPOINT  EQU   04H
(0005)   K2      EQU   05H
(0006)   K5      EQU   06H
(0007)   K8      EQU   07H
(0008)   KPROJ   EQU   08H
(0009)   K3      EQU   09H
(000A)   K6      EQU   0AH
(000B)   K9      EQU   0BH
(000C)   KSETN   EQU   0CH
(000D)   KSETZ   EQU   0DH
(000E)   KSETY   EQU   0EH
(000F)   KSETX   EQU   0FH
(0010)   KENTER  EQU   10H
(0011)   KSTPRN  EQU   11H
(0012)   KSTPDP  EQU   12H
(0013)   KCLXYZ  EQU   13H
(0014)   KTEST   EQU   14H
(0015)   KATPRN  EQU   15H
(0016)   KATPDP  EQU   16H
(0017)   KRESET  EQU   17H
         ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
(2001)   WRK1    EQU   2001H
(2002)   WRK2    EQU   2002H
(2010)   HEX     EQU   2010H
(2020)   KVALUE  EQU   2020H
(2030)   DATA    EQU   2030H
         ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
```

CROMEMCO CDOS Z80 ASSEMBLER version 02.15 PAGE 0003

```
                ;          MAIN    PROGRAM
                ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
                ;
0000°                      ORG     100H                ;0-FF RESERVE
                ;                  INITIALISE
0100  31FF2B    MAIN1      LD      SP,ASTACK
0103  ED5E                 IM2                         ;Z80 INT-MODE-2
0105  CD9901               CALL    INITKB
0108  CDA001               CALL    INITSO
010B  CDBF01               CALL    INITPO
010E  CDD101               CALL    INITCT
0111  CDD301               CALL    INITDP
                ;                  SCAN KEYBOARD
0114  CDE901    MAIN2      CALL    CHECKB
0117  28E7                 JR      Z,MAIN1
0119  CDF701               CALL    KBSCAN
011C  38E2                 JR      C,MAIN1
011E  FE14                         CP      KTEST
0120  280A                         JR      Z,SYSTST
0122  FE11                         CP      KSTPRN
0124  2809                         JR      Z,SETSIO
0126  FE10                         CP      KENTER
0128  2808                         JR      Z,MAIN3
012A  18E8                         JR      MAIN2
012C  C38A01    SYSTST     JP      MAIN12
012F  C39401    SETSIO     JP      MAIN13
0132  CDEA04    MAIN3      CALL    INHBDZ
0135  CD1803               CALL    SETX
0138  CDA903               CALL    SETY
013B  CD3A04               CALL    SETZ
013E  CDE804               CALL    SETN
0141  CDF104               CALL    ENABDZ
0144  CD5102    MAIN4      CALL    RDNZYX
0147  CDAE02    MAIN5      CALL    CONVDI
014A  CD4005    MAIN6      CALL    DISXYZ
                ;                  SCAN KEYBOARD
014D  CDE901    MAIN7      CALL    CHECKB
0150  28FB                 JR      Z,MAIN7
0152  CDF701               CALL    KBSCAN
0155  38F6                 JR      C,MAIN7
0157  FE12                         CP      KSTPDP
0159  280A                         JR      Z,MAINS
015B  FE11                         CP      KSTPRN
015D  280B                         JR      Z,MAIN9
015F  FE17                         CP      KRESET
0161  2390                         JR      Z,MAIN1
0163  18E8                         JR      MAIN7
0165  CD5205    MAINS      CALL    MPIO
0168  18DA                 JR      MAIN4
016A  CDDC02    MAIN9      CALL    CNASCI
016D  CD5A05    MAIN10     CALL    MSIO
0170  18D2                 JR      MAIN4
0172  CDE901    MAIN11     CALL    CHECKB
0175  28FB                 JR      Z,MAIN11
0177  CDF701               CALL    KBSCAN
017A  38F6                 JR      C,MAIN11
017C  FE01                         CP      K1
```

```
017E 280B       0172                    JR      Z,TST1
0180 FE05       0173                    CP      K2
0182 280A       0174                    JR      Z,TST2
0184 FE09       0175                    CP      K3
0186 2809       0176                    JR      Z,TST3
0188 18E6       0177                    JR      MAIN11
018A 00         0178 MAIN12  NOP
018B CD5C05     0179 TST1    CALL    TEST1
                0180                            ;RUN TEST1 UNTIL PRESS RESET SW
                     ITCH
018E CD5E05     0181 TST2    CALL    TEST2
                0182                            ;RUN TEST2 UNTIL PRESS RESET SW
                     ITCH
0191 CD6005     0183 TST3    CALL    TEST3
                0184                            ;RUN TEST3 UNTIL PRESS RESET SW
                     ITCH
0194 CD5805     0185 MAIN13  CALL    PRGSIO
0197 C9         0186         RET
                0187
0198 76         0188         HALT
                0189 ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
                     ;;;;;
                0190 ;       INITIALISATION MODULE
                0191 ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
                     ;;;;
                0192 ;                  SUBROUTINE INITKB
                0193 ; PURPOSE
                0194 ;       WRITE HIGH STATE TO COL1 TO COL6
                0195 ; INPUT
                0196 ;       -
                0197 ; OUTPUT
                0198 ;       -
                0199 ; REGISTERS USED
                0200 ;       A
                0201 ; DESCRIPTION
                0202 ;       -
                0203 ;.....
                     ....
                0204         NAME    INITKB
019B F5         0205 INITKB  PUSH    AF      ;SAVE A
019A 3EFF       0206         LD      A,0FFH
019C D315       0207         OUT     OUTKB,A
019E F1         0208         POP     AF
019F C9         0209         RET
                0210 ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
                     ;;;;;;;
                0211 ;                  SUBROUTINE INITSIO
                0212 ;PURPOSE
                0213 ;       SET MODE WORD TO SIO
                0214 ;       SET COMMAND WORD TO SIO
                0215 ;INPUT
                0216 ;       -
                0217 ;OUTPUT
                0218 ;       -
                0219 ;       MWSIO,CWSIO,STSIO
                0220 ;REGISTERS USED
                0221 ;       AF
```

```
                        0222 ;DESCRIPTION
                        0223 ;       PORT DESCRIPTION (C/D -† A0)
                        0224 ;       INPUT PORT 0E = READ DATA     A0=0
                        0225 ;       INPUT PORT 0F = READ STATUS   A0=1
                        0226 ;       OUTPUT PORT 1E= WRITE DATA    A0=0
                        0227 ;       OUTPUT PORT 1F= WRITE STATUS  A0=1
                        0228 ;
                        0229 ;       INITIALISE SIO:
                        0230 ;               BAUDRATE=16X
                        0231 ;               DATA LEN=8 BITS
                        0232 ;               ENABLE PARITY
                        0233 ;               PARITY  = EVEN
                        0234 ;               STOP BIT=1
                        0235 ;
                        0236 ;               TRANSMIT ENABLE
                        0237 ;               RECEIVE ENABLE
                        0238 ;               ERROR RESET
                        0239 ;
                        0240 ;MODE WORD:
                        0241 ;       D7  D6  D5  D4  D3  D2  D1  D0
                        0242 ;       0   1   1   1   1   1   1   0    = 7E HEX
                        0243 ;       |   |   |   |   |   |   |   |
                        0244 ;       |   |   |   |   |   |   *---*------BAUD RATE FACTOR
                        0245 ;       |   |   |   |   *---*--------------DATA LENGTH
                        0246 ;       |   |   |   *------------------------ENABLE PARITY
                        0247 ;       |   |   *----------------------------EVEN PARITY
                        0248 ;       *---*--------------------------------1 STOP BIT
                        0249 ;COMMAND WORD:
                        0250 ;       D7  D6  D5  D4  D3  D2  D1  D0
                        0251 ;       0   0   0   1   0   1   0   1    = 15 HEX
                        0252 ;       |   |   |   |   |   |   |   *-TRANSMIT ENABLE
                        0253 ;       |   |   |   |   |   |   *-------DTR
                        0254 ;       |   |   |   |   |   *-----------RECEIVE ENABLE
                        0255 ;       |   |   |   |   *---------------BREAK CHARACTER
                        0256 ;       |   |   |   *-------------------ERROR RESET
                        0257 ;       |   |   *-----------------------RTS
                        0258 ;       |   *-------------------------- INTERNAL RESET
                        0259 ;       *-----------------------------HUNT MODE (SYNC)
                        0260 ;
                        0261 ;STATUS WORD:
                        0262 ;       D7  D6  D5  D4  D3  D2  D1  D0
                        0263 ;       |   |   |   |   |   |   |   |
                        0264 ;       |   |   |   |   |   |   |   *-TXRDY
                        0265 ;       |   *---*---*---*---*---*-------SYNDET TXEMPTY RX
                        RDY
                        0266 ;       |       |   |   |   *-----------PARITY ERROR
                        0267 ;       |       |   |   *---------------OVERRUN ERROR
                        0268 ;       |       |   *-------------------FRAMING ERROR(ASY
                        NC)
                        0269 ;       *-----------------------------DATA SET READY
                        0270 ;.....................................................
                             ...
                        0271         NAME    INITSO
01A0  F5                0272 INITSO  PUSH    AF
01A1  3E7E              0273         LD      A,7EH
01A3  32B120            0274         LD      (MMSIO),A
01A6  3E15              0275         LD      A,15H
```

```
01A3  32B220            LD    (CWSIO),A
01A6  3AB120            LD    A,(MWSIO)
01AE  D31F              OUT   WCSIO,A
01B0  E3                      EX     (SP),HL
01B1  E3                      EX     (SP),HL
01B2  3AB220            LD    A,(CWSIO)
01B5  D31F              OUT   WCSIO,A
01B7  E3                      EX     (SP),HL
01B8  E3                      EX     (SP),HL
01B9  AF                XOR   A
01BA  32B320            LD    (STSIO),A
01BD  F1                POP   AF
01BE  C9                RET
                  ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
                  ;;;;;;;;
                  ;                SUBROUTINE INITPO
                  ;PURPOSE
                  ;        SET COMMAND WORD TO PIO:
                  ;                MODE 0 (OUTPUT ONLY) FOR PORT A AND B
                  ;INPUT
                  ;        -
                  ;OUTPUT
                  ;        CWPIO
                  ;REGISTERS USED
                  ;        AF
                  ;DESCRIPTION
                  ;        PORT DESCRIPTION (A0 -↑ B/A ; A1 -↑ C/D)
                  ;        OUTPUT PORT 00  = DATA OUTPUT PORTA
                  ;        OUTPUT PORT 01  = DATA OUTPUT PORTB
                  ;        OUTPUT PORT 02  = COMMAND MODE PORTA
                  ;        OUTPUT PORT 03  = COMMAND MODE PORTB
                  ;
                  ;        CONTROL WORD:
                  ;        D7  D6  D5  D4  D3  D2  D1  D0
                  ;        -   -   X   X   -   -   -   -
                  ;                        *---*---*---* 1111=CONTROL WORD
                  ;        *---*----------------------- MODE 0 1 2 3
                  ;
                  ;                        *---*---*---* 0111=INTERRUPT CT
                  RL WORD
                  ;        *---------------------------     87=ENABLE INTER
                  RUPT
                  ;                                         07=DISABLE INTE
                  RRUPT
                  ;
                  ;        X   X   X   X   X   X   X ' 0  INTERRUPT VECTOR
                  ;.......................................................
                  ........
                        NAME  INITPO
01BF  F5          INITPO PUSH AF
01C0  3E0F              LD    A,0FH
01C2  32B420            LD    (CWPIO),A
01C5  D302              OUT   PIO2,A
01C7  E3                      EX     (SP),HL
01C8  E3                      EX     (SP),HL
01C9  D303              OUT   PIO3,A
01CB  E3                      EX     (SP),HL
```

```
01CC  E3                              EX      (SP),HL
01CD  CD6205                  CALL    DINPIO
01D0  C9                      RET
              ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
              ;;;;;;;;
              ;                         SUBROUTINE INITCT
              ;PURPOSE
              ;               INHIBIT X,Y,Z PLUSE OF WAVESHAPE CIRCUIT
              ;               CLEAR BCD COUNTER (74LS192) TO ZERO
              ;INPUT
              ;OUTPUT
              ;REGISTERS USED
              ;DESCRIPTION
              ;......................................................
              ........
                              NAME    INITCT
01D1  CDEA04  INITCT  CALL    INHBDZ
01D4  CD0A03                  CALL    CLRCNT
01D7  C9                      RET
              ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
              ;;;;;;;;
              ;                         SUBROUTINE      INITDP
              ;PURPOSE
              ;               CLEAR DISPLAY MEMORY
              ;INPUT
              ;OUTPUT
              ;REGISTERS USED
              ;               AF,BC,DE
              ;DESCRIPTION
              ;......................................................
              ........
                              NAME    INITDP
01D8  F5      INITDP  PUSH    AF
01D9  C5                      PUSH    BC
01DA  D5                      PUSH    DE
01DB  AF                      XOR     A
01DC  110080                  LD      DE,8000H
01DF  0620                    LD      B,20H
01E1  12      CLRLOP  LD      (DE),A
01E2  13                      INC     DE
01E3  10FC                    DJNZ    CLRLOP
01E5  D1                      POP     DE
01E6  C1                      POP     BC
01E7  F1                      POP     AF
01E8  C9                      RET
              ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
              ;;
              ;                         SUBROUTINE CHECKB ; KEYIO
              ;PURPOSE
              ;               OUT LOW STATE TO KEYBOARD PORT 15H (COL1-COL6)
              ;               IN FROM KEYBOARD PORT CH (ROW1-ROW4) FOR THE
              ;               PURPOSE OF TESTING FOR THE PRESENCE OF PRESSED
              ;               KEY
              ; LOCATION
              ;               CHECKB
              ; INPUT
              ;               OUTKB = PORT#21 COL6 TO COL1
```

```
                ;          INKB  = PORT#12 ROW1 TO ROW4
                ;          FOR KEYIO 4LEASTSIG. OF A REG = COL# TO BE LOW
                ; OUTPUT
                ;          4 LEAST SIGNIFICANT BITS OF A REGISTER ARE SET
                ;          AS FOLLOWS:
                ;          D7D6D5D4 D3D2D1D0 Z    DESCRIPTION
                ;           0 0 0 0  0 0 0 0 1    NO KEY PRESSED
                ;           0 0 0 0  0 0 0 1 0    A PRESSED KEY IN ROW 1
                ;           0 0 0 0  0 0 1 0 0    A PRESSED KEY IN ROW 2
                ;           0 0 0 0  0 1 0 0 0    A PRESSED KEY IN ROW 3
                ;           0 0 0 0  1 0 0 0 0    A PRESSED KEY IN ROW 4
                ;           Z FLAG = 1  WHEN NO KEY PRESSED
                ; REGISTERS USED
                ;          AF
                ; DESCRIPTION
                ;          CL1 CL2 CL3 CL4    CL5 CL6
                ; D3 †   7   8   9   X  CLRXYZ RESET   §=ROW 4
                ; D2 †   4   5   6   Y  S-PDP  A-PDP   §=ROW 3
                ; D1 †   1   2   3   Z  S-PRN  A-PRN   §=ROW 2
                ; D0 †   0   .   ID  N  ENTER  TEST    §=ROW 1
                ;
                ;        :   :   :   :    :     :
                ;        D0  D1  D2  D3   D4    D5
                ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
                ;;
                ;
01E9  AF        CHECKB  XOR   A          ;CLEAR A
01EA  E3                EX    (SP),HL    ;DELAY 17-MICROSEC
01EB  E3                EX    (SP),HL
01EC  D315      KEYIO   OUT   OUTKB,A          ;LOW COL6 TO COL1

01EE  E3                EX    (SP),HL    ;DELAY 17-MICROSEC
01EF  E3                EX    (SP),HL
01F0  DB0C              IN    A,INKB           ;IN ROW1 TO ROW4 (D0-3)
                ;                            D3D2D1D0
                ;                             1 1 1 1   NO KEY PRESSED
                ;                             1 1 1 0   KEY ROW 1
                ;                             1 1 0 1   KEY ROW 2
                ;                             1 0 1 1   KEY ROW 3
                ;                             0 1 1 1   KEY ROW 4
01F2  E60F              AND   0FH        ;CLEAR MOSTL. 4BITS Z=0
01F4  EE0F              XOR   0FH        ;REVERSE BIT AND SET Z
                ;                          D3D2D1D0  Z
                ;                           0 0 0 0  1 NO KEY PRESSED
                ;                           0 0 0 1  0 KEY ROW 1
                ;                           0 0 1 0  0 KEY ROW 2
                ;                           0 1 0 0  0 KEY ROW 3
                ;                           1 0 0 0  0 KEY ROW 4
01F6  C9                RET
                ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
                ;;;
                ;                  SUBROUTINE KBSCAN
                ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
                ;;;
                ; PURPOSE
                ;         SCAN KEYBOARD FOR PRESSED KEYS, DETECT THE
                ;         EXISTENCE OF SINGLE PRESSED KEY,AND PASS
```

```
0434 ;       BACK ITS IDENTITY TO THE CALLING ROUTINE.
0435 ; LOCATION
0436 ;       KBSCAN
0437 ; INPUT
0438 ;       NONE
0439 ; OUTPUT
0440 ;       CARRY FLAG = 1 WHEN NOKEY OR MOREKEY PRESSED
0441 ;       A & C CONTAINS THE IDENTITY OF KEY AS FOLLOWS:
0442 ;       COL.  1    2    3    4    5    6
0443 ;       ROW ------------------------------
0444 ;        4 : 03   07   0B   0F   13   17
0445 ;        3 : 02   06   0A   0E   12   16
0446 ;        2 : 01   05   09   0D   11   15
0447 ;        1 : 00   04   08   0C   10   14
0448 ;            ------------------------------
0449 ; DESCRIPTION
0450 ;       B INIT=FB USING FOR ROW-COUNTER
0451 ;       C INIT=40 USING FOR COL-SCAN-COUNTER
0452 ;         A = C                  A = C COMPLEMENT
0453 ;       7654 3210   CY      7654 3210
0454 ;       0100 0000                    INITIAL C
0455 ;       0010 0000    0      1101 1111 1-ROTATE L-COL6
0456 ;       0001 0000    0      1110 1111 2-ROTATE L-COL5
0457 ;       0000 1000    0      1111 0111 3-ROTATE L-COL4
0458 ;       0000 0100    0      1111 1011 4-ROTATE L-COL3
0459 ;       0000 0010    0      1111 1101 5-ROTATE L-COL2
0460 ;       0000 0001    0      1111 1110 6-ROTATE L-COL1
0461 ;       0000 0000    1                END ROTATE
0462 ;
0463 ;       A IS SET BY SHIFT-RIGHT-LONG C
0464 ;         AND CALL KEYIO THEN
0465 ;               A=4BIT LEASTSIG. SHOWS KEY ROW#
0466 ;               Z FLAG =1 NO KEY ; =0 KEY PRESSED
0467 ;       ROTATE RIGHT THRU CY OF A REG AND INCREMENT
0468 ;       B REG. UNTIL CY = 1 DO NEXT
0469 ;            A D3D2D1D0   B + #  = ##
0470 ;              0 0 0 1   FB + 1  = FC
0471 ;              0 0 1 0   FC + 1  = FD
0472 ;              0 1 0 0   FD + 1  = FE
0473 ;              1 0 0 0   FE + 1  = FF
0474 ;
0475 ;       A = A.AND.0F TO MAKE SURE NO MULTIKEY
0476 ;       LOAD A BY C WHICH IS SPECIFIC LOW-COL-#
0477 ;       THEN CALL KEYIO TO MAKE SURE KEY-PRESSED
0478 ;       EXISTENCE AND KEY DEBOUNCING EFFECT.
0479 ;
0480 ;       LOAD A BY B  AND SHIFT C TO GET KEY IDENTITY
0481 ;       BY ADD A WITH 4 BEFORE ROTATE C UNTIL CY=1
0482 ;       POSSIBLE C / POSSIBLE A+4 VALUE
0483 ;       0000 0001   00 01 02 03
0484 ;                                FC+4 = 00
0485 ;                                FD+4 = 01
0486 ;                                FE+4 = 02
0487 ;                                FF+4 = 03
0488 ;       0000 0010   04 05 06 07
0489 ;       0000 0100   08 09 0A 0B
0490 ;       0000 1000   0C 0D 0E 0F
```

```
                   ;           0001 0000   10 11 12 13
                   ;           0010 0000   14 15 16 17
                   ;
                   ;           INITILIZE KEYBOARD (HIGH STATE COLS) & RETURN
                   ;
                   ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
                   ;
                               NAME    KBSCAN
01F7  0140FB       KBSCAN      LD      BC,0FB40H     ;B=FB  C=40[01000000]
01FA  CB39         CLKBS       SRL     C             ;0-↑C[7...0]-↑CY
01FC  D8                       RET     C             ;CY=1 SCAN ALL
                                                     ;FOUND NO KEY PRESSED
01FD  79                       LD      A,C           ;A=C
01FE  2F                       CPL                   ;COMPLEMENT A
01FF  CDEC01                   CALL    KEYIO         ;OUT&IN KEYBOARD
0202  28F6                     JR      Z,CLKBS       ;Z=1 FROM KEYIO MEANS
                                                     ;NO KEY THEN NEXT SCAN
                                                     ;       ELSE DO NEXT
0204  04           STPKB       INC     B             ;B=B+1
0205  1F                       RRA                   ;A[7...0]-↑CY -↑A[...]
0206  30FC                     JR      NC,STPKB      ;CY=0 REPEAT ELSE NEXT
0208  E60F                     AND     0FH           ;IF A.0F ↑ 0 THEN FOUND
020A  2019                     JR      NZ,CCF        ;    MULTIKEY,EXIT ERR.
                                                     ;            ELSE NEXT
020C  79                       LD      A,C           ;LOAD A L-COL PATTERN
020D  2F                       CPL                   ;COMPLEMENT FOR KEYIO
020E  CDEC01                   CALL    KEYIO         ;OUT&IN KEYBOARD
0211  E3                       EX      (SP),HL       ;DELAY 30-MICROSEC
0212  E3                       EX      (SP),HL
0213  E3                       EX      (SP),HL
0214  E3                       EX      (SP),HL
0215  DB0C                     IN      A,INKB        ;IN A(D0-3 =K1-4)
0217  E60F                     AND     0FH           ;THIS IN IS FOR SURE
0219  EE0F                     XOR     0FH           ;(REPEAT KEYIO INST)
021B  2808                     JR      Z,CCF         ;EXIT WHEN NO KEY
021D  78                       LD      A,B           ;A=B ROW COUNTER(STPKB)
021E  C604         LPKB1       ADD     A,04H         ;FIND OUT KEY IDENTITY
0220  CB39                     SRL     C             ;0-↑C[7...0]-↑CY
0222  30FA                     JR      NC,LPKB1      ;CY=1 DO NEXT
0224  4F                       LD      C,A           ;C=A
0225  3F           CCF         CCF                   ;CLEAR CARRY FLAG(CY=0)
0226  CD9901                   CALL    INITKB        ;HIGH ALL COLUMN
0229  C9                       RET
                   ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
                   ;;
                   ;            SUBROUTINE WAIT # SECONDS
                   ;PURPOSE
                   ;            TO DELAY SOME SECONDS
                   ;INPUT
                   ;              -
                   ;OUTPUT
                   ;              -
                   ;REGISTERS USED
                   ;            AF,HL,DE
                   ;DESCRIPTION
                   ;...............................................
                   ....
```

```
                   ;
022A  F5           WAIT5:   PUSH   AF
022B  E5                    PUSH   HL
022C  D5                    PUSH   DE
022D  210500                LD     HL,0005H
0230  180E                  JR     WAIT
0232  F5           WAIT3:   PUSH   AF
0233  E5                    PUSH   HL
0234  D5                    PUSH   DE
0235  210300                LD     HL,0003H
0238  1806                  JR     WAIT
023A  F5           WAIT1:   PUSH   AF
023B  E5                    PUSH   HL
023C  D5                    PUSH   DE
023D  210100                LD     HL,0001H
0240  11FFFF       WAIT:    LD     DE,0FFFFH
0243  1B           LPWAIT:  DEC    DE
0244  7A                    LD     A,D
0245  B3                    OR     E
0246  20FB                  JR     NZ,LPWAIT
0248  2B                    DEC    HL
0249  7D                    LD     A,L
024A  B4                    OR     H
024B  20F3                  JR     NZ,WAIT
024D  D1                    POP    DE
024E  E1                    POP    HL
024F  F1                    POP    AF
0250  C9                    RET
                   ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
                   ;;;;;;;;
                   ;                       SUBROUTINE RDNZYX
                   ;PURPOSE
                   ;INPUT
                   ;OUTPUT
                   ;REGISTERS USED
                   ;DESCRIPTION
                   ;.........................................
0251  3E07         RDNZYX   LD     A,07H
0253  D304                  OUT    WSCNT,A
0255  E3                           EX     (SP),HL
0256  E3                           EX     (SP),HL
0257  3EE7                  LD     A,0E7H
0259  D304                  OUT    WSCNT,A
025B  E3                           EX     (SP),HL
025C  E3                           EX     (SP),HL
025D  010400       READN    LD     BC,04H
0260  110021                LD     DE,BCDBUF
0263  21E020                LD     HL,NBCDBF
0266  EDB0                  LDIR
0268  110421                LD     DE,BCDBUF+4
026B  DB08                  IN     A,INZ0
026D  CDA302                CALL   WRT
0270  DB09                  IN     A,INZ1
0272  CDA302                CALL   WRT
0275  DB0A                  IN     A,INZ2
0277  CDA802                CALL   WRT
027A  DB0B                  IN     A,INZ3
```

```
027C  CDA802            CALL   WRT
027F  DB04              IN     A,INY0
0281  CDA802            CALL   WRT
0284  DB05              IN     A,INY1
0286  CDA802            CALL   WRT
0289  DB06              IN     A,INY2
028B  CDA802            CALL   WRT
028E  DB07              IN     A,INY3
0290  CDA802            CALL   WRT
0293  DB00              IN     A,INX0
0295  CDA802            CALL   WRT
0298  DB01              IN     A,INX1
029A  CDA802            CALL   WRT
029D  DB02              IN     A,INX2
029F  CDA802            CALL   WRT
02A2  DB03              IN     A,INX3
02A4  CDA802            CALL   WRT
02A7  C9                RET
02A8  E3         WRT    EX     (SP),HL
02A9  E3                EX     (SP),HL
02AA  12                LD     (DE),A
02AB  AF                XOR    A
02AC  13                INC    DE
02AD  C9                RET
                 ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
                 ;      SUBROUTINE CONVDI
                 ; PURPOSE
                 ;      CONVERT BCD VALUE OF N,Z,Y,X IN BCD-BUFFER
                 ;      TO 7-SEGMENT CODE AND WRITE INTO SEG-BUFFER
                 ; LOCATION IN MEMORY
                 ;      CONVDI
                 ; INPUT DATA
                 ;      BCDBUF  ADDR 16 BYTES (NZYX)
                 ;      SEGBUF  ADDR 32 BYTES (XYZN)
                 ;      B27TBL ADDRESS OF BCD-TO-7SEG TABLE
                 ;      BNXOUT = WORD CONTAINS START ENTRY IN BCDBUF
                 ;               FROM WHICH BCDVALUE IS READ TO
                 ;               CONVERT (7-SEG) AND WRITE TO SEGBUF
                 ; OUTPUT DATA
                 ;      COVERTED X Y Z AND N IN SEGBUF WHICH IS
                 ;      READY TO BE DISPLAY
                 ; REGISTER USED
                 ;      HL,DE,AF,B
                 ; DESCRIPTION
                 ;      1.B=BYTE COUNTER
                 ;      2.DE= ADDR OF SEGBUF
                 ;      3.HL= ADDR OF BCDVALUE
                 ;      4.LOAD 1 BYTE OF BCD TO A BY RIGHT-ROTATE
                 ;        UNTIL END OF BUFFER
                 ;      5.CONVERT RIGHTMOST BYTE IN A TO 7-SEG CODE
                 ;        AND THEN WRITE TO   SEGBUF
                 ;      6.DO STEP4 AND STEP5 UNTIL END OF DATA
                 ;      7.RETURN
                 ;
                 ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;          ;;;;;;;;;;;;;;;;
                        NAME   CONVDI
02AE  AF         CONVDI: XOR   A                               EG.
```

```
02AF  11FF1F      0658          LD      DE,SEGBUF-1     ;DE--SEGBUF-1
                  0659 ;
02B2  0610        0660 LOOPXX:  LD      B,10H           ;SET BYTE COUNT=16 WD
02B4  13          0661          INC     DE              ;INCREMENT SEGBUF
02B5  2AA120      0662          LD      HL,(BNXOUT)     ;HL--ENTRY.ADDR
                                                        OF BCDBUF
                  0663 ;
02B8  86          0664          ADD     A,(HL)          ;A--1ST BCDVALUE
02B9  77          0665          LD      (HL),A          ;FILL LAST VALUE
02BA  7B          0666          LD      A,E             ;A--LAST SEGBUF ADDR
02BB  FE20        0667          CP      020H            ;LAST ADDR=201F+1
02BD  2817        0668          JR      Z,FINISH        ;END GOTO FINISH
                                                        ELSE BEGIN CONVERT
                  0669 ;
02BF  AF          0670          XOR     A               ;CLEAR A
02C0  ED6F        0671 LOOPX:   RLD
02C2  23          0672          INC     HL              ;ROTATE AND INC HL
02C3  10FB        0673          DJNZ    LOOPX           ;ROTATE 16 TIMES
                  0674 ;
                  0675 ;                                TEST OUT OF RANGE (tF)
                  0676 ;
02C5  F5          0677                  PUSH    AF      ;SAVE A
02C6  E670        0678                  AND     70H     ; A.AND.70H
                  0679                                  ; t0 OVERFLOW GOTO
                  0680                                  ;    BCDOVF
                  0681                                  ; ELSE DO NEXT
02C8  200D        0682                  JR      NZ,BCDOVF
02CA  F1          0683                  POP     AF      ;RESTORE A
                  0684 ;
02CB  F5          0685          PUSH    AF              ;SAVE A
02CC  216405      0686          LD      HL,B27TBL       ;HL= ADDR OF TABLE
02CF  85          0687          ADD     A,L             ;CAL ENTRY NO.
02D0  6F          0688          LD      L,A             ;SET ENTRY NO.
02D1  7E          0689          LD      A,(HL)          ;GET ENTRY INTO A
02D2  12          0690          LD      (DE),A          ;WRITE SEGBUF
02D3  F1          0691          POP     AF              ;RESTORE A
02D4  18DC        0692          JR      LOOPXX          ;LOOP UNTIL END
                                                        OF BCDBUF
                  0693 ;
02D6  C9          0694 FINISH   RET
                  0695 ;
02D7  AF          0696 BCDOVF           XOR     A       ;CLEAR A
02D8  12          0697                  LD      (DE),A  ;SET BLANK CODE
02D9  F1          0698                  POP     AF      ;RESTORE A
02DA  18D6        0699                  JR      LOOPXX
                  0700 ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
                       ;;;;;;;;
                  0701 ;                SUBROUTINE CNASCI
                  0702 :
                  0703 ;PURPOSE
                  0704 ;        CONVERT BCD VALUE IN BCDBUF TO ASCII IN ASCBUF
                  0705 ;INPUT
                  0706 ;OUTPUT
                  0707 ;REGISTERS USED
                  0708 ;DESCRIPTION
                  0709 ;.....................................................
                       ........
                  0710          NAME    CNASCI
02DC  AF          0711 CNASCI   XOR     A
02DD  11FF1F      0712          LD      DE,SEGBUF-1
```

```
02E0  0610         LOOPYY  LD      B,10H
02E2  13                   INC     DE
02E3  2AA120               LD      HL,(BNXOUT)
02E6  86                   ADD     A,(HL)
02E7  77                   LD      (HL),A
02E8  7B                   LD      A,E
02E9  FE40                 CP      040H
02EB  2817                 JR      Z,FIN
02ED  AF                   XOR     A
02EE  ED6F         LOOPY   RLD
02F0  23                   INC     HL
02F1  10FB                 DJNZ    LOOPY
02F3  F5                           PUSH    AF
02F4  E670                         AND     70H
02F6  200D                         JR      NZ,ASCOVF
02F8  F1                           POP     AF
02F9  F5                   PUSH    AF
02FA  216E05               LD      HL,B2ASCI
02FD  85                   ADD     A,L
02FE  6F                   LD      L,A
02FF  7E                   LD      A,(HL)
0300  12                   LD      (DE),A
0301  F1                   POP     AF
0302  18DC                 JR      LOOPYY
0304  C9           FIN     RET
0305  AF           ASCOVF  XOR     A
0306  12                   LD      (DE),A
0307  F1                   POP     AF
0308  18D6                 JR      LOOPYY
                   ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
                   ;;;;;;;;
                   ;                       SUBROUTINE CLRCNT
                   ;
                   ;PURPOSE
                   ;               CLEAR ALL DIGITS OF XYZ
                   ;INPUT
                   ;OUTPUT
                   ;REGISTERS USED
                   ;DESCRIPTION
                   ;...........................................................
                   ........
                           NAME    CLRCNT
030A  AF           CLRCNT  XOR     A
030B  D306                 OUT     CLRX,A
030D  E3                           EX      (SP),HL
030E  E3                           EX      (SP),HL
030F  D307                 OUT     CLRY,A
0311  E3                           EX      (SP),HL
0312  E3                           EX      (SP),HL
0313  D308                 OUT     CLRZ,A
0315  E3                           EX      (SP),HL
0316  E3                           EX      (SP),HL
0317  C9                   RET
                   ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
                   ;;;;;;;;
                   ;                       SUBROUTINE SETX
                   ;
```

```
                        0767 ;PURPOSE
                        0768 ;INPUT
                        0769 ;OUTPUT
                        0770 ;REGISTERS USED
                        0771 ;DESCRIPTION
                        0772 ;       LATCH LINE
                        0773 ;       D7  D6  D5  D4  D3  D2  D1  D0
                        0774 ;
                        0775 ;       IN  IN  IN  XX  XX  MR  MR  MR
                        0776 ;        Z   Y   X           Z   Y   X
                        0777 ;
                        0778 ;       DIGIT BIT PATTERN
                        0779 ;       D7  D6  D5  D4  D3  D2  D1  D0
                        0780 ;
                        0781 ;       -   -   -   -   *---*---*---*--DG 1 3 5 7
                        0782 ;       *   *   *   *                  DG 2 4 6 8
                        0783 ;        \___\___\___\________________
                        0784 ;       DIGIT LAYOUT
                        0785 ;       DG  DG  DG  DG  DG  DG  DG  DG
                        0786 ;        8   7   6   5   4   3   2   1
                        0787 ;
                        0788 ;.....................................................
                             ........
                        0789         NAME    SETX
0318  CDCB04             0790 SETX    CALL    CWORK1
031B  3EE6               0791 LATCHX  LD      A,0E6H
031D  D304               0792         OUT     WSCNT,A
031F  E3                 0793                 EX      (SP),HL
0320  E3                 0794                 EX      (SP),HL
0321  CDD004             0795         CALL    KEY
0324  FE10               0796         CP      KENTER
0326  2654               0797         JR      Z,EXITX
0328  CD7D03             0798         CALL    XDG12
032B  CDD004             0799         CALL    KEY
032E  FE10               0800         CP      KENTER
0330  284A               0801         JR      Z,EXITX
0332  CD7D03             0802         CALL    XDG12
0335  CDCB04             0803                 CALL    CWORK1
0338  CDD0C4             0804                 CALL    KEY
033B  FE10               0805                 CP      KENTER
033D  283D               0806                 JR      Z,EXITX
033F  CD8803             0807                 CALL    XDG34
0342  CDD004             0808                 CALL    KEY
0345  FE10               0809                 CP      KENTER
0347  2833               0810                 JR      Z,EXITX
0349  CD8803             0811                 CALL    XDG34
034C  CDCB04             0812         CALL    CWORK1
034F  CDD004             0813         CALL    KEY
0352  FE10               0814         CP      KENTER
0354  2826               0815         JR      Z,EXITX
0356  CD9303             0816         CALL    XDG56
0359  CDD004             0817         CALL    KEY
035C  FE10               0818         CP      KENTER
035E  281C               0819         JR      Z,EXITX
0360  CD9303             0820         CALL    XDG56
0363  CDCB04             0821                 CALL    CWORK1
0366  CDD004             0822                 CALL    KEY
```

```
0369  FE10     0823                CP      KENTER
036B  280F     0824                JR      Z,EXITX
036D  CD9E03   0825                CALL    XDG78
0370  CDD004   0826                CALL    KEY
0373  FE10     0827                CP      KENTER
0375  2805     0828                JR      Z,EXITX
0377  CD9E03   0829                CALL    XDG78
037A  189C     0830         JR     SETX
037C  C9       0831 EXITX   RET
037D  3AC120   0832 XDG12   LD     A,(WORK1)
0380  D309     0833         OUT    SETX0,A
0382  E3       0834                EX      (SP),HL
0383  E3       0835                EX      (SP),HL
0384  CDF804   0836                CALL    DISX
0387  C9       0837         RET
0388  3AC120   0838 XDG34   LD     A,(WORK1)
038B  D30A     0839         OUT    SETX1,A
038D  E3       0840                EX      (SP),HL
038E  E3       0841                EX      (SP),HL
038F  CDF804   0842                CALL    DISX
0392  C9       0843         RET
0393  3AC120   0844 XDG56   LD     A,(WORK1)
0396  D30B     0845         OUT    SETX2,A
0398  E3       0846                EX      (SP),HL
0399  E3       0847                EX      (SP),HL
039A  CDF804   0848                CALL    DISX
039D  C9       0849         RET
039E  3AC120   0850 XDG78   LD     A,(WORK1)
03A1  D30C     0851         OUT    SETX3,A
03A3  E3       0852                EX      (SP),HL
03A4  E3       0853                EX      (SP),HL
03A5  CDF804   0854                CALL    DISX
03A8  C9       0855         RET
               0856 ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
                    ;;;;;;;;
               0857 ;              SUBROUTINE         SETY
               0858 ;PURPOSE
               0859 ;INPUT
               0860 ;OUTPUT
               0861 ;REGISTERS USED
               0862 ;DESCRIPTION
               0863 ;.........................................................
                    ........
               0864         NAME   SETY
03A9  CDCB04   0865 SETY    CALL   CWORK1
03AC  3EE5     0866 LATCHY  LD     A,0E5H
03AE  D304     0867         OUT    WSCNT,A
03B0  E3       0868                EX      (SP),HL
03B1  E3       0869                EX      (SP),HL
03B2  CDD004   0870         CALL   KEY
03B5  FE10     0871         CP     KENTER
03B7  2854     0872         JR     Z,EXITY
03B9  CD0E04   0873         CALL   YDG12
03BC  CDD004   0874         CALL   KEY
03BF  FE10     0875         CP     KENTER
03C1  284A     0876         JR     Z,EXITY
03C3  CD0E04   0877         CALL   YDG12
```

```
03C6  CDCB04              CALL  CWORK1
03C9  CDD004                    CALL    KEY
03CC  FE10                      CP      KENTER
03CE  283D                      JR      Z,EXITY
03D0  CD1904                    CALL    YDG34
03D3  CDD004                    CALL    KEY
03D6  FE10                      CP      KENTER
03D8  2833                      JR      Z,EXITY
03DA  CD1904                    CALL    YDG34
03DD  CDCB04              CALL  CWORK1
03E0  CDD004              CALL  KEY
03E3  FE10                CP    KENTER
03E5  2826                JR    Z,EXITY
03E7  CD2404              CALL  YDG56
03EA  CDD004              CALL  KEY
03ED  FE10                CP    KENTER
03EF  281C                JR    Z,EXITY
03F1  CD2404              CALL  YDG56
03F4  CDCB04                    CALL    CWORK1
03F7  CDD004                    CALL    KEY
03FA  FE10                      CP      KENTER
03FC  280F                      JR      Z,EXITY
03FE  CD2F04                    CALL    YDG78
0401  CDD004                    CALL    KEY
0404  FE10                      CP      KENTER
0406  2805                      JR      Z,EXITY
0408  CD2F04                    CALL    YDG78
040B  189C                JR    SETY
040D  C9          EXITY   RET
040E  3AC120      YDG12   LD    A,(WORK1)
0411  D30D                OUT   SETY0,A
0413  E3                        EX      (SP),HL
0414  E3                        EX      (SP),HL
0415  CD0A05                    CALL    DISY
0418  C9                  RET
0419  3AC120      YDG34   LD    A,(WORK1)
041C  D30E                OUT   SETY1,A
041E  E3                        EX      (SP),HL
041F  E3                        EX      (SP),HL
0420  CD0A05                    CALL    DISY
0423  C9                  RET
0424  3AC120      YDG56   LD    A,(WORK1)
0427  D30F                OUT   SETY2,A
0429  E3                        EX      (SP),HL
042A  E3                        EX      (SP),HL
042B  CD0A05                    CALL    DISY
042E  C9                  RET
042F  3AC120      YDG78   LD    A,(WORK1)
0432  D310                OUT   SETY3,A
0434  E3                        EX      (SP),HL
0435  E3                        EX      (SP),HL
0436  CD0A05                    CALL    DISY
0439  C9                  RET
                  ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
                  ;;;;;;;;
                  ;               SUBROUTINE      SETZ
                  ;
```

```
                    0934 ;PURPOSE
                    0935 ;INPUT
                    0936 ;OUTPUT
                    0937 ;REGISTERS USED
                    0938 ;DESCRIPTION
                    0939 ;.....................................................
                         ........
                    0940          NAME    SETZ
043A  CDCB04        0941 SETZ     CALL    CWORK1
043D  3EE3          0942 LATCH2   LD      A,0E3H
043F  D304          0943          OUT     WSCNT,A
0441  E3            0944                  EX      (SP),HL
0442  E3            0945                  EX      (SP),HL
0443  CDD004        0946          CALL    KEY
0446  FE10          0947          CP      KENTER
0448  2854          0948          JR      Z,EXITZ
044A  CD9F04        0949          CALL    ZDG12
044D  CDD004        0950          CALL    KEY
0450  FE10          0951          CP      KENTER
0452  284A          0952          JR      Z,EXITZ
0454  CD9F04        0953          CALL    ZDG12
0457  CDCB04        0954                  CALL    CWORK1
045A  CDD004        0955                  CALL    KEY
045D  FE10          0956                  CP      KENTER
045F  283D          0957                  JR      Z,EXITZ
0461  CDAA04        0958                  CALL    ZDG34
0464  CDD004        0959                  CALL    KEY
0467  FE10          0960                  CP      KENTER
0469  2833          0961                  JR      Z,EXITZ
046B  CDAA04        0962                  CALL    ZDG34
046E  CDCB04        0963          CALL    CWORK1
0471  CDD004        0964          CALL    KEY
0474  FE10          0965          CP      KENTER
0476  2826          0966          JR      Z,EXITZ
0478  CDB504        0967          CALL    ZDG56
047B  CDD004        0968          CALL    KEY
047E  FE10          0969          CP      KENTER
0480  281C          0970          JR      Z,EXITZ
0482  CDB504        0971          CALL    ZDG56
0485  CDCB04        0972                  CALL    CWORK1
0488  CDD004        0973                  CALL    KEY
048B  FE10          0974                  CP      KENTER
048D  280F          0975                  JR      Z,EXITZ
048F  CDC004        0976                  CALL    ZDG78
0492  CDD004        0977                  CALL    KEY
0495  FE10          0978                  CP      KENTER
0497  2805          0979                  JR      Z,EXITZ
0499  CDC004        0980                  CALL    ZDG78
049C  189C          0981          JR      SETZ
049E  C9            0982 EXITZ    RET
049F  3AC120        0983 ZDG12    LD      A,(WORK1)
04A2  D311          0984          OUT     SETZ0,A
04A4  E3            0985                  EX      (SP),HL
04A5  E3            0986                  EX      (SP),HL
04A6  CD1C05        0987                  CALL    DISZ
04A9  C9            0988          RET
04AA  3AC120        0989 ZDG34    LD      A,(WORK1)
```

```
04AA  3AC120       ZDG34   LD      A,(WORK1)
04AD  D312                 OUT     SETZ1,A
04AF  E3                           EX      (SP),HL
04B0  E3                           EX      (SP),HL
04B1  CDCF05                       CALL    DISZ
04B4  C9                   RET
04B5  3AC120       ZDG56   LD      A,(WORK1)
04B8  D313                 OUT     SETZ2,A
04BA  E3                           EX      (SP),HL
04BB  E3                           EX      (SP),HL
04BC  CDCF05                       CALL    DISZ
04BF  C9                   RET
04C0  3AC120       ZDG78   LD      A,(WORK1)
04C3  D314                 OUT     SETZ3,A
04C5  E3                           EX      (SP),HL
04C6  E3                           EX      (SP),HL
04C7  CDCF05                       CALL    DISZ
04CA  C9                   RET

04CB  AF           CWORK1  XOR     A
04CC  32C120               LD      (WORK1),A
04CF  C9                   RET
04D0  CDE901       KEY     CALL    CHECKB
04D3  28FB                 JR      Z,KEY
04D5  CDF701               CALL    KBSCAN
04D8  38F6                 JR      C,KEY
04DA  F5                   PUSH    AF
04DB  210D07               LD      HL,K2BCD
04DE  85                   ADD     A,L
04DF  6F                   LD      L,A
04E0  7E                   LD      A,(HL)
04E1  21C120               LD      HL,WORK1
04E4  ED6F                 RLD
04E6  F1                   POP     AF
04E7  C9                   RET
                   ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
                   ;;;;;;;;
                   ;                       SUBROUTINE SETN
                   ;PURPOSE
                   ;INPUT
                   ;OUTPUT
                   ;REGISTERS USED
                   ;DESCRIPTION
                   ;.............................................................
                   ........
                           NAME    SETN
04E8  CDCB04       SETN    CALL    CWORK1
04EB  CDD004               CALL    KEY
04EE  FE10                 CP      KENTER
04F0  284A                 JR      Z,EXITN
04F2  3AC120               LD      A,(WORK1)
04F5  32E020               LD      (NBCDBF),A
04F8  CD9105               CALL    RDN
04FB  CDE105               CALL    DISN
04FE  CDD004               CALL    KEY
0501  FE10                 CP      KENTER
0503  2837                 JR      Z,EXITN
```

```
0505  3AC120      1045          LD      A,(WORK1)
0508  32E020      1046          LD      (NBCDBF),A
050B  CD9105      1047          CALL    RDN
050E  CDE105      1048          CALL    DISN
0511  CDCB04      1049                  CALL    CWORK1
0514  CDD004      1050                  CALL    KEY
0517  FE10        1051                  CP      KENTER
0519  2821        1052                  JR      Z,EXITN
051B  3AC120      1053                  LD      A,(WORK1)
051E  32E120      1054                  LD      (NBCDBF+1),A
0521  CD9105      1055                  CALL    RDN
0524  CDE105      1056                  CALL    DISN
0527  CDD004      1057                  CALL    KEY
052A  FE10        1058                  CP      KENTER
052C  280E        1059                  JR      Z,EXITN
052E  3AC120      1060                  LD      A,(WORK1)
0531  32E120      1061                  LD      (NBCDBF+1),A
0534  CD9105      1062                  CALL    RDN
0537  CDE105      1063                  CALL    DISN
053A  1801        1064                  JR      CONTIN
053C  C9          1065 EXITN            RET
053D  00          1066 CONTIN           NOP
053E  CDCB04      1067          CALL    CWORK1
0541  CDD004      1068          CALL    KEY
0544  FE10        1069          CP      KENTER
0546  28F4        1070          JR      Z,EXITN
0548  3AC120      1071          LD      A,(WORK1)
054B  32E220      1072          LD      (NBCDBF+2),A
054E  CD9105      1073          CALL    RDN
0551  CDE105      1074          CALL    DISN
                  1075
0554  CDD004      1076          CALL    KEY
0557  FE10        1077          CP      KENTER
0559  28E1        1078          JR      Z,EXITN
055B  3AC120      1079          LD      A,(WORK1)
055E  32E220      1080          LD      (NBCDBF+2),A
0561  CD9105      1081          CALL    RDN
0564  CDE105      1082          CALL    DISN
                  1083
0567  CDCB04      1084                  CALL    CWORK1
056A  CDD004      1085                  CALL    KEY
056D  FE10        1086                  CP      KENTER
056F  28CB        1087                  JR      Z,EXITN
0571  3AC120      1088                  LD      A,(WORK1)
0574  32E320      1089                  LD      (NBCDBF+3),A
0577  CD9105      1090                  CALL    RDN
057A  CDE105      1091                  CALL    DISN
057D  CDD004      1092                  CALL    KEY
0580  FE10        1093                  CP      KENTER
0582  28B5        1094                  JR      Z,EXITN
0584  3AC120      1095                  LD      A,(WORK1)
0587  32E320      1096                  LD      (NBCDBF+3),A
058A  CD9105      1097                  CALL    RDN
058D  CDE105      1098                  CALL    DISN
0590  C9          1099          RET
0591  010400      1100 RDN      LD      BC,04H
0594  110021      1101          LD      DE,BCDBUF
```

```
0597  21E020              LD      HL,NBCDBF
059A  EDB0                LDIR
059C  C9                  RET
                ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
                ;;;;;;;;
                ;                       SUBROUTINE INHBDZ
                ;PURPOSE
                ;INPUT
                ;OUTPUT
                ;REGISTERS USED
                ;DESCRIPTION
                ;............................................................
                ........
                          NAME    INHBDZ
059D  3EE0      INHBDZ    LD      A,0E0H
059F  D304                OUT     WSCNT,A
05A1  E3                          EX      (SP),HL
05A2  E3                          EX      (SP),HL
05A3  C9                  RET
                ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
                ;;;;;;;;
                ;                       SUBROUTINE ENABDZ
                ;PURPOSE
                ;INPUT
                ;OUTPUT
                ;REGISTERS USED
                ;DESCRIPTION
                ;............................................................
                ........
                          NAME    ENABDZ
05A4  3EE7      ENABDZ    LD      A,0E7H
05A6  D304                OUT     WSCNT,A
05A8  E3                          EX      (SP),HL
05A9  E3                          EX      (SP),HL
05AA  C9                  RET
                ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
                ;         SUBROUTINE DISX,DISY,DISZ,DISN,DISXYZ
                ; PURPOSE
                ;         DISPLAY VALUE TO 7-SEG LED DISPLAY
                ; LOCATION
                ;         DISX,DISY,DISZ,DISN,DISXYZ
                ; INPUT
                ;         -
                ; OUTPUT
                ;         -
                ; REGISTERS USED
                ;         BC,DE,HL
                ; DESCRIPTION
                ;         -
                ;.........................................................
                          NAME    DISX
05AB  C5        DISX      PUSH    BC
05AC  D5                  PUSH    DE
05AD  E5                  PUSH    HL
05AE  010800              LD      BC,08H
05B1  110080              LD      DE,DISMEM
05B4  210020              LD      HL,SEGBUF
```

```
05B7  EDB0                 LDIR
05B9  E1                   POP     HL
05BA  D1                   POP     DE
05BB  C1                   POP     BC
05BC  C9                   RET
             ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
                           NAME    DISY
05BD  C5           DISY    PUSH    BC
05BE  D5                   PUSH    DE
05BF  E5                   PUSH    HL
05C0  010800               LD      BC,08H
05C3  110880               LD      DE,DISMEM+8
05C6  210820               LD      HL,SEGBUF+8
05C9  EDB0                 LDIR
05CB  E1                   POP     HL
05CC  D1                   POP     DE
05CD  C1                   POP     BC
05CE  C9                   RET
             ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
                           NAME    DISZ
05CF  C5           DISZ    PUSH    BC
05D0  D5                   PUSH    DE
05D1  E5                   PUSH    HL
05D2  010800               LD      BC,08H
05D5  111080               LD      DE,DISMEM+10H
05D8  211020               LD      HL,SEGBUF+10H
05DB  EDB0                 LDIR
05DD  E1                   POP     HL
05DE  D1                   POP     DE
05DF  C1                   POP     BC
05E0  C9                   RET
             ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
             ;             NAME    DISN
05E1  C5           DISN    PUSH    BC
05E2  D5                   PUSH    DE
05E3  E5                   PUSH    HL
05E4  010800               LD      BC,08H
05E7  111880               LD      DE,DISMEM+18H
05EA  211820               LD      HL,SEGBUF+18H
05ED  EDB0                 LDIR
05EF  E1                   POP     HL
05F0  D1                   POP     DE
05F1  C1                   POP     BC
05F2  C9                   RET
             ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
                           NAME    DISXYZ
05F3  C5           DISXYZ  PUSH    BC
05F4  D5                   PUSH    DE
05F5  E5                   PUSH    HL
05F6  012000               LD      BC,20H
05F9  110080               LD      DE,DISMEM
05FC  210020               LD      HL,SEGBUF
05FF  EDB0                 LDIR
0601  E1                   POP     HL
0602  D1                   POP     DE
```

```
0603  C1                    POP    BC
0604  C9                    RET
            ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
            ;;;;;;;;
            ;                      SUBROUTINE MPIO
            ;PURPOSE
            ;INPUT
            ;OUTPUT
            ;REGISTERS USED
            ;DESCRIPTION
            ;.....................................................
            ........
                            NAME   MPIO
0605  3A0021        MPIO    LD     A,(BCDBUF)
0608  D300                  OUT    PIO0,A
060A  E3                           EX      (SP),HL
060B  E3                           EX      (SP),HL
060C  3A0121                LD     A,(BCDBUF+1)
060F  D301                  OUT    PIO1,A
0611  E3                           EX      (SP),HL
0612  E3                           EX      (SP),HL
0613  3E02                  LD     A,2H
0615  32B520                LD     (BCTPIO),A

0618  3EF0                  LD     A,0F0H
061A  D303                  OUT    PIO3,A
061C  E3                           EX      (SP),HL
061D  E3                           EX      (SP),HL
061E  CD4C06                CALL   EINPIO
0621  C9                    RET
            ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
            ;;;;;;;;
            ;                      SUBROUTINE INIPIO
            ;PURPOSE
            ;INPUT
            ;OUTPUT
            ;REGISTERS USED
            ;DESCRIPTION
            ;.....................................................
            ........
                            NAME   INTPIO
0622  3AB520        INTPIO  LD     A,(BCTPIO)
0625  FE20                  CP     20H
0627  281F                  JR     Z,PIOEXT
0629  010021                LD     BC,BCDBUF
062C  DD2AB520              LD     IX,(BCTPIO)
0630  DD09                  ADD    IX,BC
0632  DD7E00                LD     A,(IX)
0635  D300                         OUT     PIO0,A
0637  E3                                   EX      (SP),HL
0638  E3                                   EX      (SP),HL
0639  DD23                  INC    IX
063B  DD7E00                LD     A,(IX)
063E  D301                         OUT     PIO1,A
0640  E3                                   EX      (SP),HL
0641  E3                                   EX      (SP),HL
0642  3AB520                LD     A,(BCTPIO)
```

```
0645  C602                  ADD    A,2H
0647  C9                    RET
0648  CD5306        PIOEXT  CALL   DINPIO
064B  C9                    RET
              ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
              ;;;;;;;;
              ;                     SUBROUTINE      EINPIO
              ;PURPOSE
              ;INPUT
              ;OUTPUT
              ;REGISTERS USED
              ;DESCRIPTION
              ;.....................................................
              ........
                            NAME   EINPIO
064C  3E87          EINPIO  LD     A,87H
064E  D303                  OUT    PIO3,A
0650  E3                           EX     (SP),HL
0651  E3                           EX     (SP),HL
0652  C9                    RET
              ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
              ;;;;;;;;
              ;                     SUBROUTINE      DINPIO
              ;PURPOSE
              ;INPUT
              ;OUTPUT
              ;REGISTERS USED
              ;DESCRIPTION
              ;.....................................................
              ........
                            NAME   DINPIO
0653  3E07          DINPIO  LD     A,07H
0655  D303                  OUT    PIO3,A
0657  E3                           EX     (SP),HL
0658  E3                           EX     (SP),HL
0659  C9                    RET
              ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
              ;;;;;;;;
              ;                     SUBROUTINE      PRGSIO
              ;PURPOSE
              ;INPUT
              ;OUTPUT
              ;REGISTERS USED
              ;DESCRIPTION
              ;.....................................................
              ........
065A  AF            PRGSIO  XOR    A
065B  32B120                LD     (MWSIO),A
065E  21B120                LD     HL,MWSIO

0661  CDD004        MSI00   CALL   KEY
0664  FE01                  CP     K1
0666  2002                  JR     NZ,MSI01
0668  CBC6                  SET    0,(HL)
066A  CDD004        MSI01   CALL   KEY
066D  FE01                  CP     K1
066F  2002                  JR     NZ,MSI02
```

```
0671 CBCE        1316          SET     1,(HL)
0673 CDD004      1317 MSIO2    CALL    KEY
0676 FE01        1318          CP      K1
0678 2002        1319          JR      NZ,MSIO3
067A CBD6        1320          SET     2,(HL)
067C CDD004      1321 MSIO3    CALL    KEY
067F FE01        1322          CP      K1
0681 2002        1323          JR      NZ,MSIO4
0683 CBDE        1324          SET     3,(HL)
                 1325
0685 CDD004      1326 MSIO4    CALL    KEY
0688 FE01        1327          CP      K1
068A 2002        1328          JR      NZ,MSIO5
068C CBE6        1329          SET     4,(HL)
068E CDD004      1330 MSIO5    CALL    KEY
0691 FE01        1331          CP      K1
0693 2002        1332          JR      NZ,MSIO6
0695 CBEE        1333          SET     5,(HL)
0697 CDD004      1334 MSIO6    CALL    KEY
069A FE01        1335          CP      K1
069C 2002        1336          JR      NZ,MSIO7
069E CBF6        1337          SET     6,(HL)
06A0 CDD004      1338 MSIO7    CALL    KEY
06A3 FE01        1339          CP      K1
06A5 2002        1340          JR      NZ,MSFIN
06A7 CBFE        1341          SET     7,(HL)
06A9 3AB120      1342 MSFIN    LD      A,(MWSIO)
06AC D31F        1343          OUT     WCSIO,A
06AE E3          1344                  EX      (SP),HL
06AF E5          1345                  EX      (SP),HL
06B0 C9          1346          RET
                 1347 ;                SUBROUTINE MSIO
                 1348 ;PURPOSE
                 1349 ;INPUT
                 1350 ;OUTPUT
                 1351 ;REGISTERS USED
                 1352 ;DESCRIPTION
                 1353 ;.....................................................
                      ........
                 1354          NAME    MSIO
06B1 AF          1355 MSIO     XOR     A
06B2 32B620      1356          LD      (BCTSIO),A
06B5 DD2AB620    1357          LD      IX,(BCTSIO)
06B9 012020      1358          LD      BC,ASCBUF
06BC 3AB620      1359 SIO      LD      A,(BCTSIO)
06BF FE20        1360          CP      20h
06C1 2817        1361          JR      Z,SIOEXT
06C3 DD09        1362          ADD     IX,BC
                 1363
06C5 DBC9        1364 LOPSIO   IN      A,RSSIO
06C7 32B320      1365          LD      (STSIO),A
06CA E601        1366          AND     A,1H
06CC 28F7        1367          JR      Z,LOPSIO
06CE D31E        1368          OUT     WDSIO,A
06D0 E3          1369                  EX      (SP),HL
06D1 E3          1370                  EX      (SP),HL
06D2 DD23        1371          INC     IX
```

```
06D4  DD22B620                LD    (BCTSIO),IX
06D8  18E2                    JR    SIO
06DA  C9           SIOEXT     RET
                   ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
                   ;;;;;;;;
                   ;                SUBROUTINE       TEST
                   ;PURPOSE
                   ;INPUT
                   ;OUTPUT
                   ;REGISTERS USED
                   ;DESCRIPTION
                   ;.........................................................
                   ........
06DB  00           TEST1      NOP
06DC  C9                      RET
06DD  00           TEST2      NOP
06DE  C9                      RET
06DF  00           TEST3      NOP
06E0  C9                      RET
                   ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
                   ;;
                   ;          TABLE LOOKUP
                   ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
                   ;;
                   ;
06E1  7D           B27TBL     DB    7DH      ;0
06E2  30                      DB    30H      ;1
06E3  6E                      DB    6EH      ;2
06E4  7A                      DB    7AH      ;3
06E5  33                      DB    33H      ;4
06E6  5B                      DB    5BH      ;5
06E7  5F                      DB    5FH      ;6
06E8  71                      DB    71H      ;7
06E9  7F                      DB    7FH      ;8
06EA  7B                      DB    7BH      ;9
                   ;
06EB  30           B2ASCI     DB    30H
06EC  31                      DB    31H
06ED  32                      DB    32H
06EE  33                      DB    33H
06EF  34                      DB    34H
06F0  35                      DB    35H
06F1  36                      DB    36H
06F2  37                      DB    37H
06F3  38                      DB    38H
06F4  39                      DB    39H
                   ;
06F5  7D           K27TBL     DB    7DH      ;1     1     0
06F6  30                      DB    30H      ;1     2     1
06F7  33                      DB    33H      ;1     3     4
06F8  71                      DB    71H      ;1     4     7
06F9  80                      DB    80H      ;2     1     .
06FA  6E                      DB    6EH      ;2     2     2
06FB  5B                      DB    5BH      ;2     3     5
06FC  7F                      DB    7FH      ;2     4     8
06FD  00                      DB    00H      ;3     1     /PRJ-ID
06FE  7A                      DB    7AH      ;3     2     3
```

```
06FF  5F           DB    5FH     ;3     3      6
0700  7B           DB    7BH     ;3     4      9
0701  77           DB    77H     ;4     1      A/SETN
0702  1F           DB    1FH     ;4     2      B/SETZ
0703  4D           DB    4DH     ;4     3      C/SETY
0704  3E           DB    3EH     ;4     4      D/SETX
0705  4F           DB    4FH     ;5     1      E/ENTER
0706  47           DB    47H     ;5     2      F/STP-PRN
0707  1E           DB    1EH     ;5     3      O/STP-PDP
0708  1C           DB    1CH     ;5     4      U/CLR-XYZ
0709  1A           DB    1AH     ;6     1      "/TEST
070A  37           DB    37H     ;6     2      U/AUT-PRN
070B  02           DB    02H     ;6     3      -/AUT-PDP
070C  06           DB    06H     ;6     4      R/RESET
             ;
070D  00     K2BCD DB    00H
070E  01           DB    01H
070F  04           DB    04H
0710  07           DB    07H
0711  F0           DB    0F0H
0712  02           DB    02H
0713  05           DB    05H
0714  08           DB    08H
0715  F1           DB    0F1H
0716  03           DB    03H
0717  06           DB    06H
0718  09           DB    09H
0719  0A           DB    0AH
071A  0B           DB    0BH
071B  0C           DB    0CH
071C  0D           DB    0DH
071D  0E           DB    0EH
071E  0F           DB    0FH
071F  F2           DB    0F2H
0720  F3           DB    0F3H
0721  F4           DB    0F4H
0722  F5           DB    0F5H
0723  F6           DB    0F6H
0724  F7           DB    0F7H
             ;
0725               ORG   1FF0H
1FF0  B0     VECTBL DB   0B0H    ;DEVICE 1 F0
1FF1  1E           DB    1EH
1FF2  00           DB    00H     ;DEVICE 2 F2
1FF3  1F           DB    1FH
1FF4  A0           DB    0A0H    ;DEVICE 3 F4
1FF5  1F           DB    1FH
             ;
             ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;

Errors       0

A>
```

ภาคผนวก ง

คู่มือการใช้เครื่อง

คู่มือการใช้เครื่อง

๑. ระบบเครื่องใช้ไฟ ๒๒๐ โวลท์

๒. เมื่อเสียบปลั๊กไฟแล้วให้เปิดสวิทช์ของระบบเก็บข้อมูล

๓. กดสวิทช์ RESET เครื่องจะเริ่มทำงาน

๔. กดคีย์ ENTER บนแป้นคีย์บอร์ด เพื่อเริ่มการทำงานตามปกติ

๕. ภาคแสดงค่าจะแสดงตัวอักษร ENTER บนภาคแสดงค่า เอ็คซ์ วาย แซด และเอ็น ตามลำดับ เพื่อรอการคีย์ข้อมูลกำหนดค่าเริ่มแรก

๖. กดคีย์ตัวเลขจากหลักที่ ๘ ไปหาหลักที่ ๑ เพื่อกำหนดค่าเริ่มต้น เอ็คซ์ วาย แซด และเอ็น เมื่อกำหนดครบแล้วระบบเก็บข้อมูลจะเริ่มทำงานโดยแสดงค่า เอ็คซ์ วาย แซด เปลี่ยนไปตลอดเวลา เมื่อมีการหมุนแกนของเครื่องร่างแผนที่จากภาพถ่ายทางอากาศ

๗. เมื่อกำหนดจุดพิกัดฉากที่ต้องการให้ส่งผ่านวงจรอินเตอร์เฟสให้กดคีย์ STEP-PDP สำหรับการส่งค่าพิกัดฉากผ่านวงจรอินเตอร์เฟสแบบขนาน กดคีย์ STEP-PRN สำหรับการส่งค่าพิกัดฉากผ่านวงจรอินเตอร์เฟสแบบอนุกรม

๘. การหยุดการทำงาน และเริ่มการทำงานขั้นตอนที่หนึ่งใหม่ ไม่ว่ากำลังทำขั้นตอนที่เท่าไรอยู่ก็ตาม เมื่อกดคีย์ SW-RESETหรือสวิทช์ RESET ระบบเก็บข้อมูลจะเริ่มทำงานจากขั้นตอนที่ ๑ ใหม่เสมอ

๙. เมื่อต้องการปิดเครื่อง ให้ปิดสวิทช์ของระบบเก็บข้อมูล และควรบันทึกค่าตัวเลขที่แสดงค่าครั้งสุดท้ายไว้ เพื่อใช้เป็นค่าเริ่มแรกเมื่อเปิดเครื่องครั้งใหม่สำหรับโมเดล

ประวัติผู้เขียน

นายสนธยา สุธัมมสภา เกิดวันที่ ๔ กันยายน ๒๔๙๕ ที่กรุงเทพมหานคร สำเร็จการศึกษาขั้นปริญญาบัณฑิตจากจุฬาลงกรณ์มหาวิทยาลัย ได้รับปริญญาวิศวกรรมศาสตร์บัณฑิตในปี พ.ศ. ๒๕๑๘ ปัจจุบันทำงานอยู่บริษัท คอนโทรลดาต้า (ประเทศไทย) จำกัด