เอกสารอ้างอิง

1. Field and Depot Maintenance Manual Switchboard, Telephone, Manual SB-86/P
2. Manual Telephone Central Office Group AN/FTA-13
3. Manual Telephone Central Office Group AN/GTA/6A
4. Manual Telephone Central Office Group PC-3T
5. T.O. 31W-1-22 SB-22/PT Manual Telephone Switchboard
6. ธวัชชัย เลื่อนฉวี วีระชัย เชาว์กำเนิด เทคโนโลยีโทรศัพท์ พ.ศ.2527 สยามบรรณการพิมพ์
7. International Telephone Service Network Management, Traffic Engineering, Recommendation E.401-E.543 CCITT Volume 2-Facicle 2.3
8. T.O. 31W-1-2 PT-291 Department of the Air Force Technical Order TA-312/PT, EE-8, DM-570

ผนวก ก. Erlang Table

Table of the Erlang loss formula
(Erlang No. 1 formula, also called Erlang B formula)

Loss probabilities: 1 %, 3 %, 5 %, 7 %.

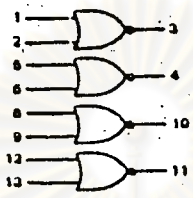
Let p = the loss probability
y = the traffic offered (in Erlang)
n = the number of circuits

Formula: $$E_{1,n}(y) = p = \frac{\frac{y^n}{n!}}{1 + \frac{y}{1} + \frac{y^2}{2!} + \ldots + \frac{y^n}{n!}}$$

n	$p = 1\%$	$p = 3\%$	$p = 5\%$	$p = 7\%$	n	$p = 1\%$	$p = 3\%$	$p = 5\%$	$p = 7\%$
1	0.01	0.03	0.05	0.08	51	38.80	42.89	45.53	47.72
2	0.15	0.28	0.38	0.47	52	39.70	43.85	46.53	48.76
3	0.46	0.72	0.90	1.06	53	40.60	44.81	47.53	49.79
4	0.87	1.26	1.53	1.75	54	41.50	45.78	48.54	50.83
5	1.36	1.88	2.22	2.50	55	42.41	46.74	49.54	51.86
6	1.91	2.54	2.96	3.30	56	43.31	47.70	50.54	52.90
7	2.50	3.25	3.74	4.14	57	44.22	48.67	51.55	53.94
8	3.13	3.99	4.54	5.00	58	45.13	49.63	52.55	54.98
9	3.78	4.75	5.37	5.88	59	46.04	50.60	53.56	56.02
10	4.46	5.53	6.22	6.78	60	46.95	51.57	54.57	57.06
11	5.16	6.33	7.08	7.69	61	47.86	52.54	55.57	58.10
12	5.88	7.14	7.95	8.61	62	48.77	53.51	56.58	59.14
13	6.61	7.97	8.84	9.54	63	49.69	54.48	57.59	60.18
14	7.35	8.80	9.73	10.48	64	50.60	55.45	58.60	61.22
15	8.11	9.65	10.63	11.43	65	51.52	56.42	59.61	62.27
16	8.88	10.51	11.54	12.39	66	52.44	57.39	60.62	63.31
17	9.65	11.37	12.46	13.35	67	53.35	58.37	61.63	64.35
18	10.44	12.24	13.39	14.32	68	54.27	59.34	62.64	65.40
19	11.23	13.11	14.31	15.29	69	55.19	60.32	63.65	66.44
20	12.03	14.00	15.25	16.27	70	56.11	61.29	64.67	67.49
21	12.84	14.89	16.19	17.25	71	57.03	62.27	65.68	68.53
22	13.65	15.78	17.13	18.24	72	57.96	63.24	66.69	69.58
23	14.47	16.68	18.08	19.23	73	58.88	64.22	67.71	70.62
24	15.29	17.58	19.03	20.22	74	59.80	65.20	68.72	71.67
25	16.13	18.48	19.99	21.21	75	60.73	66.18	69.74	72.72
26	16.96	19.39	20.94	22.21	76	61.65	67.16	70.75	73.77
27	17.80	20.31	21.90	23.21	77	62.58	68.14	71.77	74.81
28	18.64	21.22	22.87	24.22	78	63.51	69.12	72.79	75.86
29	19.49	22.14	23.83	25.22	79	64.43	70.10	73.80	76.91
30	20.34	23.06	24.80	26.23	80	65.36	71.08	74.82	77.96
31	21.19	23.99	25.77	27.24	81	66.29	72.06	75.84	79.01
32	22.05	24.91	26.75	28.25	82	67.22	73.04	76.86	80.06
33	22.91	25.84	27.72	29.26	83	68.15	74.02	77.87	81.11
34	23.77	26.78	28.70	30.28	84	69.08	75.01	78.89	82.16
35	24.64	27.71	29.68	31.29	85	70.02	75.99	79.91	83.21
36	25.51	28.65	30.66	32.31	86	70.95	76.97	80.93	84.26
37	26.38	29.59	31.64	33.33	87	71.88	77.96	81.95	85.31
38	27.25	30.53	32.62	34.35	88	72.81	78.94	82.97	86.36
39	28.13	31.47	33.61	35.37	89	73.75	79.93	83.99	87.41
40	29.01	32.41	34.60	36.40	90	74.68	80.91	85.01	88.46
41	29.89	33.36	35.58	37.42	91	75.62	81.90	86.04	89.52
42	30.77	34.30	36.57	38.45	92	76.56	82.89	87.06	90.57
43	31.66	35.25	37.57	39.47	93	77.49	83.87	88.08	91.62
44	32.54	36.20	38.56	40.50	94	78.43	84.86	89.10	92.67
45	33.43	37.16	39.55	41.53	95	79.37	85.85	90.12	93.73
46	34.32	38.11	40.54	42.56	96	80.31	86.84	91.15	94.78
47	35.22	39.06	41.54	43.59	97	81.24	87.83	92.17	95.83
48	36.11	40.02	42.54	44.62	98	82.18	88.82	93.19	96.89
49	37.00	40.98	43.53	45.65	99	83.12	89.80	94.22	97.94
50	37.90	41.93	44.53	46.69	100	84.06	90.79	95.24	98.99

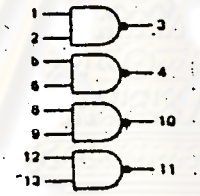
ผนวก ข. แผนผัง IC ที่ใช้

MC14001B
Quad 2-Input NOR Gate



V_{DD} = Pin 14
V_{SS} = Pin 7

MC14011B
Quad 2-Input NAND Gate



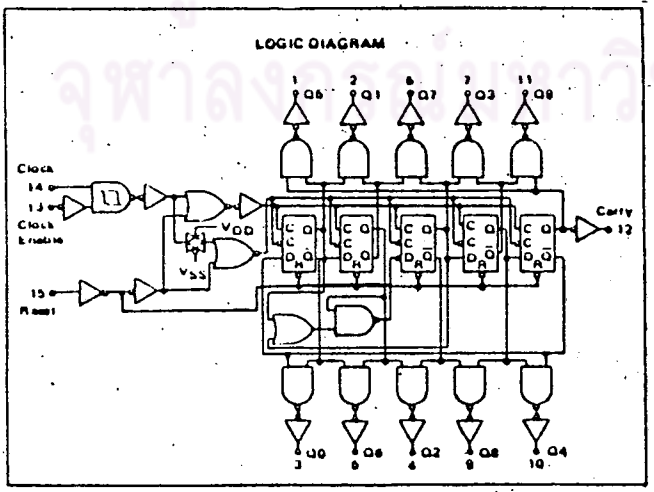
MC14017B
DECADE COUNTER/DIVIDER

FUNCTIONAL TRUTH TABLE
(Positive Logic)

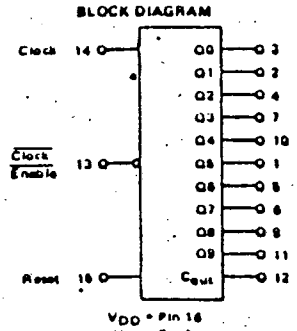
CLOCK	CLOCK ENABLE	RESET	DECODE OUTPUT = n
0	X	0	n
X	1	0	n
X	X	1	Q0
⎍	0	0	n+1
⎍	X	0	n
X	⎍	0	n
1	⎍	0	n+1

X = Don't Care If n < 5 Carry = "1", Otherwise = "0"

LOGIC DIAGRAM



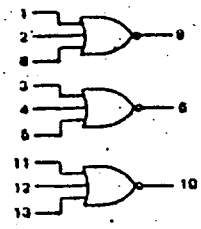
BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

MC14025B

Triple 3-Input NOR Gate



MC14027B

DUAL J-K FLIP-FLOP

TRUTH TABLE

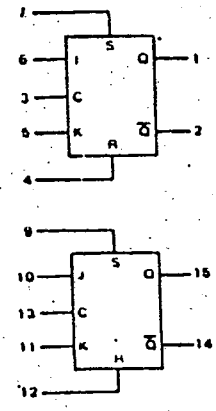
INPUTS						OUTPUTS*	
C↑	J	K	S	R	Q_n‡	Q_{n+1}*	$\overline{Q_{n+1}}$
↑	1	X	0	0	0	1	0
↑	X	0	0	0	1	1	0
↑	0	X	0	0	0	0	1
↑	X	1	0	0	1	0	1
↓	X	X	0	0	X	Q_n	$\overline{Q_n}$
X	X	X	1	0	X	1	0
X	X	X	0	1	X	0	1
X	X	X	1	1	X	1	1

No Change

X = Don't Care
↑ = Level Change
‡ = Present State
* = Next State

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

CLOCK DIAGRAM

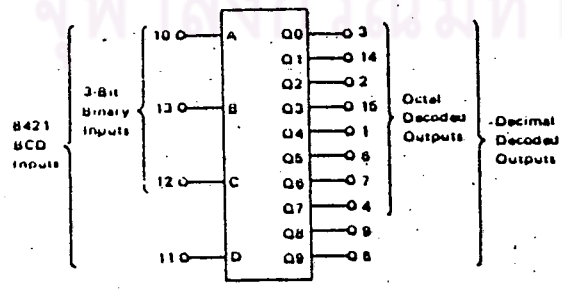


V_{DD} = Pin 16
V_{SS} = Pin 8

MC14028B

BCD-TO-DECIMAL DECODER
BINARY-TO-OCTAL DECODER

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

TRUTH TABLE

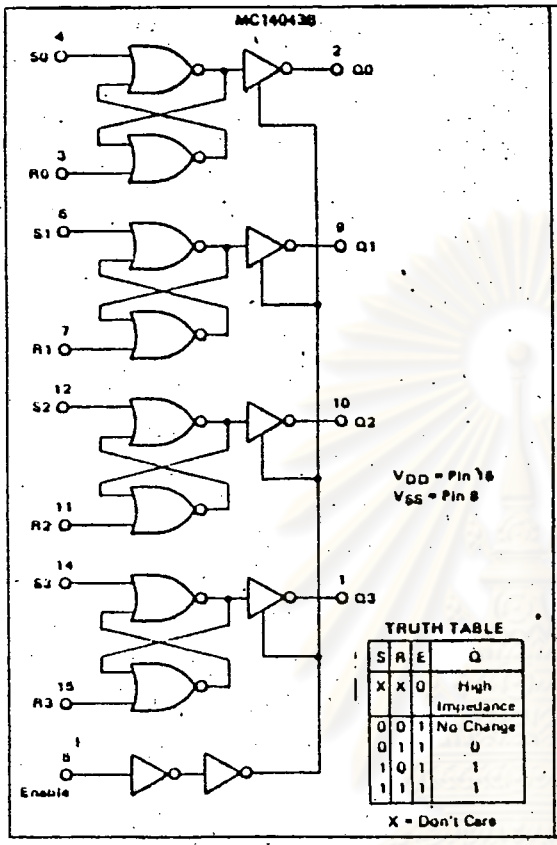
INPUT				OUTPUT									
D	C	B	A	Q9	Q8	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0
0	0	0	0	0	0	0	0	0	0	0	0	0	1
0	0	0	1	0	0	0	0	0	0	0	0	1	0
0	0	1	0	0	0	0	0	0	0	0	1	0	0
0	0	1	1	0	0	0	0	0	0	1	0	0	0
0	1	0	0	0	0	0	0	0	1	0	0	0	0
0	1	0	1	0	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	0	1	0	0	0	0	0	0
0	1	1	1	0	0	1	0	0	0	0	0	0	0
1	0	0	0	0	1	0	0	0	0	0	0	0	0
1	0	0	1	1	0	0	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0	0	0	0	0	0
1	0	1	1	0	0	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0	0	0	0
1	1	0	1	0	0	0	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0	0	0	0

MC14043B

QUAD "NOR" R-S LATCH

MC14044B

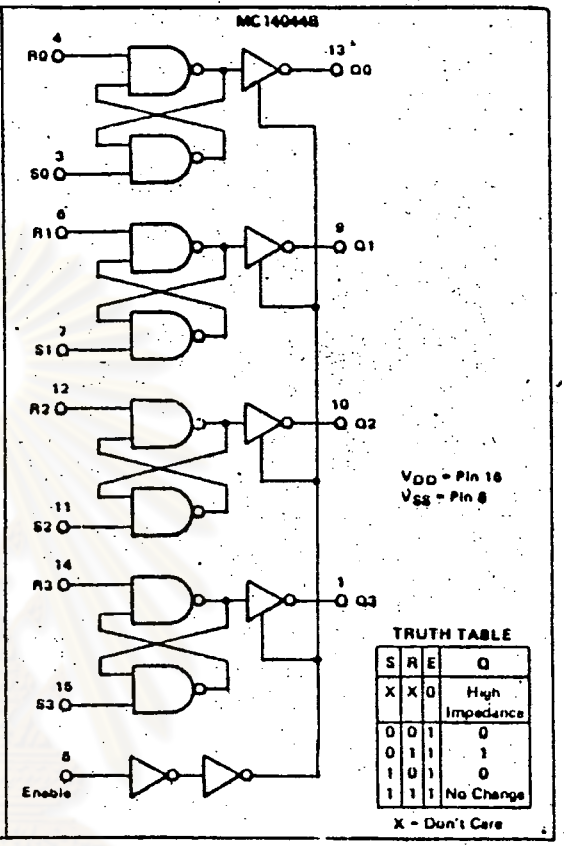
QUAD "NAND" R-S LATCH



TRUTH TABLE

S	R	E	Q
X	X	0	High Impedance
0	0	1	No Change
0	1	1	0
1	0	1	1
1	1	1	1

X = Don't Care



TRUTH TABLE

S	R	E	Q
X	X	0	High Impedance
0	0	1	0
0	1	1	1
1	0	1	0
1	1	1	No Change

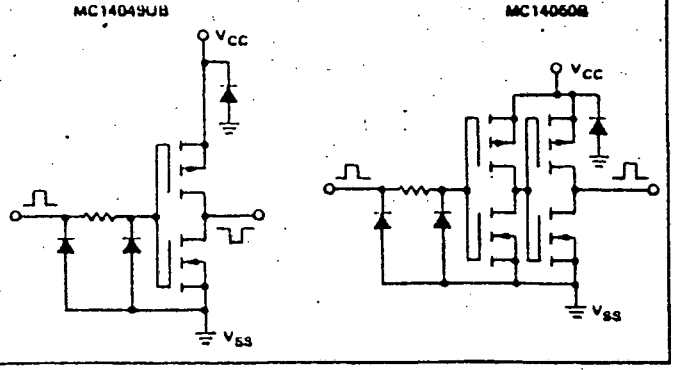
X = Don't Care

MC14049UB
MC14050B

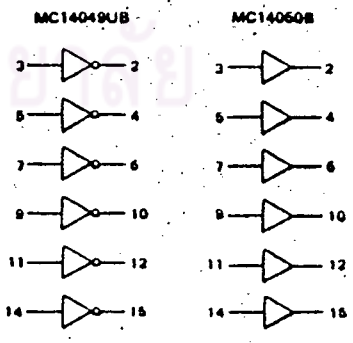
HEX BUFFERS

Inverting – MC14049UB
Noninverting – MC14050B

CIRCUIT SCHEMATIC
(1/6 OF CIRCUIT SHOWN)



LOGIC DIAGRAMS



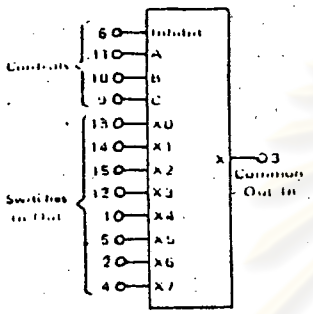
NC = Pin 13, 16
VSS = Pin 8
VCC = Pin 1

NC = Pin 13, 16
VSS = Pin 8
VCC = Pin 1

MC14051B
MC14052B
MC14053B

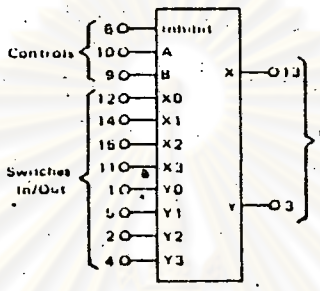
ANALOG MULTIPLEXERS/ DEMULTIPLEXERS

MC14051B
8-Channel Analog Multiplexer/Demultiplexer



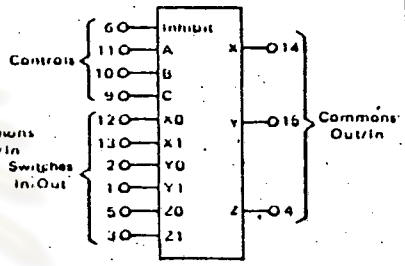
V_{DD} = Pin 16
V_{SS} = Pin 8
V_{EE} = Pin 7

MC14052B
Dual 4-Channel Analog Multiplexer/Demultiplexer



V_{DD} = Pin 16
V_{SS} = Pin 8
V_{EE} = Pin 7

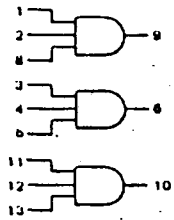
MC14053B
Triple 2-Channel Analog Multiplexer/Demultiplexer



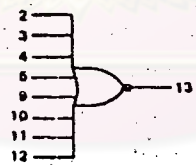
V_{DD} = Pin 16
V_{SS} = Pin 8
V_{EE} = Pin 7

Note: Control inputs referenced to V_{SS}. Analog inputs and Outputs reference to V_{EE}. V_{EE} must be $\leq V_{SS}$.

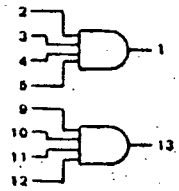
MC14073B
Triple 3-Input AND Gate



MC14078B
8-Input NOR Gate



MC14082B
Dual 4-Input AND Gate



MC14175B
QUAD TYPE D FLIP-FLOP

TRUTH TABLE
(Positive Logic)

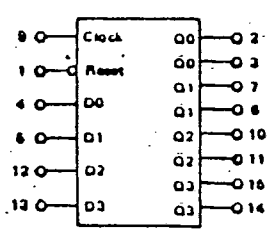
INPUTS			OUTPUTS		
Clock	Data	Reset	Q	$\bar{Q}$	
↑	0	1	0	1	
↑	1	1	1	0	
↓	X	1	Q	$\bar{Q}$	No Change
X	X	0	0	1	

X = Don't Care

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

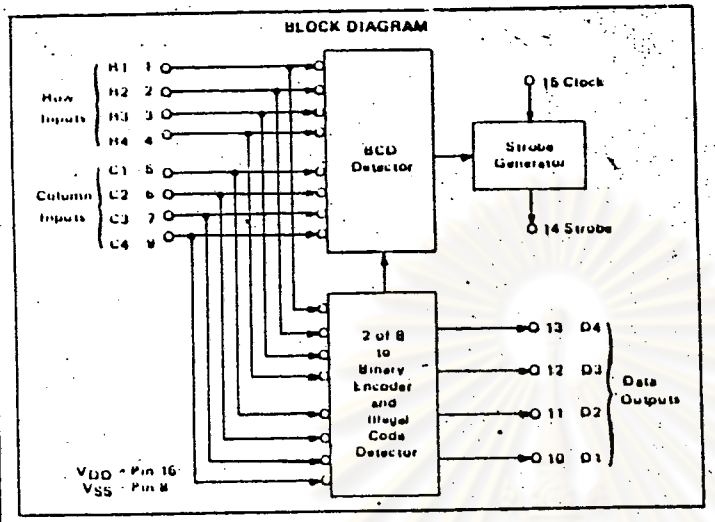
BLOCK DIAGRAM

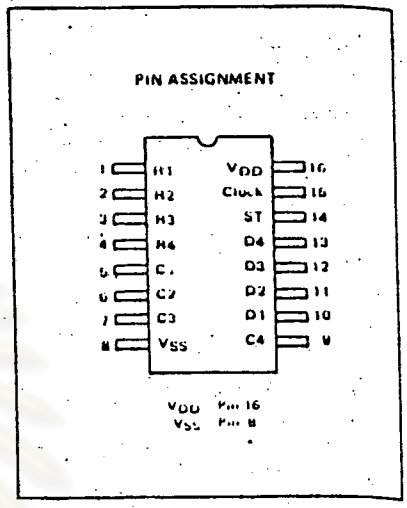


V_{DD} = Pin 16
V_{SS} = Pin 8

MC14419

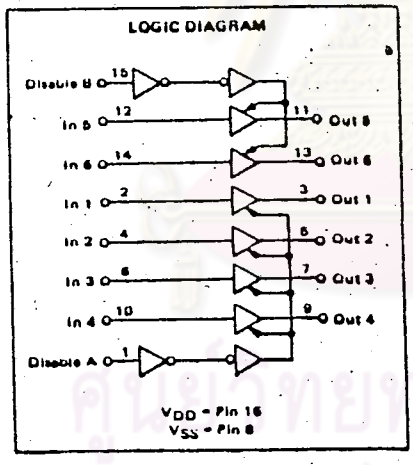
2-OF-8 KEYPAD-TO-BINARY ENCODER





MC14503B

HEX 3-STATE BUFFER



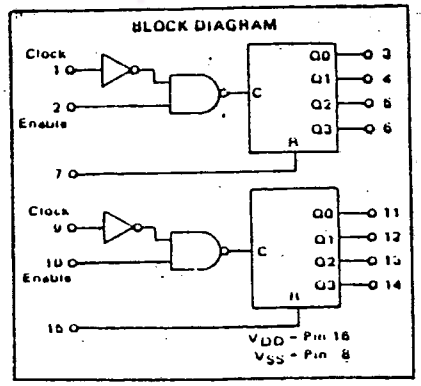
TRUTH TABLE

In_n	Appropriate Disable Input	Out_n
0	0	0
1	0	1
X	1	High Impedance

X = Don't Care

MC14520B

DUAL BINARY UP COUNTER



TRUTH TABLE

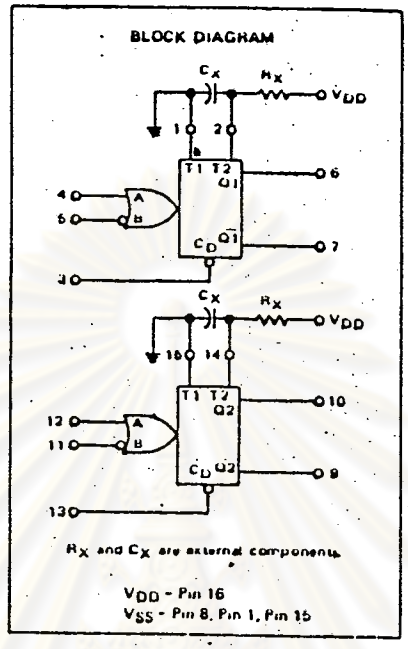
CLOCK	ENABLE	RESET	ACTION
↑	1	0	Increment Counter
0	↓	0	Increment Counter
↓	X	0	No Change
X	↑	0	No Change
↑	0	0	No Change
1	↓	0	No Change
X	X	1	Q0 thru Q3 = 0

X = Don't Care

MC14538B

DUAL PRECISION
RETRIGGERABLE/RESETTABLE
MONOSTABLE MULTIVIBRATOR

BLOCK DIAGRAM



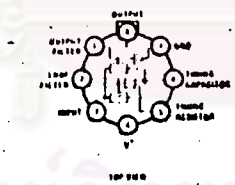
R_X and C_X are external components.

V_{DD} - Pin 16
V_{SS} - Pin 8, Pin 1, Pin 15

LM567/LM567C tone decoder

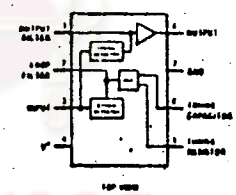
schematic and connection diagrams

Metal Can Package



Order Number LM567H or LM567CH

Dual-In-Line Package

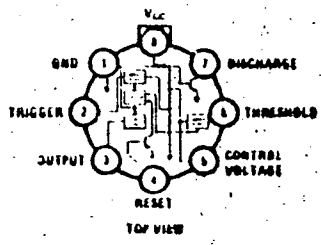


Order Number LM567CN

LM555/LM555C timer

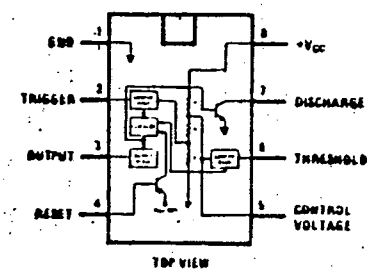
connection diagrams

Metal Can Package



Order Number LM555H or LM555CH

Dual-In-Line Package



Order Number LM555CN

ประวัติผู้เขียน

ชื่อ เรืออากาศเอก ธวัชชัย เลื่อนฉวี

วุฒิการศึกษา วิศวกรรมศาสตร์บัณฑิต สาขาวิศวกรรมไฟฟ้า สถาบันเทคโนโลยีพระจอมเกล้าวิทยาเขตเจ้าคุณทหาร ลาดกระบัง พ.ศ.2519

ตำแหน่ง ประจำกรมสื่อสารทหารอากาศ