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ภาคผนวก (ก)

ข้อมูลทางไฟฟ้าของทรานซิสเตอร์ เบอร์ 2N3904

MOTOROLA Semiconductors
BOX 955 • PHOENIX 1, ARIZONA
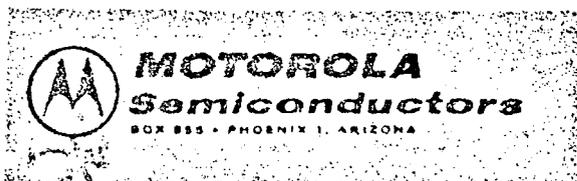
2N3903
2N3904

NPN SILICON ANNULAR* TRANSISTORS

... designed for general purpose switching and amplifier applications and for complementary circuitry with types 2N3905 and 2N3906.

- One-Piece, Injection-Molded Unibloc† Package for High Reliability
- High Voltage Ratings — $BV_{CEO} = 40$ Volts minimum
- Current Gain Specified from 100 μA to 100 mA
- Complete Switching and Amplifier Specifications
- Low Capacitance — $C_{obo} = 4.0$ pf maximum

NPN SILICON SWITCHING & AMPLIFIER TRANSISTORS

AUGUST 1965 — DS 5127

"D" shape package lies flat or easy printed circuit mounting.

Rugged, one-piece, high temperature, pressure-molded, humidity resistant, plastic package.

EBC configuration easily adaptable to standard TO-18 pin circle.

19/32 inch, gold-plated nickel, oval leads permit reliable solder connections.

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Collector-Base Voltage	V_{CB}	60	Vdc
Collector-Emitter Voltage	V_{CEO}	40	Vdc
Emitter-Base Voltage	V_{EB}	6	Vdc
Collector Current	I_C	200	mAdc
Total Device Dissipation @ T_A - 60°C	P_D	210	mW
Total Device Dissipation @ T_A - 25°C Derate above 25°C	P_D	310 2.81	mW mW/°C
Thermal Resistance, Junction to Ambient	θ_{JA}	0.357	°C/mW
Junction Operating Temperature	T_J	135	°C
Storage Temperature Range	T_{stg}	-55 to +135	°C

TO-92

*Annular semiconductors patented by Motorola Inc.
†Trademark of Motorola Inc.

MOTOROLA Semiconductor Products Inc.

SI HIGH FREQUENCY TRANSISTORS 2N3903, 2N3904

ภาคผนวก(ก)   ต่อ

## STATIC CHARACTERISTICS

FIGURE 15   NORMALIZED CURRENT GAIN
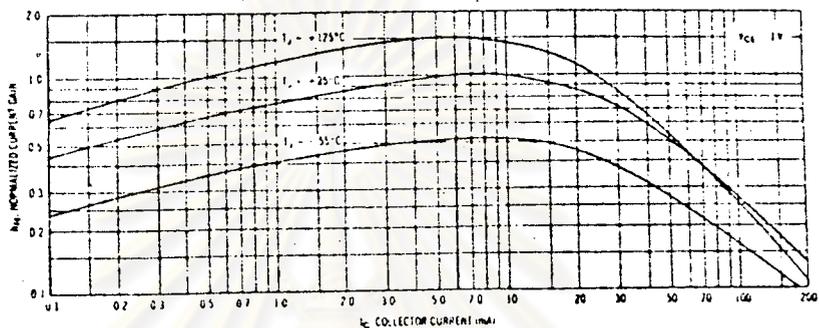

FIGURE 16   COLLECTOR SATURATION REGION
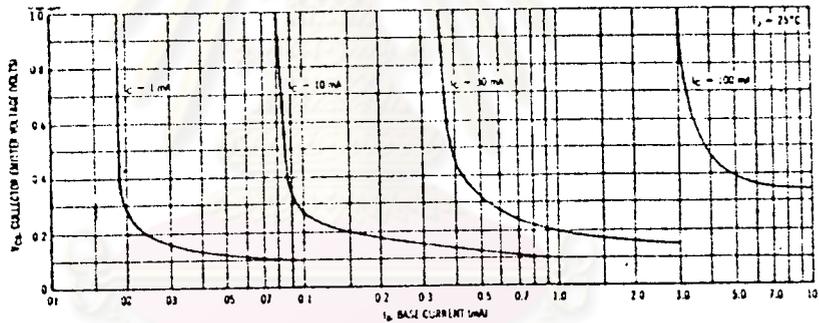

FIGURE 17   "ON" VOLTAGES
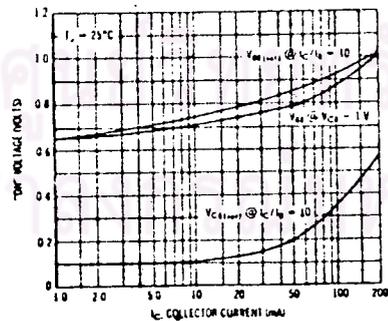
FIGURE 18   TEMPERATURE COEFFICIENTS

ภาคผนวก (ข)
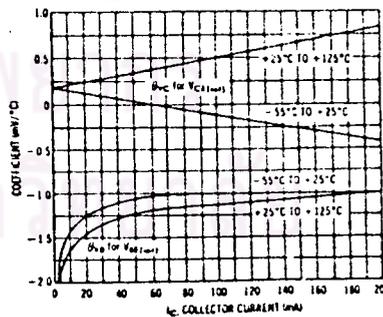
ข้อมูลทางไฟฟ้าของทรานซิสเตอร์ เบอร์ 2N5070

RF POWER TRANSISTOR — 2N5070
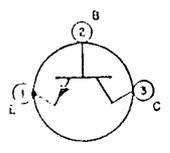
Si n-p-n "overlay" epitaxial planar type used in high-power class A or B service in a 2-to-30-MHz single-sideband power amplifier operating from a 28-volt power supply. JEDEC TO-60, Outline No.23. See Mounting Hardware for desired mounting arrangement.

MAXIMUM RATINGS

Collector-to-Emitter Voltage:			
V_{BE} = −1.5 V		V_{CEV}	65 V
R_{BE} = 5 Ω		V_{CER}	40 V
Emitter-to-Base Voltage		V_{EBO}	4 V
Collector Current		I_C	3.3 A
Peak Collector Current		i_C	10 A
Transistor Dissipation:			
T_C up to 25°C		P_T	70 W
T_C above 25°C		P_T	See curve page 300
Temperature Range:			
Operating (Junction)		T_J (opr)	−65 to 200 °C
Storage		T_{STG}	−65 to 200 °C
Lead-Soldering Temperature (10 s max)		T_L	230 °C

CHARACTERISTICS (At case temperature = 25°C)

Emitter-to-Base Breakdown Voltage (I_E = 10 mA, I_C = 0)		$V_{(BR)EBO}$	4 min V
Collector-to-Emitter Sustaining Voltage:			
V_{BE} = −1.5 V, I_C = 200 mA		V_{CEV} (sus)	65 min V
R_{BE} = 5 Ω, I_C = 200 mA		V_{CER} (sus)	40 min V
Collector-Cutoff Current:			
V_{CE} = 30 V, I_B = 0		I_{CEO}	5 max mA
V_{CB} = 30 V, I_E = 0		I_{CBO}	10 max mA
Output Capacitance (V_{CB} = 1 V, I_E = 0, f = 1 MHz)		C_{obo}	85 max pF
Thermal Resistance, Junction-to-Case		$θ_{J-C}$	2.5 max °C/W

TYPICAL OPERATION IN RF-AMPLIFIER CIRCUIT

Collector Supply Voltage	28	V
Collector Base Current	20	mA
RF Power Output:		
Average	12.5 min	W
Peak Envelope	25 min	W
Intermodulation Distortion	30 max	dB
Collector Efficiency	40 min	%

TYPICAL RF POWER-OUTPUT CHARACTERISTICS
TYPE 2N5070
COLLECTOR SUPPLY VOLTS (V_{CC}) = 28
FREQUENCIES (TWO-TONE) = 30 MHz, 30.001 MHz
COLLECTOR QUIESCENT CURRENT (I_{CQ}) = 20 mA
CASE TEMPERATURE (T_C) = 25°C OR UP TO 75°C

INTERMODULATION DISTORTION (IMD) — dB
RF POWER OUTPUT (POUT) — W(PEP)
92LS-1877T1
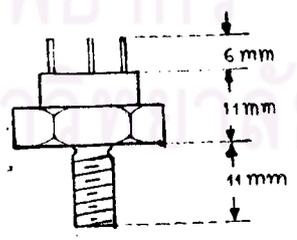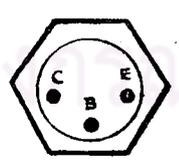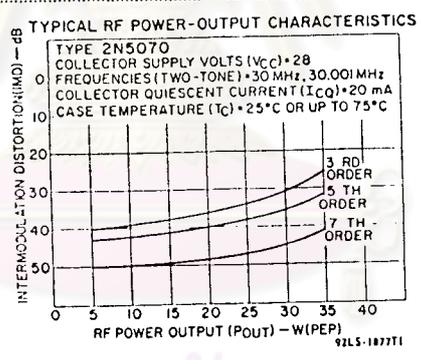
ภาคผนวก(ค)

ข้อมูลทางไฟฟ้าของไอซี เบอร์ 7404

HEX INVERTER   54/7404

SPEED/PACKAGE AVAILABILITY

54	F,W	74	A,F
54H	F,W	74H	A,F
54LS	F,W	74LS	A,F
54S	F,W	74S	A,F

PIN CONFIGURATION
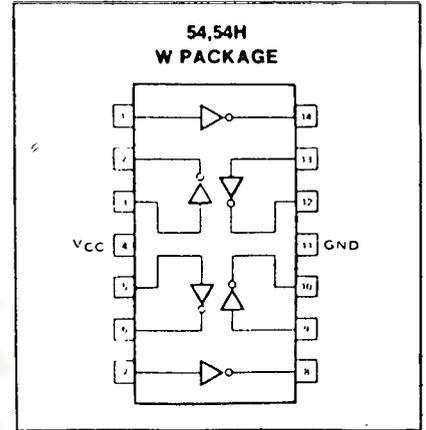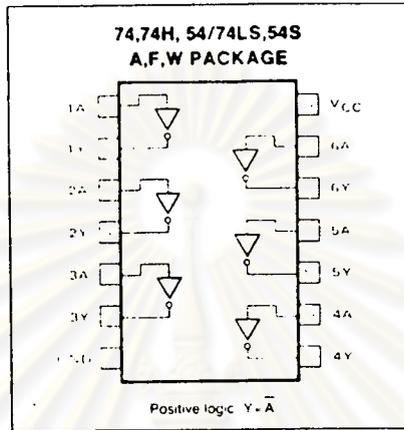
74,74H, 54/74LS,54S
A,F,W PACKAGE

Positive logic Y = $\overline{A}$

54,54H
W PACKAGE

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS	54/74 C_L = 15pF R_L = 400Ω			54/74H C_L = 25pF R_L = 280Ω			54/74LS C_L = 15pF R_L = 2kΩ			54/74S C_L = 15pF R_L = 280Ω			
PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
Propagation delay time t_{PLH} Low-to-high		12	22		6	10		5	15	2	3 C_L = 50pF 4.5	4.5	ns
t_{PHL} High-to-low		8	15		6.5	10		9	15	2	3 C_L = 50pF 5	5	ns

Load circuit and typical waveforms are shown at the front of section

ศูนย์วิทยทรัพยากร

จุฬาลงกรณ์มหาวิทยาลัย

ภาคผนวก (ง)

ข้อมูลทางไฟฟ้าของไอซี เบอร์ 7474

DUAL D-TYPE POSITIVE EDGE-TRIGGERED FLIP-FLOP · 54/7474

SPEED/PACKAGE AVAILABILITY

|			
54	F,W	74	A,F
54H	F,W	74H	A,F
54LS	F,W	74LS	A,F
54S	F,W	74S	A,F

DESCRIPTION

These monolithic dual edge-triggered D-type flip-flops feature individual D, clock, preset, and clear inputs.

Preset and clear inputs are active-low and operate independently of the clock input. When preset and clear are inactive (high), information at the D input is transferred to the Q output on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D-input signal has no effect at the output.

FUNCTIONAL BLOCK DIAGRAM (Each Flip-Flop)

PIN CONFIGURATION

A,F, PACKAGE

W PACKAGE
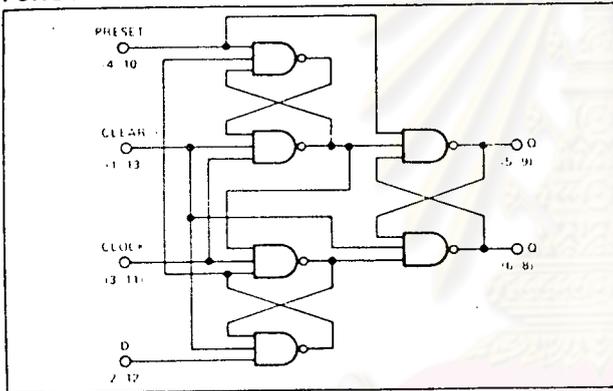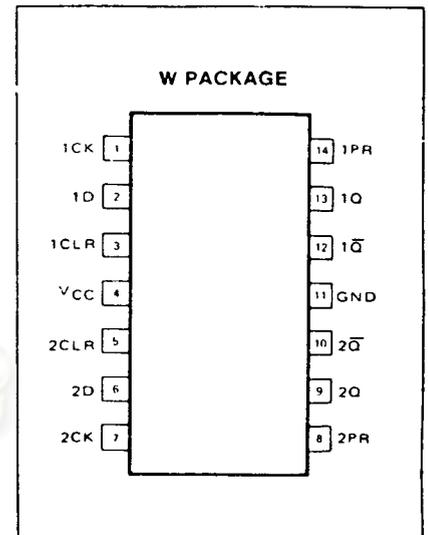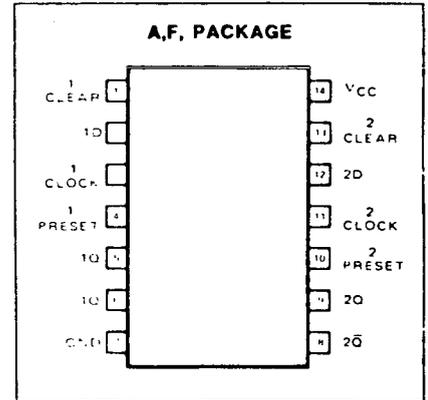
TRUTH TABLE (Each Flip-Flop)

Inputs				Outputs	
Preset	Clear	Clock	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

H – high level (steady state) L – low level (steady state)
*This condition is nonstable. It will not remain after clear and preset return to their inactive (high) state

ภาคผนวก(ง) ต่อ

ข้อมูลทางไฟฟ้าของไอซี เบอร์ 7474

DUAL D-TYPE POSITIVE EDGE-TRIGGERED FLIP-FLOP · 54/7474

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS			54/74 C_L - 15pF R_L 400Ω			54/74H C_L 25pF R_L 280Ω			54/74LS C_L 15pF R_L 2kΩ			54/74S C_L 15pF R_L 280Ω			
PARAMETER	FROM INPUT	TO OUTPUT	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
f_{Clock} Clock frequency			15	25		35	43		25 25	33		75	90		MHz
$t_{w(Clock)}$ Width of clock input pulse															ns
Clock high			30			15						6			
Clock low			37			13.5						7.3			
$t_{w(Clear)}$ Width of clear input pulse			30			25			25			7			ns
$t_{w(Preset)}$ Width of preset input pulse			30			25			25			7			ns
t_{Setup} Input setup time			20↑	15								3↓			ns
High level						10↑			25						
Low level						15↑			20						
t_{Hold} Input hold time			5*	2		5↑			5			2↓			ns
Propagation delay time															ns
t_{PLH} Low-to-high	Clear, Preset				25			20		8	25	5 8	6 CLK-1 13.5 CLK-0		
t_{PHL} High-to-low					40			30		16	40	5	8		
t_{PHL} Low-to-high	Clock		10	14	25	4	8.5	15		8	25	7	9		ns
t_{PHL} High-to-low			10	20	40		13	20		16	40	7	9		

Load circuit and typical waveforms are shown at the front of section

ภาคผนวก(จ)

ข้อมูลทางไฟฟ้าของไอซี เบอร์ 7490

DECADE COUNTER

54/7490

SPEED/PACKAGE AVAILABILITY
54   F.W   74   A.F
54LS F.W   74LS A.F

DESCRIPTION

This monolithic counter contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five.

The 54/74LS90 also has a gated zero reset and gated set-to-nine inputs for use in BCD nine's complement applications.

To use its maximum count length of this counter, the B input is connected to the Q_A output. The input count pulses are applied to input A and the outputs are as described in the function table. A symmetrical divide-by-ten count can be obtained by connecting the Q_D output to the A input and applying the input count to the B input which gives a divide-by-ten square wave at output Q_A.

BLOCK DIAGRAM 54LS/74LS

PIN CONFIGURATION

54/74
A,F,W PACKAGE

54LS/74LS
A,F,W PACKAGE

INPUT B	1	14	INPUT A
$R_{0(1)}$	2	13	NC
$R_{0(2)}$	3	12	Q_A
NC	4	11	Q_D
V_{CC}	5	10	GND
$R_{9(1)}$	6	9	Q_B
$R_{9(2)}$	7	8	Q_C
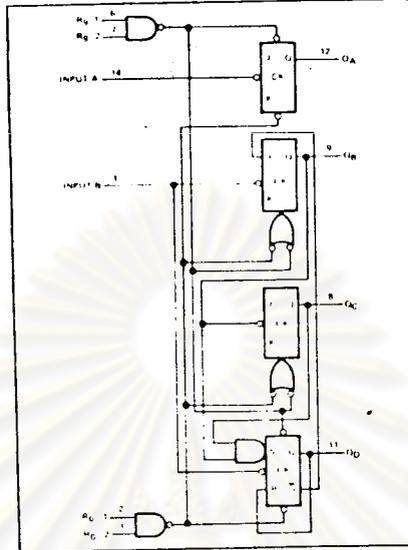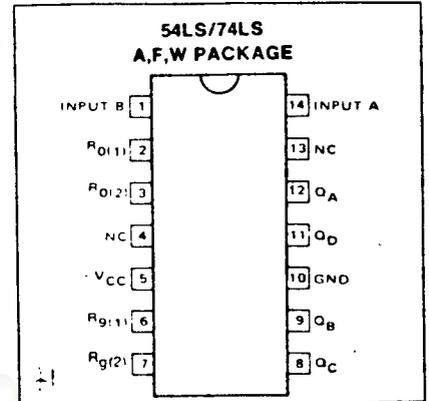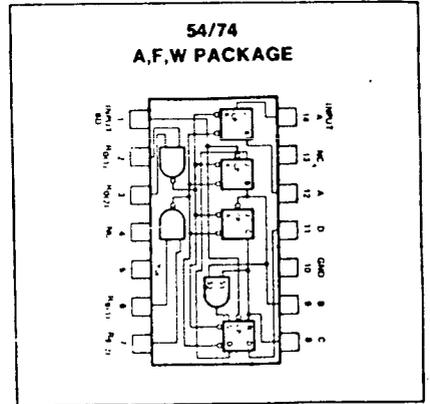
PARAMETER MEASUREMENT INFORMATION
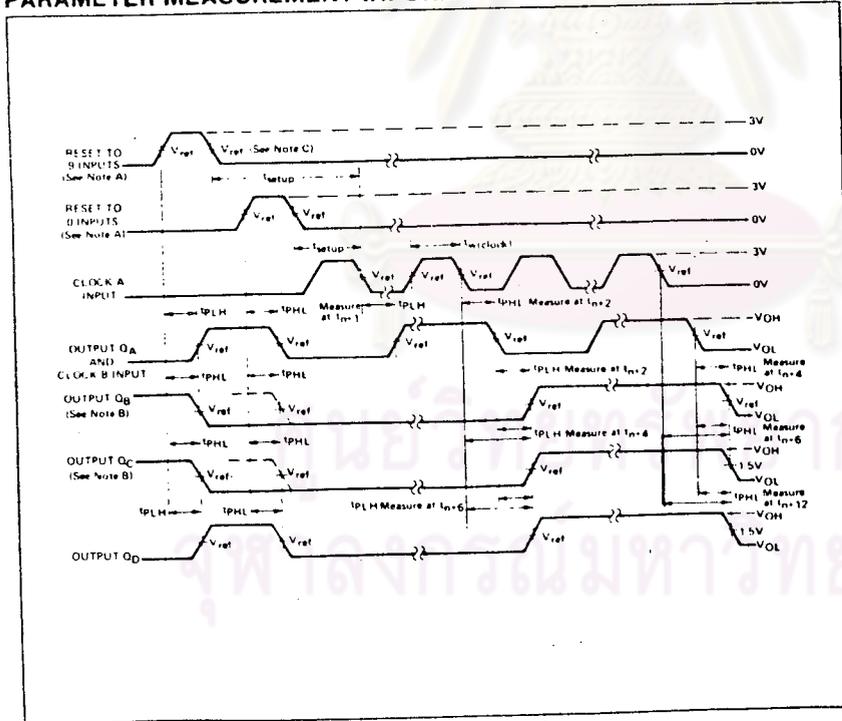
VOLTAGE WAVEFORMS

A. Each reset input is tested separately with the other reset at 4.5 V.
B. Reference waveforms are shown with dashed lines.
C. $V_{ref} = 1.3$ V
Load circuit is shown at front of section (for totem pole outputs).

DECADE COUNTER   54/7490

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS			54/74 C_L = 15pF R_L 400Ω			54/74LS C_L = 15pF R_L 2kΩ			
PARAMETER	**FROM INPUT**	**TO OUTPUT**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNIT**
f_{Count} Count frequency			10	18					MHz
	A	Q_A				32	42		
	B	Q_B				16			
$t_{w(Clock)}$ Width of			50						ns
clock pulse	A	Q				15			
	B	Q				30			
	Reset	Q				15			
$t_{w(Reset)}$ Width of			50			25			ns
reset pulse									
Propagation delay time									ns
t_{PLH} Low-to-high	Input Count Pulse	Q_C		60	100				
t_{PHL} High-to-low				60	100				
t_{PLH} Low-to-high	A	Q_A					10	16	
t_{PHL} High-to-low							12	18	
t_{PLH} Low-to-high	A	Q_D					32	48	
t_{PHL} High-to-low							34	50	
t_{PLH} Low-to-high	B	Q_B					10	16	
t_{PHL} High-to-low							14	21	
t_{PLH} Low-to-high	B	Q_C					21	32	
t_{PHL} High-to-low							23	35	
t_{PLH} Low-to-high	B	Q_D					21	32	
t_{PHL} High-to-low							23	35	
t_{PHL} High-to-low	Set-to-0	Any					26	40	
t_{PLH} Low-to-high	Set-to-9	Q_A, Q_D					20	30	
t_{PHL} High-to-low	Set-to-9	Q_B, Q_C					26	40	

Load circuit and typical waveforms shown at front of section .

BCD COUNT SEQUENCE
(See Note A)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

BI-QUINARY (5-2)
(See Note B)

COUNT	OUTPUT			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

RESET/COUNT FUNCTION TABLE

RESET INPUTS				OUTPUT			
$R_{0(1)}$	$R_{0(2)}$	$R_{9(1)}$	$R_{9(2)}$	Q_D	Q_C	Q_B	Q_A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	COUNT			
L	X	L	X	COUNT			
L	X	X	L	COUNT			
X	L	L	X	COUNT			

NOTES:
A. Output Q_A is connected to input B for BCD count.
B. Output Q_D is connected to input A for bi-quinary count.
C. Output Q_A is connected to input B.
D. H = high level, L = low level, X = irrelevant

MONOSTABLE MULTIVIBRATOR   54/74121

SPEED/PACKAGE AVAILABILITY
54   F,W   74   A,F

THRESHOLD VOLTAGE V_{CC} = Min

PARAMETER	INPUT	MIN	TYP	MAX	UNIT
V_{T+} Positive Going Threshold	A		1.4	2	V
	B		1.55	2	V
V_{T-} Negative Going Threshold	A	0.8	1.4		V
	B	0.8	1.35		V

PIN CONFIGURATION

A,F,W PACKAGE
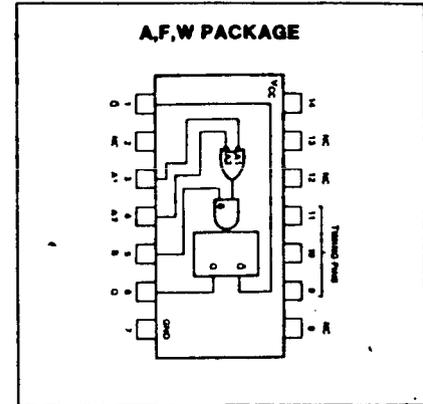
SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS			54/74			
			C_L = 15pF C_T = 80pF			
PARAMETER	FROM INPUT	TO OUTPUT	MIN	TYP	MAX	UNIT
$t_{w(in)}$			50			ns
$t_{w(out)}$			R_T = Open pin 9 to V_{CC}			
			70	110	150	ns
			C_T = 0			
			20	30	50	
			C_T = 100pF R_T = 10kΩ Pin 9 open			
			600	700	800	
			C_T = 1µF			
			6	7	8	ns
t_{Hold} Input hold time			R_T = Open pin 9 to V_{CC}			
				30	50	ns
dv/dt Input slope	B		1			V/s
	A_1,A_2		1			V/µs
R_{ext} External timing resistance			(54) 1.4		30	kΩ
			(74) 1.4		40	
C_{ext} External timing Duty cycle (%)			0		1000	µf
			R_T = 2k			
					67	kΩ
			R_T = Max R_{ext}			
					90	
Propagation delay time						
t_{PLH} Low-to-high	B	Q	15	35	55	ns
t_{PHL} High-to-low	B	Q	20	40	65	
t_{PLH} Low-to-high	A_1,A_2	Q	25	45	70	
t_{PHL} High-to-low	A_1,A_2	Q	30	50	80	
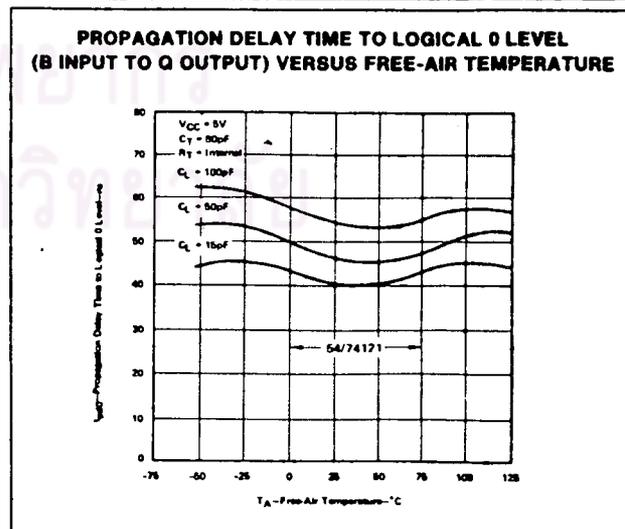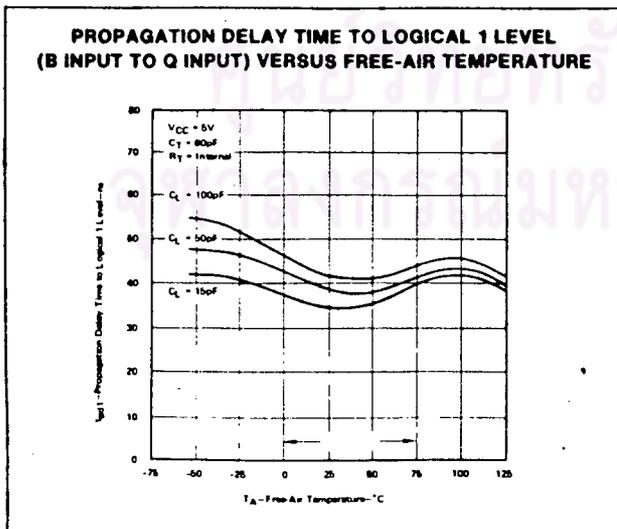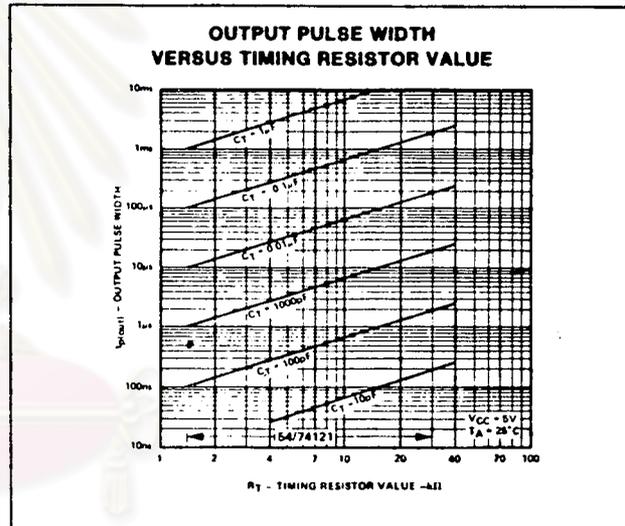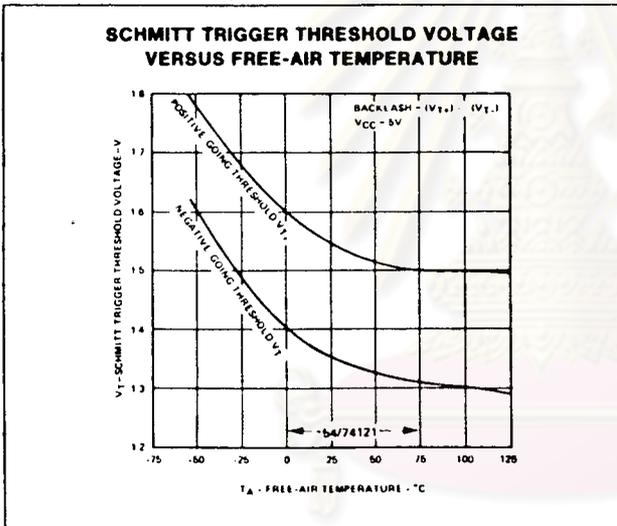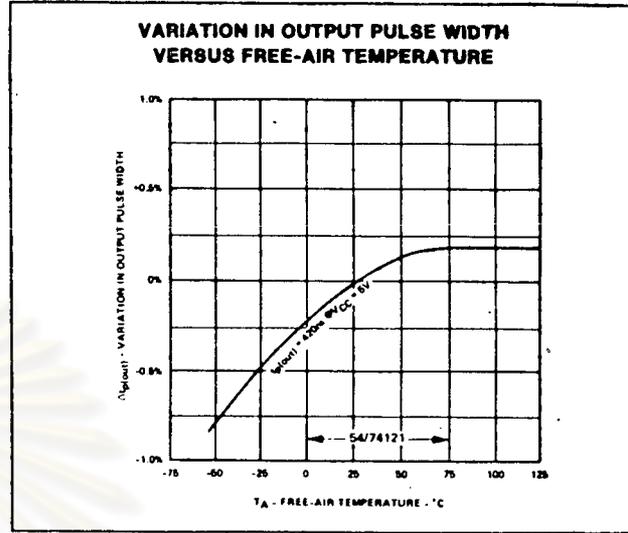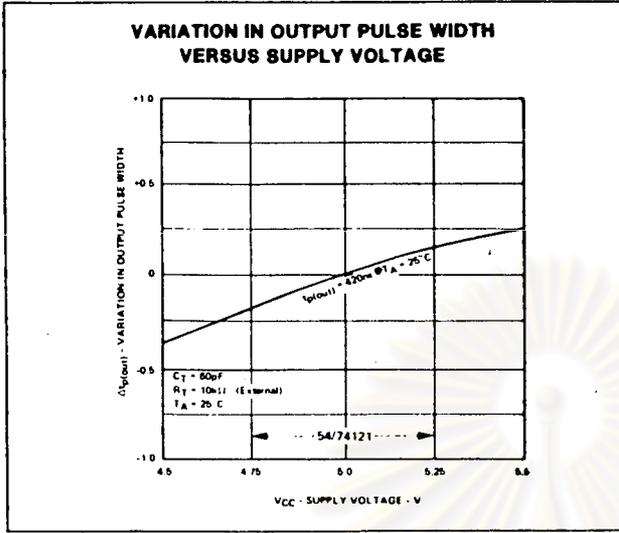
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ข้อมูลทางไฟฟ้าของไอซี เบอร์ 74121

MONOSTABLE MULTIVIBRATOR   54/74121

TYPICAL CHARACTERISTICS

VARIATION IN OUTPUT PULSE WIDTH
VERSUS SUPPLY VOLTAGE

VARIATION IN OUTPUT PULSE WIDTH
VERSUS FREE-AIR TEMPERATURE

SCHMITT TRIGGER THRESHOLD VOLTAGE
VERSUS FREE-AIR TEMPERATURE

OUTPUT PULSE WIDTH
VERSUS TIMING RESISTOR VALUE

PROPAGATION DELAY TIME TO LOGICAL 1 LEVEL
(B INPUT TO Q INPUT) VERSUS FREE-AIR TEMPERATURE

PROPAGATION DELAY TIME TO LOGICAL 0 LEVEL
(B INPUT TO Q OUTPUT) VERSUS FREE-AIR TEMPERATURE

ภาคผนวก(ฉ) ต่อ

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MONOSTABLE MULTIVIBRATOR   54/74121

TYPICAL CHARACTERISTICS, (Continued)

VARIATION IN INTERNAL TIMING RESISTOR VALUE
VERSUS FREE-AIR TEMPERATURE
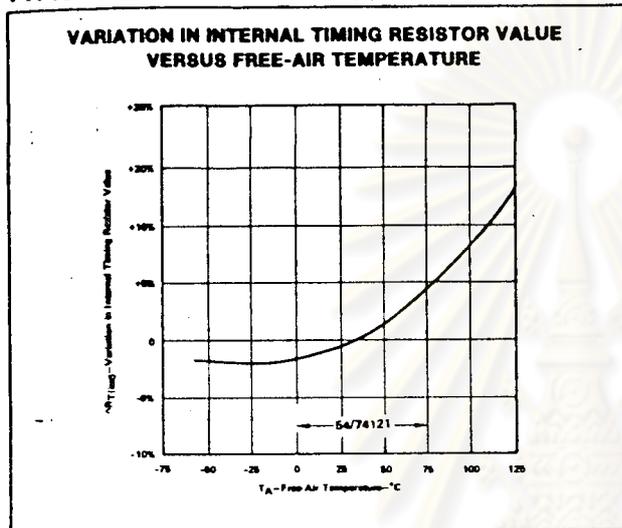
TRUTH TABLE

t_n INPUT			t_n+1 INPUT			OUTPUT
A1	A2	B	A1	A2	B	
1	1	0	1	1	1	Inhibit
0	x	1	0	x	0	Inhibit
x	0	1	x	0	0	Inhibit
0	x	0	0	x	1	One Shot
x	0	0	x	0	1	One Shot
1	1	1	x	0	1	One Shot
1	1	1	0	x	1	One Shot
x	0	0	x	1	0	Inhibit
0	x	0	1	x	0	Inhibit
x	0	1	1	1	1	Inhibit
0	x	1	1	1	1	Inhibit
1	1	0	x	0	0	Inhibit
1	1	0	0	x	0	Inhibit

$1 - V_{in(1)} \geq 2V$ $0 - V_{in(0)} \leq 0.8V$

1. A1 and A2 are negative-edge-triggered logic inputs, and will trigger the one shot when either or both go to logical 0 with B at logical 1.
2. B is a positive Schmitt-trigger input for slow edges or level detection, and will trigger the one shot when B goes to logical 1 with either A1 or A2 at logical 0 (See Truth Table)
3. External timing capacitor may be connected between pin (positive) and pin   With no external capacitance, an output pulse width of 30ns is obtained typically.
4. To use the internal timing resistor (2kΩ nominal), connect pin   to pin
5. To obtain variable pulse width connect external variable resistance between pin   and pin . No external current limiting is needed.
6. For accurate repeatable pulse widths connect an external resistor between pin   and pin   with pin   open-circuit.
7. t_n – time before input transition.
8. t_n+1 – time after input transition.
9. x indicates that either a logical 0 or 1, may be present.

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SYNCHRONOUS 4-BIT BINARY COUNTER 54/74161

SPEED/PACKAGE AVAILABILITY

54	F,W	74	B,F
54LS	F,W	74LS	B,F
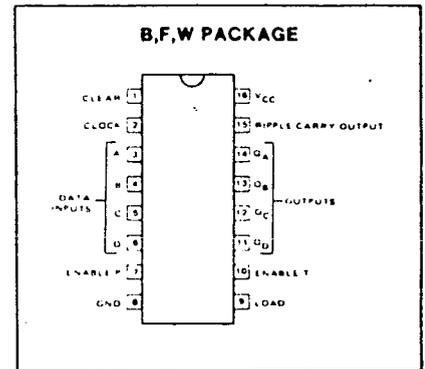
DESCRIPTION

This synchronous presettable binary counter features an internal carry look-ahead for applications in high-speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform.

This counter is fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the.

levels of the enable inputs. The clear function for the 54/74LS161 is asynchronous and a low level at the clear input sets all four of the flip-flop outputs low regardless of the levels of clock, load or enable inputs.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output. Both count-enable inputs (P and T) must be high to count, and input T is fed forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high-level output pulse with a duration approximately equal to the high-level portion of the Q_A output. This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. Transitions at the enable P or T inputs are allowed regardless of the level of the clock input.

The 54/74LS161 features a fully independent clock circuit. Changes made to control inputs (enable P or T, load or clear) that will modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

PIN CONFIGURATION

B,F,W PACKAGE

ภาคผนวก(ช)   ต่อ

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BLOCK DIAGRAMS
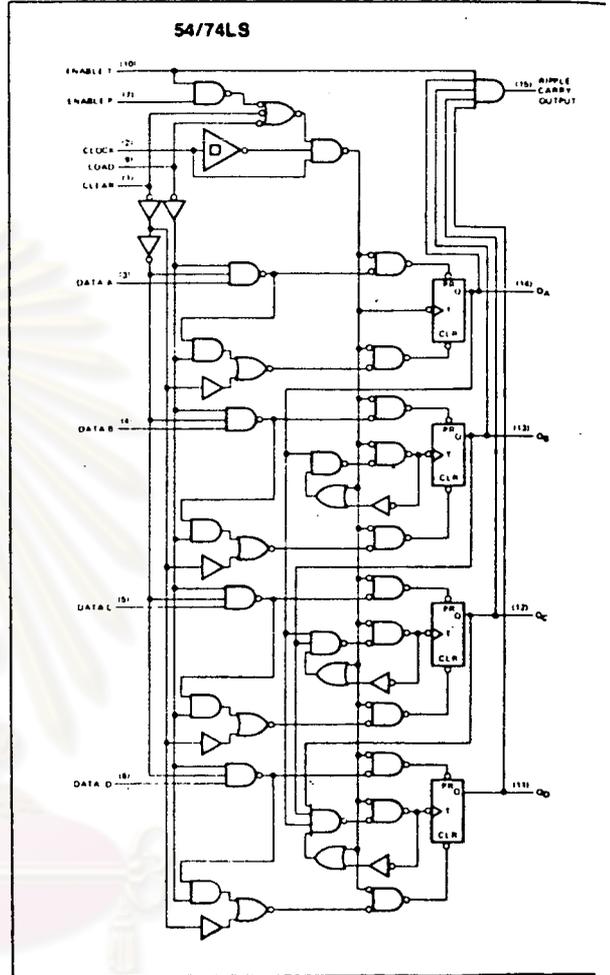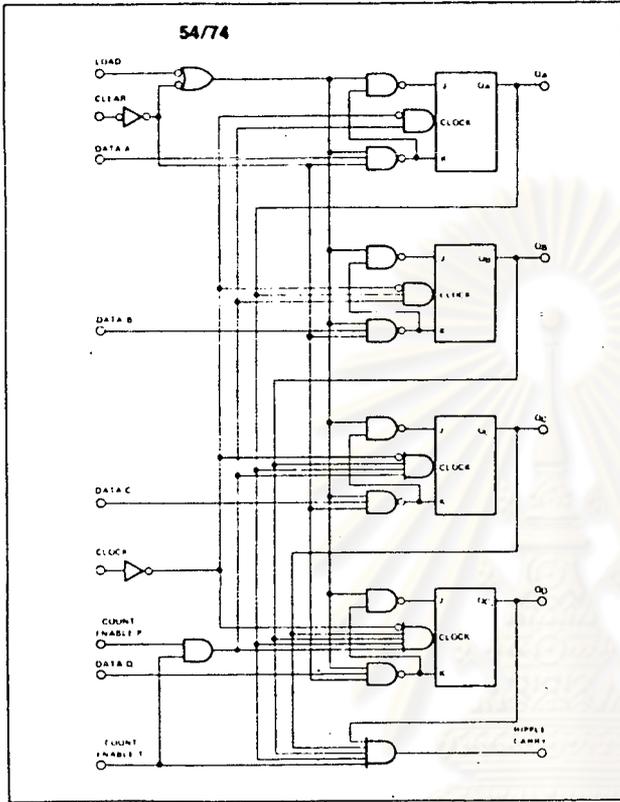
SYNCHRONOUS 4-BIT BINARY COUNTER 54/74161

PARAMETER MEASUREMENT INFORMATION

TYPICAL CLEAR, PRESET, COUNT, AND INHIBIT SEQUENCES

Illustrated below is the following sequence:

1. Clear outputs to zero
2. Preset to binary twelve
3. Count to thirteen, fourteen, fifteen, zero, one, and two
4. Inhibit
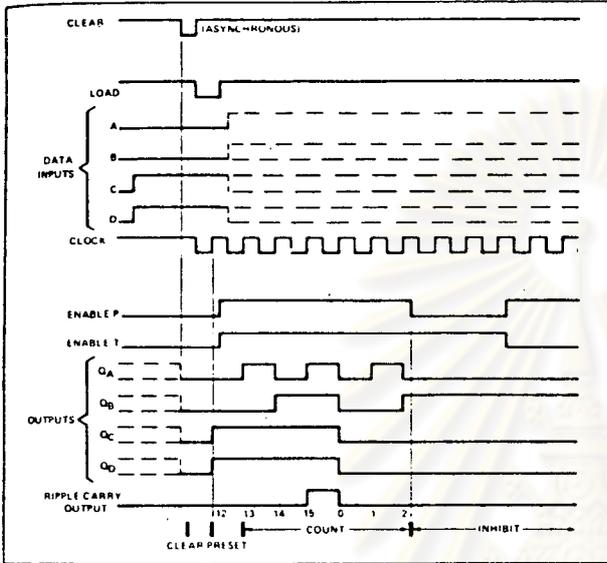
NOTES

A. The input pulses are supplied by a generator having the following characteristics. PRR ≤ 1MHz, Duty Cycle ≤ 50%. $Z_{out} = 50\Omega$, $t_r \leq 15ns$, $t_f \leq 6ns$

B. Outputs Q_D and carry are tested at t_{n+16}, where t_n is the bit time when all outputs are low.

C. $V_{ref} = 1.3V$.
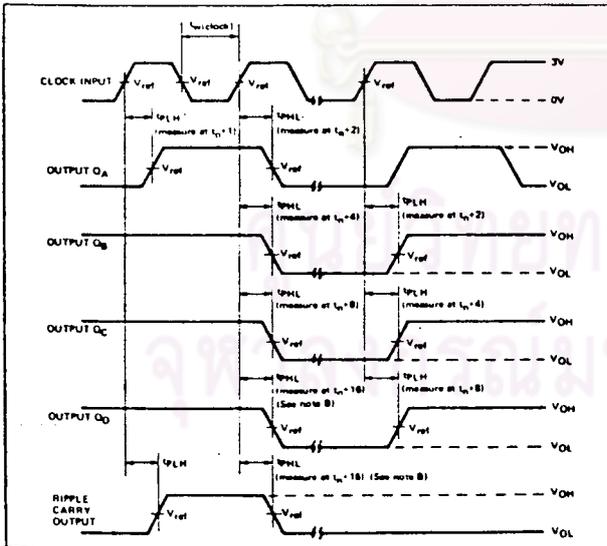
FIGURE 1—VOLTAGE WAVEFORMS
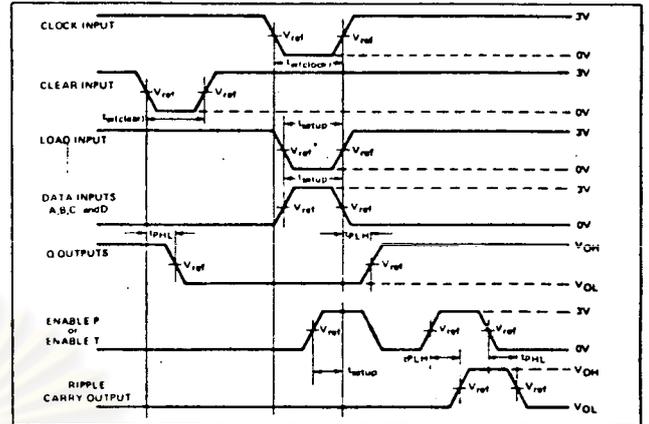
FIGURE 2—VOLTAGE WAVEFORMS

NOTES

A. The input pulses are supplied by generators having the following characteristics:
PRR ≤ 1MHz, Duty cycle ≤ 50%. $Z_{out} = 50\Omega$, $t_r \leq 15ns$, $t_f \leq 6ns$.

B. Enable P and T setup times are measured at t_{n+0}.

C. $V_{ref} = 1.3V$.

Load circuit is shown at front of book (totem pole output).

TYPICAL APPLICATION DATA

N-BIT SYNCHRONOUS COUNTERS

This application demonstrates how the look-ahead carry circuit can be used to implement a high-speed n-bit counter. The 54/74LS161 will count in binary. Virtually any count mode (modulo-N, N_1-toN_2, N_1-to-maximum) can be used with this fast look-ahead circuit.

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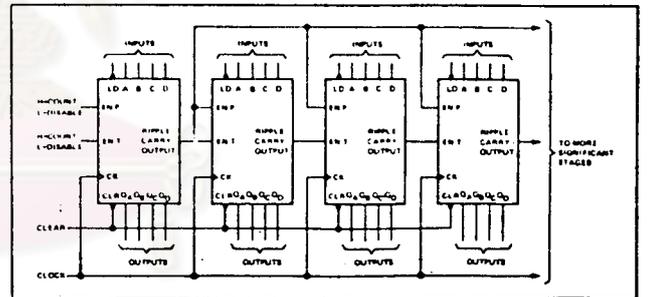
ข้อมูลทางไฟฟ้าของไอซี   เบอร์ 74161

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS			54/74 C_L = 15pF R_L = 400Ω			54/74LS C_L = 15pF R_L = 2kΩ			
PARAMETER	FROM INPUT	TO OUTPUT	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
f_{Clock} Clock frequency			25	32		25	32		MHz
t_W (Clock) Width of clock input pulse			25			25			ns
t_W (Clear) Width of clear input pulse			20			20			ns
t_{Setup} Input setup time	$D_A - D_D$		15						ns
	Enable P		26						
	Load		25						
	A,B,C,D	Q				0↑			
	Enable P, Enable T	Q				20↑			
	Load	Q				20↑			
t_{Hold} Input hold time	Any		0						ns
	A,B,C,D					25↑			
	Others					10↑			
Propagation delay time									
t_{PLH} Low-to-high	Clock	Carry		23	35		23	35	ns
t_{PHL} High-to-low				23	35		23	35	
t_{PLH} Low-to-high	Clock	Q (load input high)		13	20		16	24	
t_{PHL} High-to-low				15	23		18	27	
t_{PLH} Low-to-high	Clock	Q (load input low)		17	25		17	25	
t_{PHL} High-to-low				19	29		19	29	
t_{PLH} Low-to-high	Enable T	Carry		10	14		15	23	
t_{PHL} High-to-low				10	14		15	23	
t_{PHL} High-to-low	Clear	Q		20	30		26	38	

Load circuit and typical waveforms shown at the front of section.

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ภาคผนวก (ช)

ข้อมูลทางไฟฟ้าของไอซี เบอร์ CD4066B

SCL4066B

CMOS QUAD ANALOG SWITCH

FEATURES

- Transmission or Multiplexing of Analog or Digital Signals
- 80Ω Typical ON-Resistance for 15-Volt operation
- Switch ON-Resistance Matched to within 5Ω over 15-Volt Signal-Input Range
- ON-Resistance Flat over Full Peak-to-Peak Signal Range
- High Degree of Linearity:
  $\leq 0.5\%$ Distortion (typ) @ f_{is} = 1kHz,
  V_{is} = 5V_{p-p}, V_{DD}-V_{SS} $\geq$ 10V, R_L = 10kΩ
- Extremely Low OFF switch Leakage Resulting in very Low Offset Current and High Effective OFF Resistance:
  10pA (typ) @ V_{DD}-V_{SS} = 10V, T_A = 25°C
- Extremely High Control Input Impedance (Control Circuit Isolated from Signal Circuit):
  $10^{12}\Omega$ (typ)
- Low Crosstalk between Switches:
  -50dB (typ) @ f_{is} = 0.9MHz, R_L = 1kΩ
- Matched Control-Input to Signal-Output Capacitance Reduces Output Signal Transients
- Frequency Response, Switch ON = 40MHz (typ)

DESCRIPTION

The SCL4066B is a Quad Bilateral Switch intended for the transmission or multiplexing of analog or digital signals. It is pin-for-pin compatible with the SCL4016B, but exhibits a much lower ON-resistance. In addition, the ON-resistance is relatively constant over the full input signal range. The SCL4066 consists of four independent bilateral switches. A single control signal is required per switch. Both the P and the N device in a given switch are biased ON or OFF simultaneously by the control signal. As shown below, the well of the N-channel device on each switch is either tied to the input when the switch is ON or to V_{SS} when the switch is OFF. This configuration minimizes the variation of the switch-transistor threshold

CONNECTION DIAGRAM (all packages)

Add suffix for package:

C	14-pin Cerdip	F	14-pin Flat
D	14-pin Ceramic	H	Chip
E	14-pin Epoxy		
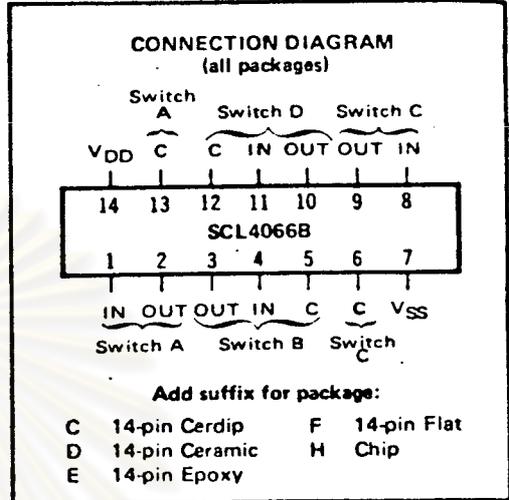
RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage V_{DD} - V_{SS} 3 to 15   Vdc

Operating Temperature T_A
C, D, F, H Device   -55 to +125 °C
E Device   -40 to +85 °C

voltage with input-signal, and thus keeps the ON-resistance low over the full operating range.

The advantages over single-channel switches include peak input-signal voltage swings equal to the full supply voltage, and more constant ON-impedance over the input-signal range. For sample-and-hold applications, however, the SCL4016 is recommended.

SCHEMATIC DIAGRAM (one of four switches)
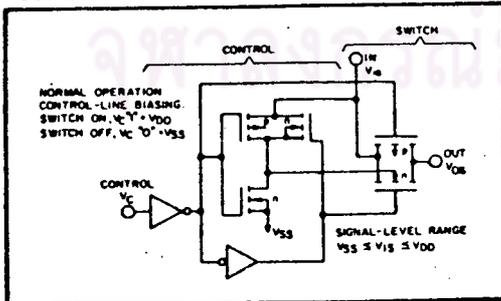
LOGIC DIAGRAM
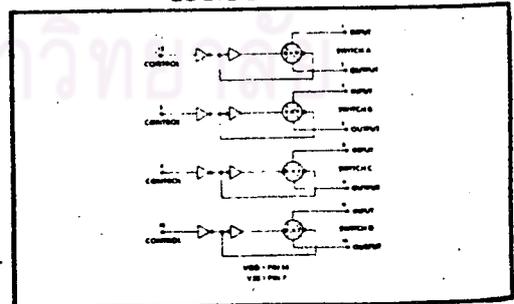
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ข้อมูลทางไฟฟ้าของไอซี   เบอร์ CD4066B

ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS [1,3]

PARAMETER		CONDITIONS	V_{SS} (Vdc)	V_{DD} (Vdc)	T_{LOW}[2]		25°C			T_{HIGH}[2]		Units
					Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I_{DD}	$V_{IN} = V_{SS}$ or V_{DD} All valid input combinations	0	5	—	0.05	—	0.0005	0.05	—	1.5	μAdc
			0	10	—	0.1	—	0.001	0.1	—	3.0	
			0	15	—	0.2	—	0.002	0.2	—	6.0	
MINIMUM INPUT HIGH VOLTAGE (Control Input)	V_{IH}	$V_{IS} = V_{SS}$	0	5	—	4.0	—	2.75	4.0	—	4.0	Vdc
		$V_{OS} = V_{DD}$	0	10	—	8.0	—	5.5	8.0	—	8.0	
		$I_{OS} = 10\mu A$	0	15	—	12.0	—	8.25	12.0	—	12.0	
MAXIMUM INPUT LOW VOLTAGE (Control Input)	V_{IL}	$V_{IS} = V_{SS}$	0	5	1.0	—	1.0	2.25	—	1.0	—	Vdc
		$V_{OS} = V_{DD}$	0	10	2.0	—	2.0	4.5	—	2.0	—	
		$I_{OS} = 10\mu A$	0	15	3.0	—	3.0	6.75	—	3.0	—	
SWITCH INPUT/OUTPUT LEAKAGE	I_{OFF}	$V_C = V_{SS}$ $V_{IS} = \pm 7.5 Vdc$	-7.5	+7.5	—	±100	—	±0.01	±100	—	±200	nAdc
ON RESISTANCE C,D,F,H device	R_{ON}	$V_C = V_{DD}$ $V_{SS} < V_{IS} < V_{DD}$ $R_L = 10k\Omega$	-7.5 0	+7.5 +15	—	220	—	80	280	—	320	Ω
			-5 0	+5 +10	—	310	—	120	400	—	650	Ω
			-2.5 0	+2.5 +5	—	2000	—	270	2500	—	3500	Ω
E device	R_{ON}	$V_C = V_{DD}$ $V_{SS} < V_{IS} < V_{DD}$ $R_L = 10k\Omega$	-7.5 0	+7.5 +15	—	250	—	80	280	—	300	Ω
			-5 0	+5 +10	—	330	—	120	400	—	620	Ω
			-2.5 0	+2.5 +5	—	2100	—	270	2500	—	3200	Ω
ON-RESISTANCE MATCH (Same package)	ΔR_{ON}	$V_C = V_{DD}$ $V_{SS} < V_{IS} < V_{DD}$ $R_L = 10k\Omega$	-7.5 0	+7.5 +15	—	—	—	5	—	—	—	Ω
			-5 0	+5 +10	—	—	—	10	—	—	—	Ω
			-2.5 0	+2.5 +5	—	—	—	10	—	—	—	Ω

NOTES: [1] Remaining Static Electrical Characteristics are listed under "SCL4000B Series Family Specifications".
[2] T_{LOW} = -55°C for C, D, F, H device.
= -40°C for E device.
T_{HIGH} = +125°C for C, D, F, H device.
= + 85°C for E device.
[3] This device has been designed for balanced output drive current specifications. Consult Family Specifications.

ภาคผนวก (ข)   ต่อ

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ELECTRICAL CHARACTERISTICS (Continued)

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		CONDITIONS		V_{SS} (Vdc)	V_{DD} (Vdc)	Min.	Typ.	Max.	Units
SIGNAL INPUTS (V_{is}) AND OUTPUTS (V_{os})									
PROPAGATION DELAY TIME	t_{PLH}, t_{PHL}	$V_c=V_{DD}$ V_{is}=Square Wave R_L = 10kΩ		0	5	—	20	40	ns
Signal Input to Signal Output				0	10	—	10	20	
				0	15	—	7.5	15	
BANDWIDTH (-3dB)	BW	$V_c=V_{DD}$ $V_{is}=5V_{p-p}$ centered @ 0.0Vdc	R_L						MHz
(Sine Wave)			1kΩ	-5	+5	—	54	—	
			10kΩ			—	40	—	
			100kΩ			—	38	—	
			1MΩ			—	37	—	
INSERTION LOSS $(=20 \log_{10} \frac{V_{os}}{V_{is}})$		$V_c=V_{DD}$ $V_{is}=5V_{p-p}$ centered @ 0.0Vdc	R_L						dB
			1kΩ	-5	+5	—	2.3	—	
			10kΩ			—	0.2	—	
			100kΩ			—	0.1	—	
			1MΩ			—	0.05	—	
SIGNAL DISTORTION (Sine Wave)		$V_c=V_{DD}$ $V_{is}=5V_{p-p}$ centered @ 0.0Vdc $f_{is}=1.0$kHz R_L = 10kΩ		-5	+5	—	0.16	—	%
FEEDTHROUGH (-50dB)		$V_c=V_{SS}$ $V_{is}=5V_{p-p}$ centered @0.0Vdc	R_L						kHz
			1kΩ	-5	+5	—	1250	—	
			10kΩ			—	140	—	
			100kΩ			—	18	—	
			1MΩ			—	2	—	
CROSSTALK (-50dB) Between two switches		$V_c(A)=V_{DD}$ $V_c(B)=V_{SS}$ $V_{is}(A)=5V_{p-p}$ centered @ 0.0Vdc R_L = 10kΩ		-5	+5	—	0.9	—	MHz
CAPACITANCE									
Input	C_{is}					—	8	—	pF
Output	C_{os}	$V_C = V_{SS}$		-5	+5	—	8	—	pF
Feedthrough	C_{ios}					—	0.5	—	pF
CONTROL INPUT (V_C)									
PROPAGATION DELAY TIME Turn on	t_{PC}	$V_{SS}<V_{is}<V_{DD}$ R_L = 10kΩ		0	5	—	50	100	ns
				0	10	—	25	50	
				0	15	—	20	40	
MAXIMUM INPUT FREQUENCY	f_c	$V_{SS}<V_{is}<V_{DD}$ R_L = 1.0kΩ		0	5	—	5	—	MHz
				0	10	—	10	—	
				0	15	—	12	—	
CROSSTALK (To signal port)		V_c=Square Wave R_L = 10kΩ R_{in} = 1.0kΩ		0	5	—	30	—	mV
				0	10	—	50	—	
				0	15	—	100	—	

ภาคผนวก(ช)   ต่อ

ข้อมูลทางไฟฟ้าของไอซี   เบอร์ CD4066B

Typical channel ON resistance vs. signal voltage for three values of supply voltage (V$_{DD}$-V$_{SS}$)
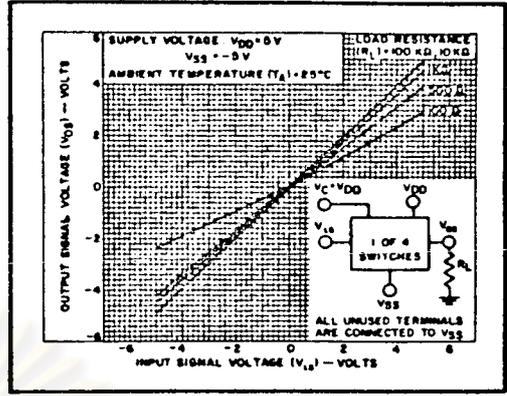
Typical ON characteristics for 1 of 4 channels.
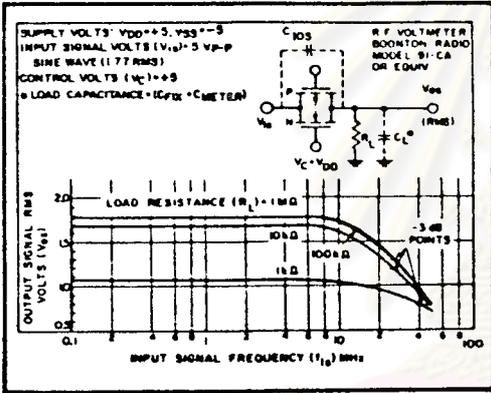
Typ. switch frequency response - switch "ON"
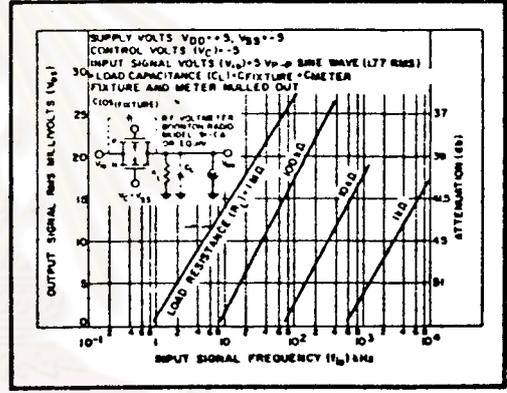
Typ. feedthru vs. freq. — switch "OFF"
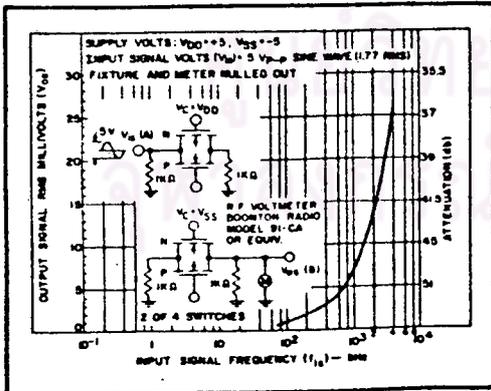
Typ. crosstalk between switch circuits in the same package
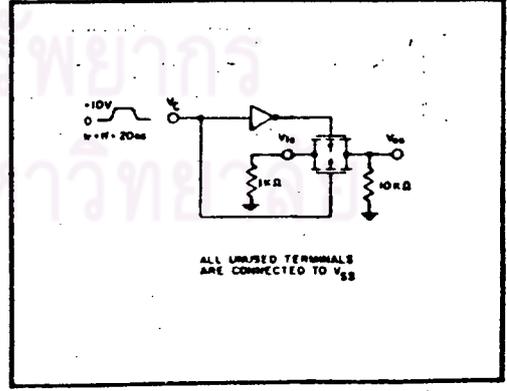
Test circuit, crosstalk-control input to signal output

ภาคผนวก(ฃ) ต่อ

ข้อมูลทางไฟฟ้าของไอซี เบอร์ CD4066B

SPECIAL CONSIDERATIONS – SCL4066B

1. In applications where separate power sources are used to drive V_{DD} and the signal inputs, the V_{DD} current capability should exceed V_{DD}/R_L (R_L = effective external load of the 4 SCL4066B bilateral switches). This provision avoids any permanent current flow or clamp action on the V_{DD} supply when power is applied or removed from SCL4066B.

2. In certain applications, the external load-resistor current may include both V_{DD} and signal-line components. To avoid drawing V_{DD} current when switch current flows into terminals 1, 4, 8, or 11, the voltage drop across the bidirectional switch must not exceed 0.8 volt (calculated from R_{ON} values shown).
   No V_{DD} current will flow through R_L if the switch current flows into terminals 2, 3, 9, or 10. Failure to observe this condition may result in distortion of the signal.

APPLICATIONS INFORMATION
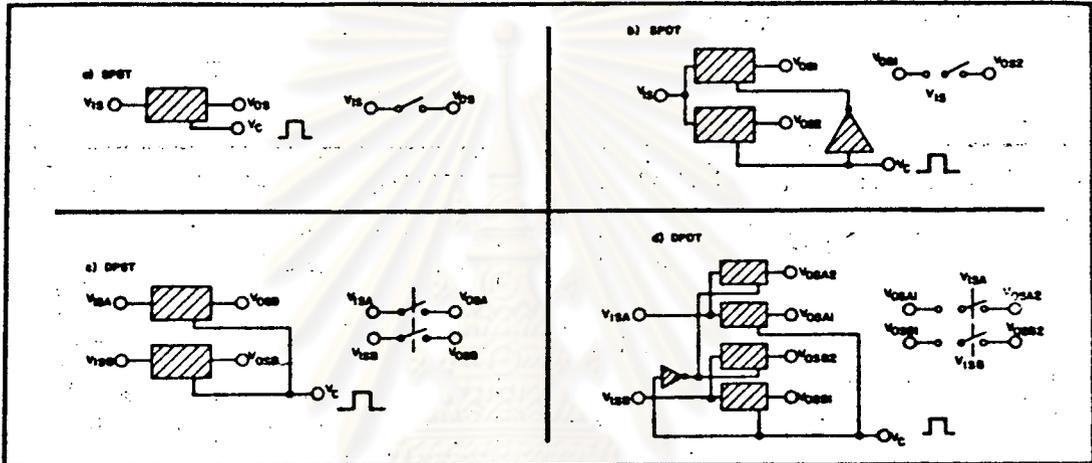
Basic Switch Functions using the SCL4066B
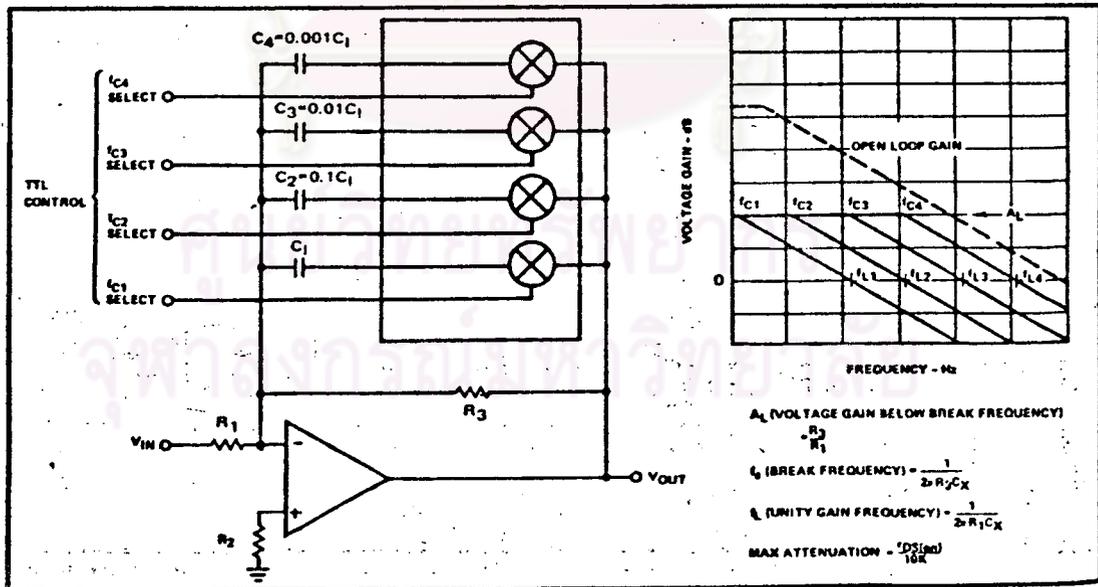
Active Low Pass Filter with Digitally Selected Break Frequency

ภาคผนวก (ฌ)

ข้อมูลทางไฟฟ้าของไอซี เบอร์ LF351

LF351

![National Semiconductor logo] National Semiconductor

Operational Amplifiers/Buffers

BI-FET II™ Technology

3

LF351 Wide Bandwidth JFET Input Operational Amplifier
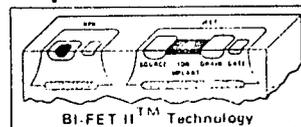
General Description

The LF351 is a low cost high speed JFET input operational amplifier with an internally trimmed input offset voltage (BI-FET II™ technology). The device requires a low supply current and yet maintains a large gain bandwidth product and a fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF351 is pin compatible with the standard LM741 and uses the same offset voltage adjustment circuitry. This feature allows designers to immediately upgrade the overall performance of existing LM741 designs.

The LF351 may be used in applications such as high speed integrators, fast D/A converters, sample-and-hold circuits and many other circuits requiring low input offset voltage, low input bias current, high input impedance, high slew rate and wide bandwidth. The device has low noise and offset voltage drift, but for applica-

tions where these requirements are critical, the LF356 is recommended. If maximum supply current is important, however, the LF351 is the better choice.

Features

- Internally trimmed offset voltage   10 mV
- Low input bias current   50 pA
- Low input noise voltage   16 nV/$\sqrt{Hz}$
- Low input noise current   0.01 pA/$\sqrt{Hz}$
- Wide gain bandwidth   4 MHz
- High slew rate   13 V/μs
- Low supply current   1.8 mA
- High input impedance $10^{12}\Omega$
- Low total harmonic distortion $A_V = 10$,   <0.02%
  $R_L = 10k$, $V_O = 20$ Vp-p, BW = 20 Hz-20 kHz
- Low 1/f noise corner   50 Hz
- Fast settling time to 0.01%   2 μs

Typical Connection
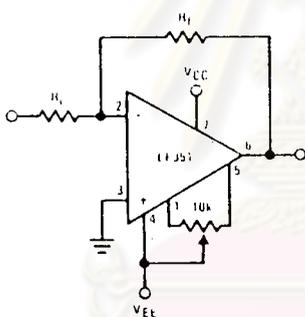
Simplified Schematic
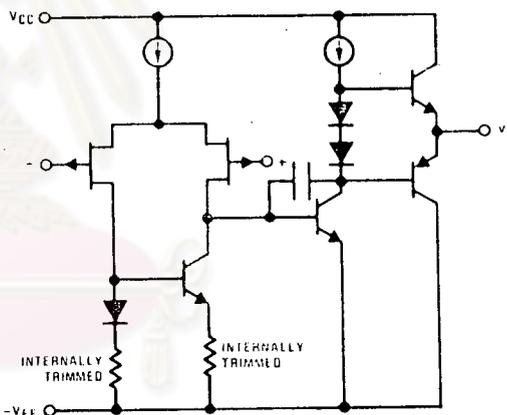
Connection Diagrams (Top Views)

Metal Can Package

Note: Pin 4 connected to case
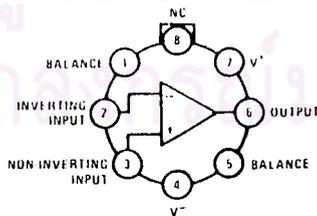
Order Number LF351H
See NS Package H08C

Dual-In-Line Package

TOP VIEW
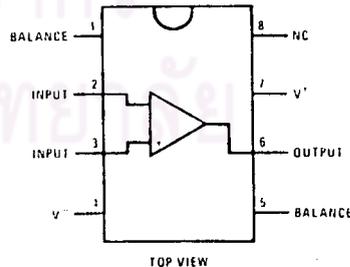
Order Number LF351N
See NS Package N08A

ภาคผนวก (ฌ)   ต่อ

ข้อมูลทางไฟฟ้าของไอซี   เบอร์ LF351

LF351

Absolute Maximum Ratings

Supply Voltage	± 18V
Power Dissipation (Note 1)	500 mW
Operating Temperature Range	0°C to +70°C
T_j(MAX)	115°C
Differential Input Voltage	± 30V
Input Voltage Range (Note 2)	± 15V
Output Short Circuit Duration	Continuous
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics (Note 3)

SYMBOL	PARAMETER	CONDITIONS	LF351			UNITS
			MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	$R_S = 10 k\Omega$, $T_A = 25°C$		5	10	mV
		Over Temperature			13	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	$R_S = 10 k\Omega$		10		µV/°C
I_{OS}	Input Offset Current	$T_j = 25°$		25	100	pA
		$T_j \leq 70°C$			4	nA
I_B	Input Bias Current	$T_j = 25°C$, (Notes 3		50	200	pA
		$T_j \leq 70°C$			8	nA
R_{IN}	Input Resistance	$T_j = 25°C$		10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	$V_S = \pm 15V$, $T_A = 25°C$ $V_O = \pm 10V$, $R_L = 2 k\Omega$	25	100		V/mV
		Over Temperature	15			V/mV
V_O	Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10 k\Omega$	± 12	± 13.5		V
V_{CM}	Input Common-Mode Voltage Range	$V_S = \pm 15V$	± 11	+ 15 − 12		V V
CMRR	Common Mode Rejection Ratio	$R_S \leq 10 k\Omega$	70	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 5)	70	100		dB
I_S	Supply Current			1.8	3.4	mA

AC Electrical Characteristics (Note 3)

SYMBOL	PARAMETER	CONDITIONS	LF351			UNITS
			MIN	TYP	MAX	
SR	Slew Rate	$V_S = \pm 15V$, $T_A = 25°C$		13		V/µs
GBW	Gain Bandwidth Product	$V_S = \pm 15V$, $T_A = 25°C$		4		MHz
e_n	Equivalent Input Noise Voltage	$T_A = 25°C$, $R_S = 100\Omega$, f = 1000 Hz		16		nV/$\sqrt{Hz}$
i_n	Equivalent Input Noise Current	$T_j = 25°C$, f = 1000 Hz		0.01		pA/$\sqrt{Hz}$

Note 1: For operating at elevated temperature, the device must be derated based on a thermal resistance of 150°C/W junction to ambient or 45°C/W junction to case.
Note 2: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.
Note 3: These specifications apply for $V_S = \pm 15V$ and $0°C \leq T_A \leq +70°C$. V_{OS}, I_B and I_{OS} are measured at $V_{CM} = 0$.
Note 4: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to the limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_j = T_A + \Theta_{jA} P_D$ where Θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.
Note 5.: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice.

ภาคผนวก (ฌ)　ต่อ

ข้อมูลทางไฟฟ้าของไอซี　เบอร์ LF351

Typical Performance Characteristics

LF351

Input Bias Current

Input Bias Current

Supply Current

Positive Common-Mode Input Voltage Limit

Negative Common-Mode Input Voltage Limit

Positive Current Limit

Negative Current Limit

Voltage Swing

Output Voltage Swing

Gain Bandwidth

Bode Plot

Slew Rate

ภาคผนวก(ฌ) ต่อ

ข้อมูลทางไฟฟ้าของไอซี เบอร์ LF351

LF351

Typical Performance Characteristics (Continued)

Distortion vs Frequency

Undistorted Output Voltage Swing

Open Loop Frequency Response

Common-Mode Rejection Ratio

Power Supply Rejection Ratio

Equivalent Input Noise Voltage

Open Loop Voltage Gain (V/V)

Output Impedance

Inverter Settling Time
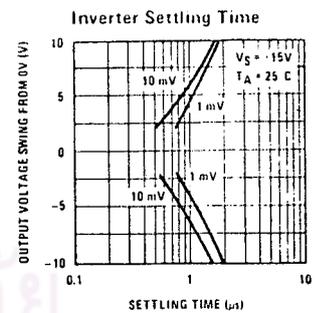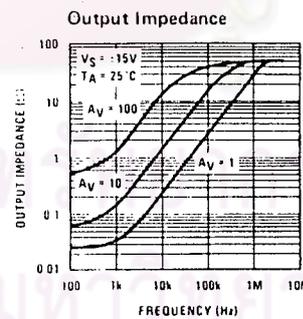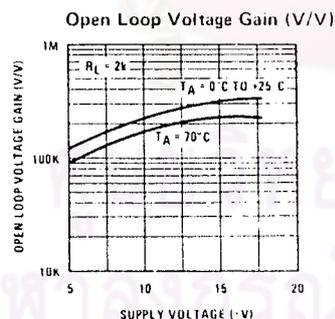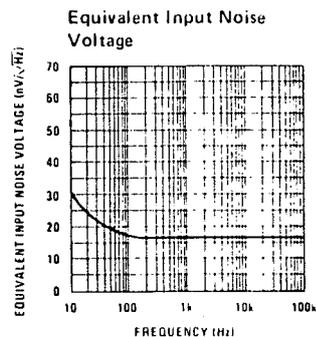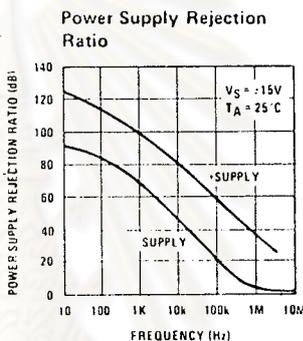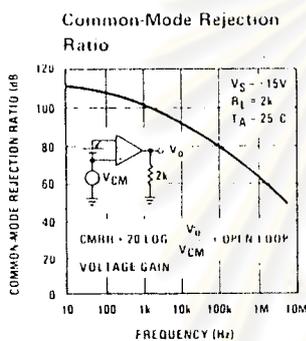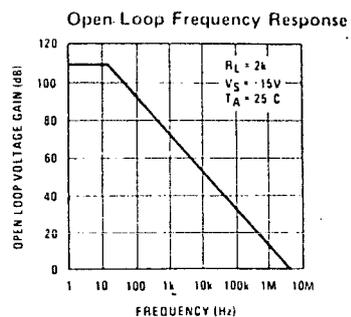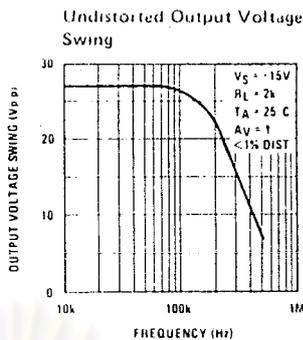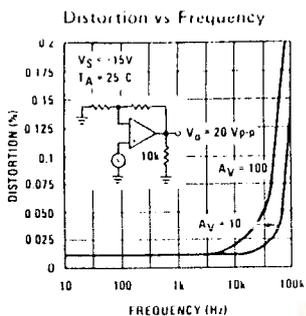
ภาคผนวก (ญ)

ของมูลทางไฟฟ้าของไอซี เบอร์ LM380

LM380 audio power amplifier
general description

The LM380 is a power audio amplifier for con-
sumer application. In order to hold system cost to
a minimum, gain is internally fixed at 34 dB. A
unique input stage allows inputs to be ground
referenced. The output is automatically self ent-
ering to one half the supply voltage.

The output is short circuit proof with internal
thermal limiting. The package outline is standard
dual-in-line. A copper lead frame is used with the
center three pins on either side comprising a heat
sink. This makes the device easy to use in standard
p-c layout.

Uses include simple phonograph amplifiers, inter-
coms, line drivers, teaching machine outputs,
alarms, ultrasonic drivers, TV sound systems, AM-
FM radio, small servo drivers, power converters,etc.

A selected part for more power on higher supply
voltages is available as the LM384. For more
information see AN-69.

features

- Wide supply voltage range
- Low quiescent power drain
- Voltage gain fixed at 50
- High peak current capability
- Input referenced to GND
- High input impedance
- Low distortion
- Quiescent output voltage is at one-half of the
  supply voltage
- Standard dual-in-line package

block and connection diagrams

Dual-In-Line Package
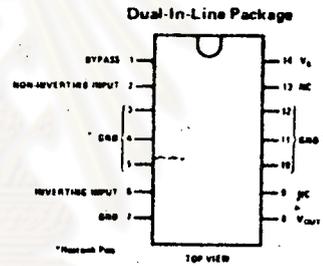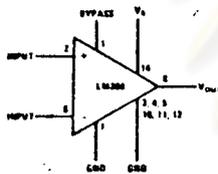
Order Number LM380N
See Package 22

schematic diagram
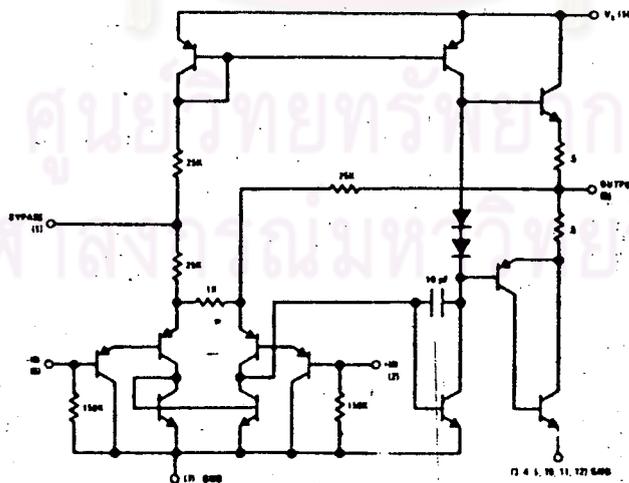
ภาคผนวก (ญ)   ต่อ

ข้อมูลทางไฟฟ้าของไอซี   เบอร์ LM380

typical performance characteristics

Device Dissipation vs Ambient Temperature

Device Dissipation vs Output Power — 4Ω Load

Device Dissipation vs Output Power — 8Ω Load

Device Dissipation vs Output Power — 16Ω Load

Power Supply Current vs Supply Voltage

Total Harmonic Distortion vs Frequency

Output Voltage Gain and Phase vs Frequency

Total Harmonic Distortion vs Output Power

Device Dissipation vs Output Power

Supply Decoupling vs Frequency
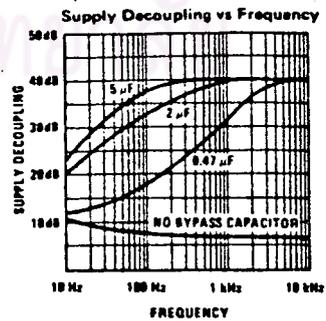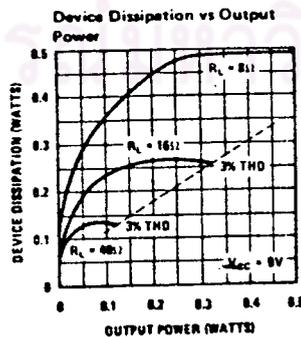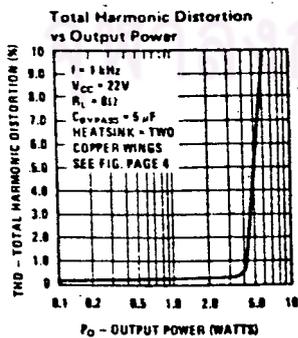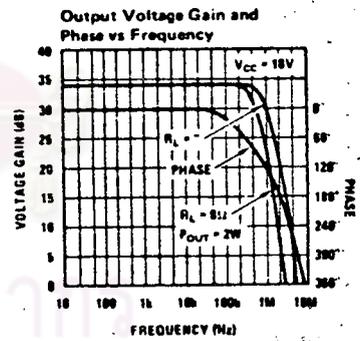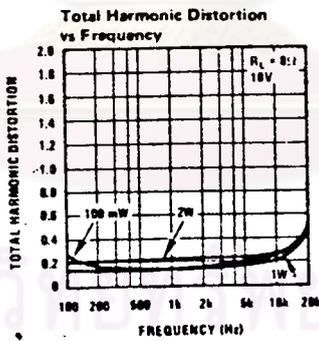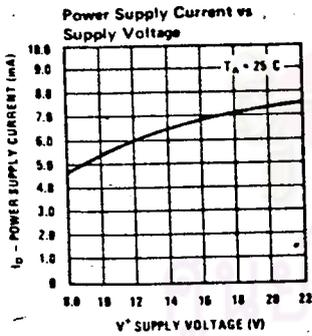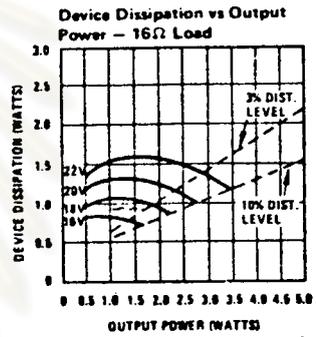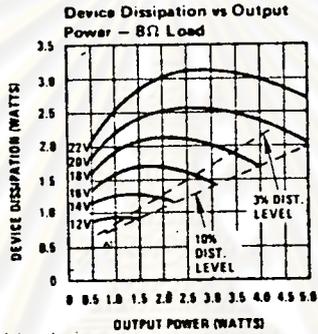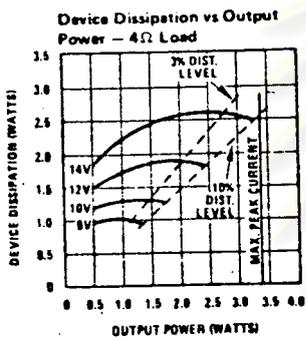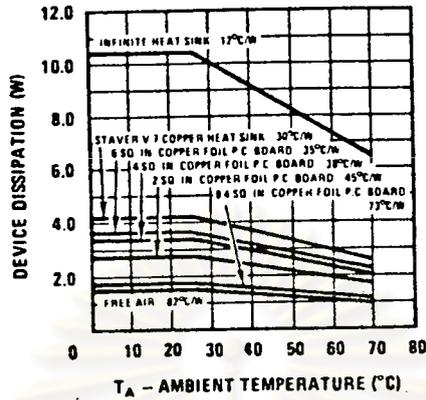
ภาคผนวก (ฏ)

ข้อมูลทางไฟฟ้าของไอซี เบอร์ µA733

DIFFERENTIAL VIDEO AMPLIFIER   µA733

FEATURES
- **120 MHz BANDWIDTH**
- **250kΩ INPUT RESISTANCE**
- **SELECTABLE GAINS OF 10, 100 and 400**
- **NO FREQUENCY COMPENSATION REQUIRED**

ABSOLUTE MAXIMUM RATINGS
Differential Input Voltage	±5V
Common Mode Input Voltage	±6V
V_{CC}	±8V
Output Current	10mA
Junction Temperature	+150°C
Storage Temperature Range	−65°C to +150°C
Operation Temperature Range	
µA733C	0°C to +75°C
µA733	−55°C to +125°C

PIN CONFIGURATION

A, I PACKAGE

ORDER PART NOS
µA733A / µA733I /
µA733CA / µA733CI

K PACKAGE

NOTE Pin 5 connected to case
ORDER PART NOS
µA733K / µA733CK

Thermal Resistance (θ_{JA}, Junction to Ambient for each package):
A Package	0.16°C/mW
I Package	0.10°C/mW
K Package	0.145°C/mW
Power Dissipation	500mW
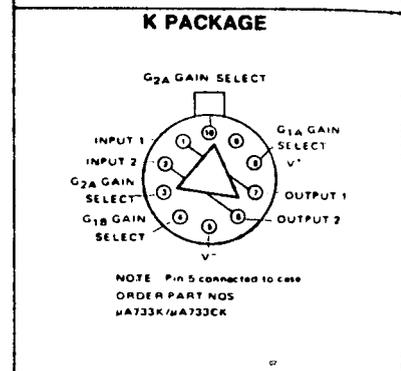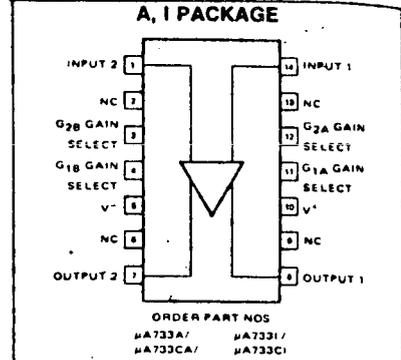
TEST CIRCUITS (T_A = 25°C unless otherwise specified)

CIRCUIT SCHEMATIC

ภาคผนวก (ฎ)   ต่อ
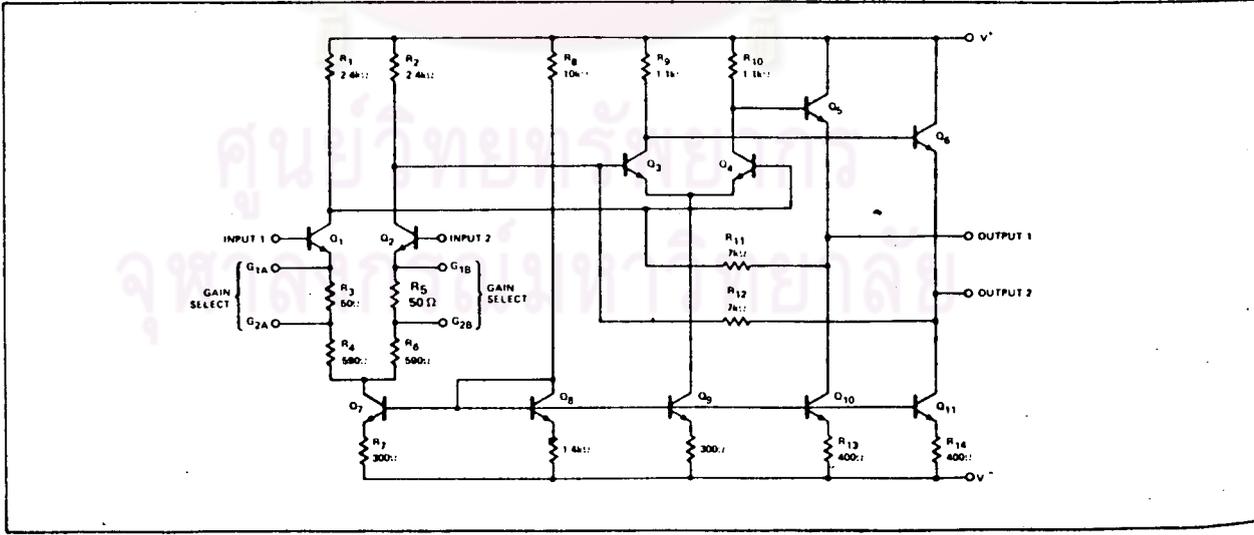
ข้อมูลทางไฟฟ้าของไอซี   เบอร์ μA733

ELECTRICAL CHARACTERISTICS
Standard Conditions (T_A = +25°C, V_S = ±V, V_{CM} = 0 unless otherwise specified)

PARAMETERS	TEST CONDITIONS		μA733C			μA733			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Differential Voltage Gain									
Gain 1		Note 1	250	400	600	300	400	500	
Gain 2	R_l = 2kΩ, V_{out} = 3V p-p	Note 2	80	100	120	90	100	110	
Gain 3		Note 3	8.0	10	12	9.0	10	11	
Bandwidth									
Gain 1		Note 1		40			40		MHz
Gain 2		Note 2		90			90		MHz
Gain 3		Note 3		120			120		MHz
Rise Time									
Gain 1		Note 1		10.5			10.5		ns
Gain 2	V_{out} = 1V p-p	Note 2		4.5	12		4.5	10	ns
Gain 3		Note 3		2.5			2.5		ns
Propagation Delay									
Gain 1		Note 1		7.5			7.5		ns
Gain 2	V_{out} = 1V p-p	Note 2		6.0	10		6.0	10	ns
Gain 3		Note 3		3.6			3.6		ns
Input Resistance									
Gain 1		Note 1		4.0			4.0		kΩ
Gain 2		Note 2	10	30		20	30		kΩ
Gain 3		Note 3		250			250		kΩ
Input Capacitance	Gain 2	Note 2		2.0			2.0		pF
Input Offset Current				0.4	5.0		0.4	3.0	μA
Input Bias Current				9.0	30		9.0	20	μA
Input Noise Voltage	BW = 1k Hz to 10 MHz			12			12		μV_{rms}
Input Voltage Range Common Mode			±1.0			±1.0			V
Rejection Ratio									
Gain 2	V_{CM} = ±V,f≤100 kHz		60	86		60	86		dB
Gain 2	V_{CM} = ±1V, F = 5 MHz			60			60		dB
Supply Voltage Rejection Ratio									
Gain 2	ΔV_S = ±0.5 V		50	70		50	70		dB
Output Offset Voltage									
Gain 1	R_L = ∞	Note 1		0.6	1.5		0.6	1.5	V
Gain 2 and 3		Notes 2,3		0.35	1.5		0.35	1.0	V
Output Common Mode Voltage	R_L = ∞		2.4	2.9	3.4	2.4	2.9	3.4	V
Output Voltage Swing	R_L = 2k		3.0	4.0		3.0	4.0		
Output Sink Current			2.5	3.6		2.5	3.6		mA
Output Resistance				20		•	20		Ω
Power Supply Current	R_L = ∞			18	24		18	24	mA

Recommended Operating Supply Voltages (V_S = ±6.0 V)

NOTES:
1. Gain select pins G_{1A} and G_{1B} connected together.
2. Gain select pins G_{2A} and G_{2B} connected together.
3. All gain select pins open.

ภาคผนวก (ฏ)   ต่อ

ข้อมูลทางไฟฟ้าของไอซี เบอร์ µA733

## TYPICAL CHARACTERISTIC CURVES

PHASE SHIFT AS A FUNCTION OF FREQUENCY
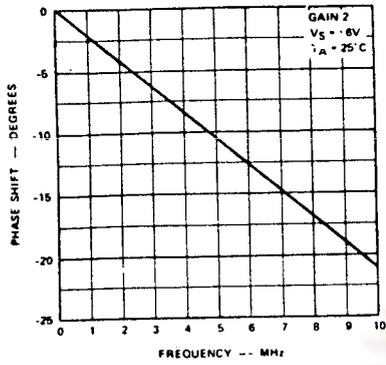
### PHASE SHIFT AS A FUNCTION OF FREQUENCY
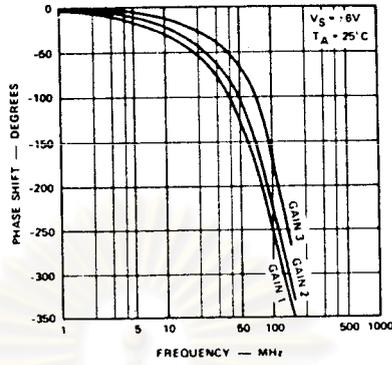
### VOLTAGE GAIN AS A FUNCTION OF FREQUENCY
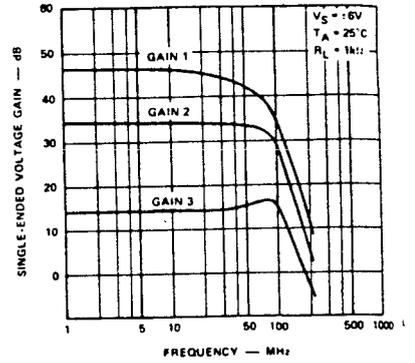
### COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY
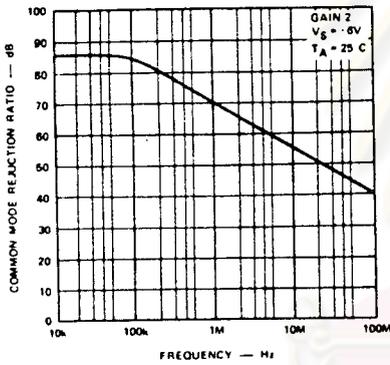
### OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY
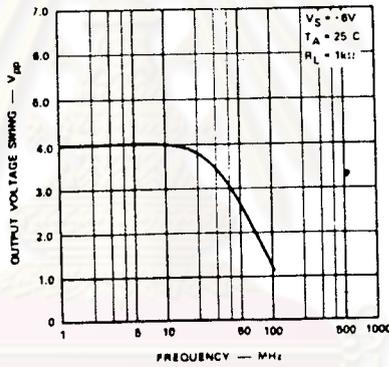
PULSE RESPONSE
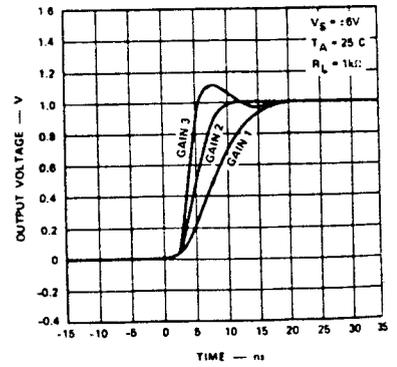
DIFFERENTIAL OVERDRIVE RECOVERY TIME
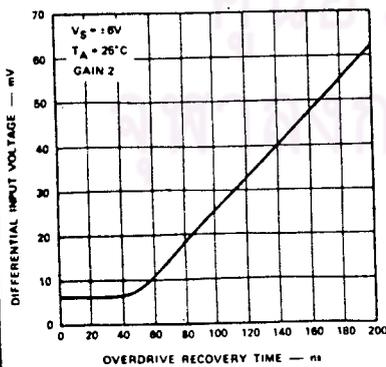
PULSE RESPONSE AS A FUNCTION OF SUPPLY VOLTAGE
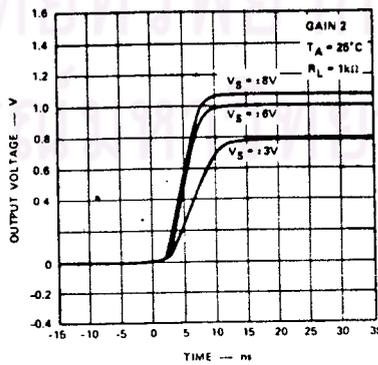
PULSE RESPONSE AS A FUNCTION OF TEMPERATURE
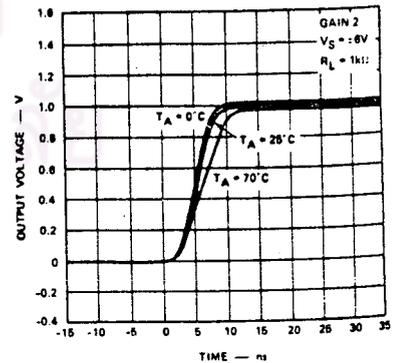
ภาคผนวก(ฎ) ต่อ

ข้อมูลทางไฟฟ้าของไอซี เบอร์ µA733

## TYPICAL CHARACTERISTIC CURVES (CONT'D)

VOLTAGE GAIN AS A FUNCTION OF TEMPERATURE
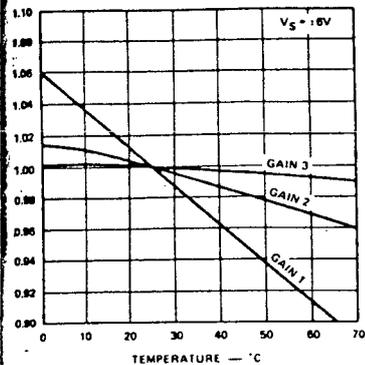
GAIN VS FREQUENCY AS A FUNCTION OF TEMPERATURE
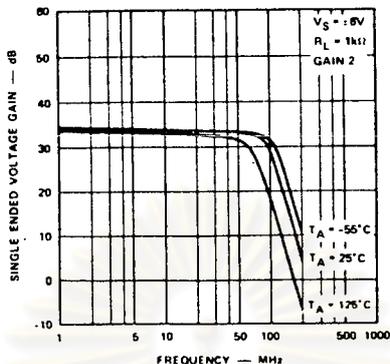
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE
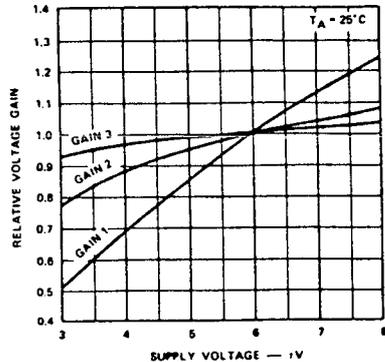
GAIN VS FREQUENCY AS A FUNCTION OF SUPPLY VOLTAGE
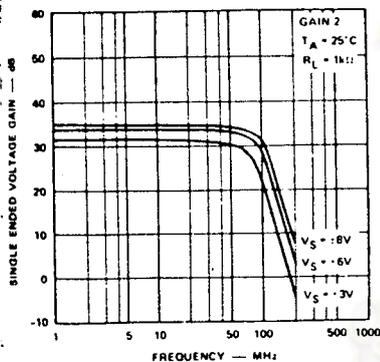
VOLTAGE GAIN ADJUST CIRCUIT

VOLTAGE GAIN AS A FUNCTION OF RADJ (FIGURE 3)
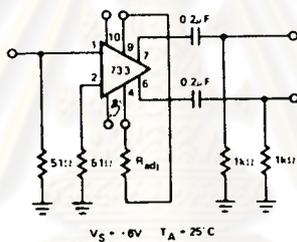
(Pin numbers apply to K Package)

FIGURE 3
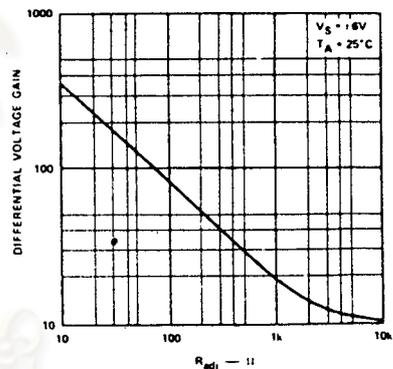
SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE
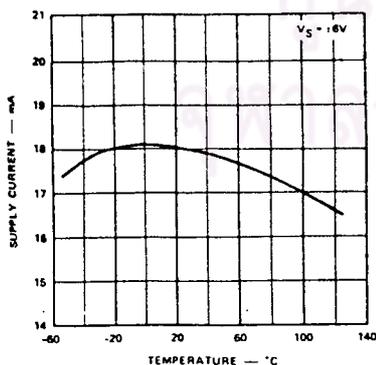
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE
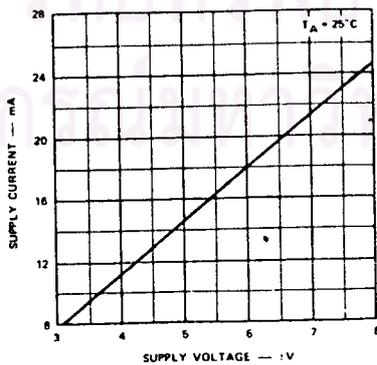
OUTPUT VOLTAGE AND CURRENT SWING AS A FUNCTION OF SUPPLY VOLTAGE
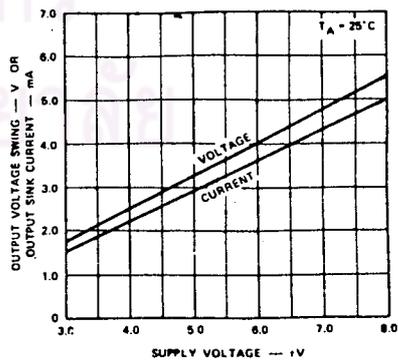
ภาคผนวก (ฏ)   ต่อ
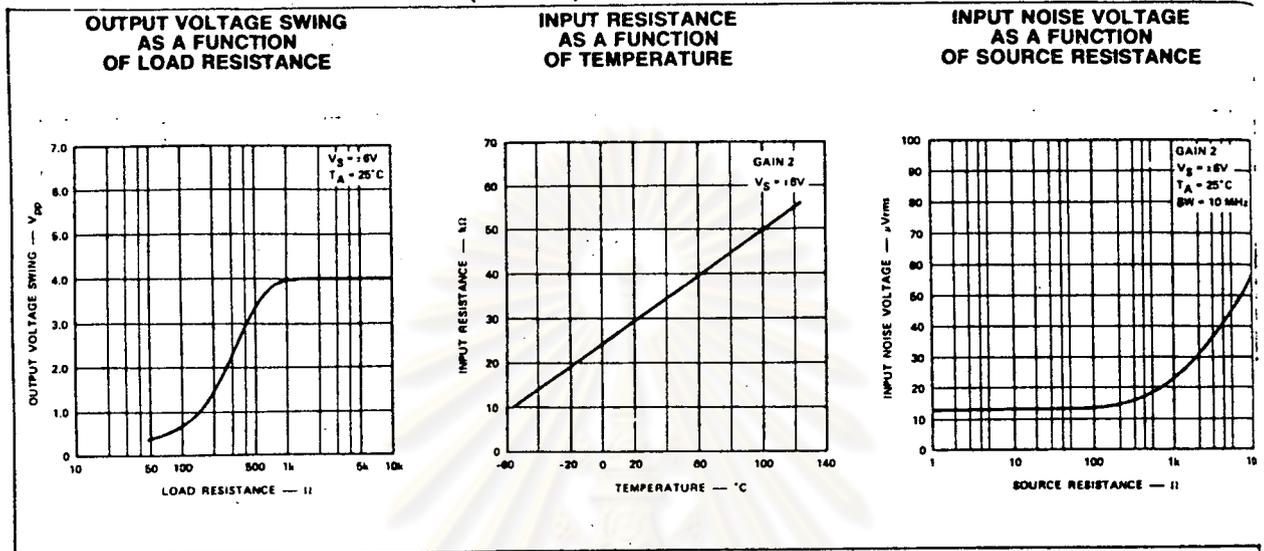
ข้อมูลทางไฟฟ้าของไอซี   เบอร์ µA733

TYPICAL CHARACTERISTIC CURVES (CONT'D)

OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE

INPUT RESISTANCE AS A FUNCTION OF TEMPERATURE

INPUT NOISE VOLTAGE AS A FUNCTION OF SOURCE RESISTANCE

ภาคผนวก (ฏ)

ข้อมูลทางไฟฟ้าของไอซี เบอร์ MC1496

BALANCED MODULATOR-DEMODULATOR   5596/MC1496/MC1596

5596/MC1496/MC1596-A,K

FEATURES
- EXCELLENT CARRIER SUPPRESSION
  - 65dB typ @ 0.5 MHz
  - 50dB typ @ 10 MHz
- ADJUSTABLE GAIN AND SIGNAL HANDLING
- BALANCED INPUTS AND OUTPUTS
- HIGH COMMON-MODE REJECTION—85dB typ

APPLICATIONS
SUPPRESSED CARRIER AND AMPLITUDE MODULATION
SYNCHRONOUS DETECTION
FM DETECTION
PHASE DETECTION
SAMPLING
SINGLE SIDEBAND
FREQUENCY DOUBLING

ABSOLUTE MAXIMUM RATINGS

Applied Voltage (Note 1)	30V
Differential Input Signal ($V_7 - V_8$)	±5.0V
Differential Input Signal ($V_4 - V_1$)	$(5 ± I_5 R_e)$ V
Input Signal ($V_2 - V_1$, $V_3 - V_4$)	5.0V
Bias Current (I_5)	10mA
Power Dissipation (Pkg. Limitation)	
K-Package	680mW.
Derate above 25°C	5.4mW/°C
A-Package (TO-116)	900mW
Derate above 25°C	7.2mW/°C
Operating Temperature Range	-555°C to +125°C
Storage Temperature Range	-65°C to +150°C

NOTES
1. Voltage applied between pins 6-7, 8-1, 9-7, 9-8, 7-4, 7-1, 8-4, 6-8, 2-5, 3-5.
2. Pin number references pertain to K package pinout only.

PIN CONFIGURATIONS (TOP VIEW)

A PACKAGE

K PACKAGE
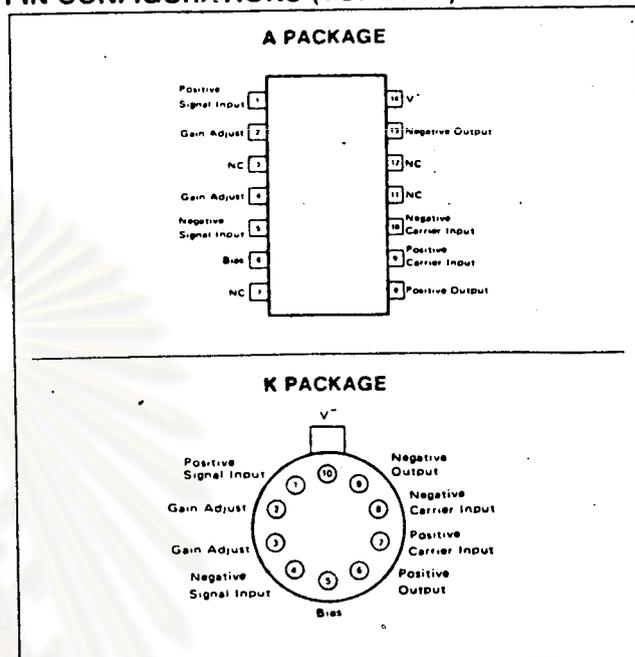
SCHEMATIC DIAGRAM
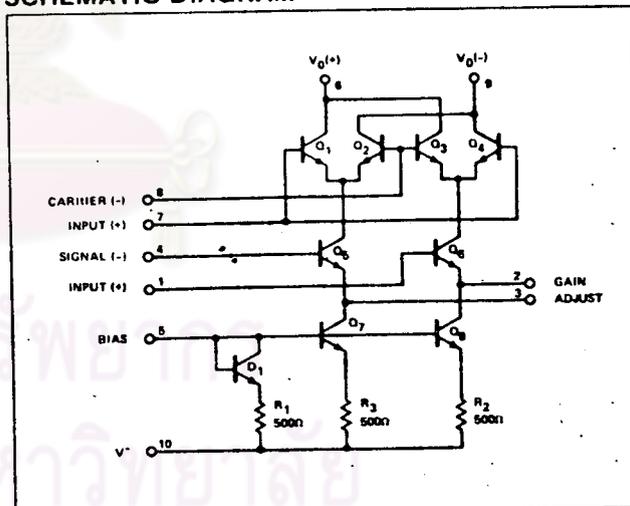
BALANCED MODULATOR-DEMODULATOR 　　　5596/MC1496/MC1596

5596/MC1496/MC1596-A.K

SIGNETICS BALANCED MODULATOR-DEMODULATOR ■ MC1596, MC1496
## ELECTRICAL CHARACTERISTICS*

(All input and output characteristics are single-ended unless otherwise noted)

PARAMETER	MC1596			MC1496			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
Carrier Feedthrough							μV(rms)
$V_C = 60$ mV(rms) sine wave and 　　$f_C = 1.0$ kHz		40			40		
offset adjusted to zero 　　　　　　　$f_C = 10$ MHz		140			140		mV(rms)
$V_C = 300$ mVp-p square wave:							
offset adjusted to zero 　　　　　　　$f_C = 1.0$ kHz		0.04	0.2		0.04	0.4	
offset not adjusted 　　　　　　　　　$f_C = 1.0$ kHz		20	100		20	200	
Carrier Suppressions							dB
$f_S = 10$ kHz, 300 mV(rms)							
$f_C = 500$ kHz, 60 mV(rms) sine wave	50	65		40	65		
$f_C = 10$ MHz, 60 mV(rms) sine wave		50			50		
Transadmittance Bandwidth (Magnitude) ($R_L = 50\Omega$)							MHz
Carrier Input Port, $V_C = 60$ mV(rms) sine wave		300			300		
$f_S = 1.0$ kHz, 300 mV(rms) sine wave							
Signal Input Port, $V_S = 300$ mV(rms) sine wave		80			80		
$|V_C| = 0.5$V dc							
Signal Gain	2.5	3.5		2.5	3.5		V/V
$V_S = 100$ mV(rms), f = 1.0 kHz; $|V_C| = 0.5$V dc							
Single-Ended Input Impedance, Signal Port, f = 5.0 MHz							kΩ
Parallel Input Resistance		200			200		
Parallel Input Capacitance		2.0			2.0		pF
Single-Ended Output Impedance, f = 10 MHz							kΩ
Parallel Output Resistance		40			40		
Parallel Output Capacitance		5.0			5.0		pF
Input Bias Current							μA
$I_{bS} = \dfrac{I_1 + I_4}{2}$: $I_{bC} = \dfrac{I_7 + I_8}{2}$		12	25		12	30	
		12	25		12	30	
Input Offset Current		0.7	5.0		0.7	7.0	μA
$I_{ioS} = I_1 - I_4$; $I_{ioC} = I_7 - I_8$		0.7	5.0		0.7	7.0	
Average Temperature Coefficient of Input Offset Current		2.0			2.0		nA/°C
($T_A = -55°$ to $+125°$C)							
Output Offset Current		14	50		15	80	μA
($I_6 - I_9$)							
Average Temperature Coefficient of Output Offset Current		90			90		nA/°C
($T_A = -55°$C to $+125°$C)							
Common-Mode Input Swing, Signal Port, $f_S = 1.0$kHz		5.0			5.0		Vp-p
Common-Mode Gain, Signal Port, $f_S = 1.0$kHz,		-85			-85		dB
$|V_C| = 0.5$V dc							
Common-Mode Quiescent Output Voltage (Pin 6 or Pin 9)		8.0			8.0		Vdc
Differential Output Voltage Swing Capability		8.0			8.0		Vp-p
Power Supply Current							mAdc
$I_6 + I_9$		2.0	3.0		2.0	4.0	
I_{10}		3.0	4.0		3.0	5.0	
DC Power Dissipation		33			33		mW

(V+ = +12V dc, V- = -8.0V dc, $I_5 = 1.0$mA dc, $R_L = 3.9$kΩ, $R_e = 1.0$kΩ, $T_A = +25°$C unless otherwise noted)

*Pin number references pertain to K package pinout only.

National Semiconductor

Industrial Blocks

LM3914 Dot/Bar Display Driver

General Description

The LM3914 is a monolithic integrated circuit that senses analog voltage levels and drives 10 LEDs, providing a linear analog display. A single pin changes the display from a moving dot to a bar graph. Current drive to the LEDs is regulated and programmable, eliminating the need for resistors. This feature is one that allows operation of the whole system from less than 3V.

The circuit contains its own adjustable reference and accurate 10-step voltage divider. The low-bias-current input buffer accepts signals down to ground, or V⁻, yet needs no protection against inputs of 35V above or below ground. The buffer drives 10 individual comparators referenced to the precision divider. Indication non-linearity can thus be held typically to 1/2%, even over a wide temperature range.

Versatility was designed into the LM3914 so that controller, visual alarm, and expanded scale functions are easily added on to the display system. The circuit can drive LEDs of many colors, or low-current incandescent lamps. Many LM3914s can be "chained" to form displays of 20 to over 100 segments. Both ends of the voltage divider are externally available so that 2 drivers can be made into a zero-center meter.

The LM3914 is very easy to apply as an analog meter circuit. A 1.2V full-scale meter requires only 1 resistor and a single 3V to 15V supply in addition to the 10 display LEDs. If the 1 resistor is a pot, it becomes the LED brightness control. The simplified block diagram illustrates this extremely simple external circuitry.

When in the dot mode, there is a small amount of overlap or "fade" (about 1 mV) between segments. This assures that at no time will all LEDs be "OFF", and

thus any ambiguous display is avoided. Various novel displays are possible.

Much of the display flexibility derives from the fact that all outputs are individual, DC regulated currents. Various effects can be achieved by modulating these currents. The individual outputs can drive a transistor as well as a LED at the same time, so controller functions including "staging" control can be performed. The LM3914 can also act as a programmer, or sequencer.

Features

- Drives LEDs, LCDs or vacuum fluorescents
- Bar or dot display mode externally selectable by user
- Expandable to displays of 100 steps
- Internal voltage reference from 1.2V to 12V
- Operates with single supply of less than 3V
- Inputs operate down to ground
- Output current programmable from 2 to 30 mA
- No multiplex switching or interaction between outputs
- Input withstands ±35V without damage or false outputs
- LED driver outputs are current regulated, open-collectors
- Outputs can interface with TTL or CMOS logic
- The internal 10-step divider is floating and can be referenced to a wide range of voltages

The LM3914 is rated for operation from 0°C to +70°C. The LM3914N is available in an 18-lead molded (N) package and the LM3914J comes in the 18-lead ceramic DIP.

The following typical application illustrates adjusting of the reference to a desired value, and proper grounding for accurate operation, and avoiding oscillations.

Typical Applications

0V to 5V Bar Graph Meter
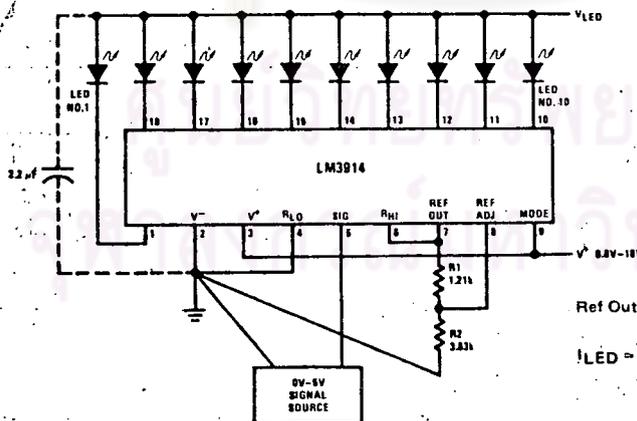
Note 1: Grounding method is typical of all uses. The 2.2 μF tantalum or 10 μF aluminum electrolytic capacitor is needed if leads to the LED supply are 6" or longer.

$$\text{Ref Out V} = 1.25 \left(1 + \frac{R2}{R1}\right)$$

$$I_{LED} = \frac{12.5}{R1}$$

ภาคผนวก (ฐ) ต่อ

Absolute Maximum Ratings

Power Dissipation (Note 5)
Ceramic DIP (J) 1W
Molded DIP (N) 625 mW
Supply Voltage 25V
Voltage on Output Drivers 25V

Input Signal Overvoltage (Note 3) ±35V
Divider Voltage −100 mV to V⁺
Reference Load Current 10 mA
Storage Temperature Range −55°C to +150°C
Lead Temperature (Soldering, 10 seconds) 300°C

Electrical Characteristics (Note 1)

PARAMETER	CONDITIONS (Note 1)	MIN	TYP	MAX	UNITS
COMPARATOR					
Offset Voltage, Buffer and First Comparator	$0V \leq V_{RLO} = V_{RHI} \leq 12V$, $I_{LED} = 1$ mA		3	10	mV
Offset Voltage, Buffer and Any Other Comparator	$0V \leq V_{RLO} = V_{RHI} \leq 12V$, $I_{LED} = 1$ mA		3	15	mV
Gain ($\Delta I_{LED}/\Delta V_{IN}$)	$I_{L(REF)} = 2$ mA, $I_{LED} = 10$ mA	3	8		mA/mV
Input Bias Current (at Pin 5)	$0V \leq V_{IN} \leq V^+ -1.5V$		10	50	nA
Input Signal Overvoltage	No Change in Display	−35		35	V
VOLTAGE-DIVIDER					
Divider Resistance	Total, Pin 6 to 4	8.5	10	15	kΩ
Accuracy	(Note 2)		0.5	2	%
VOLTAGE REFERENCE					
Output Voltage	0.1 mA $\leq I_{L(REF)} \leq 4$ mA, $V^+ - V_{LED} = 5V$	1.2	1.28	1.34	V
Line Regulation	$3V \leq V^+ \leq 18V$		0.01	0.03	%/V
Load Regulation	0.1 mA $\leq I_{L(REF)} \leq 4$ mA, $V^+ - V_{LED} = 5V$		0.4	2	%
Output Voltage Change With Temperature	$0°C \leq T_A \leq +70°C$, $I_{L(REF)} = 1$ mA, $V^+ = 5V$		1		%
Adjust Pin Current			75	120	µA
OUTPUT DRIVERS					
LED Current	$V^+ - V_{LED} = 5V$, $I_{L(REF)} = 1$ mA	7	10	13	mA
LED Current Difference (Between Largest and Smallest LED Currents)	$V_{LED} = 5V$, $I_{LED} = 2$ mA / $V_{LED} = 5V$, $I_{LED} = 20$ mA		0.12 / 1.2	0.4 / 3	mA / mA
LED Current Regulation	$2V \leq V_{LED} \leq 17V$ $I_{LED} = 2$ mA / $I_{LED} = 20$ mA		0.1 / 1	0.25 / 3	mA / mA
Dropout Voltage	$I_{LED(ON)} = 20$ mA, $V_{LED} = 5V$, $\Delta I_{LED} = 2$ mA			1.5	V
Saturation Voltage	$I_{LED} = 2.0$ mA, $I_{L(REF)} = 0.4$ mA		0.15	0.4	V
Output Leakage, Each Collector	(Bar Mode) (Note 4)		0.1	10	µA
Output Leakage Pins 10–18	(Dot Mode) (Note 4)		0.1	10	µA
Pin 1		60	150	450	µA
SUPPLY CURRENT					
Standby Supply Current (All Outputs Off)	$V^+ = 5V$, $I_{L(REF)} = 0.2$ mA		2.4	4.2	mA
	$V^+ = 20V$, $I_{L(REF)} = 1.0$ mA		6.1	9.2	mA

Note 1: Unless otherwise stated, all specifications apply with the following conditions:
$3\ V_{DC} \leq V^+ \leq 20\ V_{DC}$ $V_{REF}, V_{RHI}, V_{RLO} \leq (V^+ -1.5V)$
$3\ V_{DC} \leq V_{LED} \leq V^+$ $0V \leq V_{IN} \leq V^+ -1.5V$
$-0.015V \leq V_{RLO} \leq 12\ V_{DC}$ $T_A = +25°C$, $I_{L(REF)} = 0.2$ mA, $V_{LED} = 3.0V$, pin 9 connected to pin 3 (Bar Mode)
$-0.015V \leq V_{RHI} \leq 12\ V_{DC}$

For higher power dissipations, pulse testing is used.

Note 2: Accuracy is measured referred to +10.000 V_{DC} at pin 6, with 0.000 V_{DC} at pin 4. At lower full-scale voltages, buffer and comparator offset voltage may add significant error.

Note 3: Pin 5 input current must be limited to ±3 mA. The addition of a 39k resistor in series with pin 5 allows ±100V signals without damage.

Note 4: Bar mode results when pin 9 is within 20 mV of V⁺. Dot mode results when pin 9 is pulled at least 200 mV below V⁺ or left open circuit. LED No. 10 (pin 10 output current) is disabled if pin 9 is pulled 0.9V or more below V_{LED}.

Note 5: The maximum junction temperature of the LM3914 is 100°C. Devices must be derated for operation at elevated temperatures. Junction to ambient thermal resistance is 75°C/W for the ceramic DIP (J package) and 120°C/W for the molded DIP (N package).

ภาคผนวก (ฐ) ต่อ

Other Applications

- "Slow" – fade bar or dot display (doubles resolution)
- 20-step meter with single pot brightness control
- 10-step (or multiples) programmer
- Multi-step or "staging" controller
- Combined controller and process deviation meter
- Direction and rate indicator (to add to DVMs)
- Exclamation point display for power saving

- Graduations can be added to dot displays. Dimly light every other LED using a resistor to ground
- Electronic "meter-relay"—display could be circle or semi-circle
- Moving "hole" display—indicator LED is dark, rest of bar lit
- Drives vacuum-fluorescent and LCDs using added passive parts

Connection Diagram

Dual-In-Line Package

Pin	Signal		Pin	Signal
1	LED NO. 1		18	LED NO. 2
2	V⁻		17	LED NO. 3
3	V⁺		16	LED NO. 4
4	DIVIDER (LOW END)		15	LED NO. 5
5	SIGNAL INPUT		14	LED NO. 6
6	DIVIDER (HIGH END)		13	LED NO. 7
7	REFERENCE OUTPUT		12	LED NO. 8
8	REFERENCE ADJUST		11	LED NO. 9
9	MODE SELECT		10	LED NO. 10

TOP VIEW
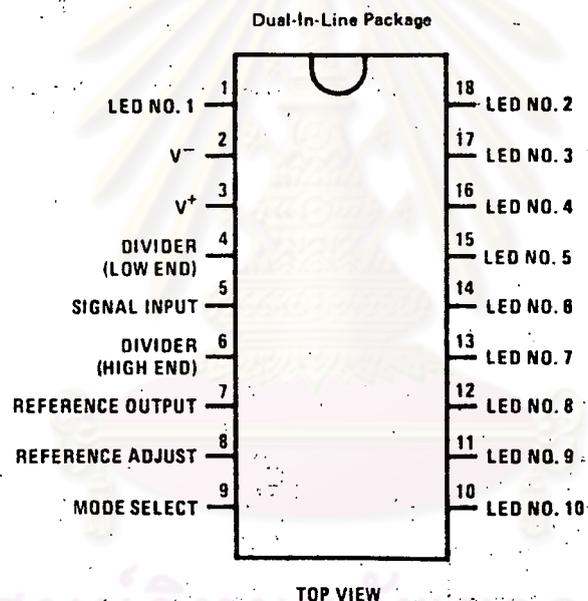
Order Number 3914J
See NS Package J18A
Order Number LM3914N
See NS Package N18A

ภาคผนวก(ฐ) ต่อ

Block Diagram (Showing Simplest Application)
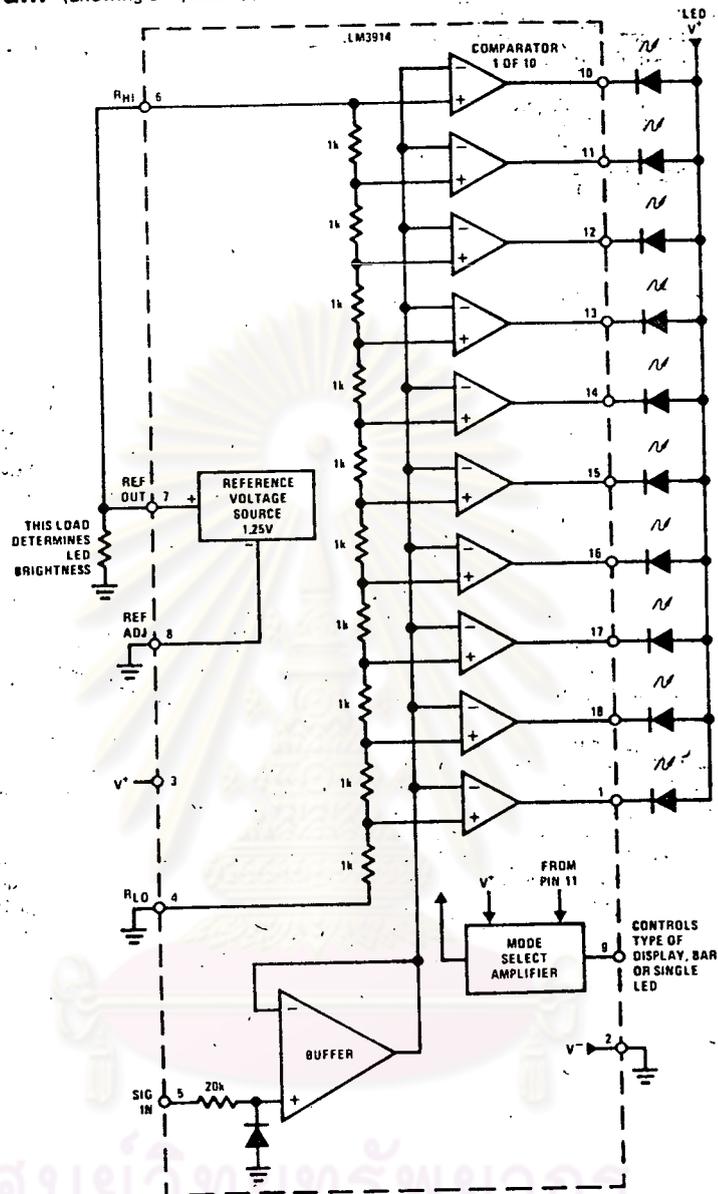
Functional Description

The simplified LM3914 block diagram is to give the general idea of the circuit's operation. A high input impedance buffer operates with signals from ground to 12V, and is protected against reverse and overvoltage signals. The signal is then applied to a series of 10 comparators; each of which is biased to a different comparison level by the resistor string.

In the example illustrated, the resistor string is connected to the internal 1.25V reference voltage. In this case, for each 125 mV that the input signal increases, a comparator will switch on another indicating LED. This resistor divider can be connected between any 2 voltages, providing that they are 1.5V below V^+ and no less than V^-. If an expanded scale meter display is desired, the total divider voltage can be as little as 200 mV. Expanded-scale meter displays are more accurate and the segments light uniformly only if bar mode is used. At 50 mV or more per step, dot mode is usable.

Internal Voltage Reference

The reference is designed to be adjustable and develops a nominal 1.25V between the REF OUT (pin 7) and

Typical Performance Characteristics

ภาคผนวก (ฐ) ต่อ
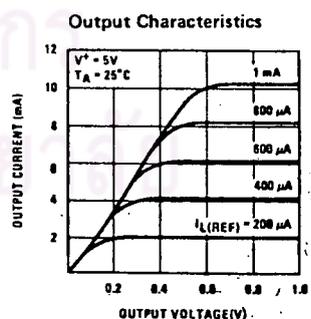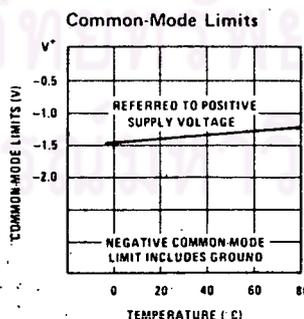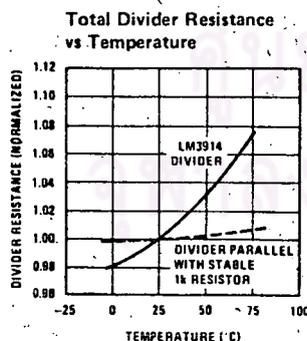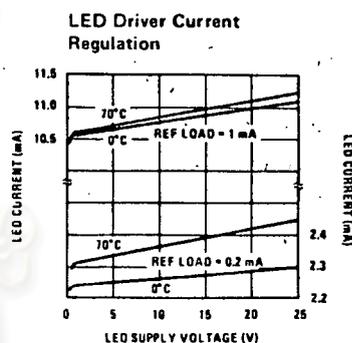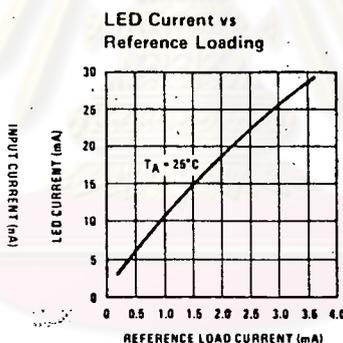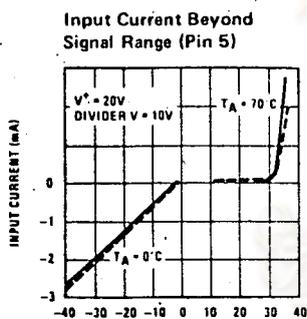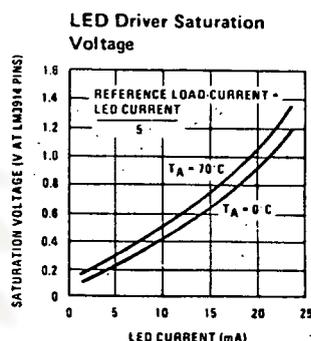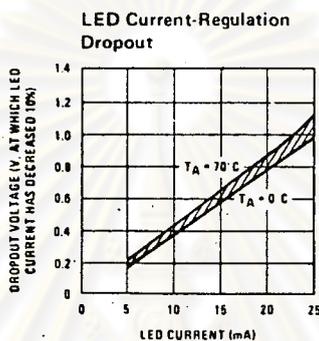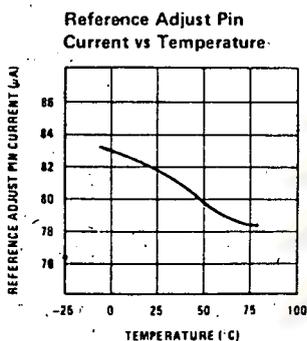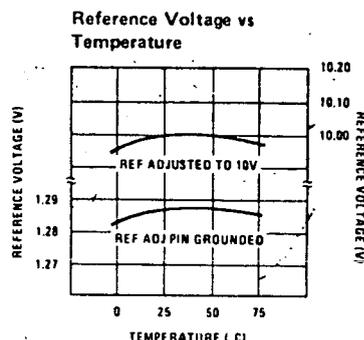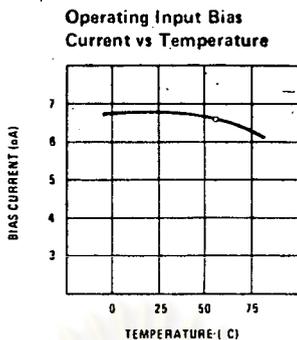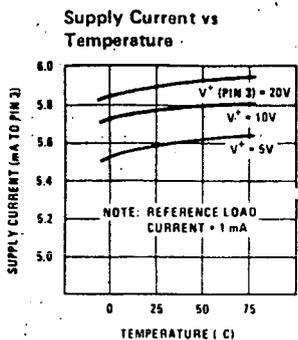
Functional Description (Continued)

REF ADJ (pin 8) terminals. The reference voltage is impressed across program resistor R1 and, since the voltage is constant, a constant current I_1 then flows through the output set resistor R2 giving an output voltage of:

$$V_{OUT} = V_{REF}\left(1 + \frac{R2}{R1}\right) + I_{ADJ}\,R2$$
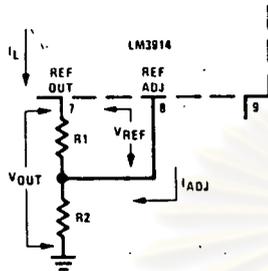
Since the 120 μA current (max) from the adjust terminal represents an error term, the reference was designed to minimize changes of this current with V^+ and load changes.

Current Programming

A feature not completely illustrated by the block diagram is the LED brightness control. The current drawn out of the reference voltage pin (pin 7) determines LED current. Approximately 10 times this current will be drawn through each lighted LED, and this current will be relatively constant despite supply voltage and temperature changes. Current drawn by the internal 10-resistor divider, as well as by the external current and voltage-setting divider should be included in calculating LED drive current. The ability to modulate LED brightness with time, or in proportion to input voltage and other signals can lead to a number of novel displays or ways of indicating input overvoltages, alarms, etc.

Mode Pin Use

Pin 9, the Mode Select input controls chaining of multiple LM3914s, and controls bar or dot mode operation. The following tabulation shows the basic ways of using this input. Other more complex uses will be illustrated in the applications.

**Bar Graph Display:** Wire Mode Select (pin 9) *directly* to pin 3 (V^+ pin).

Dot Display, Single LM3914 Driver: Leave the Mode Select pin open circuit.

Dot Display, 20 or More LEDs: Connect pin 9 of the *first* driver in the series (i.e., the one with the lowest input voltage comparison points) to pin 1 of the next higher LM3914 driver. Continue connecting pin 9 of lower input drivers to pin 1 of higher input drivers for 30, 40, or more LED displays. The last LM3914 driver in the chain will have pin 9 wired to pin 11. All previous drivers should have a 20k resistor in parallel with LED No. 9 (pin 11 to V_{LED}).

Mode Pin Functional Description

This pin actually performs two functions. Refer to the simplified block diagram below.

Block Diagram of Mode Pin Function
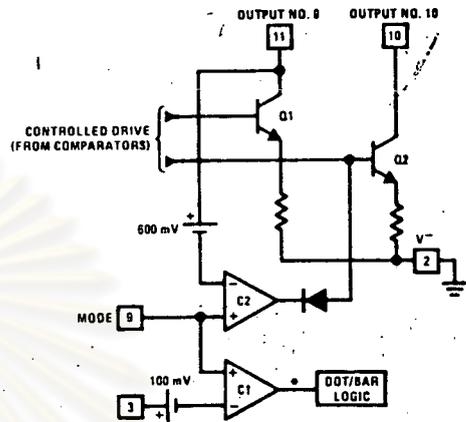
*High for bar

Dot or Bar Mode Selection

The voltage at pin 9 is sensed by comparator C1, nominally referenced to (V^+−100 mV). The chip is in bar mode when pin 9 is above this level; otherwise it's in dot mode. The comparator is designed so that pin 9 can be left open circuit for dot mode.

Taking into account comparator gain and variation in the 100 mV reference level, pin 9 should be no more than 20 mV below V^+ for bar mode and more than 200 mV below V^+ (or open circuit) for dot mode. In most applications, pin 9 is either open (dot mode) or tied to V^+ (bar mode). In bar mode, pin 9 should be connected directly to pin 3. Large currents drawn from the power supply (LED current, for example) should not share this path so that large IR drops are avoided.

Dot Mode Carry

In order for the display to make sense when multiple LM3914s are cascaded in dot mode, special circuitry has been included to shut off LED No. 10 of the first device when LED No. 1 of the second device comes on. The connection for cascading in dot mode has already been described and is depicted on the following page.

As long as the input signal voltage is below the threshold of the second LM3914, LED No. 11 is off. Pin 9 of LM3914 No. 1 thus sees effectively an open circuit so the chip is in dot mode. As soon as the input voltage reaches the threshold of LED No. 11, pin 9 of LM3914 No. 1 is pulled an LED drop (1.5V or more) below V_{LED}. This condition is sensed by comparator C2, referenced 600 mV below V_{LED}. This forces the output of C2 low, which shuts off output transistor Q2, extinguishing LED No. 10.

ตารางที่ A   Ultrasonic data for some Liquids

Luquid	f (MHz)	c (m/sec)	α/f^2 (sec^2/m)	f^Zcx10^{-6}
Mercury	20-50	1500	6.1	19.8
ethyliodine	15	869	40	1.68
ethyl bromide	15	892	62	1.27
methyl iodine	1-4	834	820	1.90
	15		247	
methylene bromide	30	971	567	2.38
methylen chloride	30	1092	1114	1.46
chloro benzene	30-192	1291	147	1.43
nitro benzene	1-192	1473	74	1.78
methy alcohol	1-192	1123	30	0.89
benzyl alcohol	1-192	1540	79	1.61
carbon tetrachloride	1-100	938	533	1.50
Water	1-192	1497	21	1.49
transformer oil	1	1425		1.28
benzene	0.1	1326	900	1.16
	104		849	
	192		775	
acetic acid	0.5	1144	9×10^4	
	67.5		158	
	192		139	
Toluene	.15	1328	205	1.15
	104-192		85	

ตารางที่ B   Ultrasonic velocity and impedance data for some
solids

Solid	Velocity (mls)		fc $\mid$ Long x 10^{-6}
	Longitudinal	transverse	
Aluminium	6260	3080	16.9
copper	4700	2260	41.8
brass	4430	2123	36.1
nickel	5630	2960	49.5
crown glass	5660	3420	14.1
perspex	2670	1121	3.2
polystelene	2350	1120	2.3
rubber	1479		1.4

References

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    (1949).

ตารางที่ C · Velocity of propagation, characteristic
impedance, attenuation

Material	Velocity (m/s)	Characteristic impedance(Rayls)	Attenuation (dB/cm)MH$_z$
Air	345	4.2×10^2	1.7
Water	1490	1.5×10^6	0.0021
Epoxy Resin	2600	3×10^6	3
Normal Saline	1530	1.55×10^6	0.002
Blood	1560	1.56×10^6	0.1
Brain	1520	1.56×10^6	0.8-1.2
Breast	1430-1570	1.56×10^6	.5-1.5
Fat	1450	1.41×10^6	.4-0.6
Kidney	1550	1.61×10^6	.8-1.2
Lens	1640	1.89×10^6	2
Liver	1550	1.64×10^6	.8-1.2
Muscle	1560	1.67×10^6	1.5-2.0
Spleen	1560	1.61×10^6	.4
Testicles	1560	1.61×10^6	-
Lung	660	0.26×10^6	36
Skull Bone	3600	5.7×10^6	12

ประวัติผู้เขียน

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