รายการอ้างอิง

1. Sang-Soo Lee and Carlos A. Laber, "A BiCMOS Continuous-Time Filter for Video Signal Processing Applications", IEEE Journal of solid-state circuits, vol.33, NO.9, September 1998.
2. Kim Scott D. Willingham, Kenneth W.Martin and A.Ganesan, "A BiCMOS Low-Distortion 8MHz Low-Pass Filter", IEEE Journal of solid-state circuits, vol.28, NO.12, December 1993.
3. Bruno Stefanelli and Andeas Kaiser, "A 2um CMOS Fifth-Order Low pass Continuous-Time Filter for Video-Frequency Application", IEEE Journal of solid-state circuits, vol.28, NO.7, July 1993.
4. Venugopal Gopinathan and Yannis P.Tsividis, "Design Consideration for High-Frequency Continuous-Time Filters and Implementation of an Anti-aliasing Filter for Digital Video", IEEE Journal of solid-state circuits, vol.25, NO.6, December 1990.
5. David A.Johns and Ken Martin, "Analog Integrated Circuit Design", USA, John Wiley & Sons Inc., pp.574-645, 1997.
6. Schauman and Van Valkenburg, "Design of Analog Filters", New York USA, Oxford university press, 2001.
7. Kendall L. Su, "Analog Filters", Massachusetts USA, Kluwer Academic Publishers, 1999.
8. Y.Sun and J.K.Fidler, "Synthesis and performance analysis of universal minimum component integrator-based IFLF OTA-grounded capacitor filter", IEEE Proc.-Circuits Devices Syst., vol.143, No.2, April 1996.
9. Yannis Tsividis, "Continuous-Time MOSFET-C Filters in VLSI", IEEE Solid - State Circuits, VOL.21, pp. 15-30, February 1986.
10. Hanspeter Schmid and George S. Moschytz, "A Tunable, Video-Frequency Low-Power Single-Amplifier Biquadratic Filter in CMOS", IEEE International Symposium on Circuits and Systems, 1999.
11. Jorge M.Canive, Jose Gabriel R., "A CMOS Low Sensitivity Switch-Capacitor Video

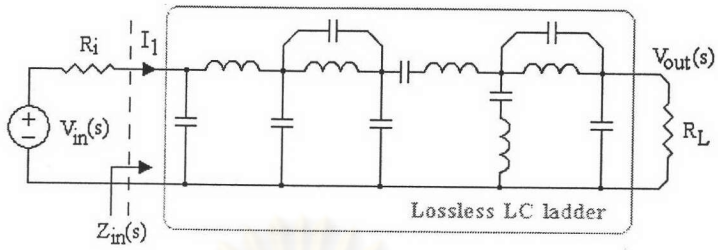
Filter", IEEE International Symposium on Circuits and Systems, 2000.

12. P.S. Racz, G.W. Roberts, M.L. Blostein, "BiCMOS Current Mode Analog Nyquist Filter at Video Rates", IEEE International Symposium on Circuits and Systems, 1992.
13. Francois Krummenacher, "A 4-MHz CMOS Continuous-Time Filter with On-Chip Automatic Tuning", IEEE Solid - State Circuits, VOL.23, pp. 750-758, June 1988.
14. F Yang and P.Loumeau, "Design of CMOS Transconductor for High Frequency Continuous-time Filter Applications", IEEE International Symposium on Circuits and Systems, 1994.
15. Carlos A.Laber and Paul R.Gray, " A 20-MHz Sixth-Order BiCMOS Parasitic-Insensitive Continuous-Time Filter and Second-Order Equalizer Optimized for Disk-Drive Read Channels", IEEE Journal of solid-state circuits, vol.28, NO.4, April 1993.
16. Fuji Yang and Christian C. Enz, "A Low-Distortion BiCMOS Seventh-Order Bessel Filter Operating at 2.5V Supply", IEEE Journal of solid-state circuits, vol.31, NO.3, March 1996.
17. Chung-Chih Hung, Kari Halonen, "Low-Voltage, Micropower Weak-Inversion CMOS Gm-C Filter", International Conference on Electronics, Circuits, and Systems, pp. 1178-1181, 1996.
18. Randy Stephens, "Measuring Differential Gain and Phase", Texas Instruments, November 1999.
19. L.H.Chew and P.Y.Xu, "Design of a Low-Voltage Rail-to-Rail Input and Output Operational Amplifier with Nested Miller Compensation", IEEE Asia-Pacific Conference on Circuits and Systems, December 2000.

ภาคผนวก

ภาคผนวก ก

การหาค่า $Z_{in}(s)$ ในโครงสร้างของวงจรกรองแบบขั้นบันไดชนิดไม่สูญเสีย จากฟังก์ชันถ่ายโอนของวงจรกรอง



รูปที่ ก.1 โครงสร้างของวงจรกรองแบบขั้นบันไดชนิดไม่สูญเสีย

กำหนดให้

$$Z_{in} = R_{in} + jX_{in} \tag{ก-1}$$

จะได้กระแสที่ไหลเข้าวงจรกรอง (I_1)

$$I_1 = \frac{V_{in}}{R_i + Z_{in}} \tag{ก-2}$$

เมื่อพิจารณาในแง่พลังงานพบว่า พลังงานที่ไหลผ่านโหลด R_L (P_{load}) คือ

$$P_{load} = \frac{|V_{out}(s)|^2}{R_L} \tag{ก-3}$$

และในกรณีที่วงจรกรองประกอบด้วยตัวเหนี่ยวนำและตัวเก็บประจุซึ่งไม่เสียพลังงานในการส่งผ่านสัญญาณดังรูปที่ ก.1 จะได้พลังงานที่ไหลผ่านโหลด R_L คือ

$$P_{load} = R_{in}|I_1(s)|^2 = R_{in}\frac{|V_{in}(s)|^2}{|R_i + Z_{in}|^2} \tag{ก-4}$$

จากสมการที่ (ก-3) และ (ก-4) สามารถจัดรูปได้ H(s) ซึ่งเป็นฟังก์ชันถ่ายโอนของวงจรกรองดังนี้

$$|H(s)|^2 = \frac{|V_{out}(s)|^2}{|V_{in}(s)|^2} = \frac{R_{in}R_L}{|R_i + Z_{in}|^2} \tag{ก-5}$$

พลังงานที่ส่งผ่านไปโหลดมากที่สุด (P_{max}) ที่เป็นไปได้จะเกิดขึ้นในกรณีที่ $Z_{in}(s)$ ดังในรูปที่ ก.1 มีค่าเท่ากับ R_i พอดี (กรณีดังกล่าวอาจจะเกิดขึ้น ณ จุดความถี่ใดๆ ขึ้นกับลักษณะการต่อวงจรและค่าอุปกรณ์ที่ใช้) ดังนั้น P_{max} คือ

$$P_{\max} = \frac{|V_{in}(s)|^2}{4R_i} \qquad \text{(ก-6)}$$

เนื่องจากไม่มีการสูญเสียพลังงานในส่วนตัวเหนี่ยวนำและตัวเก็บประจุดังนั้น $P_{load} \leq P_{max}$ และจะได้อัตราส่วนการส่งผ่านพลังงาน (Power transfer ratio, t(s)) ดังนี้

$$|t(s)|^2 = \frac{P_{Load}}{P_{\max}} = \frac{4R_i}{R_L}\left|\frac{V_{out}(s)}{V_{in}(s)}\right|^2 = \frac{4R_i}{R_L}|H(s)|^2 \leq 1 \qquad \text{(ก-7)}$$

แทนค่า H(s) จากสมการที่ (ก-5) ลงในสมการที่ (ก-7) จะได้สัมประสิทธิ์การสะท้อน (Reflection coeffecient) ดังนี้

$$|\rho(s)|^2 = 1 - |t(s)|^2 = 1 - \frac{4R_{in}R_i}{|R_i + Z_{in}(s)|^2} = \frac{|R_i - Z_{in}(s)|^2}{|R_i + Z_{in}(s)|^2}$$
$$\rho(s) = \pm\frac{R_i - Z_{in}(s)}{R_i + Z_{in}(s)} \qquad \text{(ก-8)}$$

เมื่อจัดรูปสมการแล้วจะได้ $Z_{in}(s)$ สำหรับหาค่าตัวเหนี่ยวนำและตัวเก็บประจุต่อไป

$$Z_{in}(s) = R_i\frac{1-\rho(s)}{1+\rho(s)} \quad or \quad Z_{in}(s) = R_i\frac{1+\rho(s)}{1-\rho(s)} \qquad \text{(ก-9)}$$

ภาคผนวก ข

การหาค่าตัวต้านทานและตัวเก็บประจุของฟังก์ชันถ่ายโอนต้นแบบชนิดเอลลิปติก อันดับที่ 5 ด้วยโปรแกรม MATLAB

```
%%% Solve LC values of a 5th elliptic protype filter from its prototype transfer function %%%
clear
num = [0.09925290978182  0  0.678802037  0  1];
den = [4.35588444956411  6.57442818047024  10.87054489379894  9.078809643  5.82027  2]/2;
Filter = tf(num,den)
% Transfer function:
%            0.09925 s^4 + 0.6788 s^2 + 1
% ------------------------------------------------------------
% 2.178 s^5 + 3.287 s^4 + 5.435 s^3 + 4.539 s^2 + 2.91 s + 1
%%% create num(jw) and den(jw) in polynomial of w %%%
for i=length(num):-1:1
        numW(i) = j^(length(num)-i)*num(i) ;
end
for i=length(den):-1:1
        denW(i) = j^(length(den)-i)*den(i) ;
end
%%% create num(-jw) and den(-jw) in polynomial of w %%%
for i=length(num):-1:1
        numX(i) = (-j)^(length(num)-i)*num(i) ;
end
for i=length(den):-1:1
        denX(i) = (-j)^(length(den)-i)*den(i) ;
end
%%% Determine num(jw)*num(-jw) and den(jw)*den(-jw) %%%
Tnum = conv(numW,numX);
Tden = conv(denW,denX);
tf(Tnum,Tden)
% Transfer function:
%            0.009851 s^8 - 0.1347 s^6 + 0.6593 s^4 - 1.358 s^2 + 1
% ------------------------------------------------------------------------------------
% 4.743 s^10 - 12.87 s^8 + 12.37 s^6 + (0+8.882e-016i) s^5 - 4.454 s^4 - 0.6099 s^2 + 1
%%% Notice! den(jw)*den(-jw) has a small calculation error at coeffecient of w^5 so SET it = 0 %%%
Tden(6) = 0 ;
%%% Let Power transfer ratio = PTR and Magnitude square of Reflection coeffecient = MRC %%%
PTR = tf(Tnum,Tden) ;
MRC  = 1-tf(Tnum,Tden) ;
[MRnum,MRden] = TFDATA(MRC,'v') ;
%%% Change Magnitude of Reflection coeffecient(MRC) from w domain to s domain %%%
for i=length(MRnum):-1:1
        MRnums(i) = MRnum(i)/(j)^(length(MRnum)-i) ;
end
for i=length(MRden):-1:1
        MRdens(i) = MRden(i)/(j)^(length(MRden)-i) ;
end
tf(MRnums,MRdens)
% Transfer function:
%  4.743 s^10 + 12.88 s^8 + 12.51 s^6 + 5.113 s^4 + 0.7477 s^2
% ------------------------------------------------------------
% 4.743 s^10 + 12.87 s^8 + 12.37 s^6 + 4.454 s^4 - 0.6099 s^2 - 1
%%% Determine Reflection coeffecient(RC) by select only left-half plane poles of MRC(s) %%%
RMRnums = roots(MRnums)
%      0
%      0
% -0.0000 + 0.9650i
% -0.0000 - 0.9650i
%  0.0000 + 0.9650i
%  0.0000 - 0.9650i
% -0.0000 + 0.6529i
% -0.0000 - 0.6529i
%  0.0000 + 0.6529i
```

```
% 0.0000 - 0.6529i
RMRdens = roots(MRdens)
% -0.0966 + 1.0435i
% -0.0966 - 1.0435i
% 0.0966 + 1.0435i
% 0.0966 - 1.0435i
% -0.3659 + 0.7627i
% -0.3659 - 0.7627i
% 0.3659 + 0.7627i
% 0.3659 - 0.7627i
% -0.5843
% 0.5843
Rnum = poly([RMRnums(1) RMRnums(3) RMRnums(4) RMRnums(7) RMRnums(8)]);
Rden = poly([RMRdens(1) RMRdens(2) RMRdens(5) RMRdens(6) RMRdens(9)]);
RC = tf(Rnum,Rden)
% Transfer function:
% s^5 + 3.932e-006 s^4 + 1.358 s^3 + 2.255e-006 s^2 + 0.397 s
% -----------------------------------------------------------
% s^5 + 1.509 s^4 + 2.496 s^3 + 2.084 s^2 + 1.336 s + 0.4591
%%% Determine Zin(s) by let Zin(s) = (1-RC)/(1+RC) for minimum L ladder architecture %%%
%%% Remark that If let Zin(s) = (1+RC)/(1-RC),the derived architecture is mininum C %%%
Znum = Rden-Rnum ; Zden = Rden+Rnum ;
Zin = tf(Znum,Zden)
% Transfer function:
% 1.509 s^4 + 1.138 s^3 + 2.084 s^2 + 0.9392 s + 0.4591
% -----------------------------------------------------------
% 2 s^5 + 1.509 s^4 + 3.853 s^3 + 2.084 s^2 + 1.733 s + 0.4591
%%% Determine L2*C2 and L4*C4 %%%
x = roots(num) ;
a = poly([x(1) x(2)]) ;
b = poly([x(3) x(4)]) ;
L2C2 = 1/a(3)
L4C4 = 1/b(3)
%%% Solve for C1 %%%
%%% Beware! freqs command must use W(omega rad/s) more than 1 point. %%%
%%% If use W only 1 point, the answer is wrong! %%%
Ynum = Zden ; Yden = Znum ;
C1 = freqs(Ynum,[Yden 0],[sqrt(1/L2C2) sqrt(1/L4C4)])
%C1 = [1.1579 - 0.0000i 0.9110 - 0.0000i]
%%% Notice! C1 has small complex values so neclect them.
clear x
x = real(C1(1)) ;
clear C1
C1 = x
%%% Determine Z2 , and I will select C1 that get from L2C2 for the next step %%%
Z2num = Yden ;
Z2den = [0 Ynum] - C1*[Yden 0] ;
Z2 = tf(Z2num,Z2den)
% Transfer function:
% 1.509 s^4 + 1.138 s^3 + 2.084 s^2 + 0.9392 s + 0.4591
% -----------------------------------------------------------------
% 0.2523 s^5 + 0.1916 s^4 + 1.44 s^3 + 0.9968 s^2 + 1.202 s + 0.4591
%%% Remove L2*C2*s^2 + 1 factor away from Z2den %%%
denx = roots(Z2den) ;
denx = poly([denx(3) denx(4) denx(5)])
% denx = [ 1.0000 0.7594 1.0151 0.3879 ] <<--- !!!
%%% Beware!!! s^0 coeffecient of denx must equal to s^0 coeffecient of Z2den %%%
denx = denx/denx(length(denx))*Z2den(length(Z2den))
%%% Solve for L2 and then C2 %%%
L2 = ( freqs(Z2num,denx,[sqrt(1/L2C2) 0]) )/(j*sqrt(1/L2C2)) ;
clear x
x = real(L2(1)) ;
clear L2
L2 = x
C2 = L2C2/L2
%%% Determine Y3 %%%
Y3num = denx ;
```

```
[Y3den x] = deconv(Z2num - L2*[0 denx 0],[L2C2 0 1]) ;
Y3 = tf(Y3num,Y3den)
% Transfer function:
% 1.184 s^3 + 0.8989 s^2 + 1.202 s + 0.4591
% ------------------------------------------
%      0.5797 s^2 + 0.4016 s + 0.4591
%%% Solve for C3 %%%
C3 = freqs(Y3num,[Y3den 0],[sqrt(1/L4C4) 1]) ;
clear x
x  = real(C3(1)) ;
clear C3
C3 = x
%%% Determine Z4 %%%
Z4num = Y3den ;
Z4den = [0 Y3num] - C3*[Y3den 0] ;
Z4 = tf(Z4num,Z4den)
% Transfer function:
%      0.5797 s^2 + 0.4016 s + 0.4591
% ------------------------------------------
% 0.1948 s^3 + 0.2138 s^2 + 0.4183 s + 0.4591
%%% Remove L4*C4*s^2 + 1 factor away from Z4den %%%
denx = roots(Z4den)
denx = poly(denx(3))
denx = denx/denx(length(denx))*Z4den(length(Z4den))
%%% Solve for L4 and then C4 %%%
L4 = ( freqs(Z4num,denx,[sqrt(1/L4C4) 0]) )/(j*sqrt(1/L4C4)) ;
clear x
x  = real(L4(1)) ;
clear L4
L4 = x
C4 = L4C4/L4
%%% Determine Y5 %%%
Y5num = denx ;
[Y5den x] = deconv(Z4num - L4*[0 denx 0],[L4C4 0 1]) ;
Y5 = tf(Y5num,Y5den)
% Transfer function:
% 0.4183 s + 0.4591
% -----------------
%    0.4591
%%% Solve C5 %%%
C5 = Y5num(length(Y5den)-1)/Y5den(length(Y5den))
[C1 L2 C2 C3 L4 C4 C5]
%%% 1.1579   1.1708   0.1821   1.7058   0.8747   0.5324   0.9110 %%%
```

ภาคผนวก ค
บทความที่ได้รับการตีพิมพ์ใน
2003 IEEE International Symposium on Circuits and Systems

A 0.7-μm CMOS ANTI-ALIASING FILTER FOR NON-OVERSAMPLED VIDEO SIGNAL APPLICATIONS

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ABSTRACT

This paper presents an anti-aliasing filter for non-oversampled digital video signal applications in a 0.7um CMOS technology. The filter consists of a fifth-order elliptic low-pass filter and a third-order equalizer. A new high bandwidth and high linearity transconductor which enables the filter to be implemented in CMOS and its tuning technique are presented. From the simulation, the filter meets the desktop quality of CCIR 601 digital video standard for 1Vpp single-ended input. The effects of transistor, resistor, capacitor, and temperature variations have been included in the design. The filter will be fabricated in a 0.7-μm CMOS. Power dissipation is estimated at 260mW from a single 5V power supply.

1. INTRODUCTION

Digital video signal processing has become increasingly common because of the adoption of new applications such as DVD, HDTV format, and DV format in camcorders. Therefore, the interface between the analog world and the digital processor increasingly plays an important role. For PAL digital video system, signal bandwidth covers from DC to 5.5MHz and requires 27MHz or 36MHz sampling rate for oversampling implementation and 13.5MHz sampling rate for non-oversampling implementation.

The non-oversampling implementation relaxes the requirements for the analog-to-digital converters, but requires an anti-aliasing filter with sharper cutoff. The stopband at 8MHz with more than 40dB attenuation and better than 10 bits linearity presents a steep challenge to CMOS implementation because high-order filters with sharp frequency selectivity are very sensitive to parasitic poles and zeroes (or phase error) of the integrators. For example, in a fifth-order elliptic low-pass filter, integrators with a parasitic pole or zero at 100 times the cutoff frequency will have the passband distorted by 0.32dB. In recent years, anti-aliasing filters for non-oversampled video signals have been implemented on BiCMOS [1], [2] whereas CMOS implementations [3], [4] suffers from the tradeoff between linearity and bandwidth.

This paper presents an anti-aliasing filter according to desktop quality of CCIR 601 digital video standard [1] for non-oversampled PAL digital video system in a 0.7um CMOS technology. This specification is achieved despite the use of a low cost CMOS process due to the introduction of the new high bandwidth and high linearity transconductor and its tuning technique.

Parameter	Unit	Consumer	Desktop	Industrial	Broadcast
DG/DP	%/Deg	2	0.5	0.25	0.25
Corner Freq.	%(+,-)	10	10	5	2
Gain Flatness	dB(+,-)	1.5	0.5	0.25	0.15
Group Delay	ns(+,-)	80	35	20	10
Stopband Rej.	dB(+,-)	30	35	40	40 - 60
SNR	dB of peak/rms	40 – 45	50	55	> 60

Table 1. Filter requirements according to CCIR 601 digital video standard [1].

2. FILTER REQUIREMENTS

Table 1 shows different quality levels of CCIR 601 digital video standard. Among the specifications, differential gain (DG) and the differential phase (DP) are usually the most difficult ones to achieve. These two figures of merit are used to measure linearity of video system rather than the harmonic distortion and are defined for PAL system as:

- DG = (small signal gain @ 4.43MHz, V=0) - (signal gain @ 4.43MHz, V=0.7Vpp)
- DP = (phase of system @ 4.43MHz, V=0) - (phase of system @ 4.43MHz, V=0.7Vpp)

3. FILTER ACHITECTURE

From the stopband requirements, fifth-order elliptic filter is chosen because it requires lower filter order than other conventional filters; unfortunately, its group delay does not meet the requirement. Therefore, a third-order equalizer is needed to equalize the group delay. The transfer function of the equalizer can be determined by using curve-fitting feature of MATLAB program.

Despite the single-ended nature of video signals, the filter is implemented fully differentially to improve linearity and common-mode noise rejection. Therefore, an input amplifier is required to convert the input from single-ended to differential. Also, an output amplifier is used to amplify and buffer the signal before sending it off-chip to an A/D.

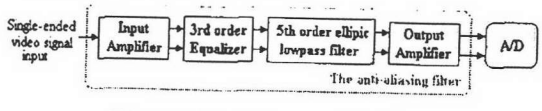

Figure 1 Block diagram of the filter

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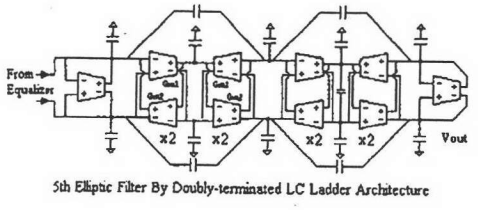

Figure 2 The fifth-order elliptic low-pass filter using doubly-terminated LC ladder architecture

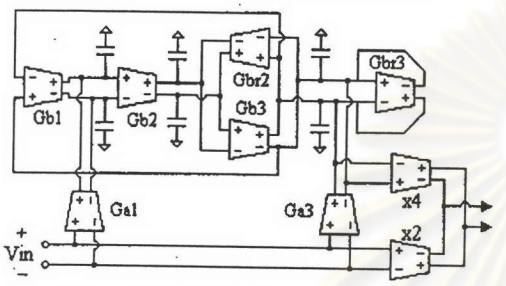

Figure 3 The third-order equalizer using IFLF architecture [5]

Figure 2 and 3 show the filter architecture. The ladder architecture is chosen for the elliptic filter because it can tolerate component mismatches and parasitic poles/zeroes of integrators better than biquads architectures. The equalizer is implemented using n integrator loop inverse follow-the-leader feedback architecture (IFLF) [5] since it requires only grounded capacitors and minimum components.

4. CIRCUIT DESCRIPTION

4.1 Integrator

The transconductor in the integrator is the building block determining the performance of the filter. Conventional CMOS transconductors, such as shown in Figure 4, have high bandwidth but not enough linearity to meet the CCIR 601 requirements. More complicated circuits [1], [2], [7], as in Figure 5 have better linearity but insufficient circuit bandwidth.

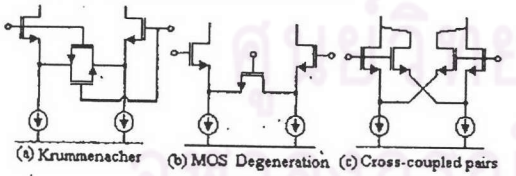

Figure 4 Examples of high bandwidth transconductors

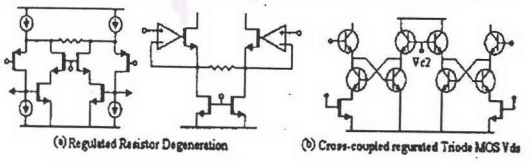

Figure 5 Examples of high linearity transconductors

Figure 6 describes the proposed high bandwidth and high linearity transconductor, which is adapted from the conventional transconductor in Figure 4(b). To improve the linearity of the, resistor degeneration is added as shown in figure 6(b). Due to fabrication tolerances in transistors, resistors, and capacitors, the transconductor must be tunable; hence, the transconductor is modified to the one shown in figure 6(c). Mr2, Mr3 and Mr4 are selectable switches for coarse tuning while Mr1 operates in triode region for fine tuning the transconductor. The resistor values are binary-weighed as shown in the figure 6(c). The fine-tuning range is a bit larger than the coarse-tuning step to allow some overlapping.

Due to the added complexity, the transconductor bandwidth becomes inadequate so a compensation capacitor C_C is added in parallel with the gate capacitance Cg of the input devices to compensate the excess phase.

The transconductor in figure 6(c) can be simplified as shown in figure 7(a) with its small-signal equivalent circuit shown in figure 7(b). Analysis shows that the transconductor has one pole and one zero as expressed below

$$Gm = Gmo\frac{(1+sRCd)}{(1+\frac{s(Cg+Cd)}{gm1+1/R})} \qquad (1)$$

Typically, the pole is at higher frequency than the zero so C_c in Figure 6(c), which is in parallel with Cg, pulls the pole down to cancel the zero. Even though process variations cause the cancellation to be imperfect, the addition of C_C still results in phase error improvement. The compensation capacitor C_C is added for the transconductor in the elliptic filter only because the equalizer is much less sensitive to phase error.

The linearity of the transconductor largely depends on transistors Mr1 and M1. Mr1 operates in triode region and has the characteristic equation as expressed below

$$I_d = K\left[2V_{ds}\times(V_g - V_s - V_t) - V_{ds}^2\right] \qquad (2)$$

For fully differential inputs, it can be shown that

$$I_d = 2KV_p(V_g - V_t) \qquad (3)$$

where $V_d = -V_s = V_p/2$

This result shows that Id is proportional to Vp ; hence, Mr1 behaves like a linear resistor. In our design, we choose the channel length of Mr1 to be 8um to avoid short channel effects.

Additional non-linearity comes from the input device M1. It can be derived from simple square law of saturated MOS transistor that

$$V_{gs}(M1_{left}) - V_{gs}(M1_{right}) = \sqrt{\frac{Io+id}{K}} - \sqrt{\frac{Io-id}{K}}$$
$$\approx \sqrt{\frac{Io}{K}}\frac{id}{Io}\times\left(1+\frac{3}{24}\left(\frac{id}{Io}\right)^2+.....\right) \qquad (4)$$

where Io is the bias current of M1 and i_d is the fully differential small signal current and K is a constant parameter. This equation shows that increasing the bias current of M1 improves linearity.

In this design, id/Io needs to be around 0.25 to achieve a THD of 0.03% THD for the transconductor.

The drawback of increasing the bias current Io, however, is the frequency response degradation. As Io is increased, the size of M1 has to be increased to keep Vdsat constant. This results in larger gm1, Cd, and Cg, which according to Eq.1, moves the zero to a lower frequency. But since the pole frequency is largely unaffected, this leads to more phase error for the integrator.

4.2 Tuning circuit

The transconductor in figure 6(c) can be coarse tuned by switching Mr2, Mr3 and Mr4 and fine tuned by calibrating gate voltage of the triode Mr1. For convenience, the gate voltages of these four transistors (Vt1, Vt2, Vt3 and Vt4) are generated from a single calibration voltage, Vcal, as shown in Figure 8.

Figure 9 shows the circuit for generating Vt1, Vt2, Vt3 and Vt4. Vcal is divided into 8 uniform segments from 0.5 to 4.5 volt by a 3-bit flash ADC to control Mr2, Mr3 and Mr4 switches. Vt1 is the residue from quantizing Vcal.

Furthermore, if Vcal contains some noise, it may cause the comparators in the flash ADC to switch randomly. Therefore, these comparators should have some hysteresis, which can be easily implemented as shown in Figure 10. Transistor Msw in the hysteresis comparator is a switch that is turned on when the comparator output is high; consequently, the comparator has an offset due to unbalance input differential pair. When the comparator output is low, Msw is turned off; the input differential pair becomes balanced so the comparator has no offset.

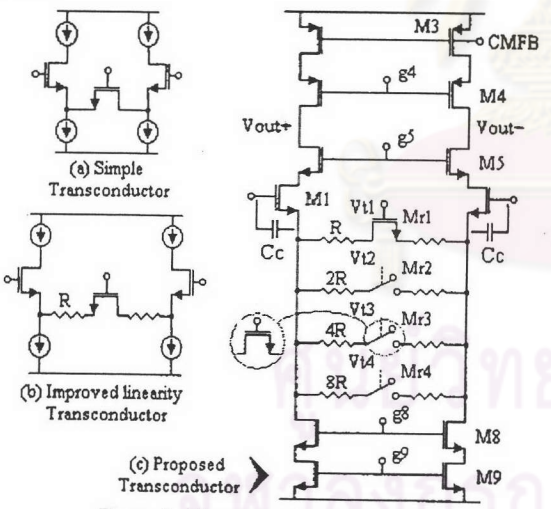

Figure 6 The proposed transconductor

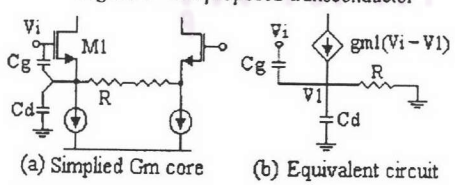

Figure 7 The simplified proposed transconductor

4.3 Input & Output amplifier

The function of the input amplifier is to convert the single-ended video signal input to a differential signal with appropriate amplitude for the filter. The amplifier consists of three parts as shown in Figure 11. In the first part, the video input signal is converted to current by R1. This current is forced to flow through transistors M1a and M1b as a differential current. The second part receives the current via M8a and M8b and converts the current to differential voltage by dropping across R2a and R2b. The third part is the common mode feedback circuit.

The output amplifier, shown in Figure 12, amplifies and buffers the differential video signal output from the filter before sending it off-chip to an analog-to-digital converter. Its gain depends on the ratio between R2 and R1. The two output buffers are conventional two-stage operational amplifiers that can drive 15pF loads.

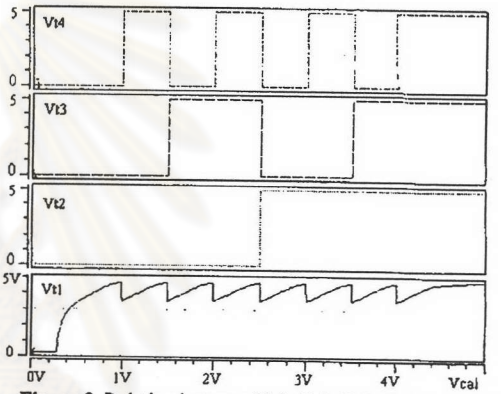

Figure 8 Relation between Vt1, Vt2, Vt3, Vt4 and Vcal

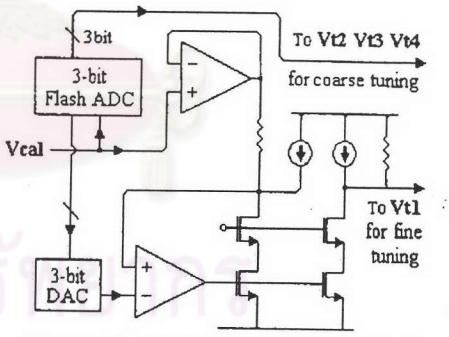

Figure 9 Circuit diagram of the tuning circuit

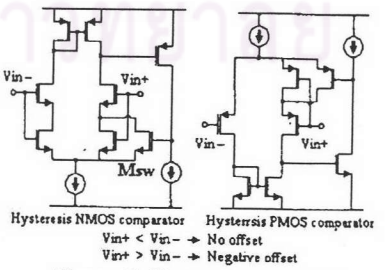

Figure 10 Hysteresis comparators

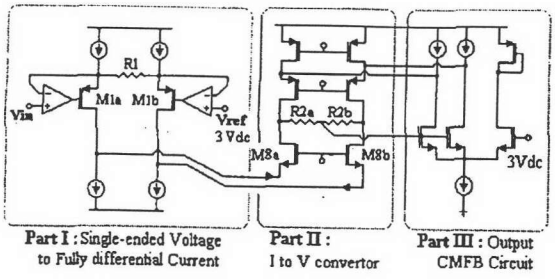

Figure 11 Input amplifier circuit

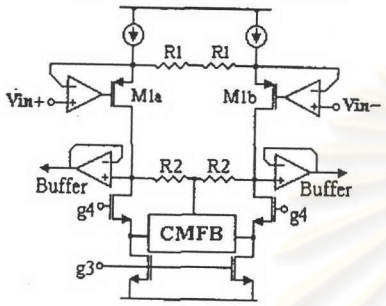

Figure 12 Output amplifier circuit

5. SIMULATION RESULTS

The complete filter has been verified by simulation and will be fabricated in a 0.7-μm CMOS process. The simulation includes the effects of transistor fabrication variation, ± 20% resistor tolerance, ±14% capacitor tolerance, and temperature variation from 0C to 70C. The results are shown in Table 2 and 3.

Parameters	Simulation results
Transconductance	317μA/V± 40%
Phase error	< 0.5 Degree @ 5.5MHz
THD	< 0.03% @ fully differential 0.6Vpp
Power dissipation	4mW

Table 2. Summary of the transconductor

Parameters	Simulation results
Cut off frequency	5.5MHz ± 6% from 0C to 70C
Stopband frequency	< 8MHz
Passband ripple	< ± 0.5dB
Stopband attenuation	> 42 dB
Group delay ripple	< ± 20ns from dc to 5MHz
DG	< 0.1% @ 4.43MHz
DP	< 0.35 Degree @ 4.43MHz
SNR (peak/rms)	> 52dB from 100Hz to 100MHz
Power dissipation	260mW @ 5V single supply
: The whole filter	198mW
: Input buffer	22mW
: Output buffer	40mW

Table 3. Summary of the filter performance

6. CONCLUSIONS

This paper demonstrates that an anti-aliasing filter for non-oversampled PAL digital video system that meets the desktop quality of CCIR 601 digital video standard can be implemented in a 0.7um CMOS technology.

7. REFERENCES

[1] Sang-Soo Lee and Carlos A. Laber, "A BiCMOS Continuous-Time Filter for Video Signal Processing Applications", IEEE Journal of solid-state circuits, vol.33, NO.9, September 1998

[2] Scott D. Willingham, Kenneth W.Martin and A.Ganesan, "A BiCMOS Low-Distortion 8MHz Low-Pass Filter", IEEE Journal of solid-state circuits, vol.28, NO.12, December 1993

[3] Venugopal Gopinathan and Yannis P.Tsividis, "Design Consideration for High-Frequency Continuous-Time Filters and Implementation of an Antialiasing Filter for Digital Video", IEEE Journal of solid-state circuits, vol.25, NO.6, December 1990

[4] Bruno Stefanelli and Andeas Kaiser, "A 2um CMOS Fifth-Order Low pass Continuous-Time Filter for Video-Frequency Application", IEEE Journal of solid-state circuits, vol.28, NO.7, July 1993

[5] Y.Sun and J.K.Fidler, "Synthesis and performance analysis of universal' minimum component integrator-based IFLF OTA-grounded capacitor filter", IEE Proc.-Circuits Devices Syst., vol.143, No.2, April 1996

[6] Carlos A.Laber and Paul R.Gray, " A 20-MHz Sixth-Order BiCMOS Parasitic-Insensitive Continuous-Time Filter and Second-Order Equalizer Optimized for Disk-Drive Read Channels", IEEE Journal of solid-state circuits, vol.28, NO.4, April 1993

[7] Fuji Yang and Christian C. Enz, "A Low-Distortion BiCMOS Seventh-Order Bessel Filter Operating at 2.5V Supply", IEEE Journal of solid-state circuits, vol.31, NO.3, March 1996

[8] Francois Krummenacher, "A 4-MHz CMOS Continuous-Time Filter with On-Chip Automatic Tuning", IEEE Solid - State Circuits, VOL.23, pp. 750-758, June 1988

[9] David A.Johns and Ken Martin, "Analog Integrated Circuit Design", John Wiley & Sons Inc., pp.574-645, 1997

[10] L.H.Chew and P.Y.Xu, "Design of a Low-Voltage Rail-to-Rail Input and Output Operational Amplifier with Nested Miller Compensation", IEEE 2000

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นายไพโรจน์ ศิรินามารัตนะ เกิดวันที่ 7 กุมภาพันธ์ พ.ศ.2523 ที่จังหวัดนทบุรี สำเร็จการศึกษาปริญญาตรีวิศวกรรมศาสตร์บัณฑิต สาขาวิศวกรรมไฟฟ้า จากคณะวิศวกรรมศาสตร์ จุฬาลงกรณ์มหาวิทยาลัยในปีการศึกษา 2544 และเข้าศึกษาต่อในหลักสูตรวิศวกรรมศาสตร์มหาบัณฑิตสาขาวิศวกรรมไฟฟ้า แขนงวิชาวิศวกรรมไฟฟ้าอิเล็กทรอนิกส์เชิงเลข ที่คณะวิศวกรรมศาสตร์ จุฬาลงกรณ์มหาวิทยาลัย ในปีการศึกษา 2544 ในระหว่างการศึกษาได้รับรางวัลชนะเลิศการแข่งขันการประกวดการออกแบบวงจรรวมแห่งชาติครั้งที่ 2 (The National IC Design Contest 2001 : NIC2001) ประเภทวงจรแอนะล็อกในระดับนิสิตนักศึกษาซึ่งจัดขึ้นโดยศูนย์เทคโนโลยีอิเล็กทรอนิกส์และคอมพิวเตอร์แห่งชาติ (NECTEC)