CHAPTER V

CONCLUSIONS

Recent technological advances have made the construction of multiple microprocessor systems relatively easy. It is also possible to build multiple-microprocessor systems with microprocessors with different processing characteristics. In this dissertation the time efficient arbiter proposed in [22] is presented for implementing the shared- memory multiple-microprocessor system. The proposed arbiter can be used with upto 6 unidentical microprocessors.

Many sophisticated architectures have been previously proposed. This shared-memory multiple-microprocessor system is still suitable for a wide variety of applications, especially for a small-to-medium scale real-time control system, since it simplifies system design and maintenance, increases system performance, and provides modularity with a little additional hardware cost. Two shared- memory multiple-microprocessor systems implemented from the proposed arbiter are presented. The first system is used as a communication controller in a data acquisition system. The second system implements the fault tolerant controller from the proposed multiple-microprocessor system.

Multiple-microprocessor systems, in fact, offer many important improvement with respect to single microprocessor systems. A careful design strategy is however necessary in order to exploit the advantages offered by multiple-microprocessor systems. So far there has been no research paper on the performance analysis of the unsymmetrical multiple-microprocessor systems, which is normally

required in most of the real-time applications. This dissertation presents the queueing model for analyzing the response time of unsymmetrical multiple-microprocessor systems. The model is based on flow equivalence technique. Two systems are discussed: the multiple-microprocessor systems with different processor priority and the multiple-microprocessor system with identical processor priority. The result from the analytical model is then verified by actual measurement from the experiment. Both results are in the same trend. The proposed model is applied to analyze and compare the performance of two real-time multiple-microprocessor systems: the communication controller and the SCADA. For the communication controller based on the unsymmetrical multiple-microprocessor system with two microprocessors, it is found that the slower microprocessor should have the processing capability of not less than 40% of the faster microprocessor in order to achieve full benefit from the multiple-microprocessor system.

For the multiple-microprocessor based SCADA systems, the shared—memory multiple-microprocessor system is appropriated for the SCADA system with high message arrival rate or the system that requires high throughput, while the loosely coupled multiple-microprocessor system should be used in the SCADA system with low throughput.

Results presented in this dissertation should therefore relevant to both computer scientists who study the behavior of multiple-microprocessor systems, and engineers who can guide the design of their multiple-microprocessor systems with performance/cost tradeoffs, rather than intuitive arguments or costly simulation programs.

The area that merits further research in the multiple-microprocessor system architecture is the design of arbiter for

multiple-bus multiple-microprocessor systems. The multiple-bus multiple-microprocessor systems retain the well understood features of the single bus, but may allow construction of large systems that can compete with the multistage systems in computing power. The system calls for two types of arbiters: a 1-of-N arbiter, as proposed in this dissertation, to select among microprocessors and a B-of-M arbiter to allocate buses to those microprocessors that successfully obtained access to shared memory. To date, only a few researches on the multiple-bus arbiter design are presented.

We conclude with some remarks on possible extension of the proposed performance model: The performance degradation due to hardware contention for bus and shared memory should be integrated into the proposed flow equivalence model of the unsymmetrical multiple microprocessor systems. This will enable us to achieve the exact performance model for the unsymmetrical microprocessor systems. It would also be desirable to be able to determine the performance of the unsymmetrical multiple-microprocessor system with multiple-bus. Since the performance model of this system is very complicated, currently there has been no developed technique to analyze such a system and much work remains to be done.