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ภาคผนวก

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PMI

PM-7572

COMPLETE HIGH-SPEED
12-BIT BiCMOS A/D CONVERTER

Precision Monolithics Inc.

PRELIMINARY

FEATURES

- 12-Bit Accuracy
- Fast Conversion Speeds: 5µs and 12µs
- Fast 90ns Bus Access Time
- No Missing Codes
- Complete ADC with On-Board Reference
- 215mW Max Power Dissipation
- Space Saving Narrow 0.3", 24-Pin DIP Package
- Alternate Source to the AD7572

APPLICATIONS

- Digital Signal Processing
- High Precision Industrial/Process Controls
- High-Speed Data Acquisition Systems
- Telecommunications
- Sonar/Radar

ORDERING INFORMATION †

5µs CONVERSION TIME††

NON-LINEARITY (FULL TEMP)	FULL SCALE (TEMPCO)	PACKAGE: MILITARY* TEMPERATURE –55°C to +125°C	PACKAGE: EXTENDED INDUSTRIAL TEMPERATURE –40°C to +85°C
±1/2 LSB	25ppm/°C	PM7572AW05	PM7572EW05
±1/2 LSB	25ppm/°C	PM7572ATC05	PM7572EP05
±1/2 LSB	25ppm/°C	–	PM7572ES05
±1 LSB	45ppm/°C	–	PM7572FW05
±1 LSB	45ppm/°C	–	PM7572FP05
±1 LSB	45ppm/°C	–	PM7572FS05†††

12µs CONVERSION TIME††

NON-LINEARITY (FULL TEMP)	FULL SCALE (TEMPCO)	PACKAGE: MILITARY* TEMPERATURE –55°C to +125°C	PACKAGE: EXTENDED INDUSTRIAL TEMPERATURE –40°C to +85°C
±1/2 LSB	25ppm/°C	PM7572AW12	PM7572EW12
±1/2 LSB	25ppm/°C	PM7572ATC12	PM7572EP12
±1/2 LSB	25ppm/°C	–	PM7572ES12
±1 LSB	45ppm/°C	–	PM7572FW12
±1 LSB	45ppm/°C	–	PM7572FP12
±1 LSB	45ppm/°C	–	PM7572FS12†††

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP and plastic DIP packages. For ordering information, see PMI's Data Book, Section 2.

†† Last two (2) part number digits signify conversion speed.

††† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

CROSS REFERENCE†

PMI	ADI	TEMPERATURE RANGE
PM7572AW	AD7572UQ	MIL
PM7572AW	AD7572TQ	
PM7572AW	AD7572SQ	
PM7572EW	AD7572CQ	IND
PM7572FW	AD7572BQ	
PM7572FW	AD7572AQ	
PM7572EP	AD7572LN	COM
PM7572FP	AD7572KN	
PM7572FP	AD7572JN	

† Conversion speed part number digits omitted for clarity.

GENERAL DESCRIPTION

The PM-7572 is a complete 12-bit BiCMOS Analog-to-Digital converter that is designed for high speed and low power applications. It uses a successive approximation technique to convert an analog input signal to a 12-bit digital output code. Simplified control circuitry makes the PM-7572 easy to use and interface to most microprocessors; its data output lines are controlled by read ($\overline{RD}$) and chip select ($\overline{CS}$) inputs. It also uses few microprocessor interface control lines and requires no external components.

The PM-7572's 3-state outputs are speed compatible with most popular microprocessors, thus, eliminating the need for wait states. It also has internal clock circuitry that allows it to be clocked from an external source, or for stand alone applications, can use its internal clock by using an external crystal.

The PM-7572 is fabricated using PMI's advanced BiCMOS process that combines bipolar and CMOS circuits on the same silicon chip.

The PM-7572 is offered in two conversion speeds, 5µs and 12µs. An 05 or 12 part number suffix differentiates the two devices; see ordering information. CerDIP and plastic packaged devices are offered in the extended industrial temperature range of –40°C to +85°C.

This preliminary product information is based on testing of a limited number of devices. Final specifications may vary. Please contact local sales office or distributor for final data sheet.

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

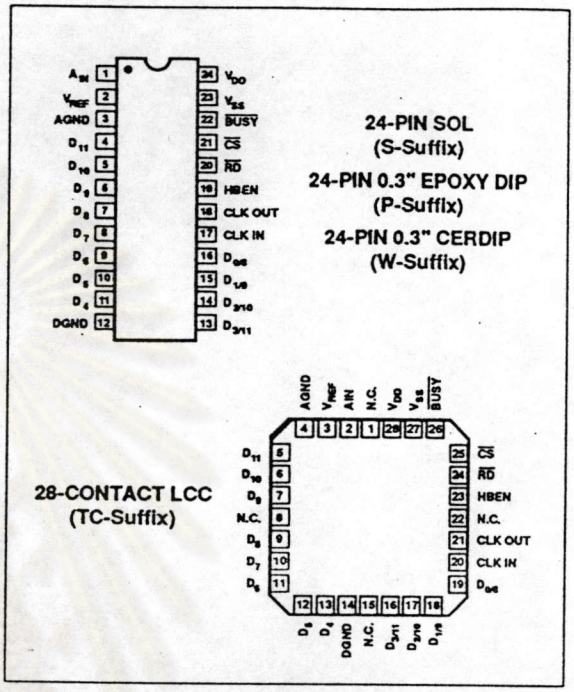
V_{DD} to DGND ..... –0.3 to +7V
V_{SS} to DGND ..... +0.3V to –17V
AGND to DGND ..... –0.3V, V_{DD} + 0.3V
A_{IN} to AGND ..... –15V to +15V
Digital Input Voltage to DGND
Pins 17, 19-21 ..... –0.3V, V_{DD} + 0.3V
Digital Output Voltage to DGND
Pins 4-11, 13-16, 18, 22 ..... –0.3V, V_{DD} + 0.3V
Junction Temperature ..... +150°C
Storage Temperature ..... –65°C to +150°C
Lead Soldering Temperature ..... +300°C
Operating Temperature Ranges
PM-7572AW Version ..... –55°C to +125°C
PM-7572EW/FW/EP/FP/ES/FS ..... –40°C to +85°C

PACKAGE TYPE	Θ_{JA} (Note 1)	Θ_{JC}	UNITS
24-Pin Hermetic DIP (W)	64	7	°C/W
24-Pin Plastic DIP (P)	57	26	°C/W
28-Contact LCC (TC)	70	–	°C/W
24-Pin SOL (S)	70	22	°C/W

NOTE:
1. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP, P-DIP, and LCC packages; Θ_{JA} is specified for device soldered to printed circuit board for SOL package.

CAUTION:
Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONNECTIONS



ELECTRICAL CHARACTERISTICS at V_{DD} = +5V ± 5%; V_{SS} = –15V ± 5%; f_{CLK} = 2.5MHz for PM-7572XX05, 1MHz for PM-7572XX12; Specifications apply to Slow Memory Mode. T_A = Full Temperature Range as specified under Absolute Maximum Ratings, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-7572 MIN	PM-7572 TYP	PM-7572 MAX	UNITS
ACCURACY						
Resolution	N		12	–	–	Bits
Integral Nonlinearity	INL	PM-7572AW/EW/EP/ES	–	–	±1/2	LSB
		PM-7572FW/FP/FS	–	–	±1	
Differential Nonlinearity	DNL	Guaranteed Monotonic over Temperature	–	–	±1	LSB
Offset Error	V_{ZSE}	T_A = +25°C				LSB
		PM-7572AW/EW/EP/ES	–	–	±2	
		PM-7572FW/FP/FS	–	–	±3	
		T_A = Full Temperature Range				
		PM-7572AW/EW/EP/ES	–	–	±4	
		PM-7572FW/FP/FS	–	–	±6	
Full Scale Error	G_{FSE}	V_{DD} = +5V; V_{SS} = –15V; FS = +5V; Ideal Last Code Transition = FS – 3/2 LSBs	–	–	±10	LSB
Full Scale Tempco (Note 1)	TCG_{FS}	PM-7572AW/EW/EP/ES	–	–	±25	ppm/°C
		PM-7572FW/FP/FS	–	–	±45	
ANALOG INPUT						
Input Voltage Range	V_{IN}		0	–	+5	V
Input Current	I_{IN}		–	–	3.5	mA

ELECTRICAL CHARACTERISTICS at V_{DD} = +5V ± 5%; V_{SS} = –15V ± 5%; f_{CLK} = 2.5MHz for PM-7572XX05, 1MHz for PM-7572XX12; Specifications apply to Slow Memory Mode. T_A = Full Temperature Range as specified under Absolute Maximum Ratings, unless otherwise noted. *Continued*

PARAMETER	SYMBOL	CONDITIONS	PM-7572 MIN	PM-7572 TYP	PM-7572 MAX	UNITS
INTERNAL REFERENCE						
V_{REF} Output Voltage	V_{REF}	T_A = +25°C	–5.2	–5.25	–5.3	V
V_{REF} Output Tempco	$V_{REF}TC$		–	20	–	ppm/°C
Output Current Sink Capability	I_{SINK}	External Load Should Not Change During Conversion	–	–	500	µA
POWER SUPPLY REJECTION						
V_{DD} Only	PSR+	FS Change, V_{SS} = –15V, V_{DD} = +4.75 to +5.25V	–	±1/2	–	LSB
V_{SS} Only	PSR–	FS Change, V_{DD} = 5V, V_{SS} = –14.25 to –15.75V	–	±1/2	–	LSB
LOGIC INPUTS						
$\overline{CS}$, $\overline{RD}$, HBEN, CLK IN						
Input Low Voltage	V_{INL}		–	–	+0.8	V
Input High Voltage	V_{INH}		+2.4	–	–	
Input Capacitance	C_{IN}		–	–	10	pF
$\overline{CS}$, $\overline{RD}$, HBEN Input Current	I_{IN}	V_{IN} = 0V to V_{DD}	–	–	±10	µA
CLK IN Input Current	I_{IN}	V_{IN} = 0V to V_{DD}	–	–	±20	µA
LOGIC OUTPUTS						
D11 - D0/8, $\overline{BUSY}$, CLK OUT						
Output Low Voltage	V_{OL}	I_{SINK} = 1.6m	–	–	+0.4	V
Output High Voltage	V_{OH}	I_{SOURCE} = 200µA	+4.0	–	–	
Floating State Leakage Current D11 - D0/8	I_{LKG}		–	–	10	µA
Floating State Output Capacitance	C_{OUT}		–	–	15	pF
CONVERSION TIME						
PM-7572XX05						
Synchronous Clock	t_{CONV}	f_{CLK} = 2.5MHz	–	–	5	µs
Asynchronous Clock			4.8	–	5.2	
PM7572XX12						
Synchronous Clock	t_{CONV}	f_{CLK} = 1.0MHz	–	–	12.5	µs
Asynchronous Clock			12	–	13	
POWER REQUIREMENTS						
Positive Power Supply	V_{DD}	For Specified Performance	4.75	5	5.25	V
Negative Power Supply	V_{SS}	For Specified Performance	–14.25	–15	–15.75	V
Positive Supply Current	I_{DD}	$\overline{CS}$ = $\overline{RD}$ = BUSY = V_{DD}; A_{IN} = +5V	–	–	7	mA
Negative Supply Current	I_{SS}	$\overline{CS}$ = $\overline{RD}$ = BUSY = V_{DD}; A_{IN} = +5V	–	–	12	mA
Power Dissipation	P_{DISS}	$\overline{CS}$ = $\overline{RD}$ = BUSY = V_{DD}; A_{IN} = +5V 5VX 7mA + 15VX 12mA	–	135	215	mW

ELECTRICAL CHARACTERISTICS at V_{DD} = +5V ± 5%; V_{SS} = –15V ± 5%; f_{CLK} = 2.5MHz for PM-7572XX05, 1MHz for PM-7572XX12; Specifications apply to Slow Memory Mode. T_A = Full Temperature Range as specified under Absolute Maximum Ratings, unless otherwise noted. *Continued*

PARAMETER	SYMBOL	CONDITIONS	PM-7572 MIN	PM-7572 TYP	PM-7572 MAX	UNITS
TIMING CHARACTERISTICS (V_{DD} = +5V; V_{SS} = –5V) (Note 2)						
$\overline{CS}$ to $\overline{RD}$ Setup Time	t_1		0	–	–	ns
$\overline{RD}$ to $\overline{BUSY}$ Propagation Delay	t_2	T_A = +25°C All Grades	–	–	190	ns
		T_A = Full Temperature PM-7572EW/FW/EP/ES/FS	–	–	230	
		T_A = Full Temperature PM-7572AW	–	–	270	
Data Access Time after $\overline{RD}$ (Note 3)	t_3	C_L = 20pF T_A = +25°C All Grades	–	–	90	ns
		T_A = Full Temperature PM-7572EW/FW/EP/ES/FS	–	–	110	
		T_A = Full Temperature PM-7572AW	–	–	120	
		C_L = 100pF T_A = +25°C All Grades	–	–	125	ns
		T_A = Full Temperature PM-7572EW/FW/EP/ES/FS	–	–	150	
		T_A = Full Temperature PM-7572AW	–	–	170	
$\overline{RD}$ Pulse Width	t_4		t_3	–	–	ns
$\overline{CS}$ to $\overline{RD}$ Hold Time	t_5		0	–	–	ns
Data Setup Time after $\overline{BUSY}$ (Note 3)	t_6	T_A = +25°C All Grades	–	–	70	ns
		T_A = Full Temperature PM-7572EW/FW/EP/ES/FS	–	–	90	
		T_A = Full Temperature PM-7572AW	–	–	100	
Bus Relinquish Time (Note 4)	t_7	T_A = +25°C All Grades	20	–	75	ns
		T_A = Full Temperature PM-7572EW/FW/EP/ES/FS	20	–	85	
		T_A = Full Temperature PM-7572AW	20	–	90	
HBEN to $\overline{RD}$	t_8		0	–	–	ns
HBEN to $\overline{RD}$ Hold Time	t_9		0	–	–	ns
Delay Between Successive Read Operations	t_{10}		500	–	–	ns

NOTES:
1. Full Scale TC = ΔFS/ΔT, where ΔFS is Full Scale change from T_A = +25°C to T_{MIN} or T_{MAX}.
2. All timing input control signals are specified with t_r = t_f = 5ns (10% to 90% of +5V) and timed from a voltage level of 1.6V.
3. Timing signal t_3 and t_6 are defined as the time required for the output to cross 0.8V or 2.4V.
4. Timing signal t_7 is defined as the time required for the data lines to change 0.5V when loaded with a specified circuit.

PIN DESCRIPTION

PIN	MNEMONIC	DESCRIPTION
1	A_{IN}	Analog Input.
2	V_{REF}	–5.25V; Voltage Reference Output.
3	AGND	Analog Ground.
4-11	D_{11}-D_4	Three-State Outputs; active when $\overline{CS}$ and $\overline{RD}$ are brought low.
12	DGND	Digital Ground.
13-16	$D_{3/11}$-$D_{0/8}$	HBEN (High Byte Enable Input) determines individual pin functions.

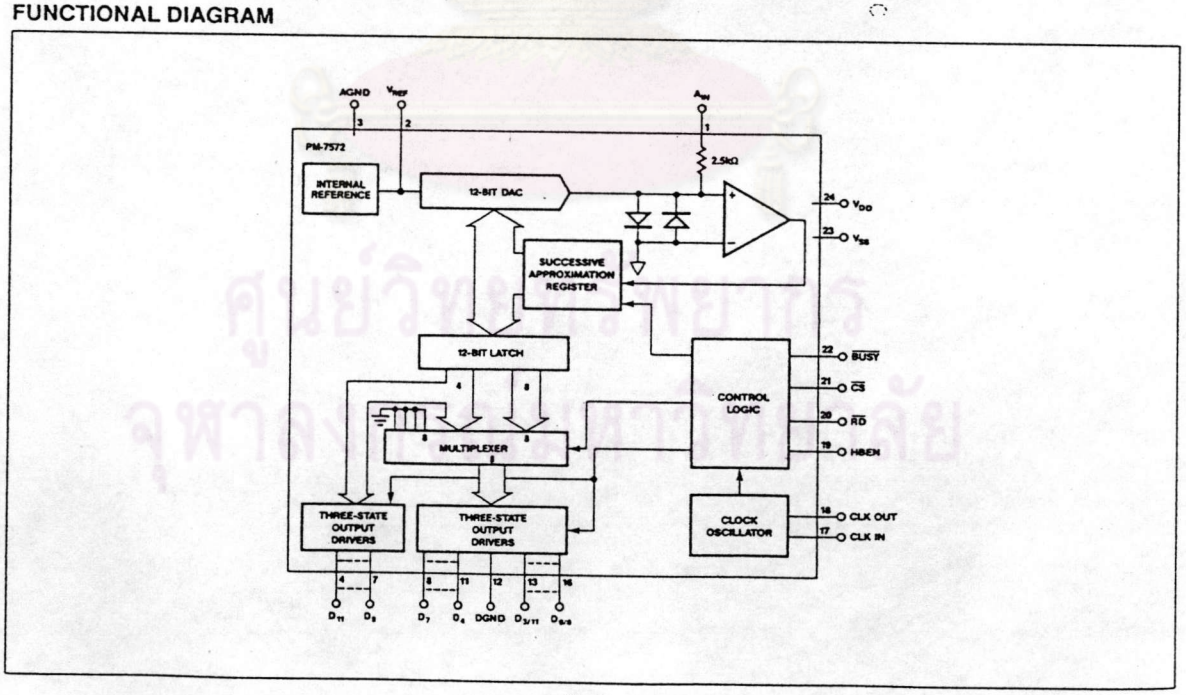
DATA BUS OUTPUT, $\overline{CS}$ & $\overline{RD}$ = LOW

	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8	Pin 9	Pin 10	Pin 11	Pin 13	Pin 14	Pin 15	Pin 16
MNEMONIC*	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	$D_{3/11}$	$D_{2/10}$	$D_{1/9}$	$D_{0/8}$
HBEN = LOW	DB_{11}	DB_{10}	DB_9	DB_8	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
HBEN = HIGH	DB_{11}	DB_{10}	DB_9	DB_8	LOW	LOW	LOW	LOW	DB_{11}	DB_{10}	DB_9	DB_8

*D_{11}-$D_{0/8}$ are the ADC's data output pins.
DB_{11}-DB_0 are the 12-bit conversion results; DB_{11} is the MSB.

17	CLK IN	Clock Input. Accepts a TTL compatible external clock, or crystal between pin 17 (CLK IN) and pin 18 (CLK OUT).
18	CLK OUT	Clock Output. An inverted CLK IN signal appears at this pin when an external clock is used.
19	HBEN	High Byte Enable Input. Multiplexes the 12-bit conversion results into the lower bit outputs, D_7-$D_{0/8}$ (4 MSBs or 8 LSBs). It also disables conversion start when HBEN is high.
20	$\overline{RD}$	Read Input. Active LOW, starts conversion if $\overline{CS}$ is also low and enables the output data three state drivers.
21	$\overline{CS}$	Chip Select Input. Active LOW, starts conversion if $\overline{RD}$ and HBEN are also low and enables the output data drivers.
22	$\overline{BUSY}$	$\overline{BUSY}$ Output. LOW when a conversion is in progress.
23	V_{SS}	Negative Supply, –15V.
24	V_{DD}	Positive Supply, +5V.

FUNCTIONAL DIAGRAM



CONVERTER OPERATION

The PM-7572 uses a successive approximation technique to convert an unknown analog input signal to a 12-bit digital output code. $\overline{CS}$, $\overline{RD}$, and HBEN control inputs are used to start a conversion. With HBEN low (or coincident with the $\overline{RD}$ input falling edge), the falling edge of $\overline{CS}$ and $\overline{RD}$ starts the conversion. Conversion start resets the internal successive approximation register (SAR) and enables the three-state output buffers.

The SAR sequences the voltage output DAC from the most-significant-bit (MSB) to the least-significant-bit (LSB). The analog input connects to the comparator via a 2.5kΩ resistor. The DAC, which has a 2.5kΩ output resistance, connects to the same comparator input. The comparator, performing a zero crossing detection, tests the addition of successively weighted bits from the DAC output versus the analog input signal. The MSB decision occurs after the second negative edge of the CLK IN following conversion initiation. The remaining 11-bit trials occur on the next 11 negative CLK IN edges.

Once a conversion cycle is started, it cannot be stopped or re-started without upsetting the remaining bit decisions. Every conversion cycle must have 13 negative CLK IN edges. At the end of conversion, the comparator input voltage is zero, and the SAR contains the 12-bit data word representing the analog input voltage. Data is then transferred from the SAR to the three-state output buffers when the $\overline{BUSY}$ line returns to logic high, signaling end of conversion.

CONTROL INPUTS SYNCHRONIZATION

Conversion time can vary from 12 to 13 CLK IN periods if the $\overline{RD}$ control input is not synchronized with the ADC clock. This delay can vary from zero to an entire clock period. To ensure a constant conversion time, $\overline{RD}$ must go low on either the rising edge of CLK IN or falling edge of CLK OUT. The delay between the falling edge of $\overline{RD}$ to the falling edge of CLK IN must not be less than 180ns to ensure 12.5 clock cycle conversion time, see Figure 1.

POWER-ON INITIALIZATION

During system power-up, the PM-7572 comes up in a random state. Once the clock is operating or an external clock is applied, the first valid conversion begins with the application of a high-to-low transition of both $\overline{CS}$ and $\overline{RD}$. The next 13 negative clock edges completes the first conversion producing valid data at the digital outputs. This is important in battery operated systems where power supplies are shut down between measurements.

DRIVING ANALOG INPUT

During conversion, the internal DAC output current modulates the analog input at the CLK IN frequency. For accurate conversions, the analog input to the PM-7572 must not change during the conversion periods. This requires an external buffer with low output impedance at the CLK IN frequency. Suitable devices meeting this requirement include the OP-27, OP-42, and SMP-11.

CLOCK OSCILLATOR

A simplified clock oscillator diagram for the PM-7572 is shown in Figure 2. As shown, an external crystal can be used between pins 17 and 18 to generate the internal clock signal required for the ADC. Capacitance values, C_1 and C_2, depend on the crystal or ceramic resonator manufacture and varies typically from 30pF and 100pF.

The CLK IN input accepts a TTL compatible external clock signal. The external clock must have a 45% to 55% duty cycle. No connection is necessary for the CLK OUT pin.

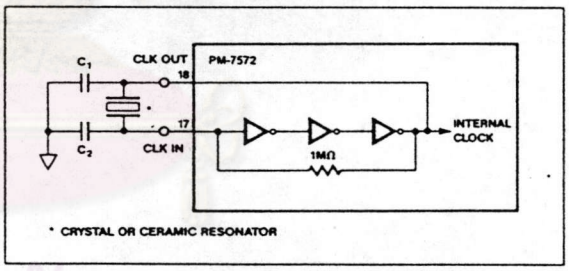


FIGURE 2: *Simplified Internal Clock Circuit*

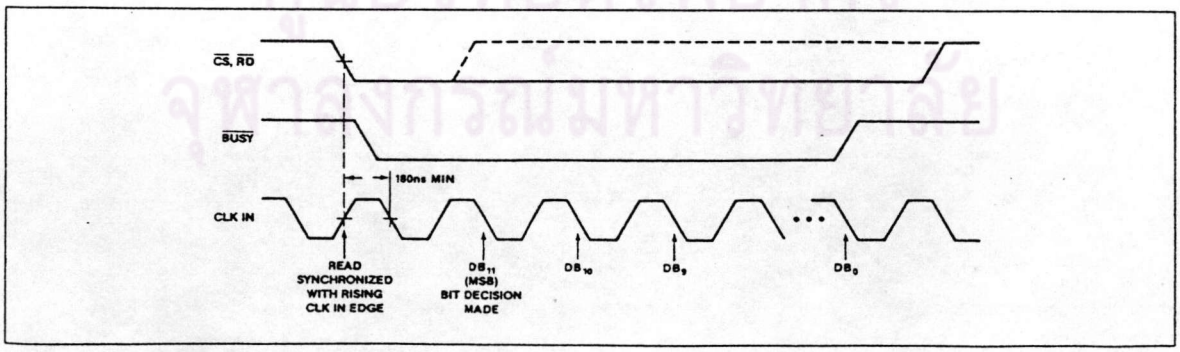


FIGURE 1: *External Clock Input Synchronization*

INTERNAL REFERENCE

The PM-7572 has an internal reference that provides the internal DAC with its reference voltage. This reference voltage is also made avilable at Pin 2 with a current sink capability of 500µA. The reference is internally trimmed during manufacture to –5.25V ± 1%, and is temperature compensated to minimize drift over temperature.

The PM-7572's reference pin (Pin 2) should be bypassed to AGND (Pin 3) with a 47µF capacitor in parallel with a 0.1µF capacitor.

UNIPOLAR OPERATION

The PM-7572's input to output transfer function is shown in Figure 3. Its output code is binary, and for a 0V to +5V analog input, the output code for 1 LSB = FS/4096 = 5/4096 = 1.22mV. The maximum full-scale input voltage for a 5V analog input is FS x 4095/4096 = 5 x 4095/4096 = 4.9988V. Code transitions occur halfway between successive integer LSB values; for example, 0.5 LSB, 1.5 LSB, 2.5 LSB ... FS - 1.5 LSBs.

OFFSET AND FULL-SCALE ERROR ADJUSTMENT, UNIPOLAR OPERATION

Full-scale error and offset error may need to be adjusted to 0V in those applications requiring absolute accuracy. This can be easily accomplished by using several external components as shown in Figure 4. This is also the unipolar mode of operation configuration. Zero offset error must be adjusted first. It is adjusted by applying 0.61mV (1/2 LSB for a 5V analog input) to V_{IN} and adjusting the op amp offset until the PM-7572's output code toggles between 0000 0000 0000 and 0000 0000 0001.

The full-scale error adjustment is performed by applying 4.99817V (equivalent to FS - 1.5 LSB) at V_{IN} and adjusting the full-scale adjust pot until the PM-7572's output toggles between 1111 1111 1110 and 1111 1111 1111.

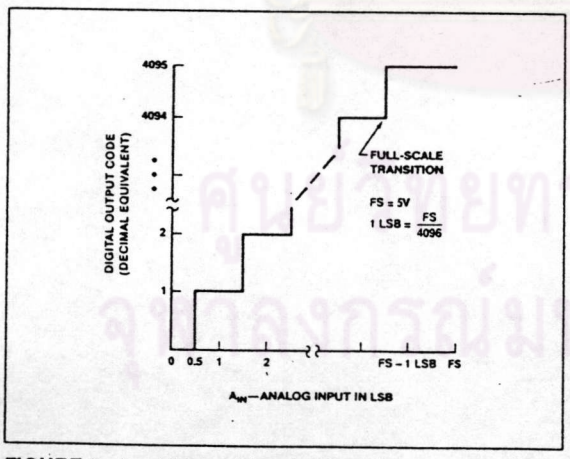


FIGURE 3: *Input/Output Transfer Function*

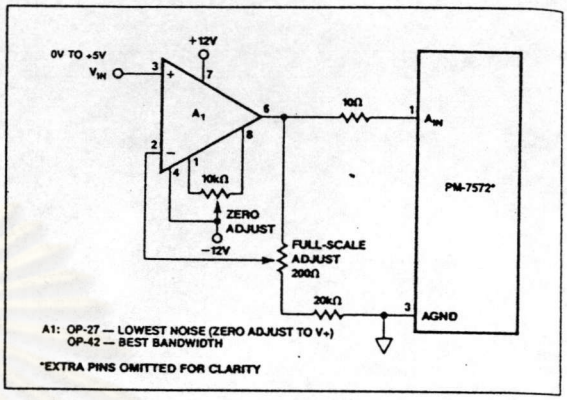


FIGURE 4: *Unipolar 0V to +5V Operation with Zero and Full-Scale Adjust*

BIPOLAR ANALOG INPUT OPERATION

Bipolar operation is achieved with an external amplifier that provides an analog offset voltage of 2.5V. If desired, a sample-and-hold can replace the amplifier. Figure 5 shows a circuit that provides offset binary, and Figure 6 complementary offset binary.

In Figure 5, offset binary coding is produced when the external amplifier is connected in the noninverting mode. The op amp transfer function is shown in Figure 7 and is given by:

$A_{IN} = V_{IN} + 2.5V$

The analog input voltage range is ±2.5V; an LSB is equal to 1.22mV.

In Figure 6, complementary offset binary coding is produced when the external amplifier is connected in the inverting mode. The op amp transfer function is also shown in Figure 7 and is given by:

$A_{IN} = -V_{IN} + 2.5V$

The analog input voltage range is also ±2.5V and an LSB 1.22mV.

If other values of the analog input signal are desired, change R_3 and R_4 in Figure 5 and R_2 in Figure 6. Regardless of resistor values chosen, the full range of 0V to +5V at A_{IN} must be maintained.

To obtain good performance over temperature in these configurations, the scaling resistors chosen should be of the same type and from the same manufacture, and be 0.1% tolerance.

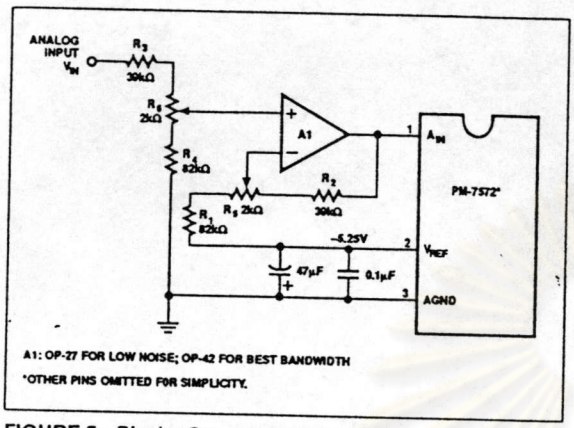


FIGURE 5: *Bipolar Operation (Offset Binary)*

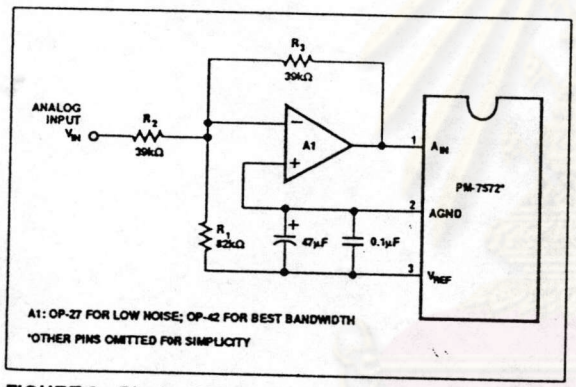


FIGURE 6: *Bipolar Operation (Complementary Offset Binary)*

OFFSET AND FULL-SCALE ERROR ADJUSTMENT BIPOLAR OPERATION

As with the unipolar adjustment, zero adjustment is performed first. Referring to Figure 5, apply 0.61mV (±1/2 LSB) analog input to V_{IN} and adjust R_5 until the successive digital output codes toggle between 1000 0000 0000 and 1000 0000 0001.

For the inverting configuration, Figure 6, replace R_1 with a potentiometer and adjust the output to toggle between 0111 1111 1111 and 0111 1111 1110.

Full-scale is adjusted (for Figure 5) by applying a FS - 1.5 LSB analog input signal to V_{IN} (for Consistency) and adjust R_6 until the successive digital output codes toggle between 1111 1111 1110 and 1111 1111 1111.

For Figure 6, apply 2.49817V at V_{IN} and adjust R_2 until the output code varies between 0000 0000 0001 and 0000 0000 0000.

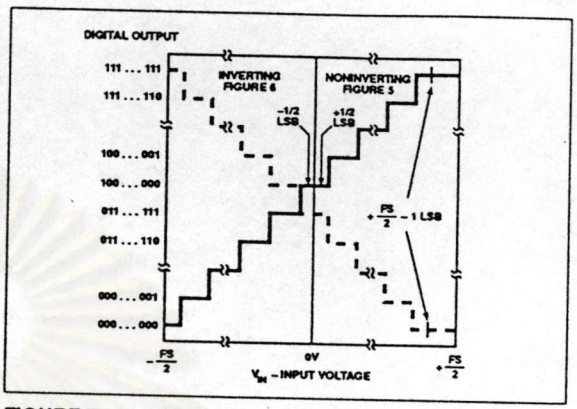


FIGURE 7: *Ideal Input/Output Transfer Characteristics for Bipolar Input Circuits*

DATA FORMAT

The PM-7572 has self-contained logic for both 8-bit and 16-bit data bus interfacing. Data output can be formatted into either a 12-bit parallel word for 16-bit data bus systems, or two byte word for an 8-bit data bus. The format is selected with HBEN that controls an internal multiplexer.

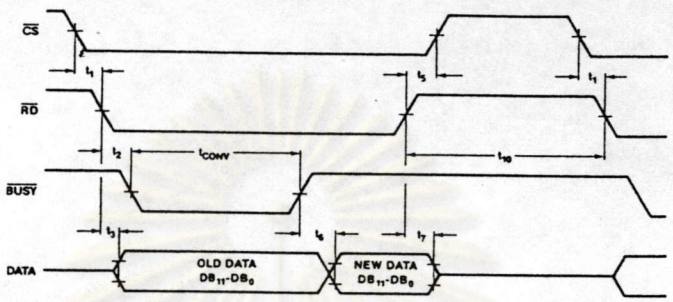
With HBEN LOW, converted data is directed to D_{11} ... $D_{0/8}$ outputs for the 12-bit data format. For two byte operation, data is presented to D_7 ... $D_{0/8}$ outputs. With HBEN LOW, the lower 8 bits are presented to the data outputs, and when HBEN goes high, the upper 4 bits are presented to the outputs with the leading 4 bits being low for D_7 ... $D_{0/8}$. See Pin Description table for pins 13-16. Note that the 4 MSBs always appear at the digital outputs D_{11} ... D_8 whenever the outputs are enabled, regardless of the state of HBEN.

CONVERSION MODES

The PM-7572's versatile processor interfacing offers two A/D conversion modes of operation for both data bus sizes. It offers the Slow-Memory mode and ROM mode. Processors that can be forced into WAIT states for the PM-7572's conversion time, can use the Slow-Memory mode. Other processors that cannot be forced into WAIT states can use the ROM mode. In both modes, a processor READ operation to the ADC address starts the conversion. A second READ operation is required to access the conversion result in the ROM mode.

SLOW-MEMORY MODE, PARALLEL READ (HBEN = LOW)

Slow-Memory mode is the simplest mode to use. It is the method of choice where compact coding is essential, or where software bugs are a hazard. In this mode, a single READ instruction will initiate a data conversion, interrupt the microprocessor until completion (WAIT states are introduced), then read the results.



SLOW-MEMORY MODE, PARALLEL READ DATA BUS STATUS

PM-7572 DATA OUTPUTS	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	$D_{3/11}$	$D_{2/10}$	$D_{1/9}$	$D_{0/8}$
READ	DB_{11}	DB_{10}	DB_9	DB_8	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0

FIGURE 8: *Parallel Read Timing Diagram, Slow-Memory Mode (HBEN = LOW)*

If the system throughput tolerates WAIT states and the hardware is correct, then Slow-Memory mode is virtually immune to subsequent software modifications. Placing the microprocessor in the WAIT state has the additional advantage of quieting digital systems to reduce noise pickup, especially in analog conversion circuitry. The Slow-Memory, 12-bit parallel mode provides the fastest analog sampling and digital data transfer rate for sampled data systems. The timing diagram and data bus status are shown in Figure 8.

The conversion process starts when $\overline{CS}$ and $\overline{RD}$ are taken low, the PM-7572 acknowledges that conversion is taking place by taking BUSY low. During this conversion period, data from the previous conversion appears at the digital outputs. At the end of conversion, the output latches are updated and the conversion result is placed on data outputs D_{11} ... $D_{0/8}$. BUSY returns high.

SLOW-MEMORY MODE, TWO BYTE READ

Slow-Memory mode can also be used for 8-bit data bus systems. The operation is the same as for the Slow-Memory mode, parallel load, with the addition of a second memory read with HBEN HIGH. The first read, with HBEN LOW, places the end of conversion data on the low data outputs, DB_7 ... DB_0. The second read, with HBEN HIGH, places the high byte data on outputs $D_{3/11}$ ... $D_{0/8}$, and disables conversion start. The timing diagram and data bus status are shown in Figure 9.

ROM MODE, PARALLEL READ (HBEN = LOW)

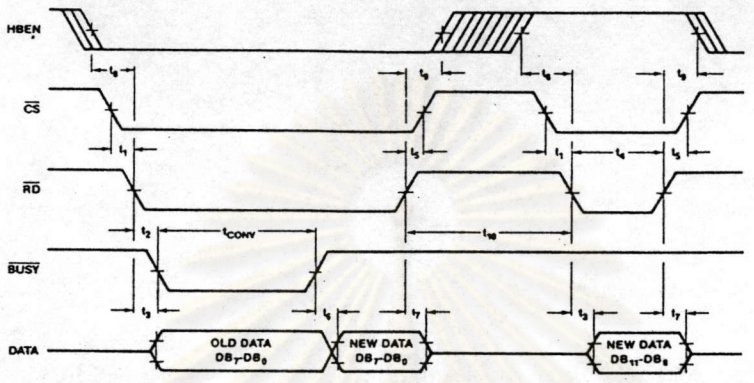
The ROM mode operates the same as for the Slow-Memory mode except that a second READ is taken. This mode avoids placing the microprocessor into a wait state. The first READ starts the conversion and places 12 bits of previous conversion on data outputs D_{11} ... $D_{0/8}$. This data, if not required, can be discarded. The second READ operation reads the new data, D_{11} ... DB_0, and starts another conversion. See the timing diagram and data bus status in Figure 10. The second read operation must have a delay time of at least as long as the PM-7572's conversion time.

ROM MODE, TWO BYTE READ

Data outputs D_7 ... $D_{0/8}$ are used for the two-byte READ mode. Conversion is started by taking READ LOW with HBEN LOW. The 8 LSBs from a previous conversion is then placed on the data outputs; this data can be discarded if not used. The new conversion results are then obtained with two more READ operations. The second READ operation, with HBEN HIGH, stops the conversion and places the high byte (4 MSBs) on the data outputs $D_{3/11}$ ... $D_{0/8}$. See the timing diagram and data bus status in Figure 11. A delay equal to the PM-7572's conversion time must be allowed between conversion start and the second data READ operation.

MICROPROCESSOR INTERFACING

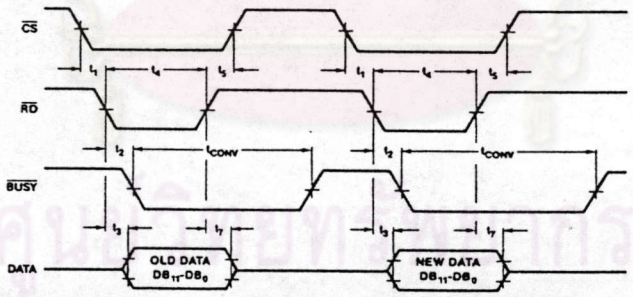
The PM-7572's interface structure allows interfacing to microprocessors as a memory mapped device. Control inputs, $\overline{CS}$ and $\overline{RD}$, are common to all peripheral memory interfacing. For 8-bit microprocessors, HBEN is connected to the microprocessor address bus for the data byte select. The PM-7572's 3-state data outputs allow direct connection to the data bus.



SLOW-MEMORY MODE, TWO-BYTE READ DATA BUS STATUS

PM-7572 DATA OUTPUTS	D_7	D_6	D_5	D_4	$D_{3/11}$	$D_{2/10}$	$D_{1/9}$	$D_{0/8}$
FIRST READ	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
SECOND READ	LOW	LOW	LOW	LOW	DB_{11}	DB_{10}	DB_9	DB_8

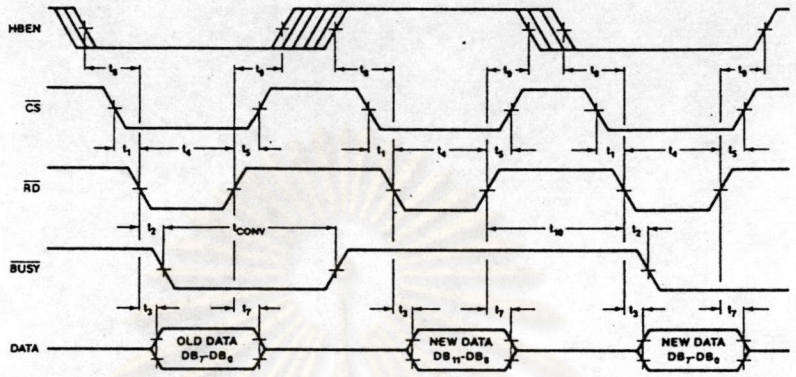
FIGURE 9: *Two-Byte Read Timing Diagram, Slow-Memory Mode*



SLOW-MEMORY MODE, TWO-BYTE READ DATA BUS STATUS

PM-7572 DATA OUTPUTS	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	$D_{3/11}$	$D_{2/10}$	$D_{1/9}$	$D_{0/8}$
FIRST READ	DB_{11}	DB_{10}	DB_9	DB_8	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
SECOND READ	DB_{11}	DB_{10}	DB_9	DB_8	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0

FIGURE 10: *Parallel Read Timing Diagram, ROM Mode (HBEN = LOW)*



SLOW-MEMORY MODE, TWO-BYTE READ DATA BUS STATUS

PM-7572 DATA OUTPUTS	D_7	D_6	D_5	D_4	$D_{3/11}$	$D_{2/10}$	$D_{1/9}$	$D_{0/8}$
FIRST READ	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
SECOND READ	LOW	LOW	LOW	LOW	DB_{11}	DB_{10}	DB_9	DB_8
THIRD READ	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0

FIGURE 11: *Two-Byte Read Timing Diagram, ROM Mode*

National Semiconductor

LF155/LF156/LF157 Series Monolithic JFET Input Operational Amplifiers

LF155/LF155A/LF255/LF355/LF355A/ LF355B Low Supply Current LF156/LF156A/LF256/LF356/LF356A/ LF356B Wide Band LF157/LF157A/LF257/LF357/LF357A/ LF357B Wide Band Decompensated ($A_{VMIN} = 5$)

General Description

These are the first monolithic JFET input operational amplifiers to incorporate well matched, high voltage JFETs on the same chip with standard bipolar transistors (BI-FET™ Technology). These amplifiers feature low input bias and offset currents/low offset voltage and offset voltage drift, coupled with offset adjust which does not degrade drift or common-mode rejection. The devices are also designed for high slew rate, wide bandwidth, extremely fast settling time, low voltage and current noise and a low 1/f noise corner.

Advantages

- Replace expensive hybrid and module FET op amps
- Rugged JFETs allow blow-out free handling compared with MOSFET input devices
- Excellent for low noise applications using either high or low source impedance—very low 1/f corner
- Offset adjust does not degrade drift or common-mode rejection as in most monolithic amplifiers
- New output stage allows use of large capacitive loads (10,000 pF) without stability problems
- Internal compensation and large differential input voltage capability

Applications

- Precision high speed integrators
- Fast D/A and A/D converters
- High impedance buffers
- Wideband, low noise, low drift amplifiers
- Logarithmic amplifiers
- Photocell amplifiers
- Sample and Hold circuits

Common Features

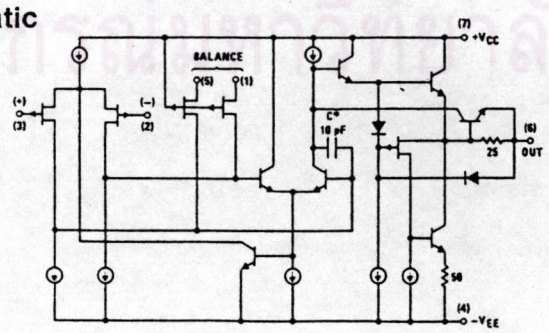
(LF155A, LF156A, LF157A)

- Low input bias current: 30 pA
- Low Input Offset Current: 3 pA
- High input impedance: $10^{12}\Omega$
- Low input offset voltage: 1 mV
- Low input offset voltage temp. drift: 3 μV/°C
- Low input noise current: 0.01 pA/√Hz
- High common-mode rejection ratio: 100 dB
- Large dc voltage gain: 106 dB

Uncommon Features

	LF155A	LF156A	LF157A ($A_V = 5$)	Units
■ Extremely fast settling time to 0.01%	4	1.5	1.5	μs
■ Fast slew rate	5	12	50	V/μs
■ Wide gain bandwidth	2.5	5	20	MHz
■ Low input noise voltage	20	12	12	nV/√Hz

Simplified Schematic



*3 pF in LF157 series.

TL/H/5646–1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

(Note 8)

	LF155A/6A/7A	LF155/6/7	LF355B/6B/7B LF255/6/7	LF355/6/7 LF355A/6A/7A
Supply Voltage	±22V	±22V	±22V	±18V
Differential Input Voltage	±40V	±40V	±40V	±30V
Input Voltage Range (Note 2)	±20V	±20V	±20V	±16V
Output Short Circuit Duration	Continuous	Continuous	Continuous	Continuous
T_{jMAX}				
H-Package	150°C	150°C	115°C	115°C
N-Package			100°C	100°C
J-Package		150°C	115°C	115°C
M-Package			100°C	100°C
Power Dissipation at T_A = 25°C (Notes 1 and 9)				
H-Package (Still Air)	560 mW	560 mW	400 mW	400 mW
H-Package (400 LF/Min Air Flow)	1200 mW	1200 mW	1000 mW	1000 mW
N-Package			670 mW	670 mW
J-Package		1260 mW	900 mW	900 mW
M-Package			380 mW	380 mW
Thermal Resistance (Typical) θ_{JA}				
H-Package (Still Air)	160°C/W	160°C/W	160°C/W	160°C/W
H-Package (400 LF/Min Air Flow)	65°C/W	65°C/W	65°C/W	65°C/W
N-Package			130°C/W	130°C/W
J-Package		100°C/W	100°C/W	100°C/W
M-Package			195°C/W	195°C/W
(Typical) θ_{JC}				
H-Package	23°C/W	23°C/W	23°C/W	23°C/W
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C
Soldering Information (Lead Temp.)				
Metal Can Package				
Soldering (10 sec.)	300°C	300°C	300°C	300°C
Dual-In-Line Package				
Soldering (10 sec.)		260°C	260°C	260°C
Small Outline Package				
Vapor Phase (60 sec.)			215°C	215°C
Infrared (15 sec.)			220°C	220°C
See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.				
ESD tolerance				
(100 pF discharged through 1.5 kΩ)	1200V	1200V	1200V	1200V

DC Electrical Characteristics (Note 3) $T_A = T_j = 25°C$

Symbol	Parameter	Conditions	LF155A/6A/7A			LF355A/6A/7A			Units
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input Offset Voltage	$R_S = 50\Omega$, $T_A = 25°C$ Over Temperature		1	2 2.5		1	2 2.3	mV mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	$R_S = 50\Omega$		3	5		3	5	µV/°C
$\Delta TC/\Delta V_{OS}$	Change in Average TC with V_{OS} Adjust	$R_S = 50\Omega$, (Note 4)		0.5			0.5		µV/°C per mV
I_{OS}	Input Offset Current	$T_j = 25°C$, (Notes 3, 5) $T_j \leq T_{HIGH}$		3	10 10		3	10 1	pA nA
I_B	Input Bias Current	$T_j = 25°C$, (Notes 3, 5) $T_j \leq T_{HIGH}$		30	50 25		30	50 5	pA nA
R_{IN}	Input Resistance	$T_j = 25°C$		10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	$V_S = \pm 15V$, $T_A = 25°C$ $V_O = \pm 10V$, $R_L = 2k$ Over Temperature	50 25	200		50 25	200		V/mV V/mV
V_O	Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10k$ $V_S = \pm 15V$, $R_L = 2k$	±12 ±10	±13 ±12		±12 ±10	±13 ±12		V V

DC Electrical Characteristics (Note 3) $T_A = T_j = 25°C$ (Continued)

Symbol	Parameter	Conditions	LF155A/6A/7A			LF355A/6A/7A			Units
			Min	Typ	Max	Min	Typ	Max	
V_{CM}	Input Common-Mode Voltage Range	$V_S = \pm 15V$	±11	+15.1 −12		±11	+15.1 −12		V V
CMRR	Common-Mode Rejection Ratio		85	100		85	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 6)	85	100		85	100		dB

AC Electrical Characteristics $T_A = T_j = 25°C$, $V_S = \pm 15V$

Symbol	Parameter	Conditions	LF155A/355A			LF156A/356A			LF157A/357A			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
SR	Slew Rate	LF155A/6A; $A_V = 1$, LF157A; $A_V = 5$	3	5		10	12		 40	 50		V/μs V/μs
GBW	Gain Bandwidth Product			2.5		4	4.5		15	20		MHz
t_s	Settling Time to 0.01%	(Note 7)		4			1.5			1.5		μs
e_n	Equivalent Input Noise Voltage	$R_S = 100\Omega$ f = 100 Hz f = 1000 Hz		 25 25			 15 12			 15 12		 nV/√Hz nV/√Hz
i_n	Equivalent Input Noise Current	f = 100 Hz f = 1000 Hz		0.01 0.01			0.01 0.01			0.01 0.01		pA/√Hz pA/√Hz
C_{IN}	Input Capacitance			3			3			3		pF

DC Electrical Characteristics (Note 3)

Symbol	Parameter	Conditions	LF155/6/7			LF255/6/7 LF355B/6B/7B			LF355/6/7			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input Offset Voltage	$R_S = 50\Omega$, $T_A = 25°C$ Over Temperature		3	5 7		3	5 6.5		3	10 13	mV mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	$R_S = 50\Omega$		5			5			5		μV/°C
$\Delta TC/\Delta V_{OS}$	Change in Average TC with V_{OS} Adjust	$R_S = 50\Omega$, (Note 4)		0.5			0.5			0.5		μV/°C per mV
I_{OS}	Input Offset Current	$T_j = 25°C$, (Notes 3, 5) $T_j \leq T_{HIGH}$		3	20 20		3	20 1		3	50 2	pA nA
I_B	Input Bias Current	$T_j = 25°C$, (Notes 3, 5) $T_j \leq T_{HIGH}$		30	100 50		30	100 5		30	200 8	pA nA
R_{IN}	Input Resistance	$T_j = 25°C$		10^{12}			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	$V_S = \pm 15V$, $T_A = 25°C$ $V_O = \pm 10V$, $R_L = 2k$ Over Temperature	50 25	200		50 25	200		25 15	200		V/mV V/mV
V_O	Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10k$ $V_S = \pm 15V$, $R_L = 2k$	±12 ±10	±13 ±12		±12 ±10	±13 ±12		±12 ±10	±13 ±12		V V
V_{CM}	Input Common-Mode Voltage Range	$V_S = \pm 15V$	±11	+15.1 −12		±11	±15.1 −12		+10	+15.1 −12		V V
CMRR	Common-Mode Rejection Ratio		85	100		85	100		80	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 6)	85	100		85	100		80	100		dB

DC Electrical Characteristics $T_A = T_j = 25°C, V_S = \pm 15V$

Parameter	LF155A/155, LF255, LF355A/355B		LF355		LF156A/156, LF256/356B		LF356A/356		LF157A/157 LF257/357B		LF357A/357		Units
	Typ	Max	Typ	Max	Typ	Max	Typ	Max	Typ	Max	Typ	Max	
Supply Current	2	4	2	4	5	7	5	10	5	7	5	10	mA

AC Electrical Characteristics $T_A = T_j = 25°C, V_S = \pm 15V$

Symbol	Parameter	Conditions	LF155/255/ 355/355B	LF156/256, LF356B	LF156/256/ 356/356B	LF157/257, LF357B	LF157/257/ 357/357B	Units
			Typ	Min	Typ	Min	Typ	
SR	Slew Rate	LF155/6: $A_V = 1$, LF157: $A_V = 5$	5	7.5	12	30	50	V/μs V/μs
GBW	Gain Bandwidth Product		2.5		5		20	MHz
t_s	Settling Time to 0.01%	(Note 7)	4		1.5		1.5	μs
e_n	Equivalent Input Noise Voltage	$R_S = 100\Omega$ f = 100 Hz f = 1000 Hz	25 20		15 12		15 12	nV/√Hz nV/√Hz
i_n	Equivalent Input Current Noise	f = 100 Hz f = 1000 Hz	0.01 0.01		0.01 0.01		0.01 0.01	pA/√Hz pA/√Hz
C_{IN}	Input Capacitance		3		3		3	pF

Notes for Electrical Characteristics

Note 1: The maximum power dissipation for these devices must be derated at elevated temperatures and is dictated by T_{jMAX}, θ_{jA}, and the ambient temperature, T_A. The maximum available power dissipation at any temperature is $P_d = (T_{jMAX} - T_A)/\theta_{jA}$ or the 25°C P_{dMAX}, whichever is less.

Note 2: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 3: Unless otherwise stated, these test conditions apply:

	LF155A/6A/7A LF155//6/7	LF255//6/7	LF355A/6A/7A	LF355B/6B/7B	LF355//6/7
Supply Voltage, V_S	$\pm 15V \le V_S \le \pm 20V$	$\pm 15V \le V_S \le \pm 20V$	$\pm 15V \le V_S \le \pm 18V$	$\pm 15V \le V_S \pm 20V$	$V_S = \pm 15V$
T_A	$-55°C \le T_A \le +125°C$	$-25°C \le T_A \le +85°C$	$0°C \le T_A \le +70°C$	$0°C \le T_A \le +70°C$	$0°C \le T_A \le +70°C$
T_{HIGH}	+125°C	+85°C	+70°C	+70°C	+70°C

and V_{OS}, I_B and I_{OS} are measured at $V_{CM} = 0$.

Note 4: The Temperature Coefficient of the adjusted input offset voltage changes only a small amount (0.5μV/°C typically) for each mV of adjustment from its original unadjusted value. Common-mode rejection and open loop voltage gain are also unaffected by offset adjustment.

Note 5: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_J. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, Pd. $T_j = T_A + \theta_{jA}$ Pd where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

Note 6: Supply Voltage Rejection is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.

Note 7: Settling time is defined here, for a unity gain inverter connection using 2 kΩ resistors for the LF155/6. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value from the time a 10V step input is applied to the inverter. For the LF157, $A_V = -5$, the feedback resistor from output to input is 2 kΩ and the output step is 10V (See Settling Time Test Circuit).

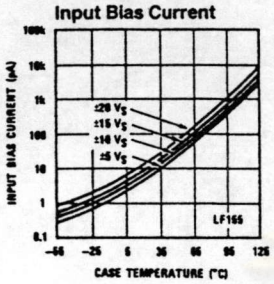
Note 8: Refer to RETS155AX for LF155A, RETS155X for LF155, RETSF156AX for LF156A, RETS156X for LF156, RETS157A for LF157A and RETS157X for LF157 military specifications.

Note 9: Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside guaranteed limits.

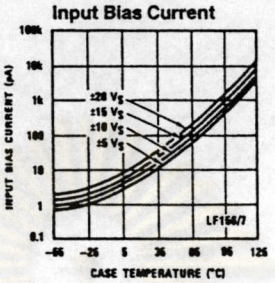
Typical DC Performance Characteristics

Curves are for LF155, LF156 and LF157 unless otherwise specified.

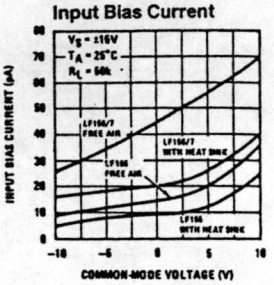
Input Bias Current



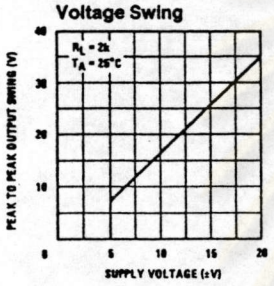
Input Bias Current



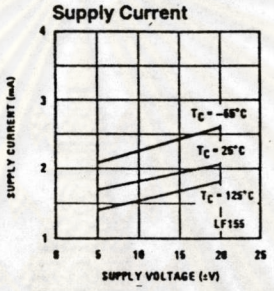
Input Bias Current



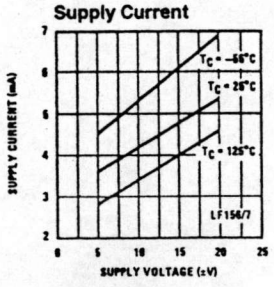
Voltage Swing



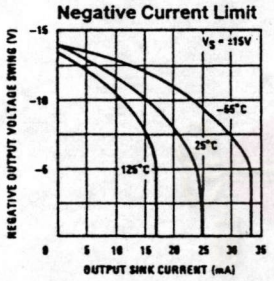
Supply Current



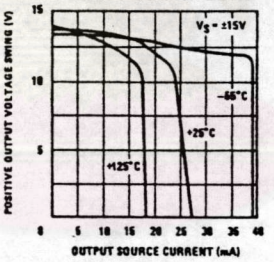
Supply Current



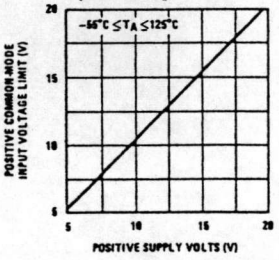
Negative Current Limit



Positive Current Limit

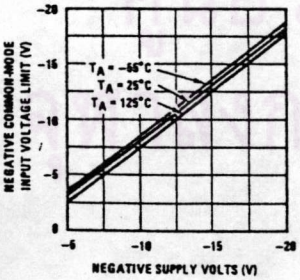


Positive Common-Mode Input Voltage Limit

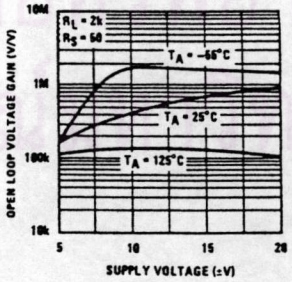


TL/H/5646–2

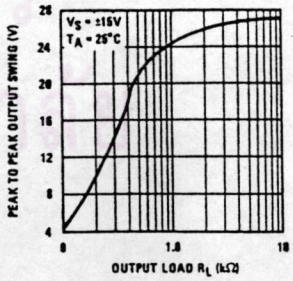
Negative Common-Mode Input Voltage Limit



Open Loop Voltage Gain



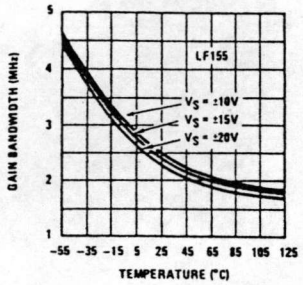
Output Voltage Swing



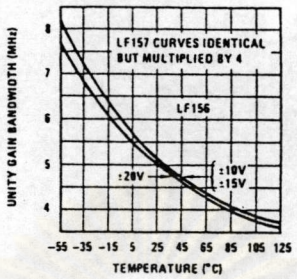
TL/H/5646–3

Typical AC Performance Characteristics

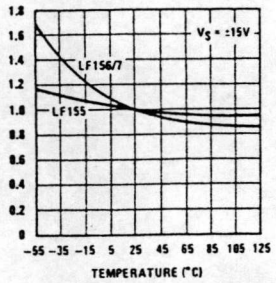
Gain Bandwidth



Gain Bandwidth

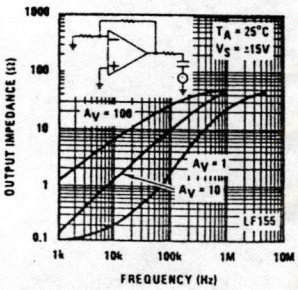


Normalized Slew Rate

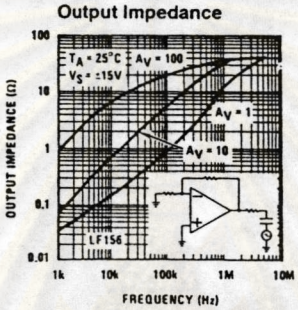


TL/H/5646–4

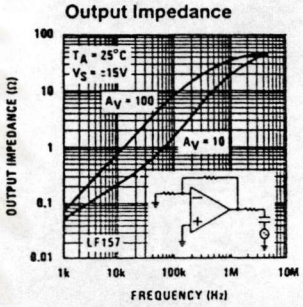
Output Impedance



Output Impedance

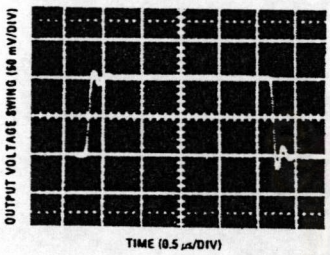


Output Impedance



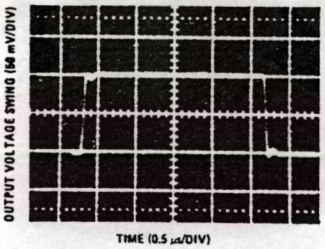
TL/H/5646–12

LF155 Small Signal Pulse Response, $A_V = +1$



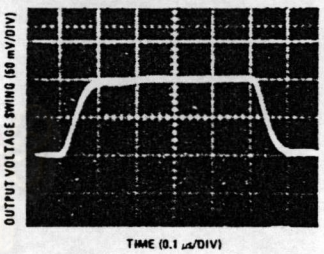
TL/H/5646–5

LF156 Small Signal Pulse Response, $A_V = +1$



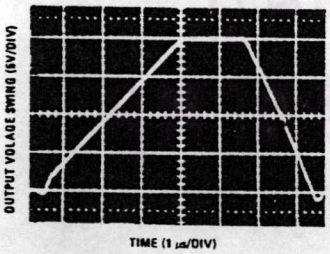
TL/H/5646–6

Small Signal Pulse Response, $A_V = +5$



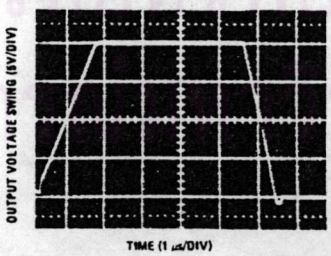
TL/H/5646–7

LF155 Large Signal Pulse Response, $A_V = +1$



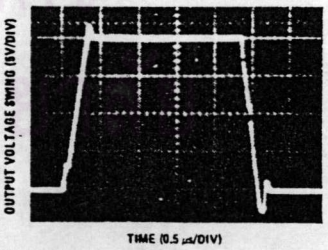
TL/H/5646–8

LF156 Large Signal Pulse Response, $A_V = +1$



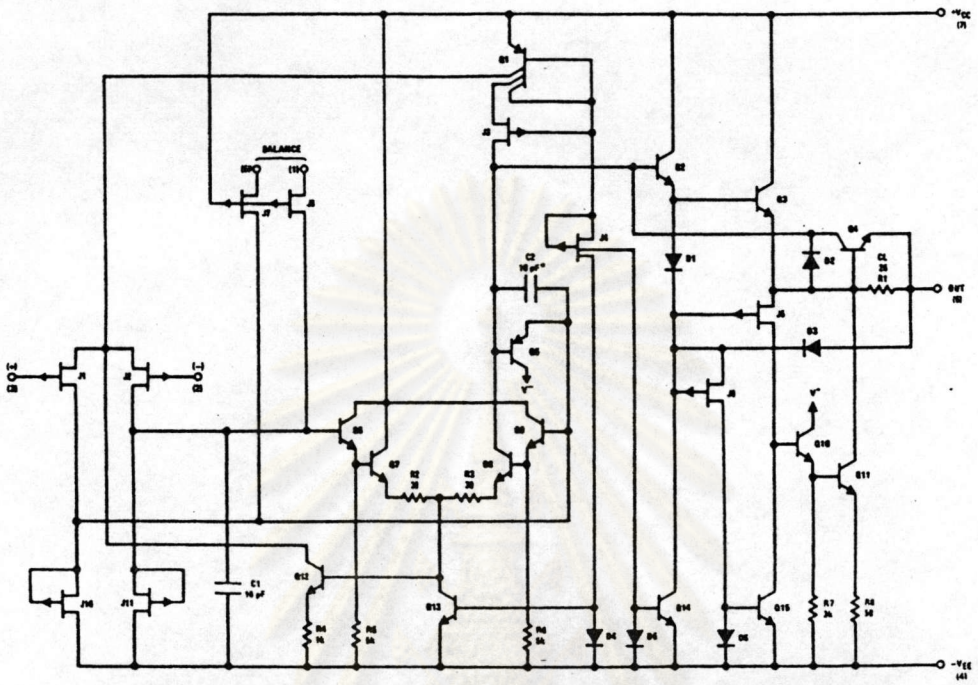
TL/H/5646–9

LF157 Large Signal Pulse Response, $A_V = +5$



TL/H/5646–10

Detailed Schematic

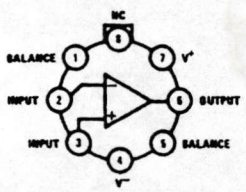


*C = 3 pF in LF157 series.

TL/H/5646–13

Connection Diagrams (Top Views)

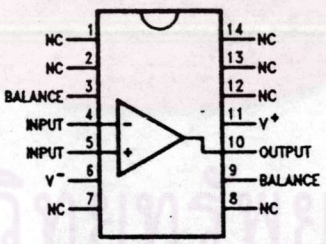
Metal Can Package (H)



TL/H/5646–14

Order Number
LF155AH, LF156AH, LF157AH,
LF155H, LF156H, LF157H,
LF255H, LF256H, LF257H,
LF355AH, LF356AH, LF357AH,
LF355BH, LF356BH, LF357BH,
LF355H, LF356H or LF357H
See NS Package Number H08C

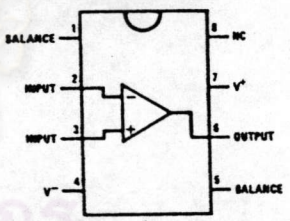
Dual-In-Line Package (J)



TL/H/5646–30

Order Number
LF155J, LF156J, LF157J,
LF355J, LF356J, LF357J,
LF355BJ, LF356BJ or LF357BJ
See NS Package Number J14A

Dual-In-Line Package (M and N)



TL/H/5646–29

Order Number
LF355M, LF356M, LF357M,
LF356BM, LF355BN, LF356BN,
LF357BN, LF355N, LF356N or
LF357N
See NS Package Number
M08A or N08E

3

Application Hints

The LF155/6/7 series are op amps with JFET input devices. These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore large differential input voltages can easily be accomodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

These amplifiers will operate with the common-mode input voltage equal to the positive supply. In fact, the common-mode voltage can exceed the positive supply by approximately 100 mV independent of supply voltage and over the full operating temperature range. The positive supply can therefore be used as a reference on an input as, for example, in a supply current monitor and/or limiter.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Because these amplifiers are JFET rather than MOSFET input op amps they do not require special handling.

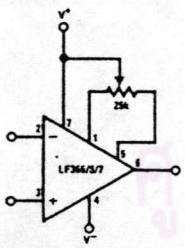
All of the bias currents in these amplifiers are set by FET current sources. The drain currents for the amplifiers are therefore essentially independent of supply voltage.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pickup" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to ac ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

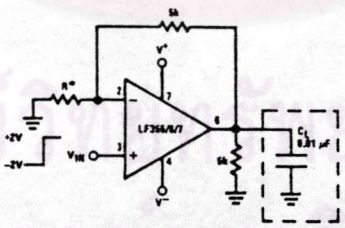
Typical Circuit Connections

V_{OS} Adjustment



- V_{OS} is adjusted with a 25k potentiometer
- The potentiometer wiper is connected to V+
- For potentiometers with temperature coefficient of 100 ppm/°C or less the additional drift with adjust is ≈ 0.5 μV/°C/mV of adjustment
- Typical overall drift: 5 μV/°C ±(0.5 μV/°C/mV of adj.)

Driving Capacitive Loads



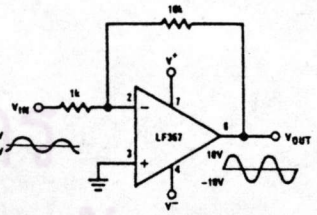
*LF155/6 R = 5k
LF157 R = 1.25k

Due to a unique output stage design, these amplifiers have the ability to drive large capacitive loads and still maintain stability. $C_{L(MAX)} \approx 0.01$ μF.

Overshoot ≤ 20%

Settling time (t_s) ≈ 5 μs

LF157. A Large Power BW Amplifier

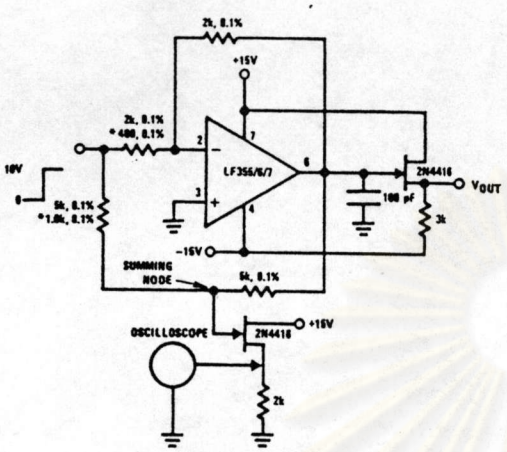


TL/H/5646–15

For distortion ≤ 1% and a 20 Vp-p V_{OUT} swing, power bandwidth is: 500 kHz.

Typical Applications

Settling Time Test Circuit

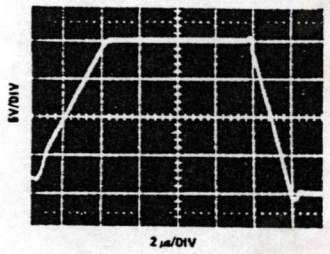


- Settling time is tested with the LF155/6 connected as unity gain inverter and LF157 connected for $A_V = -5$
- FET used to isolate the probe capacitance
- Output = 10V step
- $A_V = -5$ for LF157

TL/H/5646–16

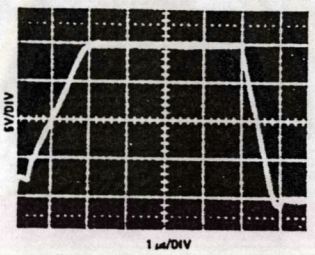
Large Signal Inverter Output, V_{OUT} (from Settling Time Circuit)

LF355



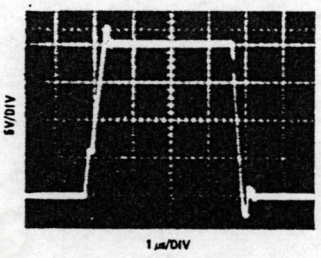
TL/H/5646–17

LF356



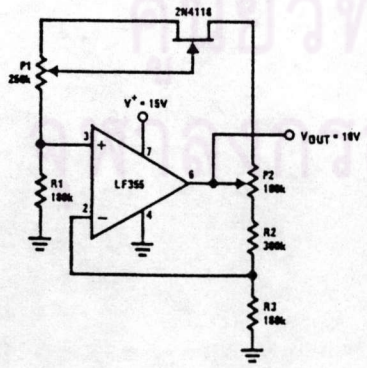
TL/H/5646–18

LF357



TL/H/5646–19

Low Drift Adjustable Voltage Reference

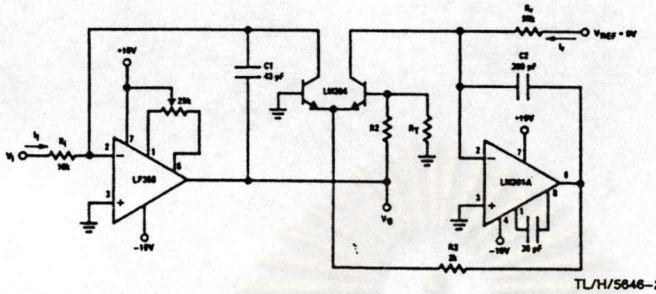


- $\Delta V_{OUT}/\Delta T = \pm 0.002\%/°C$
- All resistors and potentiometers should be wire-wound
- P1: drift adjust
- P2: V_{OUT} adjust
- Use LF155 for
  - Low I_B
  - Low drift
  - Low supply current

TL/H/5646–20

Typical Applications (Continued)

Fast Logarithmic Converter

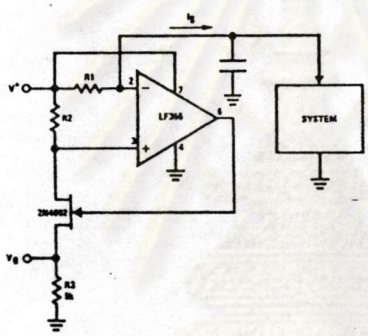


TL/H/5646–21

- Dynamic range: 100 μA ≤ I_I ≤ 1 mA (5 decades), $|V_O|$ = 1V/decade
- Transient response: 3 μs for ΔI_I = 1 decade
- C1, C2, R2, R3: added dynamic compensation
- V_{OS} adjust the LF156 to minimize quiescent error
- R_T: Tel Labs type Q81 + 0.3%/°C

$$|V_{OUT}| = \left[1 + \frac{R2}{R_T}\right]\frac{kT}{q}\ln V_I\left[\frac{R_T}{V_{REF}\,R_I}\right] = \log V_I\,\frac{1}{R_I}\,R2 = 15.7k,\ R_T = 1k,\ 0.3\%/°C \text{ (for temperature compensation)}$$

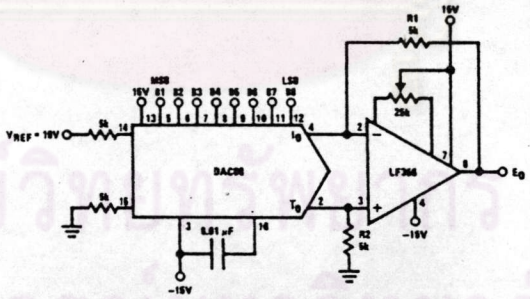
Precision Current Monitor



TL/H/5646–31

- V_O = 5 R1/R2 (V/mA of I_S)
- R1, R2, R3: 0.1% resistors
- Use LF155 for
  - Common-mode range to supply range
  - Low I_B
  - Low V_{OS}
  - Low Supply Current

8-Bit D/A Converter with Symmetrical Offset Binary Operation



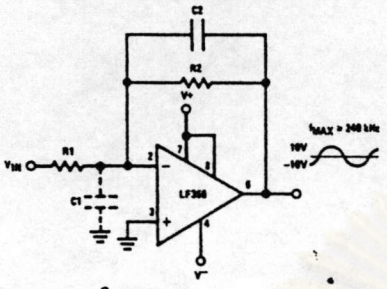
TL/H/5646–32

- R1, R2 should be matched within ±0.05%
- Full-scale response time: 3μs

E_O	B1	B2	B3	B4	B5	B6	B7	B8	Comments
+9.920	1	1	1	1	1	1	1	1	Positive Full-Scale
+0.040	1	0	0	0	0	0	0	0	(+) Zero-Scale
−0.040	0	1	1	1	1	1	1	1	(−) Zero-Scale
−9.920	0	0	0	0	0	0	0	0	Negative Full-Scale

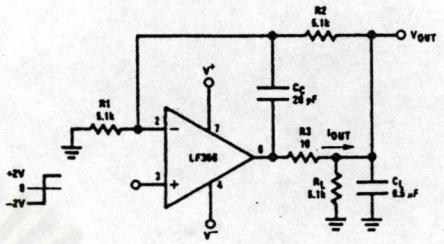
Typical Applications (Continued)

Wide BW Low Noise, Low Drift Amplifier



- Power BW: $f_{MAX} = \frac{S_r}{2\pi V_p} \simeq 240$ kHz
- Parasitic input capacitance C1 ≃ (3 pF for LF155, LF156 and LF157 plus any additional layout capacitance) interacts with feedback elements and creates undesirable high frequency pole. To compensate add C2 such that: R2C2 ≃ R1C1.

Isolating Large Capacitive Loads

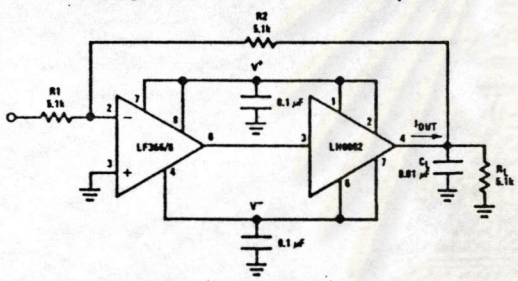


- Overshoot 6%
- t_s 10 μs
- When driving large C_L, the V_{OUT} slew rate determined by C_L and $I_{OUT(MAX)}$:

$$\frac{\Delta V_{OUT}}{\Delta T} = \frac{I_{OUT}}{C_L} \simeq \frac{0.02}{0.5} V/\mu s = 0.04\ V/\mu s \text{ (with } C_L \text{ shown)}$$

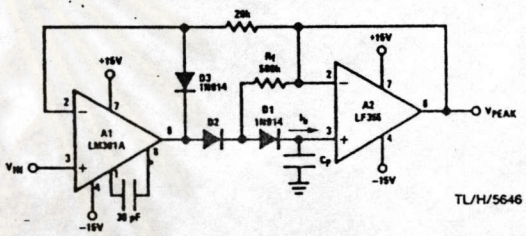
TL/H/5646–22

Boosting the LF156 with a Current Amplifier



- $I_{OUT(MAX)} \simeq 150$ mA (will drive $R_L \geq 100\Omega$)
- $\frac{\Delta V_{OUT}}{\Delta T} = \frac{0.15}{10^{-2}} V/\mu s$ (with C_L shown)
- No additional phase shift added by the current amplifier

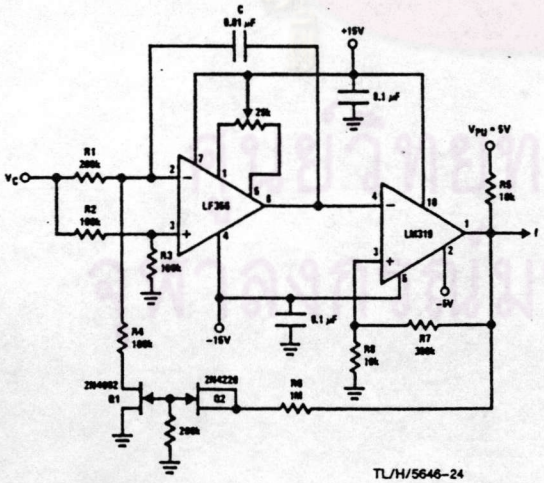
Low Drift Peak Detector



TL/H/5646

- By adding D1 and R_f, $V_{D1} = 0$ during hold mode. Leakage of D2 provided by feedback path through R_f.
- Leakage of circuit is essentially *Ib* (LF155, LF156) plus capacitor leakage of Cp.
- Diode D3 clamps V_{OUT} (A1) to $V_{IN} - V_{D3}$ to improve speed and to limit reverse bias of D2.
- Maximum input frequency should be $<< \frac{1}{2\pi R_f C_{D2}}$ where C_{D2} is the shunt capacitance of D2.

3 Decades VCO

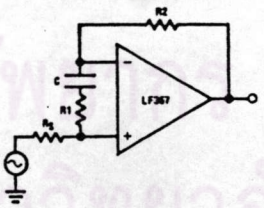


TL/H/5646–24

$f = \frac{V_C (R8 + R7)}{(8\ V_{PU}\ R8\ R1)\ C}$, $0 \leq V_C \leq 30V$, $10\ Hz \leq f \leq 10\ kHz$

R1, R4 matched. Linearity 0.1% over 2 decades.

Non-Inverting Unity Gain Operation for LF157



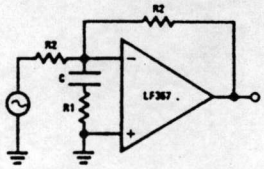
$R1C \geq \frac{1}{(2\pi)(5\ MHz)}$

$R1 = \frac{R2 + R_S}{4}$

$A_{V(DC)} = 1$

$f_{-3\ dB} \simeq 5$ MHz

Inverting Unity Gain for LF157



$R1C \geq \frac{1}{(2\pi)(5\ MHz)}$

$R1 = \frac{R2}{4}$

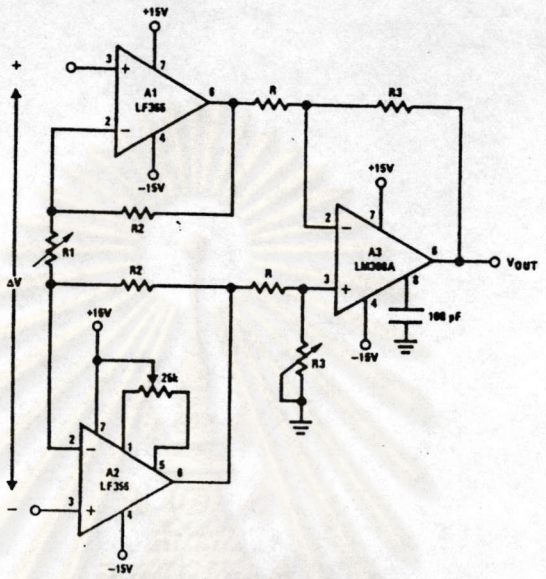
$A_{V(DC)} = -1$

$f_{-3\ dB} \simeq 5$ MHz

TL/H/5646–25

Typical Applications (Continued)

High Impedance, Low Drift Instrumentation Amplifier

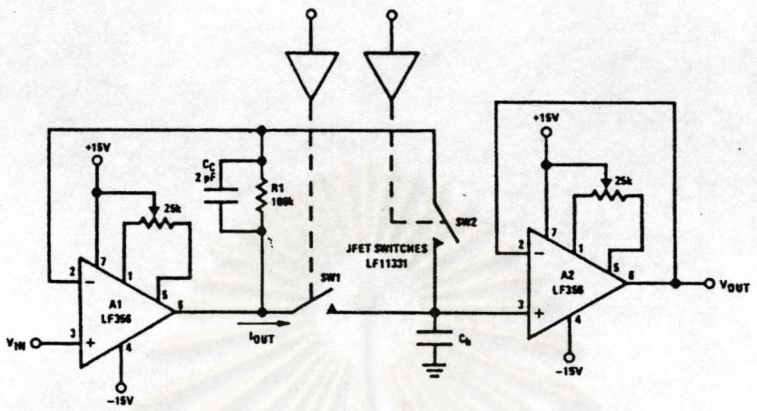


TL/H/5646–26

- $V_{OUT} = \frac{R3}{R}\left[\frac{2R2}{R1} + 1\right] \Delta V, V^- + 2V \leq V_{IN}$ common-mode $\leq V^+$
- System V_{OS} adjusted via A2 V_{OS} adjust
- Trim R3 to boost up CMRR to 120 dB. Instrumentation amplifier resistor array recommended for best accuracy and lowest drift

Typical Applications (Continued)

Fast Sample and Hold



TL/H/5646–33

- Both amplifiers (A1, A2) have feedback loops individually closed with stable responses (overshoot negligible)
- Acquisition time T_A, estimated by:

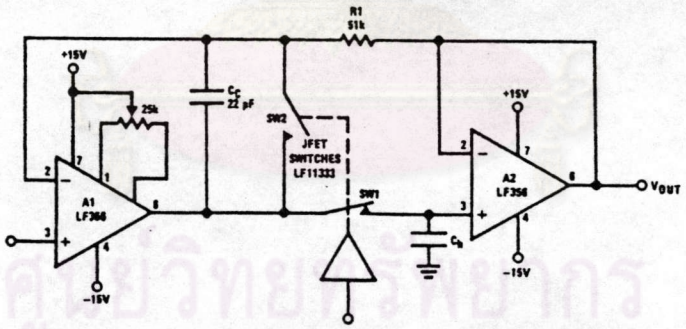
$$T_A \simeq \left[\frac{2R_{ON} \cdot V_{IN} \cdot C_h}{S_r}\right] \text{ ½ provided that:}$$

$$V_{IN} < 2\pi S_r R_{ON} C_h \text{ and } T_A > \frac{V_{IN} C_h}{I_{OUT(MAX)}}, R_{ON} \text{ is of SW1}$$

$$\text{If inequality not satisfied: } T_A \simeq \frac{V_{IN} C_h}{20\ mA}$$

- LF156 develops full S_r output capability for $V_{IN} \geq 1V$
- Addition of SW2 improves accuracy by putting the voltage drop across SW1 inside the feedback loop
- Overall accuracy of system determined by the accuracy of both amplifiers, A1 and A2

High Accuracy Sample and Hold

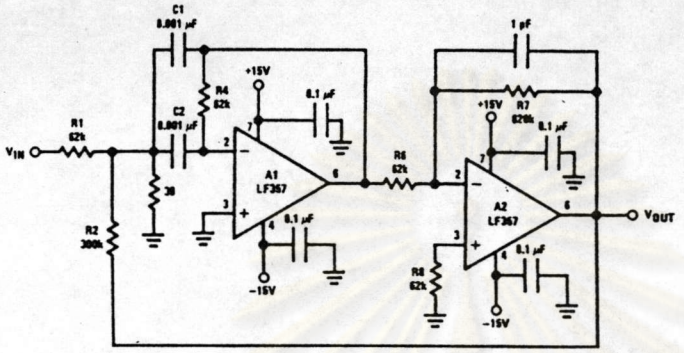


TL/H/5646–27

- By closing the loop through A2, the V_{OUT} accuracy will be determined uniquely by A1. No V_{OS} adjust required for A2.
- T_A can be estimated by same considerations as previously but, because of the added propagation delay in the feedback loop (A2) the overshoot is not negligible.
- Overall system slower than fast sample and hold
- R1, C_C: additional compensation
- Use LF156 for
  - Fast settling time
  - Low V_{OS}

Typical Applications (Continued)

High Q Band Pass Filter



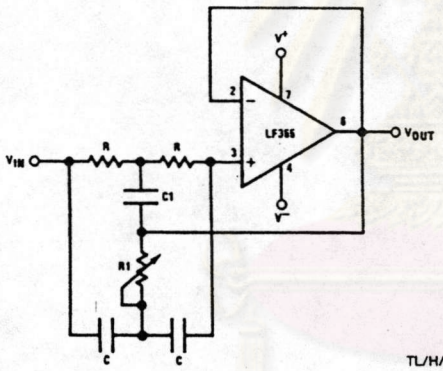
TL/H/5646–28

- By adding positive feedback (R2) Q increases to 40
- f_{BP} = 100 kHz

$$\frac{V_{OUT}}{V_{IN}} = 10\sqrt{Q}$$

- Clean layout recommended
- Response to a 1 Vp-p tone burst: 300 µs

High Q Notch Filter



TL/H/5646–34

- 2R1 = R = 10 MΩ
  2C = C1 = 300 pF
- Capacitors should be matched to obtain high Q
- f_{NOTCH} = 120 Hz, notch = −55 dB, Q > 100
- Use LF155 for
  - Low I_B
  - Low supply current

MICRO POWER SYSTEMS

ภาคผนวก ข.

ข้อมูลวงจรรวม

CMOS 11ビット, 1MHz フラッシュA/Dコンバータ

MP7685

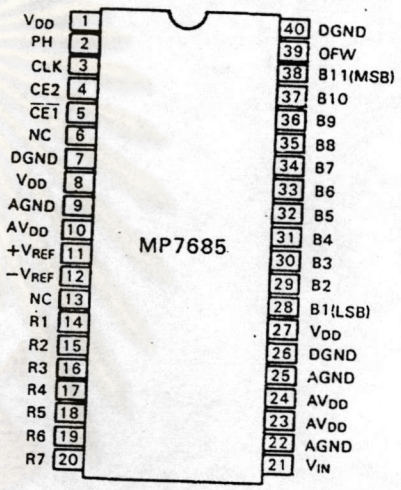
特　長

- 11ビット分解能
- 1 MHz サンプル・レート
- ±1LSB 精度
- 低消費電力　150mW typ
- +3V～+8V単一電源動作
- 2個直列使いで12ビット分解能

アプリケーション

- ハイブリッドADCの低価格/高性能版としての置き換え
- 高分解能、高速、ローパワーを必要とする用途
- 振動分析器
- 高速マルチプレクスト・データ集収

ピン接続図



概　要

MP7685KDは、マイクロ・パワー・システムズ社の誇るモリブデンゲートCMOSプロセスを駆使して開発された高速変換11ビット・モノリシックA/Dコンバータです。CMOS構造かつフラッシュ・タイプで11ビットという高分解能を実現した業界初のモデルで、低消費電力と高速変換速度を要求する用途に最適です。MP7685KDは、40ピン・サーディップの1タイプのみで、0°C～+70°Cの温度範囲で動作します。

いわゆる直並列比較方式のA/Dコンバータで、2ステップのフラッシュ技術が使用されており、A/D変換は2つのセグメントによって行なわれます。まず第一のセグメントは32個のラッチ付オートバランス・コンパレータ、エンコーダ、およびバッファストレージ・レジスタによって構成され、上位5ビットの変換を行ないます。一方、64個のコンパレータから成る第2のセグメントによって、下位6ビットのA/D変換が行なわれます。

MP7685KDは3Vから8Vまでの単一電源で動作し、変換時間は1μs typ、また消費電力は150mW typ(200mW max.)とローパワーになっています。またオーバーフロー・ビットを利用することによって、MP7685KDを2個直列使いで12ビット分解能を得ることができます。

11ビット分解能で1 MHz の動作を可能にしたマイクロ・パワー・システムズ社のモリブデンゲート・プロセスは、シート抵抗がわずか0.5Ω/□で、通常のポリシリコンに比べて1/100となっており、このため10ミクロン長当たりの遅延はわずか0.5psです。モリブデンはゲートのみならず、2層配線の第一配線としても使用されています。この配線ともう一つのアルミ配線とによってオートゼロのキャパシタが形成されています。

仕　様　(特に指定のない限り、25℃、V_{DD}＝＋5V、V_{REF}＝＋4V，Clock 1MHz)

パラメータ	MIN	TYP	MAX	単位	試験条件/備考
分解能			11	ビット	
精度					
非直線性誤差		±1	±2	LSB	
微分非直線性誤差		±1	±2	LSB	
量子化誤差	−1/2		+1/2	LSB	
アナログ入力					
フルスケール範囲	V_{SS}		V_{DD}	V	$3V_{p-p}$ Min
入力容量[1]		60		pF	
入力インピーダンス[1]	100			KΩ	
ラダー抵抗[2]	1.0	1.8		KΩ	
レファレンス電圧		5.0	V_{DD}	V	
最高変換速度	0.5	1.0		MHz	
アパチャ時間[1]		20		ns	
デジタル出力ディレイ(Td)[2]		40		ns	
デジタル入力[1]					
ロジック "0" 電圧			1.5	V	
ロジック "1" 電圧	3.5			V	
入力電流		1.0	10	μA	
デジタル出力[1]					
出力LOW(シンク)電流	2			mA	V_O=0.4V
出力HIGH(ソース)電流	1			mA	$V_O=V_{DD}-0.4V$
OFF電流		1.0	10	μA	
デバイス電流(I_{REF}を除く)[2]		12	20	mA	CLK=1MHz
電源電圧 V_{DD}	3.0	5.0	8	V	

注）1. 設計のみの保証で、製品検査は行なっていません。
2. 仕様を満足するように、＋25℃でサンプル・テストをしています。
＊ 仕様は予告なしに変更することがあります。

絶対最大定格

(特に指定のない限り、T_A＝＋25℃)

V_{DD}(対V_{SS})……＋7V
＋REF、−REF……V_{SS}〜V_{DD}
V_{IN}……V_{SS}〜V_{DD}
デジタル入力……V_{SS}〜V_{DD}
デジタル出力……V_{SS}〜V_{DD}
動作温度範囲……−25℃〜＋85℃
保存温度……−65℃〜＋150℃
リード温度(ハンダ付け、10秒)……＋300℃

注意
絶対最大定格に示された以上のストレスを加えると、デバイスは永久的に破損する場合があります。また、これはストレスの定格のみを示すもので、この動作仕様に示されている値以上の条件または最大定格では、機能動作することは保証していません。デバイスの信頼性を損うことがありますので、絶対最大定格の条件下に長時間置かないで下さい。

構成

7685KDの内部回路は、図1のブロック図に示される7つの主要機能ブロックから構成されています。すなわち2048個のレファレンス抵抗、スイッチ・マトリックス、2個のラッチされたコース(coarse. 粗い)コンパレータ、2個のラッチされたファイン(fine. 細い)コンパレータ、コース・エンコーダ、ファイン・エンコーダ、クロック・バッファおよびデータ出力バッファです。クロック・バッファによって、外部から印加されるクロックよりタイミングが少し遅れた内部クロックが発生します。

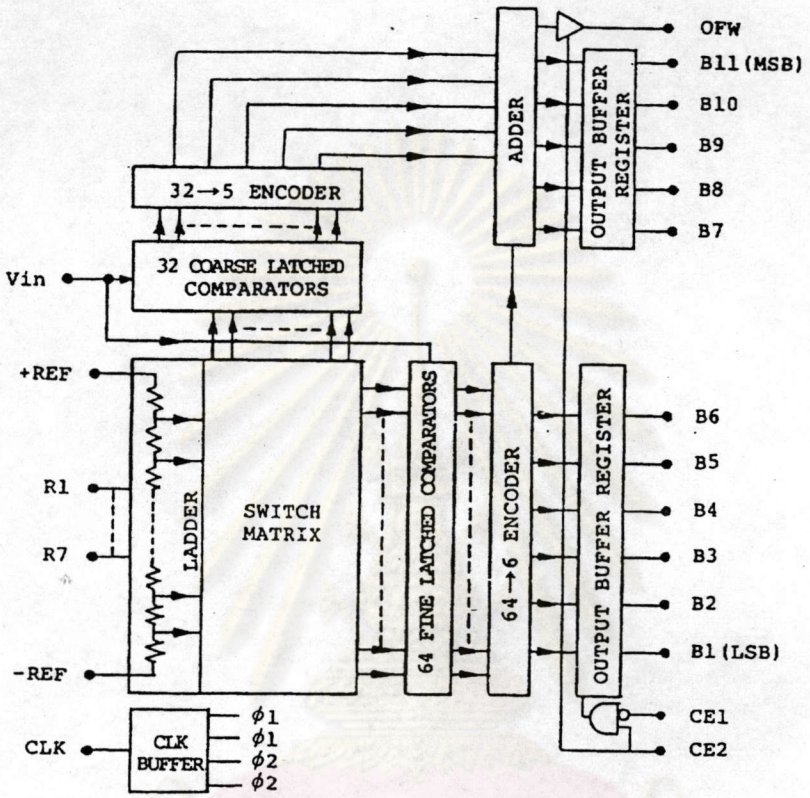


図1. MP7685KDのブロック図

ベイス動作

2のタイミング・チャートにおいて、A／D変換は1ック・サイクル毎に行われます。ピン2のPhaseコントレへの信号レベルによって、クロックの極性を選択することができます。

まPhase＝0の場合を考えると、サンプル・フェーズりの立上りパルスで、その時点での入力電圧をA／Dバータは取り込み、直ちに上位5ビットをA／D変換す。次にオートバランス・フェーズの終りの立下りパで、先に取り込んだ入力値の下位6ビットのA／D変行ないます。続いて、サンプル・フェーズの終りの立ッジで、オーバフロー・ビットを含めた12ビットのが出力レジスタに転送され、デジタル出力ディレイTd)の後に、デジタル出力が得られます。

ミりサンプル・フェーズの終りの立上りエッジのタイで、アナログ入力電圧をA／Dコンバータに取り込と、1クロック・サイクル前に取り込まれたアナロ電圧を、デジタル値として出力する作業の2つが同行われます。

7685KDの内部には、デジタルV_{DD}とアナログV_{DD}の2源回路があるため、対ラッチアップという点から一応の注意が必要です。まずアナログ入力、レファレンス電圧、およびクロックは、V_{SS}～V_{DD}という条件があります。V_{SS}を接地するとコンバータはV_{DD}のみの単一電源で動作しますが、上の条件を満すためにはまずV_{DD}が先に(または同時に)オンする必要があります。

アナログV_{IN}(ピン21)、REF(ピン11)、クロック(ピン3)の端子にショットキ・ダイオードを使用して、これらの電圧レベルを0V～V_{DD}にクランプして下さい。デジタルV_{DD}とアナログV_{DD}は、できるだけICに近いところで接続してから単一の+5Vに接続します。またDGNDとAGNDもICの近くで接続してから、共通のグランドに落します。

3ステート・バッファは、$\overline{CE1}$とCE2の2つのチップ・イネーブル信号によってコントロールされます。

$\overline{CE1}$	CE2	B1－B11	OFW
0	1	有効	有効
1	1	トライステート	有効
X	0	トライステート	トライステート

1＝HIGH, 0＝LOW, X＝ドントケア

表1. 真理値表

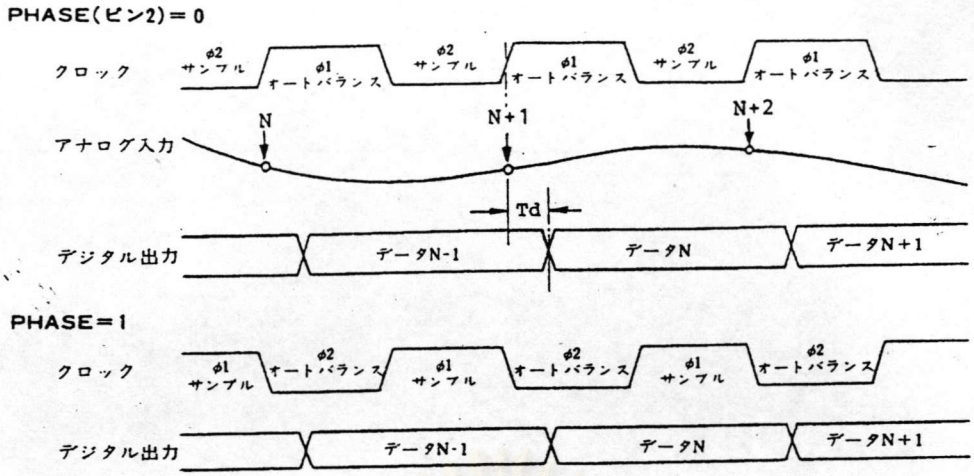
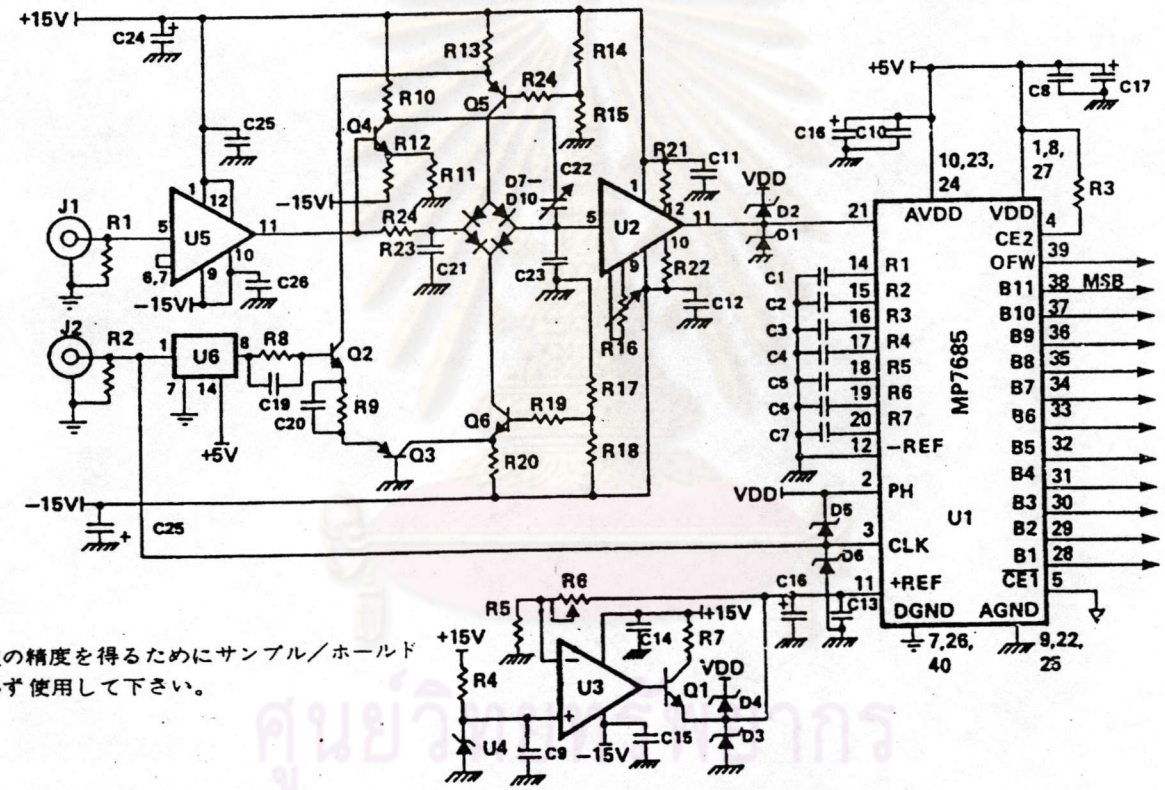


図2. タイミング図

回路例



注）規定の精度を得るためにサンプル／ホールドを必ず使用して下さい。

図3. MP7685LDの使用回路例

パーツ・リスト

IC

U1 ..... MP7685 ADC
U2 ..... MP2004 Buffer/Amp
U3 ..... MPOP02 Op Amp
U4 ..... MP5010 Voltage Ref (1.22 V)
U5 ..... MP2004 Buffer/Amp
U6 .... Delay Line (Bel Fuse Delay Line)
Part No. 0447-100-02)

コンデンサ

C1 - C15 ..... 0.1 μf mylar
C16 - C18 ..... Tantalum (>10μf)
C19 ..... 10 pf
C20 ..... 22 pf
C21 ..... 20 pf
C22 ..... Variable Cap
C23 ..... 680 pf
C24, 25 ..... Tantalum (>10μf)

抵抗

(指定のない限り、抵抗はすべて1%のメタル・フィルム)

R1, R2 .... Terminating R's
R3 ..... 1 KΩ
R4 ..... 20 KΩ
R5 ..... 1 KΩ
R6 ..... 5 KΩ Trimpot
R7 ..... 100 Ω
R8 ..... 100 Ω
R9 ..... 100 Ω
R10 ..... 430 Ω
R11 ..... 1.5 KΩ
R12 ..... 750 Ω
R13 ..... 560 Ω
R14 ..... 1.5 KΩ
R15 ..... 1 KΩ
R16 ..... 500 Ω Trimpot
R17 ..... 1 KΩ
R18 ..... 1 KΩ
R19 ..... 100 Ω
R20 ..... 560 Ω
R21 ..... 150 Ω, 1/4w Carbon
R22 ..... 150 Ω, 1/4w Carbon
R23 ..... 100 Ω
R24 ..... 160 Ω

ダイオード

D1 - D6 ..... Schottky
(NEC 1SS101 ,HP HSCH-1001)
D7 - D10 ..... Schottky
(HP5082-2811)

トランジスタ

Q2, Q4, Q6 ..... 2N5179
Q3, Q5 ..... 2N5910

アプリケーション

1．基板として、低インピーダンスのグランドプレーン(通称ベタアース）を持ったＰＣＢの使用を推奨します。またアナログＧＮＤとデジタルＧＮＤは、グランドループをさけるため一点アースにすることが望ましいです。

2．電源Vddとレファレンス電圧はＩＣにできるだけ近いところで、.01−0.1μFのセラミック・コンデンサと10μFのタンタル・コンデンサでデカップリングします。

3．アナログ入力回路は高スルーレート、高帯域特性を持ったビデオ・オペアンプ、バッファ、あるいはエミッタ・フォロアを使用してインピーダンスをできるだけ低く（＜25Ω）します。

4．アナログ入力は最もクリティカルであり、クロックやデジタル出力からはできるだけ離し、これらとのクロスカップリングを最小に抑え、かつノイズがのらないようにします。

5．コンバータ内のコンパレータのオフセットによる誤差を抑え、特性表の非直線精度を得るために、ピン21でのアナログ入力信号の振幅は3V$_{p-p}$以上とします。

6．AVDDラインにインダクタ(100μH)を挿入して、クロックノイズがVDDに流れ込まないようにします。

7．クロックとしては、デューティ・サイクルがほぼ50：50のものを推奨します。50：50の比率から多少ずれた所に最良の性能が得られる場合があります。

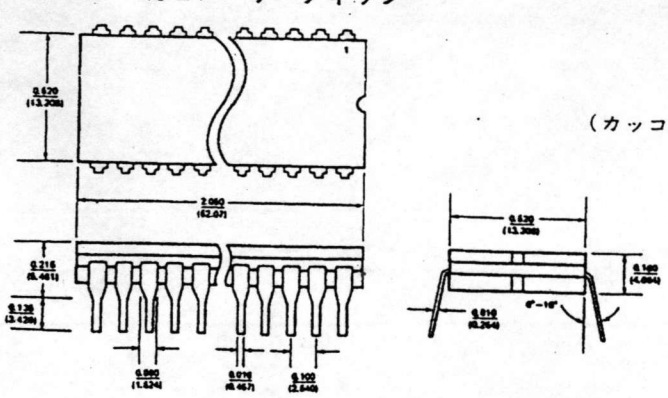
8．デジタル出力ピンからのリード線はできるだけ短くして、容量性カップリングや反射によるノイズを抑えます。離れた負荷をドライブする際は、バッファを使用します。

アナログ入力		デジタル出力											
	VREF=4.096	OFW	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1
OF	4.096V	1	1	1	1	1	1	1	1	1	1	1	1
FS	4.094	0	1	1	1	1	1	1	1	1	1	1	1
FS-1LSB	4.092	0	1	1	1	1	1	1	1	1	1	1	0
FS-2LSB	4.090	0	1	1	1	1	1	1	1	1	1	0	1
3/4FS	3.072	0	1	1	0	0	0	0	0	0	0	0	0
1/2FS+1LSB	2.050	0	1	0	0	0	0	0	0	0	0	0	1
1/2FS	2.048	0	1	0	0	0	0	0	0	0	0	0	0
1/2FS-1LSB	2.046	0	0	1	1	1	1	1	1	1	1	1	1
1/4FS	1.024	0	0	1	0	0	0	0	0	0	0	0	0
2LSB	0.004	0	0	0	0	0	0	0	0	0	0	1	0
1LSB	0.002	0	0	0	0	0	0	0	0	0	0	0	1
0	0.000	0	0	0	0	0	0	0	0	0	0	0	0

表2. 出力コード表

パッケージ

40ピン・サーディップ



（カッコ内：mm）

ภาคผนวก ค.

รายการอธิบายคำย่อ

Signal	Definition
ACQ	Acquire. Bistable output indicating the analyzer is in the PHA or MCS modes.
AD0 through	ADC address outputs.
ADC IN	High level (0 to +4 volts) input to ADC
AOF	Address Over Flow. Indicates address scaler use in display and MCS has exceeded the group size.
AOS	Start monostable for the Analysis mode
CFS	Calibrate Full Scale. True when calibrating plotter full-scale output.
CHO	Channel 0. True when in the least significant address where experiment time is recorded.
CLEAR	Frees the ADC to accept new data. Occurs when memory has completed storage of previous event.
DT	Dead Time. Signal indicating busy condition of ADC. Used to gate time base clock for dead time correction.
DTM	Dead Time Meter. Integrated DT signal for driving front panel % DEAD TIME meter
FUL	Full memory. Switch condition selecting full memory for analysis and display.
GATE	Gate input to ADC allowing selective strobing of input information
LTM	Live Time Memory cycle. Flag denoting that ADC STORE command is for time as opposed to input data.
LTS	One seconds output of time base which sets LTM
MCS	Multichannel Scaling. True during this analysis mode.
MMOD	Memory Modified. Gate signal during MCS which allows counting during the dwell period and inhibits counting when the address is being changed.
PHA	Pulse Height Analysis. True when this mode is active.

SCA — Single Channel Analyzer output pulse. Delivers a.1 μSec positive TTL logic pulse (3.5 V) for any event occuring within the LLD and ULD window. The SCA output is triggered when the peak of the analog input pulse is detected. The SCA output is gated off when the ADC is busy, so that only analyzed events will generate an SCA output pulse. The SCA output is bracketed by the LLD and ULD in either PHA or MCS mode.

STORE — Flag from ADC indicating a valid event requires storage in memory

ประวัติผู้เขียน

นายบัญชา อุนพานิช เกิดวันที่ 10 มิถุนายน พ.ศ. 2504 ที่ อำเภอวัดสิงห์ จังหวัดชัยนาท สำเร็จการศึกษาปริญญาตรีครุศาสตร์อุตสาหกรรมบัณฑิต สาขาวิชาวิศวกรรมไฟฟ้าสื่อสาร จากสถาบันเทคโนโลยีราชมงคล วิทยาเขตเทเวศน์ ในปีการศึกษา 2534 แล้วศึกษาต่อปริญญาโท ที่ภาควิชานิวเคลียร์เทคโนโลยี คณะวิศวกรรมศาสตร์ จุฬาลงกรณ์มหาวิทยาลัย ปัจจุบันทำงานตำแหน่ง นายช่างอิเล็กทรอนิกส์ระดับ 5 ที่ ภาควิชานิวเคลียร์เทคโนโลยี คณะวิศวกรรมศาสตร์ จุฬาลงกรณ์มหาวิทยาลัย