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APPENDICES

Appendix A

PHASE LOCKED LOOP DATA

PHASE-LOCKED LOOP

The HEF4046B is a phase-locked loop circuit that consists of a linear voltage controlled oscillator (VCO) and two different phase comparators with a common signal input amplifier and a common comparator input. A 7 V regulator (zener) diode is provided for supply voltage regulation if necessary. For functional description see further on in this data.

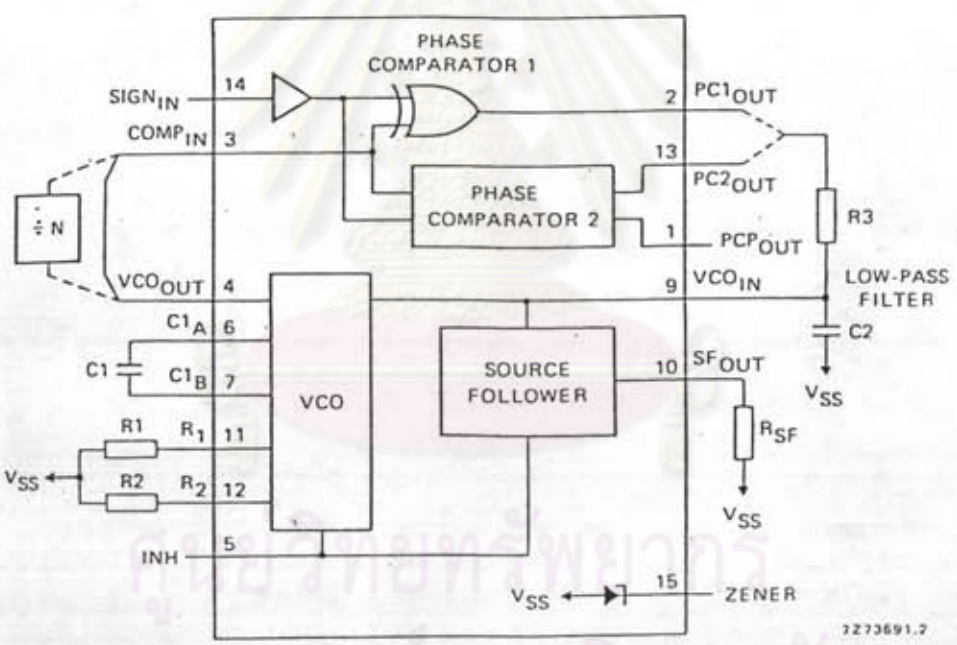


Fig. 1 Functional diagram.

HEF4046BP: 16-lead DIL; plastic (SOT-38Z).
HEF4046BD: 16-lead DIL; ceramic (SOT-74).
HEF4046BT: 16-lead flat pack; plastic (SO-16; SOT-109A).

FAMILY DATA: see Family Specifications

I_{DD} LIMITS category MSI: see further on in this data.

Products approved to CECC 90 104-035.

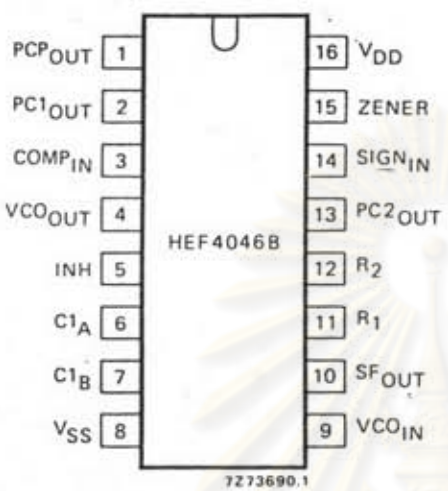


Fig. 2 Pinning diagram.

PINNING

1. Phase comparator pulse output
2. Phase comparator 1 output
3. Comparator input
4. VCO output
5. Inhibit input
6. Capacitor C1 connection A
7. Capacitor C1 connection B
8. V_{SS}
9. VCO input
10. Source-follower output
11. Resistor R1 connection
12. Resistor R2 connection
13. Phase comparator 2 output
14. Signal input
15. Zener diode input for regulated supply.

FUNCTIONAL DESCRIPTION

VCO part

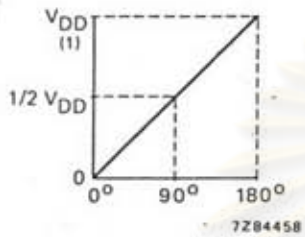
The VCO requires one external capacitor (C1) and one or two external resistors (R1 or R1 and R2). Resistor R1 and capacitor C1 determine the frequency range of the VCO. Resistor R2 enables the VCO to have a frequency off-set if required. The high input impedance of the VCO simplifies the design of low-pass filters; it permits the designer a wide choice of resistor/capacitor ranges. In order not to load the low-pass filter, a source-follower output of the VCO input voltage is provided at pin 10. If this pin (SF_{OUT}) is used, a load resistor (R_{SF}) should be connected from this pin to V_{SS}; if unused, this pin should be left open. The VCO output (pin 4) can either be connected directly to the comparator input (pin 3) or via a frequency divider. A LOW level at the inhibit input (pin 5) enables the VCO and the source follower, while a HIGH level turns off both to minimize stand-by power consumption.

Phase comparators

The phase-comparator signal input (pin 14) can be direct-coupled, provided the signal swing is between the standard HE4000B family input logic levels. The signal must be capacitively coupled to the self-biasing amplifier at the signal input in case of smaller swings. Phase comparator 1 is an EXCLUSIVE-OR network. The signal and comparator input frequencies must have a 50% duty factor to obtain the maximum lock range. The average output voltage of the phase comparator is equal to ½ V_{DD} when there is no signal or noise at the signal input. The average voltage to the VCO input is supplied by the low-pass filter connected to the output of phase comparator 1. This also causes the VCO to oscillate at the centre frequency (f_o). The frequency capture range (2 f_c) is defined as the frequency range of input signals on which the PLL will lock if it was inititally out of lock. The frequency lock range (2 f_L) is defined as the frequency range of input signals on which the loop will stay locked if it was initially in lock. The capture range is smaller or equal to the lock range.

With phase comparator 1, the range of frequencies over which the PLL can acquire lock (capture range) depends on the low-pass filter characteristics and this range can be made as large as the lock range. Phase comparator 1 enables the PLL system to remain in lock in spite of high amounts of noise in the input signal. A typical behaviour of this type of phase comparator is that it may lock onto input

frequencies that are close to harmonics of the VCO centre frequency. Another typical behaviour is, that the phase angle between the signal and comparator input varies between 0° and 180° and is 90° at the centre frequency. Figure 3 shows the typical phase-to-output response characteristic.



(1) Average output voltage.

Fig. 3 Signal-to-comparator inputs phase difference for comparator 1.

Figure 4 shows the typical waveforms for a PLL employing phase comparator 1 in locked condition of f_o.

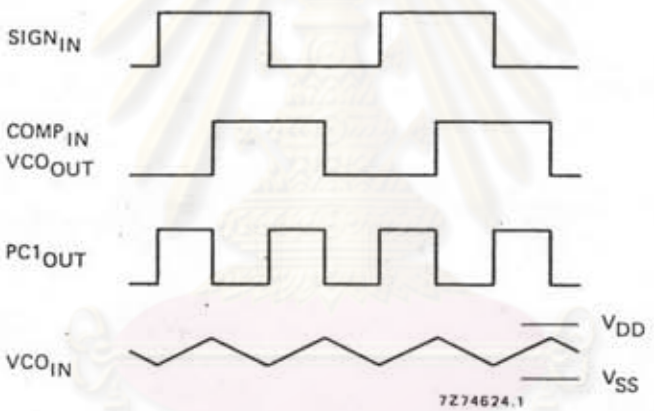


Fig. 4 Typical waveforms for phase-locked loop employing phase comparator 1 in locked condition of f_o.

FUNCTIONAL DESCRIPTION (continued)

Phase comparator 2 is an edge-controlled digital memory network. It consists of four flip-flops, control gating and a 3-state output circuit comprising p and n-type drivers having a common output node. When the p-type or n-type drivers are ON, they pull the output up to V_{DD} or down to V_{SS} respectively. This type of phase comparator only acts on the positive-going edges of the signals at $SIGN_{IN}$ and $COMP_{IN}$. Therefore, the duty factors of these signals are not of importance.

If the signal input frequency is higher than the comparator input frequency, the p-type output driver is maintained ON most of the time, and both the n and p-type drivers are OFF (3-state) the remainder of the time. If the signal input frequency is lower than the comparator input frequency, the n-type output driver is maintained ON most of the time, and both the n and p-type drivers are OFF the remainder of the time. If the signal input and comparator input frequencies are equal, but the signal input lags the comparator input in phase, the n-type output driver is maintained ON for a time corresponding to the phase difference. If the comparator input lags the signal input in phase, the p-type output driver is maintained ON for a time corresponding to the phase difference. Subsequently, the voltage at the capacitor of the low-pass filter connected to this phase comparator is adjusted until the signal and comparator inputs are equal in both phase and frequency. At this stable point, both p and n-type drivers remain OFF and thus the phase comparator output becomes an open circuit and keeps the voltage at the capacitor of the low-pass filter constant.

Moreover, the signal at the phase comparator pulse output (PCP_{OUT}) is a HIGH level which can be used for indicating a locked condition. Thus, for phase comparator 2 no phase difference exists between the signal and comparator inputs over the full VCO frequency range. Moreover, the power dissipation due to the low-pass filter is reduced when this type of phase comparator is used because both p and n-type output drivers are OFF for most of the signal input cycle. It should be noted that the PLL lock range for this type of phase comparator is equal to the capture range, independent of the low-pass filter. With no signal present at the signal input, the VCO is adjusted to its lowest frequency for phase comparator 2. Figure 5 shows typical waveforms for a PLL employing this type of phase comparator in locked condition.

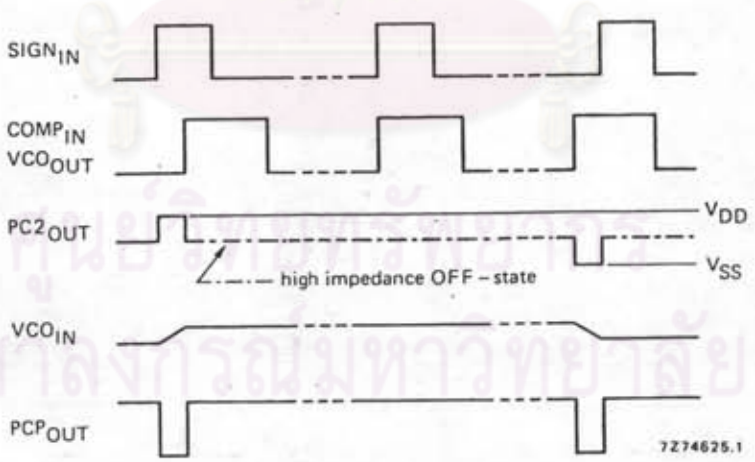
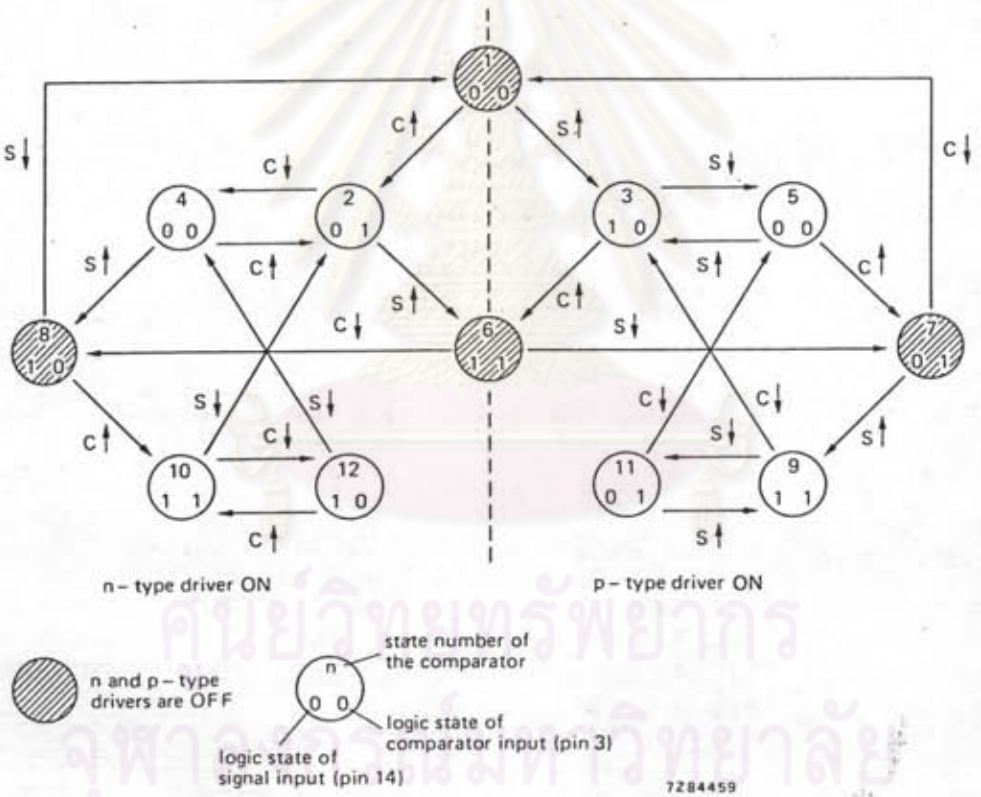


Fig. 5 Typical waveforms for phase-locked loop employing phase comparator 2 in locked condition.

Figure 6 shows the state diagram for phase comparator 2. Each circle represents a state of the comparator. The number at the top, inside each circle, represents the state of the comparator, while the logic state of the signal and comparator inputs are represented by a '0' for a logic LOW or a '1' for a logic HIGH, and they are shown in the left and right bottom of each circle.

The transitions from one to another result from either a logic change at the signal input (S) or the comparator input (C). A positive-going and a negative-going transition are shown by an arrow pointing up or down respectively.

The state diagram assumes that only one transition on either the signal input or comparator input occurs at any instant. States 3, 5, 9 and 11 represent the condition at the output when the p-type driver is ON, while states 2, 4, 10 and 12 determine the condition when the n-type driver is ON. States 1, 6, 7 and 8 represent the condition when the output is in its high impedance OFF state; i.e. both p and n-type drivers are OFF, and the PCP_{OUT} output is HIGH. The condition at output PCP_{OUT} for all other states is LOW.



S ↑ : 0 to 1 transition at the signal input.
C ↓ : 1 to 0 transition at the comparator input.

Fig. 6 State diagram for comparator 2.

D.C. CHARACTERISTICS

V_{SS} = 0 V

	V_{DD} V	symbol	T_{amb} (°C) −40 typ.	−40 max.	+25 typ.	+25 max.	+85 typ.	+85 max.	
Supply current (note 1)	5	I_D	–	–	20	–	–	–	μA
	10		–	–	300	–	–	–	μA
	15		–	–	750	–	–	–	μA
Quiescent device current (note 2)	5	I_{DD}	–	20	–	20	–	150	μA
	10		–	40	–	40	–	300	μA
	15		–	80	–	80	–	600	μA

Notes

1. Pin 15 open; pin 5 at V_{DD}; pins 3 and 9 at V_{SS}; pin 14 open.
2. Pin 15 open; pin 5 at V_{DD}; pins 3 and 9 at V_{SS}; pin 14 at V_{DD}; input current pin 14 not included.

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns

	V_{DD} V	symbol	min.	typ.	max.		
Phase comparators							
Operating supply voltage		V_{DD}	3		15	V	
Input resistance at $SIGN_{IN}$	5	R_{IN}		750		kΩ	at self-bias operating point
	10			220		kΩ	
	15			140		kΩ	
A.C. coupled input sensitivity at $SIGN_{IN}$	5	V_{IN}		150		mV	peak-to-peak values; R1 = 10 kΩ; R2 = ∞; C1 = 100 pF; independent of the lock range
	10			150		mV	
	15			200		mV	
D.C. coupled input sensitivity at $SIGN_{IN}$; $COMP_{IN}$ LOW level	5	V_{IL}			1,5	V	full temperature range
	10				3,0	V	
	15				4,0	V	
HIGH level	5	V_{IH}	3,5			V	full temperature range
	10		7,0			V	
	15		11,0			V	
Input current at $SIGN_{IN}$	5	$+I_{IN}$		7		μA	$SIGN_{IN}$ at V_{DD}
	10			30		μA	
	15			70		μA	
	5	$-I_{IN}$		3		μA	$SIGN_{IN}$ at V_{SS}
	10			18		μA	
	15			45		μA	

A.C. CHARACTERISTICS V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns

	V_{DD} V	symbol	min.	typ.	max.		
VCO							
Operating supply voltage		V_{DD}	3		15	V	as fixed oscillator only
			5		15	V	phase-locked loop operation
Power dissipation	5			150		μW	f_o = 10 kHz; R1 = 1 MΩ; R2 = ∞; VCO_{IN} at ½ V_{DD}; see also Figs 10 and 11
	10	P		2500		μW	
	15			9000		μW	
Maximum operating frequency	5		0,5	1,0		MHz	VCO_{IN} at V_{DD}; R1 = 10 kΩ; R2 = ∞; C1 = 50 pF
	10	f_{max}	1,0	2,0		MHz	
	15		1,3	2,7		MHz	
Temperature/ frequency stability	5			0,22–0,30		%/°C	no frequency offset (f_{min} = 0); see also note 1
	10			0,04–0,05		%/°C	
	15			0,01–0,05		%/°C	
	5			0–0,22		%/°C	with frequency offset (f_{min} > 0); see also note 1
	10			0–0,04		%/°C	
	15			0–0,01		%/°C	
Linearity	5			0,50		%	R1 > 10 kΩ; see Fig. 13
	10			0,25		%	R1 > 400 kΩ; see Figs 14 and 15
	15			0,25		%	R1 = 1 MΩ; see Figs 14 and 16
Duty factor at VCO_{OUT}	5			50		%	
	10	δ		50		%	
	15			50		%	
Input resistance at VCO_{IN}	5			10^6		MΩ	
	10	R_{IN}		10^6		MΩ	
	15			10^6		MΩ	
Source follower							
Offset voltage VCO_{IN} minus SF_{OUT}	5			1,7		V	R_{SF} = 10 kΩ; VCO_{IN} at ½ V_{DD}
	10			2,0		V	
	15			2,1		V	
	5			1,5		V	R_{SF} = 50 kΩ; VCO_{IN} at ½ V_{DD}
	10			1,7		V	
	15			1,8		V	
Linearity	5			0,3		%	R_{SF} > 50 kΩ; see Fig. 13
	10			1,0		%	
	15			1,3		%	
Zener diode							
Zener voltage		V_Z		7,3		V	I_Z = 50 μA
Dynamic resistance		R_Z		25		Ω	I_Z = 1 mA

Notes
1. Over the recommended component range.

DESIGN INFORMATION

characteristic	using phase comparator 1	using phase comparator 2
No signal on $SIGN_{IN}$	VCO in PLL system adjusts to centre frequency (f_o)	VCO in PLL system adjusts to min. frequency (f_{min})
Phase angle between $SIGN_{IN}$ and $COMP_{IN}$	90° at centre frequency (f_o), approaching 0° and 180° at ends of lock range (2 f_L)	always 0° in lock (positive-going edges)
Locks on harmonics of centre frequency	yes	no
Signal input noise rejection	high	low
Lock frequency range (2 f_L)	the frequency range of the input signal on which the loop will stay locked if it was initially in lock; 2 f_L = full VCO frequency range = $f_{max} - f_{min}$	
Capture frequency range (2 f_C)	the frequency range of the input signal on which the loop will lock if it was initially out of lock	
	depends on low-pass filter characteristics; $f_C < f_L$	$f_C = f_L$
Centre frequency (f_o)	the frequency of the VCO when VCO_{IN} at $\frac{1}{2}V_{DD}$	

VCO component selection

Recommended range for R1 and R2: 10 kΩ to 1 MΩ; for C1: 50 pF to any practical value.

1. VCO without frequency offset (R2 = ∞).
   a. Given f_o: use f_o with Fig. 7 to determine R1 and C1.
   b. Given f_{max}: calculate f_o from $f_o = \frac{1}{2} f_{max}$; use f_o with Fig. 7 to determine R1 and C1.
2. VCO with frequency offset.
   a. Given f_o and f_L: calculate f_{min} from the equation $f_{min} = f_o - f_L$; use f_{min} with Fig. 8 to determine R2 and C1; calculate $\frac{f_{max}}{f_{min}}$ from the equation $\frac{f_{max}}{f_{min}} = \frac{f_o + f_L}{f_o - f_L}$; use $\frac{f_{max}}{f_{min}}$ with Fig. 9 to determine the ratio R2/R1 to obtain R1.
   b. Given f_{min} and f_{max}: use f_{min} with Fig. 8 to determine R2 and C1; calculate $\frac{f_{max}}{f_{min}}$; use $\frac{f_{max}}{f_{min}}$ with Fig. 9 to determine R2/R1 to obtain R1.

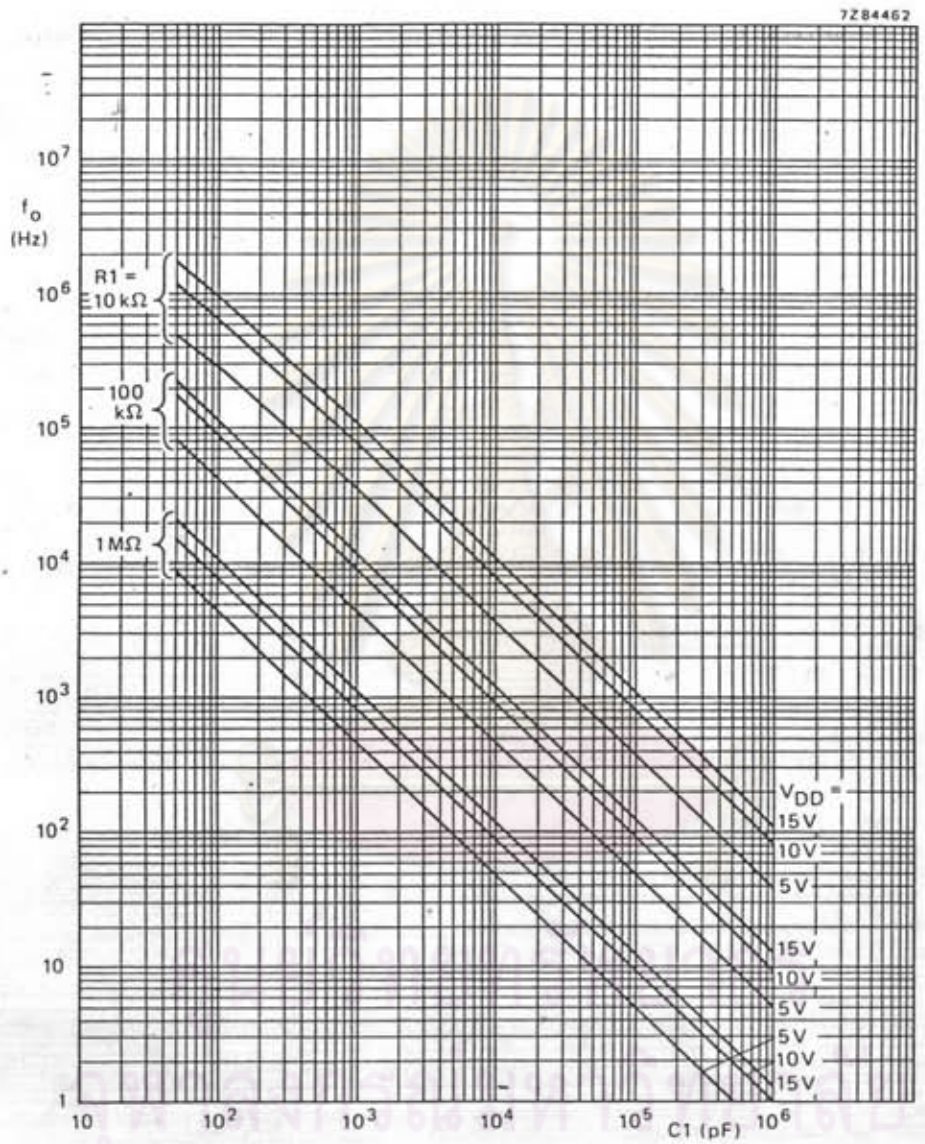


Fig. 7 Typical centre frequency as a function of capacitor C1; T_{amb} = 25 °C; VCO_{IN} at ½ V_{DD}; INH at V_{SS}; R2 = ∞.

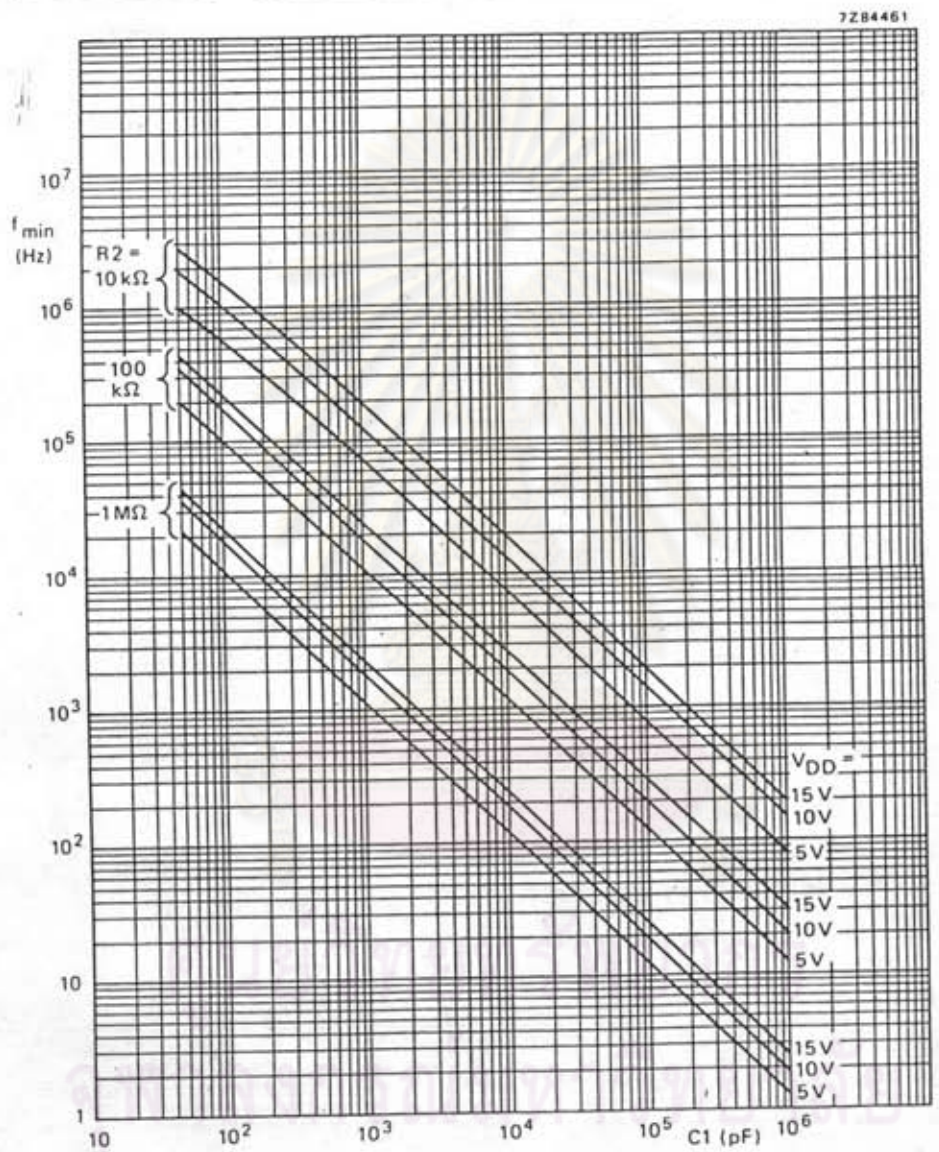


Fig. 8 Typical frequency offset as a function of capacitor C1; T_{amb} = 25 °C; VCO_{IN} at V_{SS}; INH at V_{SS}; R1 = ∞.

Appendix B

PHASE LOCKED LOOP THEORY (5)

INTRODUCTION

Phase Locked Loop (PLLs) are a new class of monolithic circuits developed by Signetics, but they are based on frequency feedback technology which dates back 40 years.

A phase locked loop is basically an electronic servo loop consisting of a phase detector, a low pass filter and a voltage controlled oscillator. Its controlled oscillator phase makes it capable of locking or synchronizing with an incoming signal. If the phase changes, indicating the incoming frequency is changing , the phase detector output voltage increases or decreases just enough to keep the oscillator frequency the same as the incoming frequency, preserving the locked condition. Thus, the average voltage applied to the controlled oscillator is a function of the frequency of the incoming signal. In fact, the low pass filter voltage *is* the demodulated output when the incoming signal is frequency modulated (provided the controlled oscillator has linear voltage-to-frequency transfer characteristic). The synchronous reception of radio signals using PLL techniques was described (Ref. 1) in the early thirties. You may have heard of the "homodyne" receiver.

The first widespread use of the phase lock, however, was in TV receivers to synchronize the horizontal and vertical sweep oscillators to the transmitted sync pulses. Lately, narrowband phase locked receivers have proved to be of considerable benefit in tracking weak satellite signals because of their superior noise immunity. Applicaitons such as these were implemented primarily in discrete component form and involved considerable complexity even after the advent of transistors. This complexity made PLL techniques impractical or uneconomical in the majority of systems.

The development of complete, single-chip phase locked loops has changed this situation considerably. Now, a single packaged device with a few external components will offer the user all the benefits of phase locked loop operation, including independent center frequency and bandwidth adjustment, high noise immunity, high selectivity, high frequency operation and center frequency tuning by means of a single external component.

Signetics makes three basic classes of single-chip PLL circuits: the general purpose PLL, the PLL with an added multiplier and the PLL tone decoder.

The 560N, 562N and 565 are general purpose phase locked loops containing an oscillator, phase detector and amplifier. When locked to an incoming signal, they provide two outputs: a voltage proportional to the frequency of the incoming signal (FM output) and the square wave oscillator output which, during lock, is equal to the incoming frequency. All general purpose devices are optimized to provide a linear frequency-to-voltage transfer characteristic.

The 561N contains a complete PLL as those above, plus the additional multiplier or quadrature phase detector required for AM demodulation. In addition to the standard FM and oscillator outputs, it also provides an output voltage which is proportional to the amplitude of the incoming signal (AM output). The 561N is opitmized for highly linear FM and AM demodulation.

The 567 is a special purpose phase locked loop intended solely for use as a tone decoder. It contains a complete PLL including oscillator, phase detector and amplifier as well as a quadrature phase detector or multiplier. If the signal amplitude at the locked frequency is above a minimal value, the driver amplifier turns on, driving a load as much as 200mA. It, thus, gives an output whenever an inband tone is present. The 567 is optimized for both center frequency and bandwidth stability.

The 566 is not a phase locked loop, but a precision voltage-controllable waveform generator derived from the oscillator of the 565 general purpose loop. Because of its similarity to the 565 and because it lends itself well to use in, and in conjunction with, phased locked loops, it has been included in this section.

Table 9-1 summarizes the characteristics of Signetics phase locked loop products.

A considerable quantity of detailed specifications and publications information for these products is included in the Linear Spec. Handbook. Because many readers are likely to be unfamiliar with the terminology and operating characteristics of phase locked loops, a glossary of terms and a general explanation of PLL principles are included here with a detailed discussion of the action of the individual loop elements.

The tradeoff and setup section will assist the reader in some of the considerations involved in selecting and applying the loop products to meet system requirements. A brief summary of measurement techniques has been presented to aid the user in achieving his performance goals.

Detailed descriptions have been provided for each of the loop products. The user can supplement the suggested connection diagrams with his own schemes.

Perhaps the best way to become familiar with the many uses of phase locked loops is to actually study the various application circuits provided. These circuits have been drawn from many sources—textbooks, users, Signetics' applications engineers and the 1970 Signetics—EDN Phase Locked Loop contest. Every effort has been made to provide usable, workable circuits which may be copied directly or used as jumping-off points for other imaginative applications.

The section on interfacing will aid the user in driving different forms of logic from PLL outputs and the section on expanding loop capabilities will show how to achieve improved performance in certain difficult applications.

PHASED LOCKED LOOP TERMINOLOGY

The following is a brief glossary of terms encountered in PLL literature.

Capture Range ($2\omega_C$)—Although the loop will remain in lock throughout its lock range, it may not be able to acquire lock at the tracking range extremes. The range over which the loop *can* acquire lock is termed capture range. The capture range is sometimes called the *Lock-in Range*.(The latter refers to how close a signal must be to the center frequency before acquisition can occur. It is thus one-half the capture range of ω_C.)

Current Controlled Oscillator (CCO)—An oscillator similar to a VCO in which the frequency is determined by an applied current.

Damping Factor (ζ)—The standard damping constant of a second order feedback system. In the case of the PLL, it refers to the ability of the loop to respond quickly to an input frequency step without excessive overshoot.

Free-Running Frequency (f_o, ω_o)—Also called the *Center Frequency*, this is the frequency at which the loop VCO operates when not locked to an input signal. The same symbols (f_o, ω_o) used for the free-running frequency are commonly used for the general oscillator frequency. It is usually clear which is meant from the context.

Lock Range ($2\omega_L$)—The range of input frequencies over which the loop will remain in lock. It is also called the *Tracking Range* or *Hold-In Range*. (The latter refers to how far the loop frequency can be deviated from the center frequency and is one-half the lock range or ω_L.)

Loop Gain (K_v)—The product of the dc gains of all the loop elements, in units of $(sec)^{-1}$.

USER'S QUICK-LOOK GUIDE TO SIGNETICS PLLs										
	UPPER FREQUENCY (MHz)	MAXIMUM LOCK RANGE (%f_o)	FM DISTORTION	OUTPUT SWING ±5% DEVIATION (volts p-p)	CENTER FREQUENCY STABILITY (ppm/°C)	FREQUENCY DRIFT WITH SUPPLY VOLTAGE (%/volt)	INPUT RESISTANCE	AM OUTPUT AVAILABLE	TYPICAL SUPPLY CURRENT (mA)	SUPPLY VOLTAGE RANGE (volts)
NE560	30	40%	.3%	1	±600	.3	2K**	No	9	+16 to +26
NE561	30	40%	.3%	1	±600	.3	2K**	Yes	10	+16 to +26
NE562	30	40%	.5%	1	±600	.3	2K**	No	12	+16 to +30
NE564	50	40%	.5%	.1	±400	.3	3K	No	30	+4.5 to +12
NE565	.5	120%	.2%	.15	±200	.16	5K	No	8	± 5 to ±12
SE565	.5	120%	.2%	.15	±100	.08	5K	No	8	± 5 to ±12
NE567	.5	14%	5%*	.20	35±60	.7	20K**	Yes*	7	± 4.5 to +9
SE567	.5	14%	5%*	.20	35±60	.5	20K**	Yes*	6	+ 4.5 to +9
NE566	.5		.2%	30%/V***	±200	.16			7	+10 to +26
SE566	.5		.2%	30%/V***	±100	.08			7	+10 to +26

* The 567 AM and FM outputs are available, but are not optimized for linear demodulation.
** Input biased internally.
*** Figure shown is VCO gain in percent deviation per volt.

Table 9-1

Loop Noise Bandwidth (B_L)—A loop property related to damping and natural frequency which describes the effective bandwidth of the received signal. Noise and signal components outside this band are greatly attenuated.

Low Pass Filter (LPF)—A low pass filter in the loop which permits only dc and low frequency voltages to travel around the loop. It controls the capture range and the noise and out-band signal rejection characteristics.

Natural Frequency (ω_n)—The characteristic frequency of the loop, determined mathematically by the final pole positions in the complex plane. May be determined experimentally as the modulation frequency for which an underdamped loop gives the maximum output and at which phase error swing is the greatest.

Phase Detector Gain Factor (K_d)—The conversion factor between the phase detector output voltage and the phase difference between input and VCO signals in volts/radian. At low input signal amplitudes, the gain is also a function of input level.

Phase Detector (PD)—A circuit which compares the input and VCO signals and produces an error voltage which is dependent upon their relative phase difference. This error corrects the VCO frequency during tracking. Also called *Phase Comparator, A Multiplier* or *Mixer* is often used as a phase detector.

Quadrature Phase Detector (QPD)—A phase detector operated in quadrature (90° out of phase) with the loop phase detector. It is used primarily for AM demodulation and lock detection.

BLOCK DIAGRAM OF PHASE LOCKED LOOP

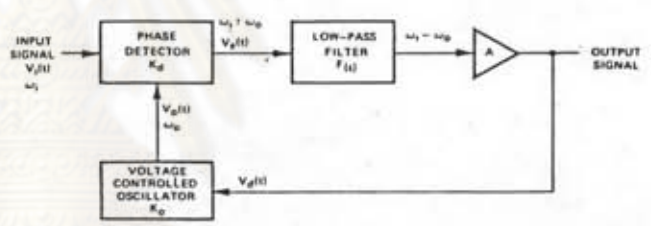


Figure 9-1

VCO Conversion Gain (K_o)—The conversion factor between VCO frequency and control voltage in radians/second/volt.

Voltage Controlled Oscillator (VCO)—An oscillator whose frequency is determined by an applied control voltage.

THE PHASE LOCKED LOOP PRINCIPLE

The phase locked loop is a feedback system comprised of a phase comparator, a low pass filter and an error amplifier in the forward signal path and a voltage-controlled oscillator (VCO) in the feedback path. The block diagram of a basic PLL system is shown in Figure 9-1. Detailed analysis of the PLL as a feedback control system has been discussed in the literature (Ref. 2). Perhaps the single most important point to realize when designing with the PLL is that it is a feedback system and, hence, is characterized mathematically by the same equations that apply to other, more conventional feedback systems. The parameters in the equations are somewhat different, however, since the feedback error signal in the phase locked system is a phase rather than a current or voltage signal, as is usually the case in conventional feedback systems.

Loop Operation

A rigorous mathematical analysis of the system is quite cumbersome and will not be repeated here. However, from a qualitative point of view, the basic principle of PLL operation can be briefly explained as follows: With no signal input applied to the system, the error voltage V_d is equal to zero. The VCO operates at a set frequency ω_o, which is known as the free-running frequency. If an output signal is applied to the system, the phase comparator compares the phase and the frequency of the input with the VCO frequency and generates an error voltage $V_e(t)$ that is related to the phase and the frequency difference between the two signals. This error voltage is then filtered, amplified and applied to the control terminal of the VCO. In this manner, the control voltage $V_d(t)$ forces the VCO fre-

quency to vary in a direction that reduces the frequency difference between f_o and the input signal. If the input frequency ω_i is sufficiently close to ω_o, the feedback nature of the PLL causes the VCO to synchronize or lock with the incoming signal. Once in lock, the VCO frequency is identical to the input signal except for a finite phase difference. This net phase difference θ_o is necessary to generate the corrective error voltage V_d to shift the VCO frequency from its free-running value to the input signal frequency ω_i and, thus, keep the PLL in lock. This self-correcting ability of the system also allows the PLL to track the frequency changes of the input signal once it is locked. The range of frequencies over which the PLL can maintain lock with an input signal is defined as the "lock range" of the system. The band of frequencies over which the PLL can acquire lock with an incoming signal is known as the "capture range" of the system and is never greater than the "lock range."

Another means of describing the operation of the PLL is to observe that the phase comparator is in actuality a multipler circuit that mixes the input signal with the VCO signal. This mix produces the sum and difference frequencies $\omega_i \pm \omega_o$ shown in Figure 9-1. When the loop is in lock, the VCO duplicates the input frequency so that the difference frequency component $(\omega_i - \omega_o)$ is zero; hence, the output of the phase comparator contains a dc component. The low pass filter removes the sum frequency component $(\omega_i = \omega_o)$ but passes the dc component which is then amplified and fed back to the VCO. Notice that when the loop is in lock, the difference frequency component is always dc, so the lock range is independent of the band edge of the low pass filter.

Lock and Capture

Consider now the case where the loop is not yet in lock. The phase comparator again mixes the input and VCO signals to produce sum and difference frequency components. Now, however, the difference component may fall outside the band edge of the low pass filter and be removed along with the sum frequency component. If this is the case, no information is transmitted around the loop and the VCO remains at its initial free-running frequency. As the input frequency approaches that of VCO, the frequency of the difference component decreases and approaches the band edge of the low pass filter. Now some of the difference component is passed, which tends to drive the VCO towards the frequency of the input signal. This, in turn, decreases the frequency of the difference component and allows more information to be transmitted through the low pass filter to the VCO. This is essentially a positive feedback mechanism which causes the VCO to snap into lock with the input signal. With this mechanism in mind, the term "capture range" can again be defined as *the frequency range centered about the VCO initial free-running frequency over which the loop can acquire lock with the input signal.* The capture range is a measure of how close the input signal must be in frequency to that of the VCO to acquire lock. The "capture range" can assume any value within the lock range and depends primarily upon the band edge of the low pass filter together with the closed loop gain of the system. It is this signal capturing phenomenon which gives the loop its frequency selective properties.

It is important to distinguish the "capture range" from the "lock range" which can, again, be defined as *the frequency range usually centered about the VCO initial free running frequency over which the loop can track the input signal once lock has been achieved.*

When the loop is in lock, the difference frequency component on the output of the phase comparator (error voltage) is dc and will always be passed by the low pass filter. Thus, the lock range is limited by the range of error voltage that can be generated and the corresponding VCO frequency deviation produced. The lock range is essentially a dc parameter and is not affected by the band edge of the low pass filter.

The Capture Transient

The capture process is highly complex and does not lend itself to simple mathematical analysis. However, a qualitative description of the capture mechanism may be given as follows: Since frequency is the time derivative of phase, the frequency and the phase errors in the loop can be related as

$$\Delta\omega = \frac{d\theta_o}{dt} \qquad \text{(Equation 9-1)}$$

where $\Delta\omega$ is the instantaneous frequency separation between the signal and VCO frequencies and θ_o is the phase difference between the input signal and VCO signals.

If the feedback loop of the PLL was opened, say between the low pass filter and the VCO control input, then for a given condition of ω_o and ω_i the phase comparator output would be a sinusoidal beat note at a fixed frequency $\Delta\omega$. If ω_i and ω_o were sufficiently close in frequency, this beat note would appear at the filter output with negligible attenuation. Now suppose that the feedback loop is closed by connecting the low pass filter output to the VCO control terminal. The VCO frequency will be modulated by the beat note. When this happens, $\Delta\omega$ itself will become a function of time. If during this modulation process, the VCO frequency moves closer to ω_i (i.e., decreasing $\Delta\omega$), then $d\theta_o/dt$ decreases and the output of the phase comparator becomes a slowly varying function of time. Similarly, if the VCO is modulated away from ω_i, $d\theta/dt$ increases and the error voltage becomes a rapidly varying function of time. Under this condition the beat note waveform no longer looks sinusoidal; it looks like a series of aperiodic cusps, depicted schematically in Figure 9-2a. Because of its asymmetry, the beat note waveform contains a finite dc component that pushes the average value of the VCO toward ω_i, thus increasing $\Delta\omega$. In this manner, the beat note frequency rapidly decreases toward zero, the VCO frequency drifts toward ω_i and the lock is established. When the system is in lock, $\Delta\omega$ is equal to zero and only a steady-state dc error voltage remains.

Figure 9-2b displays an oscillogram of the loop error voltage V_d in an actual PLL system during the capture process. Note that as lock is approached, $\Delta\omega$ is reduced, the low pass filter attenuation becomes less and the amplitude of the beat note increases.

The total time taken by the PLL to establish lock is called the pull-in time. Pull-in time depends on the initial frequency and phase differences between the two signals as well as on the overall loop gain and the low pass filter bandwidth. Under certain conditions, the pull-in time may be shorter than the period of the beat note and the loop can lock without an oscillatory error transient.

A specific case to illustrate this is shown in Figure 9-3. The 565 PLL is shown acquiring lock within the first cycle of the input signal. The PLL was able to capture in this short time because it was operated as a first order loop (no low pass filter) and the input tone-burst frequency was within its lock and capture range.

Effect of the Low Pass Filter

In the operation of the loop, the loop pass filter serves a dual function: First, by attenuating the high frequency error components at the output of the phase comparator, it enhances the inteference-rejection characteristics; second, it provides a short-term memory for the PLL and ensures a rapid recapture of the signal if the system is thrown out of lock due to a noise transient. The low pass filter bandwidth has the following effects on system performance:

ASYNCHRONOUS ERROR BEAT FREQUENCY DURING THE CAPTURE PROCESS

Figure 9-2a

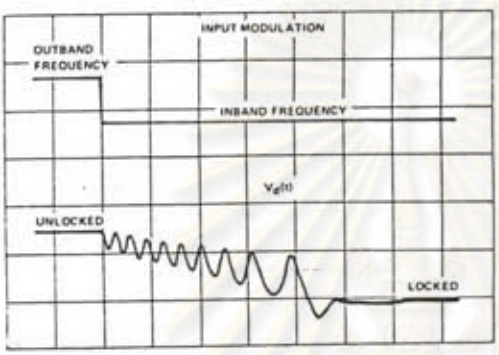


Figure 9-2b

FAST CAPTURE EXHIBITED BY FIRST ORDER LOOP

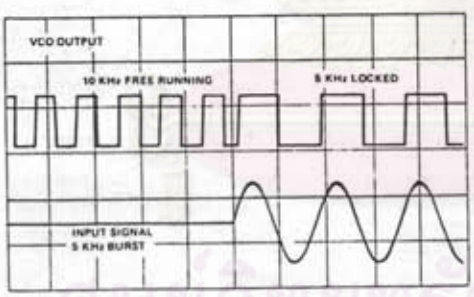


Figure 9-3

LINEARIZED MODEL OF THE PLL AS A NEGATIVE FEEDBACK SYSTEM

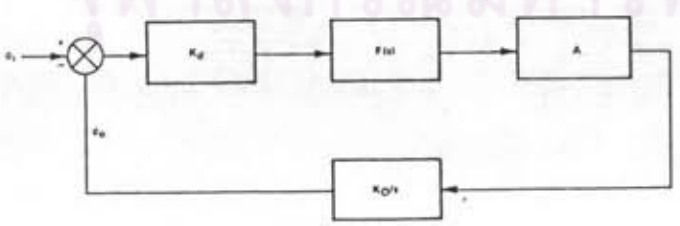


Figure 9-4

a. The capture process becomes slower, and the pull-in time increases.
b. The capture range decreases.
c. Interference-rejection properties of the PLL improve since the error voltage caused by an interfering frequency is attenuated further by the low pass filter.
d. The transient responce of the loop (the response of the PLL to sudden changes of the input frequency within the capture range) becomes undamped.

The last effect also produces a practical limitation on the low pass loop filter bandwidth and roll-off characteristics from a stability standpoint. These points will be explained further in the following analysis.

Linear Analysis for Lock Condition—Frequency Tracking

When the PLL is in lock, the non-linear capture transients are no longer present. Therefore, under lock condition, the PLL can often be approximated as a linear control system (see Figure 9-4) and can be analyzed using Laplace transform techniques. In this case, it is convenient to use the net phase error in the loop ($\theta_s - \theta_o$) as the system variable. Each of the gain terms associated with the blocks can be defined as follows:

K_d = conversion gain of phase detector (volt/rad)

$F(s)$ = transfer characteristic of low pass filter

A = amplifier voltage gain

K_θ = VCO conversion gain (rad/sec/volt)

Note that, since the VCO converts a voltage to a frequency and since phase is the integral of frequency, the VCO functions as an integrator in the feedback loop.

The open loop transfer function for the PLL can be written as

(Equation 9-2)

$$T(s) = \frac{K_v F(s)}{s}$$

where K_v is the total loop gain, i.e., $K_v = K_O K_\theta A$. Using the linear feedback analysis techniques, the closed loop transfer characteristics H(s) can be related to the open loop performance as

(Equation 9-3)

$$H(s) = \frac{T(s)}{1 + T(s)}$$

and the roots of the characteristic system polynomial can be readily determined by root locus techniques.

From these equations, it is apparent that the transient performance and frequency re-

sponse of the loop is heavily dependent upon the choice of filter and its corresponding transfer characteristic, F(s).

The simplest case is that of the first order loop where F(s) = 1 (no filter). The closed loop transfer function then becomes

(Equation 9-4)

$$T(s) = \frac{K_v}{s + K_v}$$

This transfer function gives the root locus as a function of the total loop gain K_v and the corresponding frequency response shown in Figure 9-5a. The open loop pole at the origin is due to the integrating action of the VCO. Note that the frequency response is actually the amplitude of the difference frequency component versus modulating frequency when the PLL is used to track a frequency modulated input signal. Since there is no low pass filter in this case, sum frequency components are also present on the phase detector output and must be filtered outside of the loop if the difference frequency component (demodulated FM) is to be measured.

With the addition of a single pole low pass filter F(s) of the form

(Equation 9-5)

$$F(s) = \frac{1}{1 + \tau_1 s}$$

where $\tau_1 = R1C$, the PLL becomes a second order system with the root locus shown in Figure 9-5b. Here, we again have an open loop pole at the origin because of the integrating action of the VCO and another open loop pole at a position equal to $-1/\tau_1$ where τ_1 is the time constant of the low pass filter.

One can make the following observations from the root locus characteristics of Figure 9-5b.

a. As the loop gain K_v increases for a given choice of τ_1, the imaginary part of the closed loop poles increase; thus, the natural frequency of the loop increases and the loop becomes more and more undamped.
b. If the filter time constant is increased, the real part of the closed loop poles becomes smaller and the damping is reduced.

As in any practical feedback system, excess shifts or non-dominant poles associated with the blocks within the PLL can cause the root loci to bend toward the right half plane as shown by the dashed line in Figure 9-5b. This is likely to happen if either the loop gain or the filter time constant is too large and may cause the loop to break into sustained oscillations.

ROOT LOCUS AND FREQUENCY RESPONSE PLOTS OF FIRST AND SECOND ORDER LOOPS

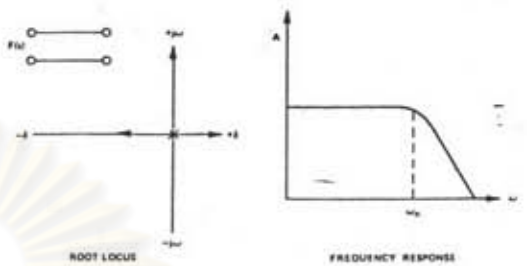


Figure 9-5a

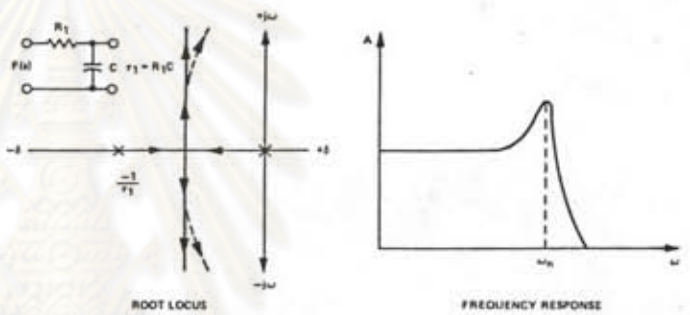


Figure 9-5b

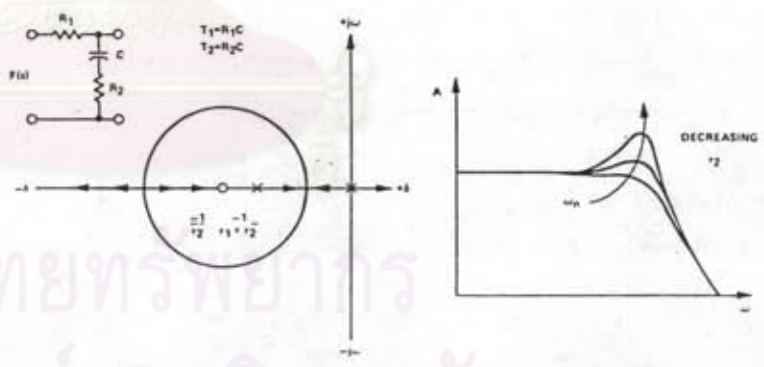


Figure 9-5c

The stability problem can be eliminated by using a lag-lead type of filter, as indicated in Figure 9-5c. This type of filter has a transfer function

(Equation 9-6)

$$F(s) = \frac{1 + \tau_2 s}{1 + (\tau_1 + \tau_2)s}$$

where $\tau_2 = R2C$ and $\tau_1 = R1C$. By the proper choice of R2, this type of filter confines the root locus to the left half plane and ensures stability. The lag-lead filter gives a frequency response dependent on the damping, which can now be controlled by the proper adjustment of τ_1 and τ_2. In practice, this type of filter is important because it allows the loop to be used with a response between that of the first and second order loops and it provides an additional control over the loop transient response. If R2 = 0, the loop

behaves as a second order loop and if R2 = ∞, the loop behaves as a first order loop due to a pole-zero cancellation. Note, however, that as first order operation is approached, the noise bandwidth increases and interference rejection decreases since the high frequency error components in the loop are now attenuated to a lesser degree.

In terms of the basic gain expressions in the system, the lock range of the PLL ω_L can be shown to be numerically equal to the dc loop gain

(Equation 9-7)

$$2\omega_L = 4\pi f_L = 2K_v$$

Since the capture range ω_C denotes a transient condition, it is not as readily derived as the lock range. However, an approximate expression for the capture range can be written as

(Equation 9-8)

$$2\omega_C = 4\pi f_C = 2K_v \cdot F(j\omega_C)$$

where $F(j\omega_C)$ is the low pass filter amplitude response at $\omega = \omega_L$. Note that at all times the capture range is smaller than the lock range. If the simple lag filter of Figure 9-5b is used, the capture range equation can be approximated as

(Equation 9-9)

$$2\omega_C \approx 2\sqrt{\frac{\omega_L}{\tau_1}}\sqrt{\frac{K_v}{\tau_1}}$$

Thus, the capture range increased as the low pass filter time constant is decreased, whereas the lock range is unaffected by the filter and is determined solely by the loop gain.

Figure 9-6 shows the typical frequency-to-voltage transfer characterisitcs of the PLL. The input is assumed to be a sine wave whose frequency is swept slowly over a broad frequency range. The vertical scale is the corresponding loop error voltage. In Figure 9-6a, the input frequency is being gradually increased. The loop does not respond to the signal until it reaches frequency ω_1, corresponding to the lower edge of the capture range. Then, the loop suddenly locks on the input and causes a negative jump of the loop error voltage. Next, V_d varies with frequency with a slope equal to the reciprocal of VCO gain ($1/K_o$) and goes through zero as $\omega_i = \omega_o$. The loop tracks the input until the input frequency reaches ω_2, corresponding to the upper edge of the lock range. The PLL then loses lock and the error voltage drops to zero. If the input frequency is swept slowly back now, the cycle repeats itself, but it is inverted, as shown in Figure 9-6b. The loop recaptures the signal at ω_3 and tracks it down to ω_4. The total capture and lock ranges of the system are:

TYPICAL PLL FREQUENCY- TO-VOLTAGE TRANSFER CHARACTERISTICS FOR INPUT FREQUENCY INCREASING AND DECREASING

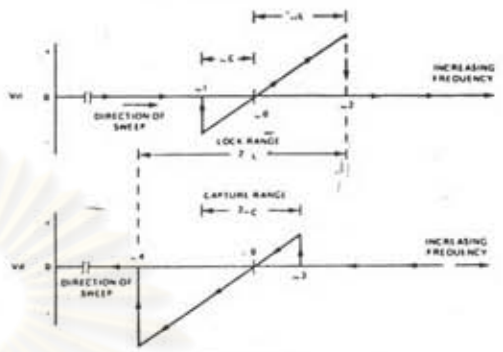


Figure 9-6

(Equation 9-10)

$$2\omega_C = \omega_3 - \omega_1 \text{ and } 2\omega_L = \omega_2 - \omega_4$$

Note that, as indicated by the transfer characteristics of Figure 9-6, the PLL system has an inherent selectivity about the center frequency set by the VCO free-running frequency ω_o. It will respond only to the input signal frequencies that are separated from ω_o by less than ω_C or ω_L, depending on whether the loop starts with or without an initial lock condition. The linearity of the frequency-to-voltage conversion characteristics for the PLL is determined solely by the VCO conversion gain. Therefore, in most PLL applications, the VCO is required to have a highly linear voltage-to-frequency transfer characteristic.

PHASE LOCKED LOOP BUILDING BLOCKS

Voltage Controlled Oscillator

Since three different forms of VCO have been used in the Signetics PLL series, the VCO details will not be discussed until the individual loops are described. However, a few general comments about VCOs are in order.

When the PLL is locked to a signal, the VCO voltage is a function of the frequency of the input signal. Since the VCO control voltage is the demodulated output during FM demodulation, it is important that the VCO voltage-to-frequency characteristic be linear so that the output is not distorted. Over the linear range of the VCO, the conversion gain is given by K_o (in radian/sec/volt).

(Equation 9-11)

$$K_o = \frac{\Delta\omega_o}{\Delta V_o}$$

Since the output voltage is the VCO voltage, we can get the loop output voltage as

(Equation 9-12)

$$\Delta V_o = \frac{\Delta\omega_o}{K_o}$$

The gain K_o can be found from the data sheet by taking the change in VCO control voltage for a given percentage frequency deviation and multiplying by the center frequency. When the VCO voltage is changed, the frequency change is virtually instantaneous.

Phase Detector

All Signetics phase locked loops use the same form of phase detector—often called the doubly-balanced multiplier or mixer. Such a circuit is shown in Figure 9-7.

The input stage formed by transistors Q1 and Q2 may be viewed as a differential amplifier which has a collector resistance R_c and whose differential gain at balance is the ratio of R_c to the emitter resistance r_e of Q1 and Q2.

(Equation 9-13)

$$A_d = \frac{R_C}{r_e} = \frac{R_C}{\frac{0.026}{I_e/2}} = \frac{R_C}{0.0131_e}$$

The switching stage formed by Q3 - Q6 is switched on and off by the VCO square wave. Since the collector current swing of Q2 is the negative of the collector current swing of Q1, the switching action has the effect of multiplying the differential stage output first by +1 and then by -1. That is, when the base of Q4 is positive, R_{C2} receives I1 and when the base of Q6 is positive, R_C2 receives I2 = I1. Since we have called this a multiplier, let us perform the multiplication to gain further insight into the action of the phase detector.

Suppose we have an input signal which consists of two added components: a component at frequency ω_i which is close to the free-running frequency and a component at frequency ω_k which may be at any frequency. The input signal is

(Equation 9-14)

$$V_i + V_k = V_i \sin(\omega_i t + \theta_i) + V_k \sin(\omega_k t + \theta_k)$$

where θ_i and θ_k are the phase in relation to the VCO signal. The unity square wave developed in the multiplier by the VCO signal is

(Equation 9-15)

$$\frac{4}{\pi(2n+1)} \sin\left[(2n+1)\omega_0 t\right]$$

where ω_0 is the VCO frequency. Multiplying the two terms, using the appropriate trigonometric relationship and inserting the differential stage gain A_d, we get

(Equation 9-16)

$$V_d = \frac{2A_d}{\pi}\left[\sum_{n=0}^{\infty}\frac{V_i}{(2n+1)}\cos\left[(2n+1)\omega_0 t - \omega_i t - \theta_i\right]\right.$$

$$-\sum_{n=0}^{\infty}\frac{V_i}{(2n+1)}\cos\left[(2n+1)\omega_0 t + \omega_i t + \theta_i\right]$$

$$+\sum_{n=0}^{\infty}\frac{V_k}{(2n+1)}\cos\left[(2n+1)\omega_0 t - \omega_k t - \theta_k\right]$$

$$\left.-\sum_{n=0}^{\infty}\frac{V_k}{(2n+1)}\cos\left[(2n+1)\omega_0 t + \omega_k t + \theta_k\right]\right]$$

Assuming the V_k is zero, temporarily, if ω_i is close to ω_0, the first term (n = 0) has a low frequency difference frequency component. This is the beat frequency component that feeds around the loop and causes lock up by modulating the VCO. As ω_0 is driven closer to ω_i, this difference component becomes lower and lower in frequency until $\omega_0 = \omega_i$ and lock is achieved. The first term then becomes

(Equation 9-17)

$$\frac{2A_d V_i}{\pi}\cos\theta_i$$

which is the usual phase detector formula showing the dc component of the phase detector during lock. This component must equal the voltage necessary to keep the VCO at ω_0. it is possible for ω_0 to equal ω_i momentarily during the lock up process and, yet, for the phase to be incorrect so that ω_0 passes through ω_i without the lock being achieved. This explains why lock is usually not achieved instantaneously, even when $\omega_i = \omega_0$ at t = 0.

If $n \neq 0$ in the first term, the loop can lock when $\omega_i = (2n+1)\omega_0$, giving the dc phase detector component

(Equation 9-18)

$$\frac{2A_d V_i}{\pi(2n+1)}\cos\theta_i$$

showing that the loop can lock odd harmonics of the center frequency. The (2n + 1) term in the denominator shows that the phase detector output is lower for harmonic lock, which explains why the lock range decreases as higher and higher odd harmonics are used to achieve lock.

Note also that the phase detector during lock is (assuming A_d is constant) also a function of the input amplitude V_i. Thus, for a given dc phase detector output V_d, an input amplitude decrease must be accompanied by a phase change. Since the loop can remain locked only for θ_i between 0 and 180°, the lower V_i becomes, the more reduced is the lock range.

Going to the second term, we note that during lock the lowest possible frequency is $\omega_0 + \omega_i = 2\omega_i$. A sum frequency component is always present at the phase detector output. This component is usually greatly attenuated by the low pass filter capacitor connected to the phase detector output. However, when rapid tracking is required (as with high-speed FM detection or FSK-frequency shift keying), the requirement for a relatively high frequency cutoff in the low pass filter may leave this component unattenuated to the extent that it interferes with detection. At the very least, additional filtering may be required to remove this component. Components caused by $n \neq 0$ in the second term are both attenuated and of much higher frequency, so they may be neglected.

Suppose that we have other frequencies represented by V_k present. What is their effect for $V_k \neq 0$?

The third term shows that V_k introduces another difference frequency component. Obviously, if ω_k is close to ω_i, it can interfere with the locking process since it may form a beat frequency of the same magnitude as the desired locking beat frequency. Suppose lock has been achieved, however, so that $\omega_0 = \omega_i$. In order for lock to be maintained, the average phase detector output must be constant. If $\omega_0 = \omega_k$ is relatively low in frequency, the phase θ_i must change to compensate for this beat frequency. Broadly speaking, any signal in addition to the signal to which the loop is locked causes a phase variation. Usually this is negligible since ω_k is often far removed from ω_i. However, it has been stated that the phase θ_i can move only between 0 and 180°. Suppose the phase limit has been reached and V_k appears. Since it cannot be compensated for, it will drive the loop out of lock. This explains why extraneous signals can result in a decrease in the lock range. If V_k is assumed to be an instantaneous noise component, the same effect occurs. When the full swing of the loop is being utilized, noise will decrease the lock or tracking range. We can reduce this effect by decreasing the cutoff frequency of the low pass filter so that the $\omega_0 - \omega_k$ is attentuated to a greater extent, which illustrates that noise immunity and out-

INTEGRATED PHASE DETECTOR

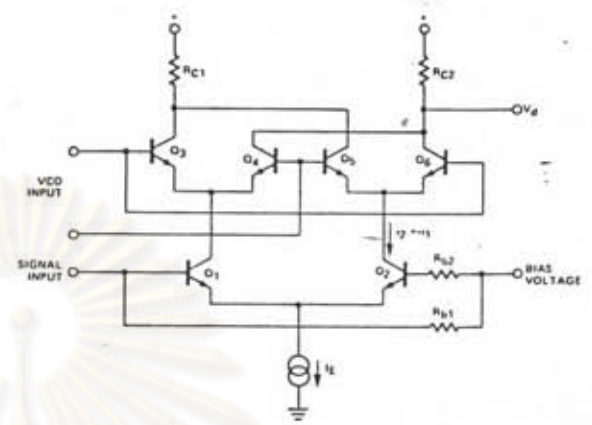


Figure 9-7

band frequency rejection is improved (at the expense of capture range since $\omega_o - \omega_i$ is likewise attenuated) when the low pass filter capacitor is large.

The third term can have a dc component when ω_k is an odd harmonic of the locked frequency so that $(2n+1)(\omega_o - \omega_i)$ is zero and θ_k makes its appearance. This will have an effect on θ_i which will change the θ_i versus frequency ω_i. This is most noticeable when the waveform of the incoming signal is, for example, a square wave. The θ_k term will combine with the θ_i term so that the phase is a linear function of input frequency. Other waveforms will give different phase versus frequency functions. When the input amplitude V_i is large and the loop gain is large, the phase will be close to 90° throughout the range of VCO swing, so this effect is often unnoticed.

The fourth term is of little consequence except that if ω_k approaches zero, the phase detector output will have a component at the locked frequency ω_o at the output. For example, a dc offset at the input differential stage will appear as a square wave of fundamental ω_o at the phase detector output. This is usually small and well attenuated by the low pass filter. Since many out-band signals or noise components may be present, many V_k terms may be combining to influence locking and phase during lock. Fortunately, we need only worry about those close to the locked frequency.

The quadrature phase detector action is exactly the same except that its output is proportional to the sine of the phase angle. When the phase θ_i is 90°, the quadrature phase detector output is then at its maximum, which explains why it makes a useful lock or amplitude detector. The output of the quadrature phase detector is given by:

(Equation 9-19)

$$V_Q = \frac{2A_Q V_i}{\pi} \sin \theta_i$$

where V_i is the constant or modulated AM signal and $\theta_i \approx 90°$ in most cases so that sine $\theta_i = 1$ and

(Equation 9-20)

$$V_Q = \frac{2A_Q V_i}{\pi}$$

This is the demodulation principle of the autodyne receiver and the basis for the 567 tone decoder operation.

FUNCTIONAL APPLICATIONS

Low Pass Filter

The simplest type of low pass filter for the second order loop is a single pole RC type shown in Figure 9-5b. In all Signetics' loops, the resistor is internal and the capacitor is external. The inside resistor greatly improves the center frequency stability of the loop with temperature variations. Fortunately, the capture range and loop damping are related to the square root of this internal resistor value, so variations in its absolute value have little effect on loop performance. The nominal value of the internal resistor for each loop is given in the circuit diagrams of the detailed circuit descriptions in this chapter. The typical tolerance on these integrated resistors is ±20%.

As a functional building block, the phase locked loop is suitable for a wide variety of frequency related applications. These applications generally fall into one or more of the following categories:

a. FM demodulation
b. Frequency synthesizing
c. Frequency synchronization
d. Signal conditioning
e. AM demodulation

FM Demodulation

If the PLL is locked to a frequency modulated (FM) signal, the VCO tracks the instantaneous frequency of the input signal. The filtered error voltage, which forces the VCO to maintain lock with the input signal then becomes the demodulated FM output. The linearity of this demodulated signal depends solely on the linearity of the VCO control-voltage-to-frequency transfer characteristic.

It should be noted that since the PLL is in lock during the FM demodulation process, the response is linear and can be readily predicted from a root locus plot.

FM demodulation applications are numerous; however, some of the more popular are:

BROADCAST FM DETECTION

Here, the PLL can be used as a complete IF strip, limiter and FM detector which may be used for detecting either wide or narrow band FM signals with greater linearity than can be obtained by other means. For frequencies within the range of the VCO, the PLL functions as a self contained receiver since it combines the functions of frequency selectivity and demodulation. One increasingly popular use of the PLL is in scanning-receivers where a number of broadcast channels may be sequentially monitored by simply varying the VCO free-running frequency.

FM TELEMETRY

This application involves demodulation of a frequency modulated subcarrier of the main channel. A popular example here is the use of the PLL to recover the SCA (storecast music) signal from the combined signal of many commercial FM broadcast stations. The SCA signal is a 67kHz frequency modulated subcarrier which puts it above the frequency spectrum of the normal stereo or monaural FM program material. By connecting the circuit of Figure 9-8 to a point between the FM discriminator and the de-emphasis filter of a commercial band (home) FM receiver and tuning the receiver to a station which broadcasts an SCA signal, one can obtain hours of commercial free background music.

FREQUENCY SHIFT KEYING (FSK)

This refers to what is essentially digital frequency modulation. FSK is a means for transmitting digital information by a carrier which is shifted between two discrete frequencies. In this case, the two discrete frequencies correspond to a digital "1" and a digital "0," respectively. When the PLL is locked to a FSK signal, the demodulated output (error voltage) shifts between two discrete voltage levels, corresponding to the demodulated binary output. FSK techniques are often used in modems (modulator-demodulators), intended for transmitting data over telephone lines.

SCA DECODER

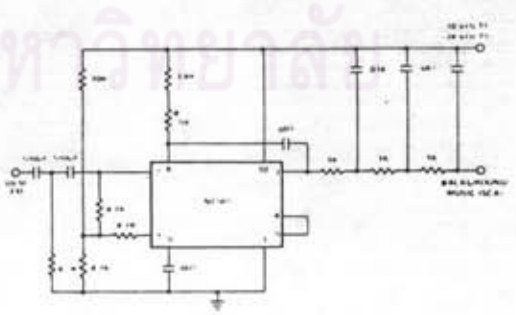


Figure 9-8

Appendix C

ACTIVE RESONANT BANDPASS FILTERS (6)

The idealized bandpass filter has a constant response for $f_{ol} < f < f_{oh}$ and zero gain outside this range. An infinite number of Butterworth sections are required to obtain this filter response. A very simple approximation to a narrowband characteristic is obtained using a single LC resonant circuit. Such a bandpass filter has a response which peaks at some center frequency f_o and drops off with frequency on both sides of f_o. A basic prototype for a resonant filter is the second-order section, whose transfer function we now derive. If we assure that the amplifier provides a gain $A_o = V_o/V_i$ which is positive and constant for all frequencies, we find

$$A_v(j\omega) = \frac{V_o}{V_s} = \frac{V_o}{V_i}\frac{V_i}{V_s} = \frac{RA_o}{R + J(\omega L - 1/\omega C)} \qquad .....(1)$$

The center, or resonant, frequency $f_o = \omega_o/2\pi$ is defined as that frequency at which the inductance resonates with the capacitance; in other words, the inductive and capacitive reactances are equal (in magnitude), or

$$\omega_o^2 = \frac{1}{LC} \qquad .....(2)$$

It is convenient to define the quality factor Q of this circuit by

$$Q = \frac{\omega_o L}{R} = \frac{1}{\omega_o CR} = \frac{1}{R}\sqrt{\frac{L}{C}} \qquad .....(3)$$

Substituting Eq. 3 in Eq. 1, we obtain the magnitude and phase of the transfer function.

$$|A_v(j\omega)| = \frac{A_o}{\left[1 + Q^2\left(\frac{\omega}{\omega_o} - \frac{\omega_o}{\omega}\right)^2\right]^{\frac{1}{2}}} \quad \text{.....(4)}$$

$$Q = -\arctan Q\left(\frac{\omega}{\omega_o} - \frac{\omega_o}{\omega}\right) \quad \text{.....(5)}$$

1. Active RC Bandpass Filter

The general form for the second-order bandpass filter is obtained if we let $s = j\omega$ in Eq . 1

$$A_v(s) = \frac{RA_o}{R + sL + 1/sC} = \frac{(R/L)A_o S}{s^2 + s(R/L) + 1/LC} \quad \text{.....(6)}$$

Substituting Eqs. 2 and 3 into 6 yields

$$A_v(s) = \frac{(\omega_o/Q)A_o s}{s^2 + (\omega_o/Q)s + \omega_o^2} \quad \text{.....(7)}$$

The transfer function of Eq. 7 obtained from the RLC circuit can be implemented with the multiple-feedback circuit of Figure 1, which uses two capacitors, three resistors, and one OP AMP, but no inductors. If we assume that the OP AMP voltage gain is infinite, we can derive that

$$\frac{V_o(s)}{V_s} = \frac{s/R_1C_1}{s^2 + \frac{C_1 + C_2}{R_3C_1C_2}s + \frac{1}{R'R_3C_1C_2}} \quad \text{.....(8)}$$

where $R' = R_1 \quad R_2$, or

$$R' \quad \frac{R_1R_2}{R_1 + R_2} \quad \text{.....(9)}$$

Equating the corresponding coefficients in the three transfer functions of Eqs. 6, 7, and 8 yields.

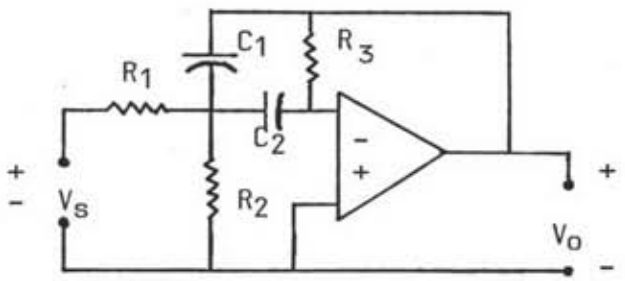


Figure 1 : An Active resonant filter without an inductance.

$$R_1C_1 = \frac{L}{RA_o} = \frac{Q}{\omega_o A_o} \qquad \text{.....(21)}$$

$$R_3\frac{C_1C_2}{C_1 + C_2} = \frac{L}{R} = \frac{Q}{\omega_o} \qquad \text{.....(22)}$$

$$R'R_3C_1C_2 = LC = \frac{1}{\omega_o^2} \qquad \text{.....(23)}$$

Any real positive values for R_1, R', R_3, C_1, and C_2 which satisfy Eqs. 10 to 12 are acceptable for the design of the active bandpass filter. Since we have only three equations for the five parameters, two of these (say C_1 and C_2) may be chosen arbitrarily.

Appendix D

CONTROLLED-SOURCE CIRCUITS (7)

A noninverting voltage-controlled voltage source (VCVS) implemented with an operational amplifier is illustrated in figure 1. The input impedance is very large, tens to hundreds of thousands of megohms, depending upon the type of operational amplifier, and the output impedance is very low, usually less than 1 Ω for K between 1 and 10. The voltage transfer function is

$$\frac{E_o}{E_1}(s) = 1 + \frac{R_b}{R_a} = K \qquad \text{.....(1)}$$

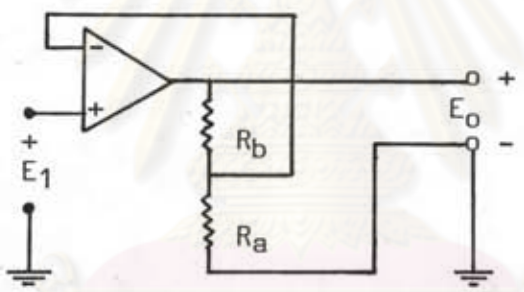


Figure 1 : Noninverting operational amplifier VCVS

The sensitivities of K to the two resistors are

$$S_{R_b}^{K} = 1 \qquad \text{.....(2)}$$

$$S_{R_a}^{K} = -1 \qquad \text{.....(3)}$$

Figure 2 shows the controlled-source connection for a circuit which may be used to realize voltage transfer functions with a single pair of complex conjugate s-plane poles with zeros restricted to the origin or infinity. The Yi are restricted to be single elements, R's and C's. These five elements may be chosen so as to realize low-pass, high-pass, and bandpass network functions. Realizations are possible

with K 0; but since this operational amplifier circuit always has K greater than +1, these will not be discussed. The voltage transfer function is

$$\frac{E_o(s)}{E_1} = \frac{KY_1Y_4}{Y_5(Y_1 + Y_2 + Y_3 + Y_4) + Y_4[Y_1 + Y_2(1 - K) + Y_3]} \quad \ldots\ldots\ldots(3)$$

1. Low Pass

A VCVS circuit for a low-pass network function is shown in figure 12. The voltage transfer function is

$$\frac{E_o(s)}{E_1} = \frac{K/R_1R_2C_1C_2}{s^2 + s[1/R_1C_1 + 1/R_2C_1 + (1 - K)/R_2C_2] + 1/R_1R_2C_1C_2} \quad \ldots\ldots\ldots(4)$$

The network parameters are

$$H_o = K \quad \ldots\ldots\ldots(5)$$

$$\omega_o = \left(\frac{1}{R_1R_2C_1C_2}\right)^{\frac{1}{2}} \quad \ldots\ldots\ldots(6)$$

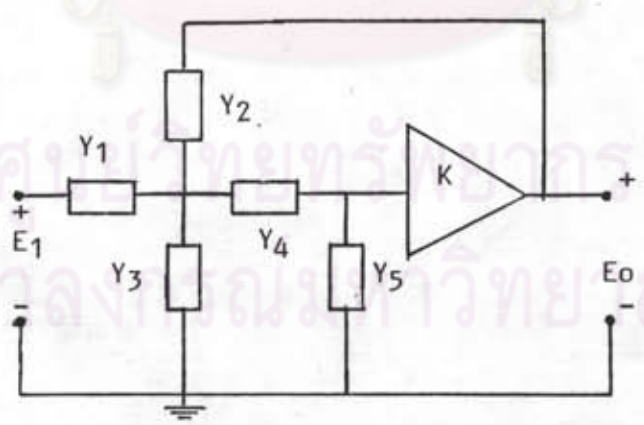


Figure 2

VCVS configuration for a second-degree voltage transfer function

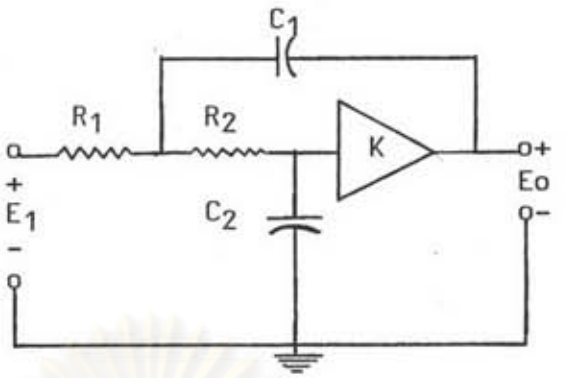


Figure 3 : The VSVS low-pass network

$$\alpha = \left(\frac{R_2C_2}{R_1C_1}\right)^{\frac{1}{2}} + \left(\frac{R_1C_2}{R_2C_1}\right)^{\frac{1}{2}} + \left(\frac{R_1C_1}{R_2C_2}\right)^{\frac{1}{2}} - K\left(\frac{R_1C_1}{R_2C_2}\right)^{\frac{1}{2}} \quad \text{.....(7)}$$

$$\phi = \phi_{LP} \quad \text{.....(8)}$$

$$T = T_{LP} \quad \text{.....(9)}$$

Controlled-source circuits are easier to tune than other circuit realizations. In fact, they can be adjusted over wide ranges without interaction of the network parameters. ω_o is tuned by adjusting R_1 and R_2 by equal percentages: α will not be affected. Capacitance C_1 and C_2 can be adjusted in the same way for the same result. α is trimmed by adjusting K. the sensitivities of the network parameters to element value changes are

$$S_{R_1}^{\omega_o} = S_{R_2}^{\omega_o} = S_{C_1}^{\omega_o} = S_{C_2}^{\omega_o} = -\frac{1}{2} \quad \text{.....(10)}$$

$$S_K^{H_o} = 1 \quad \text{.....(11)}$$

$$S_{R_1}^{\alpha} = \frac{1}{2} \quad \frac{1}{\alpha\omega_o R_1 C_1} \quad \text{.....(12)}$$

$$S_{R_2}^{\alpha} = \frac{1}{2} - \frac{1}{\alpha\omega_o R_2}\left(\frac{1}{C} + \frac{1-K}{C_2}\right) \quad \text{.....(13)}$$

$$S_{C_1}^{\alpha} = \frac{1}{2} - \frac{1}{\alpha\omega_o C_1}\left(\frac{1}{R_1} + \frac{1}{R_2}\right) \quad \text{.....(14)}$$

$$S_{C_2}^{\alpha} = \frac{1}{2} - \frac{1-K}{\alpha\omega_o R_2 C_2} \quad \text{.....(15)}$$

$$S_K^{\alpha} = \frac{-K}{\alpha\omega_o R_2 C_2} \qquad \text{.....(16)}$$

Design Procedure

Given : $H_o, \alpha, \omega_o = 2\pi f_o$

Choose : $C_1 = C_2 = C$, a convenient value

Calculate : $K = H_o > 2$

$$R_2 = \frac{\alpha}{2\omega_o C}\left[1 + \sqrt{1 + \frac{4(H_o - 2)}{\alpha^2}}\right] \qquad \text{.....(17)}$$

$$R_1 = \frac{1}{\omega_o^2 C^2 R_2} \qquad \text{.....(18)}$$

If H_o is large, say greater than 10, there will be large spreads in element values and high sensitivities. An interesting design procedure is to use K to vary the sensitivities of circuit parameters.

Capacitors are ofter the components which have the largest temperature coefficients. It is possible to set K such that the overall α sensitivity is minimum, assuming that the capacitors drift equally. In this case we set

$$S_{C_1}^{\alpha} = -S_{C_2}^{\alpha}$$

Choose $C = C_1 = C_2$ and let $R_1 = R_2 = R$; then $K = 3 - \alpha$ and $R = 1/\omega_o C$.

Appendix E

CIRCUIT DIAGRAM OF POWER SUPPLY AND TTL INTERFACE

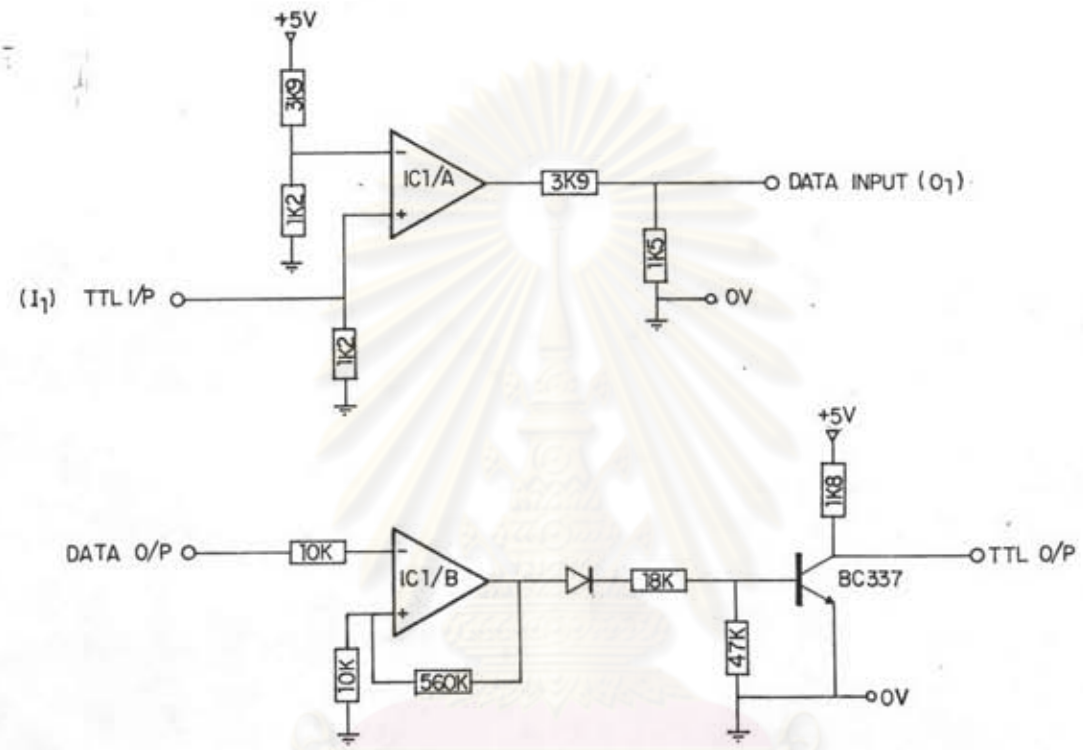


Figure 1 : Circuit diagram of TTL interface

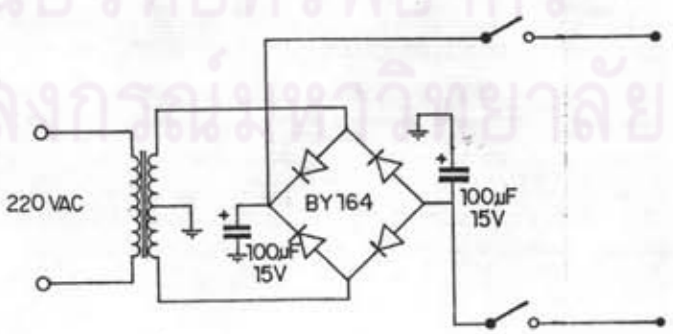


Figure 2 : Circuit diagram of power supply

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