CHAPTER II

CIRCUIT DESIGN

Principle of Design

Commercial tape recorders are normally relatively insensitive to low frequency audio input signals due to speed of tape related to the head, the width of air-gap in the head and the uniformity of magnetic particles on the tape itself. Therefore, from Figure 3 which is the frequency response of typical commercial tape recorder, we found that the response at low frequency is limited.

For this research we use 7 KHz as a carrier frequency (f_o). The amplitude of the input signal is limited by the breakdown voltage of the light emitting diode (LED) of the limiter and clip indicator circuit in order to make sure that carrier frequency (f_o) will not deviate higher than 9,000 Hz or lower than 5,000 Hz for particularly positive and negative input signal amplitude respectively.

The required specifications are summarized below:-

analog input

frequency : 0 - 300 Hz

amplitude : +1.5 V — -1.5 Vpp

digital input

bit rate : 0 - 600 bits/sec

amplitude : TTL level 0 - 5 V

output : 400 mv. to line input of tape recorder

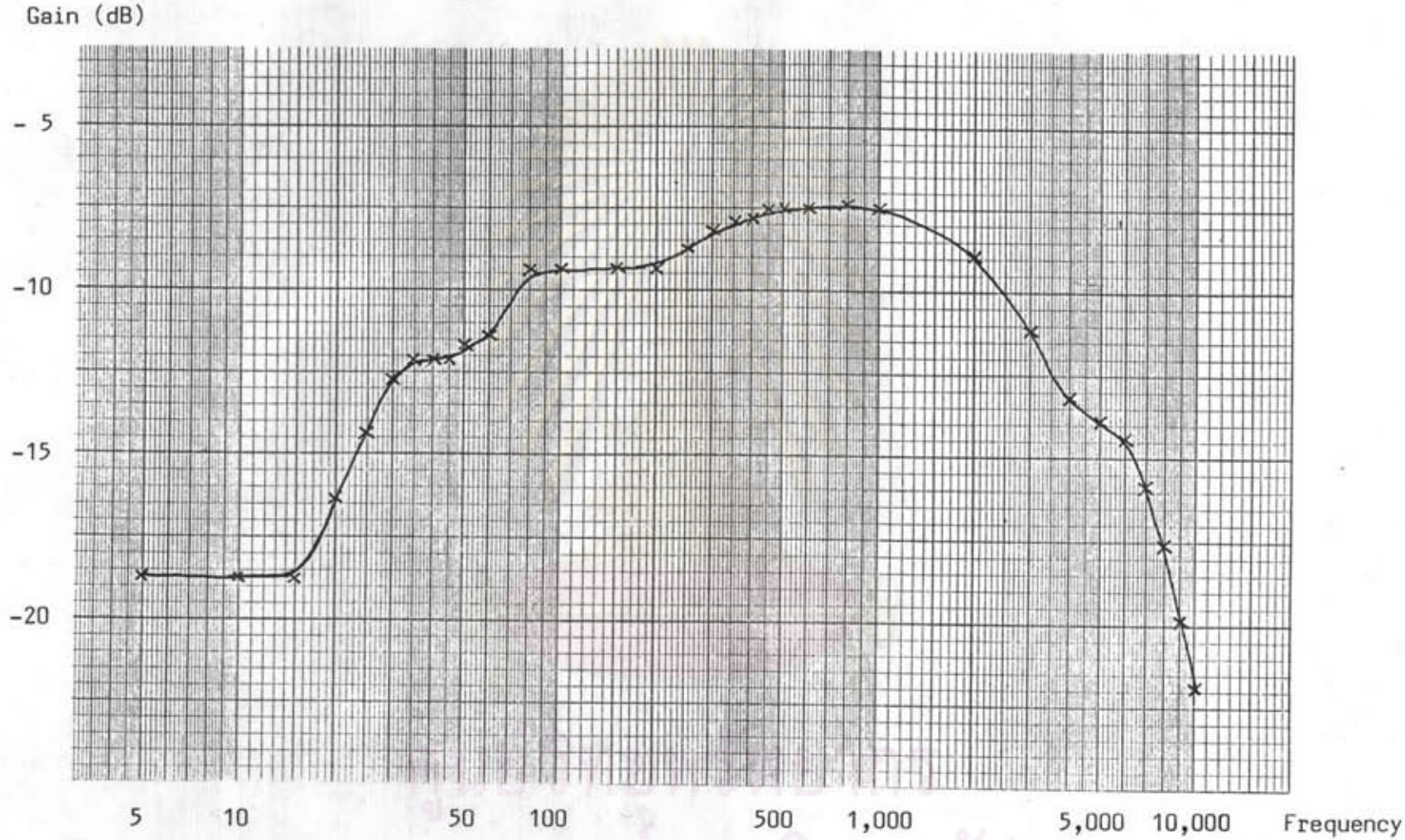


Figure 3 : Frequency response of commercial tape recorder

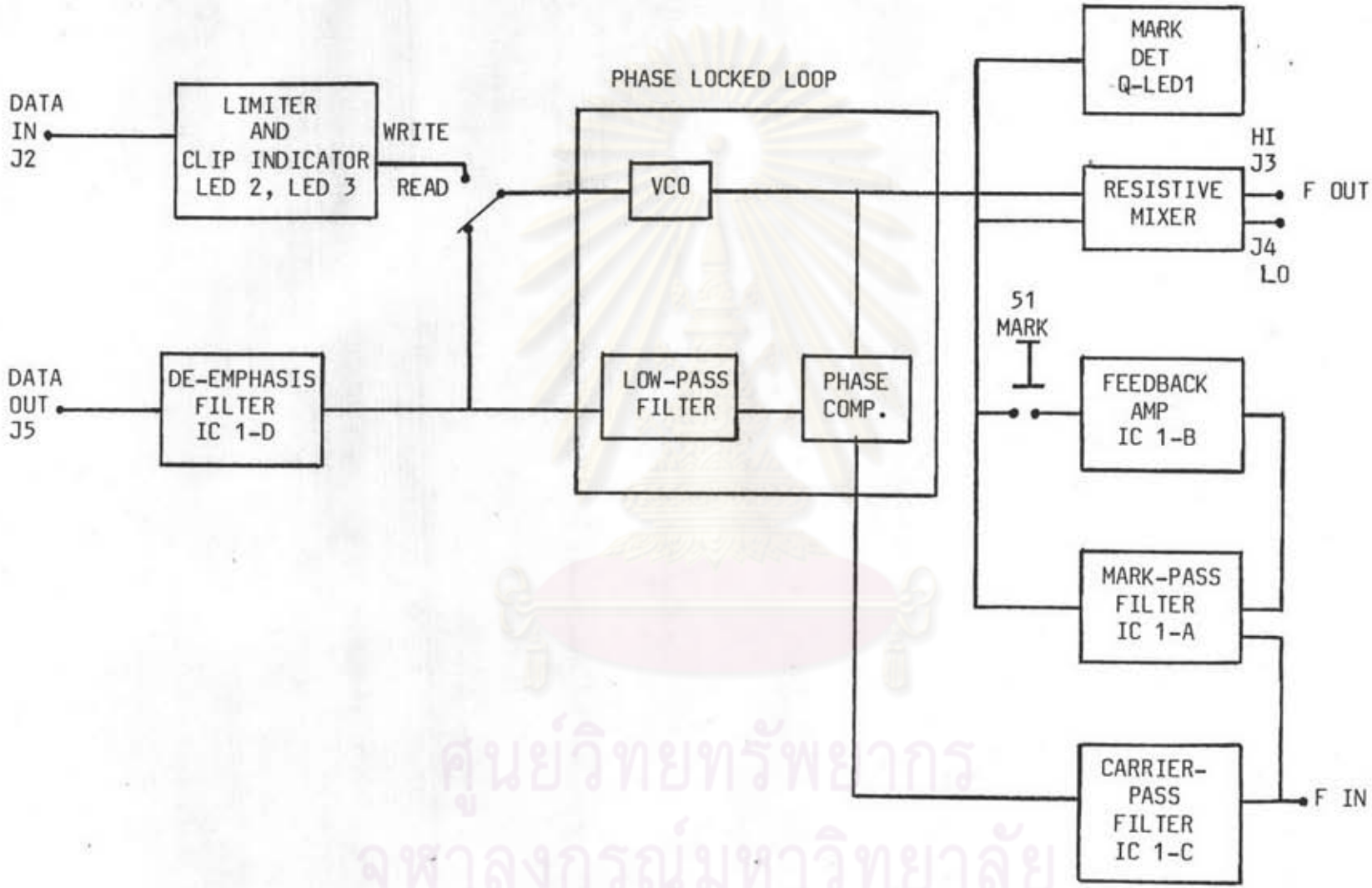


Figure 4 : Block diagram of data translator

Another feature should also be provided for application purposes such as the marker pulse and the TTL interface. Marker pulse can be injected on the tape to identify particular important portion of the recorded information. This feature is especially useful for data alignment and synchronization. TTL interface is also provided to record or reproduce logical input signal. Thus, computer data can be recorded through this data translator.

Data Translator Block Diagram

From the block diagram of Figure 4 the data input is firstly applied to a level limiter and clip indicator. The light emitting diodes LED 2 and LED 3 will be illuminated respectively when the negative or positive peaks of input signal exceed the diode breakdown voltage of 1.5 V. With the system in WRITE mode, the input signal is then applied to a phase-locked loop (IC2). The internal frequency is designed to be about 7 KHz when the input signal is zero. Positive and negative variations of the input signal will cause instantaneous frequency deviations of VCO output. The latter is applied to the tape recorder via resistive mixer. There are two outputs provided, 400 MV rms output for connecting with the tape recorder's line input and 30 MV rms signal for the recorder's microphone input. The frequency modulation output swings between 5,000 and 9,000 Hz which is suitable for every commercial recorder.

The mark-pass filter is an active, high Q, 600 Hz band-pass filter. When depressing the "MARK" switch, it will introduce this filter into the feedback amplifier and causing it to oscillate at about 600 Hz. This signal is added by resistive mixer with the frequency modulation signal, the combined signal will then pass

to the recorder and at the same time the mark detector will initiate the "LED MARK" indicator.

When the system is in the "READ" mode, the input signal from the tape recorder will go through a carrier-pass filter which protects the phase-locked loop from unnecessary noise (especially the 600 Hz marker signal). The signal from the tape recorder varies the frequency of the phase-locked loop and the de-emphasis filter removes the carrier from the signal, then reproduces the original signal back. If the 600Hz marker pulse is also recorded on the cassette tape, the mark-pass filter will detect and illuminate the "LED MARK" indicator.

Coder Circuit

Typical coder circuit of data translator is shown in Figure 5.

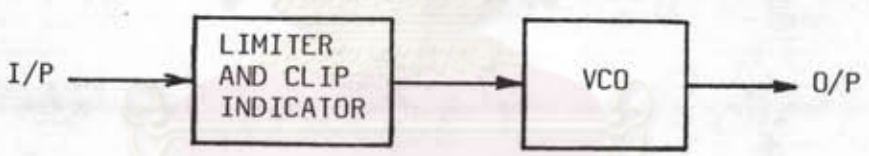


Figure 5 : Coder circuit

The function of limiter and clip indicator circuit is to limit the input signal at the desired magnitude according to the designed frequency deviation. This circuit does not only ensure that the VCO remains locked for the entire range of the limited input signal but also illuminate the LED indicator in order to enable the user to attenuate the input signal to the usable magnitude range.

The VCO is part of the PLL which will oscillate at the centre frequency (f_o) when there is no signal or noise at the input. VCO output will change according to the signal from the limiter and clip indicator circuit.

1. Voltage Control Oscillator

The HEF 40468-is selected to be used as a phase-locked loop. It consists of a linear voltage controlled oscillator (VCO) and two different phase comparators with a common signal input amplifier and a common comparator input.

From the graph of Figure 7 of appendix A between typical centre frequency as a function of capacitor C_1, the centre frequency is selected at 7,000 Hz and since VDD-Vss = 10 V, we found that

$$R_1 = 100\ k\Omega$$
$$\text{and} \quad C_1 = 1{,}300\ pf \qquad \text{.....(1)}$$

So the RC time constant of Eq. 1 is equal to 0.13 msec. The capacitor used in this circuit must be high precisioned of only 5% tolerance in order to ensure the oscillator stability. For the value of 1,500 pf can easily be found in the local market.

$$\text{Choose} \quad C_1 = 1{,}500\ pf$$
$$R_1 = 82\ k\Omega$$

Selected deviation frequency (f) = 2KHz

so f max = 7 + 2 = 9 KHz

and f min = 7 - 2 = 5 KHz

2. Limiter and Clip Indicator Circuit

We can use the breakdown voltage of LED to limit the signal input and also to be used as an oversignal input indicator. Connecting the two LEDs in parallel with reverse polarity can serve as the limiter circuit for input signal as shown in Figure 6.

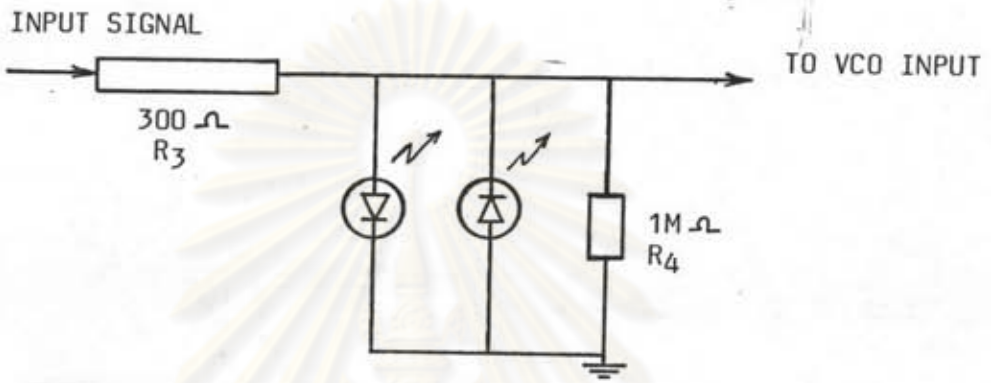


Figure 6 : Limiter circuit for input signal

R_3 is the potentiometer which is used to vary the required signal between 1.5 V. to -1.5 V. R_4 is used for high input impedance of VCO circuit. The complete circuit diagram of the limiter circuit and VCO is shown in Figure 7.

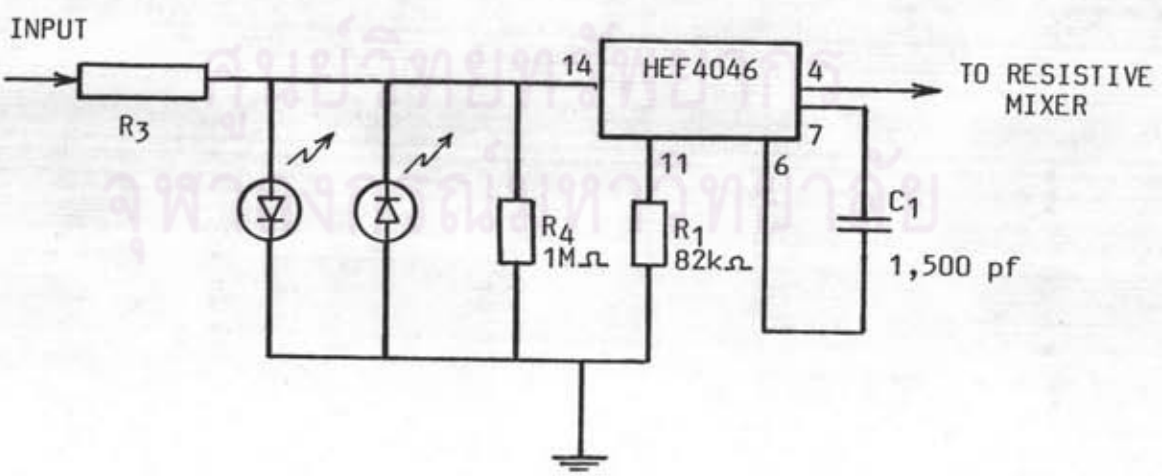


Figure 7

Complete circuit diagram for limiter circuit and VCO

Decoder Circuit

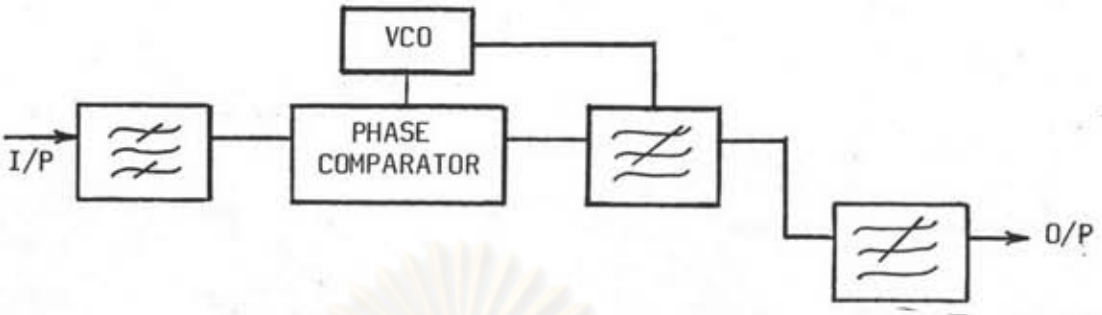


Figure 8 : Decoder circuit

The phase comparator and VCO are part of PLL. The input signal goes through the carrier-pass filter or band-pass filter which is designed to pass only 7 KHz carrier frequency for the purpose of protecting PLL from the noise bandwidth.

The phase comparator compares VCO frequency with input frequency. The different frequencies will go through the low-pass filter which has the bandwidth of more than 2 KHz. This demodulated signal will pass through the de-emphasis network for carrier rejection. Thus, the original signal is reproduced.

1. Carrier-Pass Filter

The carrier-pass filter is the active RC band-pass filter of the second order as shown in Figure 9.

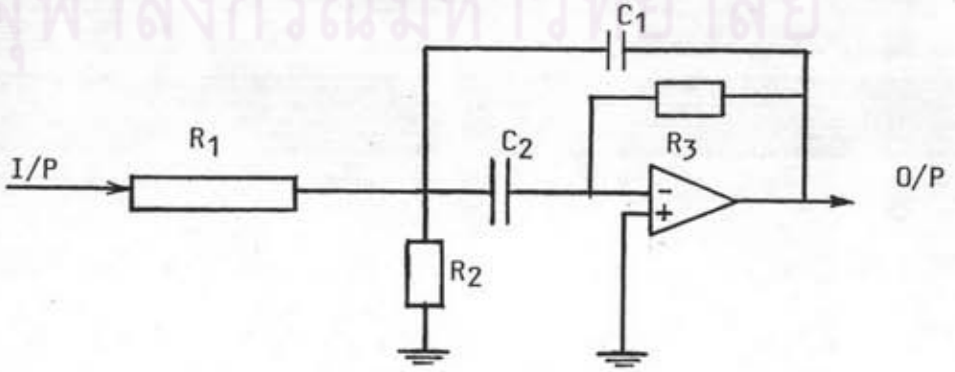


Figure 9 : Active RC band-pass filter of the second order

From appendix C

$$R' = \frac{R_1 R_2}{R_1 + R_2} \quad \text{.....(2)}$$

$$R_1 C_1 = \frac{Q}{\omega_o A_o} \quad \text{.....(3)}$$

$$R_3 \frac{C_1 C_2}{C_1 + C_2} = \frac{Q}{\omega_o} \quad \text{.....(4)}$$

$$R' R_3 C_1 C_2 = \frac{1}{\omega_o^2} \quad \text{.....(5)}$$

When Q = Quality factor

A_o = Midband voltage gain

o = Centre angular frequency

Choosen f_o = 7 KHz , A_o = 2 , Q = 3

C_1 = C_2 = 470 pf

o = $2\pi f_o = 2 \times \pi \times 7 \times 10^3$

= 43982 radian/sec .....(6)

Substitute ω_o in Eq. 3 yields

$$R_1 = \frac{Q}{C_1 \omega_o A_o} = \frac{3}{470 \times 10^{-12} \times 43982 \times 2}$$

= 72.56 kΩ .....(7)

From Eq. 4

$$R_3 = \frac{Q(C_1 + C_2)}{\omega_o C_1 C_2} = \frac{3\,(470 + 470) \times 10^{-12}}{43982\,(470 \times 10^{-12})^2}$$

= 290.25 kΩ .....(8)

From Eq. 5

$$R' = \frac{1}{R_3 C_1 C_2 \omega_o^2} = \frac{1}{290.25 \times 10^3\,(470 \times 10^{-12})^2\,(43982)^2}$$

= 8.06 kΩ .....(9)

Substitute R_1 and R' in Eq. 2 yields.

$$R_2 = \frac{R'R_1}{R_1 - R'} = \frac{(8.06)(72.56) \times 10^6}{(72.56 - 8.06) \times 10^3}$$

$$= 9.06 \text{ k}\Omega \qquad \text{.....(10)}$$

From calculation we found that

$R_1 = 72.56$ kΩ We choose $R_1 = 68$ kΩ

$R_2 = 9.06$ kΩ We choose $R_2 = 10$ kΩ

$R_3 = 290$ kΩ We choose $R_3 = 270$ kΩ

Then re-check by substitute $R_1 = 68$ kΩ and $R_2 = 10$ kΩ in Eq. 2 yields

$$R' = \frac{(68)(10) \times 10^6}{(68 + 10) \times 10^3} = 8.717 \text{ k}\Omega \qquad \text{.....(11)}$$

From Eq. 5

$$\omega_o^2 = \frac{1}{R'R_3 C_1 C_2}$$

$$= \frac{1}{8.717 \times 10^3 \times 270 \times 10^3 \times 470 \times 10^{-12} \times 470 \times 10^{-12}}$$

$$= 43856.78 \text{ radian/sec} \qquad \text{.....(12)}$$

$$f_o = 6.980 \text{ KHz} \qquad \text{.....(13)}$$

From Eq. 4

$$Q = \frac{\omega_o R_3 C_1 C_2}{C_1 + C_2}$$

$$= \frac{43856.78 \times 270 \times 10^3 \times 470 \times 10^{-12} \times 470 \times 10^{-12}}{(470 + 470) \times 10^{-12}}$$

$$= 2.78 \qquad \text{.....(14)}$$

From Eq. 3

$$A_o = \frac{Q}{\omega_o R_1 C_1} = \frac{2.78}{43856.78 \times 68 \times 10^3 \times 470 \times 10^{-12}}$$

$$= 1.983 \qquad \text{.....(15)}$$

Thus, from the assumption f_o, Q and A_o is deviate -0.28 %, -7.3 %, and -0.85 % respectively. The complete circuit diagram for the band-pass filter is shown in Figure 10.

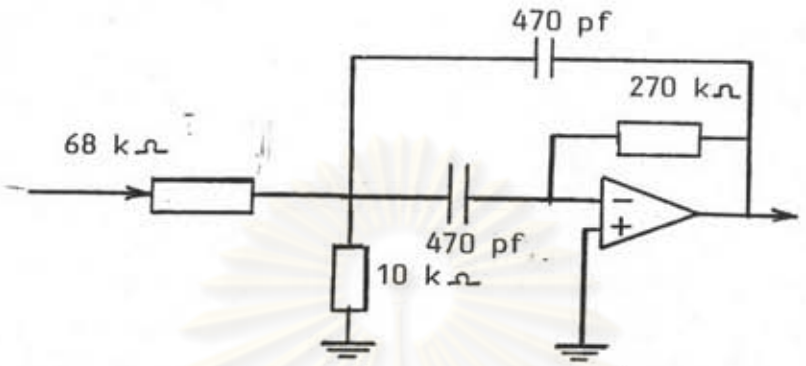


Figure 10 : Complete circuit diagram for the band-pass filter

2. Low-pass RC Filter

The output of built in phase comparator of HEF 4046B is fed through the external low-pass filter in order to control the VCO. The low-pass filter characteristics will determine the PLL capture range. Since the PLL can deviate from upto 2 KHz, therefore the low-pass filter should have the corner frequency more than 2 KHz.

Assuming f_c = 2.5 KHz

From $f_c = \frac{1}{2\pi RC}$

let C = 1,500 pf then

$$R = \frac{1}{2\pi f_c C} = \frac{1}{2 \times \pi \times 2.5 \times 10^3 \times 1{,}500 \times 10^{-12}}$$

$$= 42.44 \text{ k}\Omega \qquad \text{.....(16)}$$

Then we choose C = 1,500 pf and R = 39 kΩ

$$f_c = \frac{1}{2 \times \quad \times 1{,}500 \times 10^{-12} \times 39 \times 10^3}$$

$$= 2.720 \text{ kHz} \qquad \text{.....(17)}$$

Thus, f_c = 2.720 kHz is only +8 % deviate from the assumption. The complete circuit diagram is shown in Figure 11.

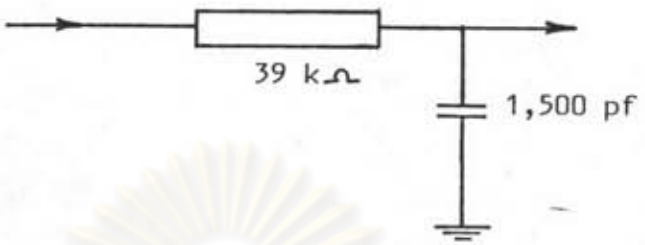


Figure 11 : Low-pass filter circuit

3. Low-pass Filter in "READ" Mode

The signal of phase comparator output during "READ" mode will pass through the low-pass filter for carrier rejection. This filter must have the impedance that should not load the control voltage so much. Therefore, the value of R must be equal to or higher than 39 kΩ. The typical RC low-pass circuit is shown in Figure 12.

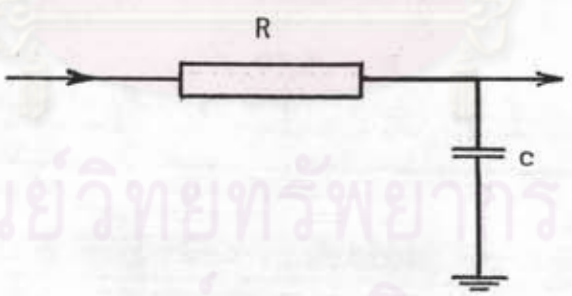


Figure 12 : The RC low-pass filter

$f = 6$ kHz

$R \geq 39$ kΩ

let $R = 39$ kΩ

$$C = \frac{1}{2\pi fR}$$

$$= \frac{1}{2 \times \pi \times 6 \times 10^3 \times 39 \times 10^3}$$

$$= 680 \text{ pf}$$

4. De-emphasis Filter

Since the analog signal is upto 300 Hz and the digital signal is 600 bits/sec, de-emphasis filter is designed to reject the carrier frequency above 600 Hz.

let $C_1 = C_2 = 4{,}700$ pf

and $R_1 = R_2 = R$

$f = 600$ Hz

From Eq. 18 of appendix D.

$$R_1R_2 = \frac{1}{\omega_o^2 C^2}$$

$$R = \frac{1}{2\pi f_o C}$$

$$R = \frac{1}{2 \times \pi \times 600 \times 4{,}700 \times 10^{-12}}$$

$$= \frac{10^8}{2 \times \pi \times 6 \times 47}$$

$$= 56.415 \text{ k}\Omega$$

used R $= 56 \text{ k}\Omega$

The complete circuit diagram of 3 and 4 is combined together as shown in Figure 13.

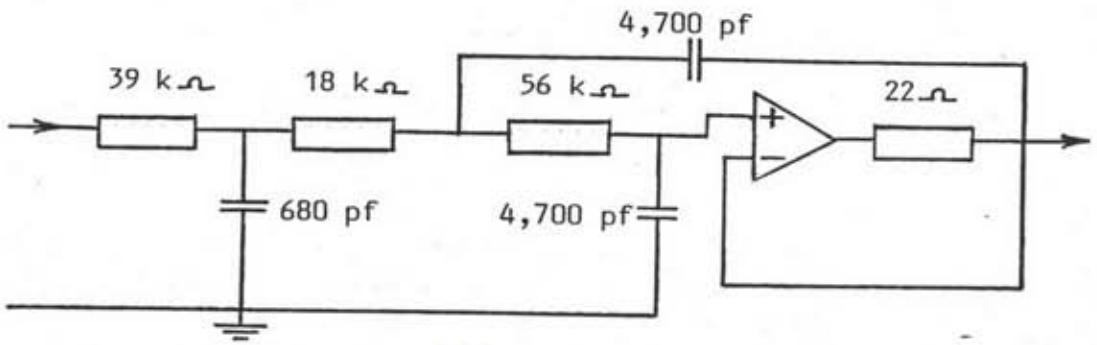
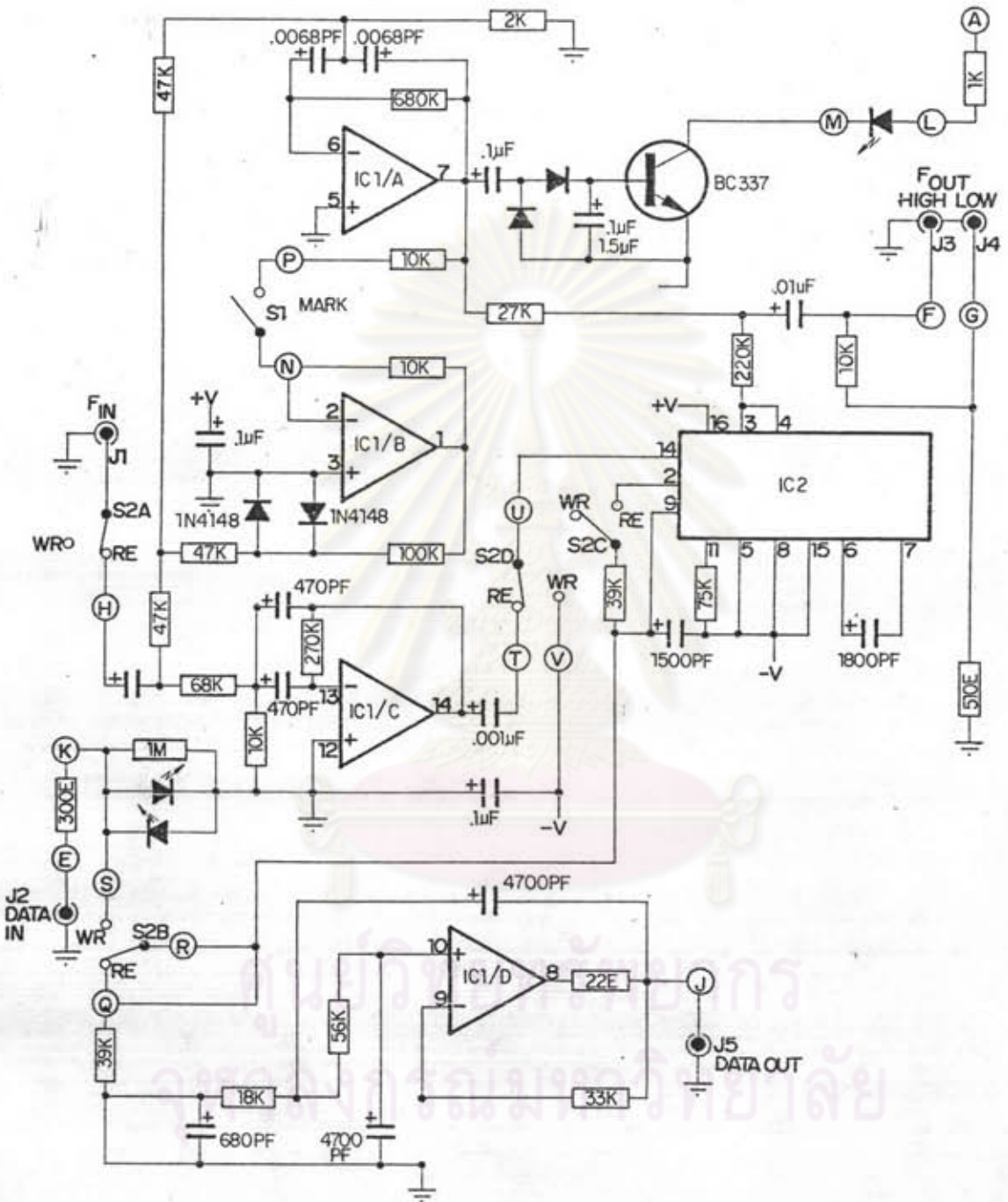


Figure 13 : Complete circuit diagram for de-emphasis filter

The 22Ω resistor is used for output short circuit protection. The overall circuit diagram of the data translator is shown Figure 14.



IC 1 – LM 324 N

IC 2 – HEF 4046 B

Figure 14 : Circuit diagram of the data translator