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ภาคผนวก ก

ข้อมูลของไมโครโปรเซสเซอร์ Z80

Z80®-CPU
Z80A-CPU

Product Specification

MARCH 1978

The Zilog Z80 product line is a complete set of microcomputer components, development systems and support software. The Z80 microcomputer component set includes all of the circuits necessary to build high-performance microcomputer systems with virtually no other logic and a minimum number of low cost standard memory elements.

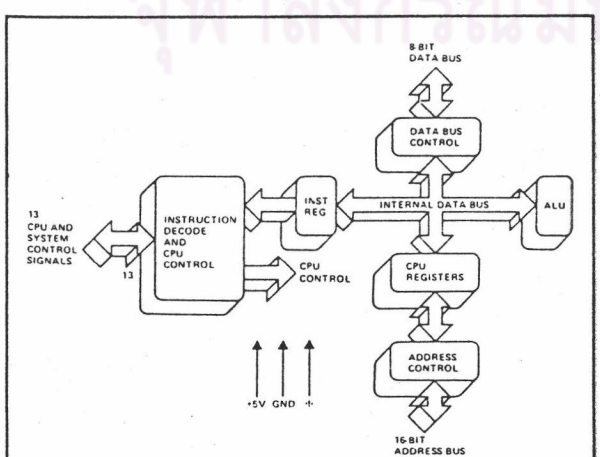
The Z80 and Z80A CPU's are third generation single chip microprocessors with unrivaled computational power. This increased computational power results in higher system through-put and more efficient memory utilization when compared to second generation microprocessors. In addition, the Z80 and Z80A CPU's are very easy to implement into a system because of their single voltage requirement plus all output signals are fully decoded and timed to control standard memory or peripheral circuits. The circuit is implemented using an N-channel, ion implanted, silicon gate MOS process.

Figure 1 is a block diagram of the CPU, Figure 2 details the internal register configuration which contains 208 bits of Read/Write memory that are accessible to the programmer. The registers include two sets of six general purpose registers that may be used individually as 8-bit registers or as 16-bit register pairs. There are also two sets of accumulator and flag registers. The programmer has access to either set of main or alternate registers through a group of exchange instructions. This alternate set allows foreground/background mode of operation or may be reserved for very fast Interrupt response. Each CPU also contains a 16-bit stack pointer which permits simple implementation of multiple level interrupts, unlimited subroutine nesting and simplification of many types of data handling.

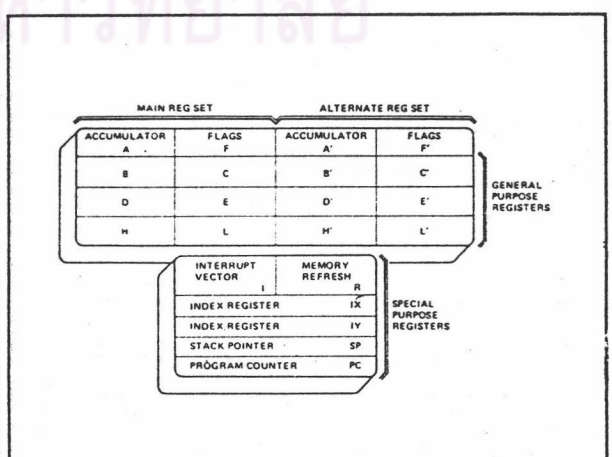
The two 16-bit index registers allow tabular data manipulation and easy implementation of relocatable code. The Refresh register provides for automatic, totally transparent refresh of external dynamic memories. The I register is used in a powerful interrupt response mode to form the upper 8 bits of a pointer to a interrupt service address table, while the interrupting device supplies the lower 8 bits of the pointer. An indirect call is then made to this service address.

FEATURES

- Single chip, N-channel Silicon Gate CPU.
- 158 instructions—includes all 78 of the 8080A instructions with total software compatibility. New instructions include 4-, 8- and 16-bit operations with more useful addressing modes such as indexed, bit and relative.
- 17 internal registers.
- Three modes of fast interrupt response plus a non-maskable interrupt.
- Directly interfaces standard speed static or dynamic memories with virtually no external logic.
- 1.0 μs instruction execution speed.
- Single 5 VDC supply and single-phase 5 volt Clock.
- Out-performs any other single chip microcomputer in 4-, 8-, or 16-bit applications.
- All pins TTL Compatible
- Built-in dynamic RAM refresh circuitry.

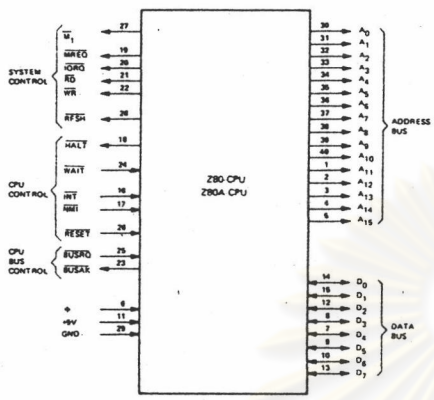


Z80, Z80A CPU BLOCK DIAGRAM



Z80, Z80A CPU REGISTERS

Z80, Z80A-CPU Pin Description



Z80, Z80A CPU PIN CONFIGURATION

A_0-A_{15} (Address Bus)
Tri-state output, active high. A_0-A_{15} constitute a 16-bit address bus. The address bus provides the address for memory (up to 64K bytes) data exchanges and for I/O device data exchanges.

D_0-D_7 (Data Bus)
Tri-state input/output, active high. D_0-D_7 constitute an 8-bit bidirectional data bus. The data bus is used for data exchanges with memory and I/O devices.

$\overline{M_1}$ (Machine Cycle one)
Output, active low. $\overline{M_1}$ indicates that the current machine cycle is the OP code fetch cycle of an instruction execution.

$\overline{MREQ}$ (Memory Request)
Tri-state output, active low. The memory request signal indicates that the address bus holds a valid address for a memory read or memory write operation.

$\overline{IORQ}$ (Input/ Output Request)
Tri-state output, active low. The $\overline{IORQ}$ signal indicates that the lower half of the address bus holds a valid I/O address for a I/O read or write operation. An $\overline{IORQ}$ signal is also generated when an interrupt is being acknowledged to indicate that an interrupt response vector can be placed on the data bus.

$\overline{RD}$ (Memory Read)
Tri-state output, active low. $\overline{RD}$ indicates that the CPU wants to read data from memory or an I/O device. The addressed I/O device or memory should use this signal to gate data onto the CPU data bus.

$\overline{WR}$ (Memory Write)
Tri-state output, active low. $\overline{WR}$ indicates that the CPU data bus holds valid data to be stored in the addressed memory or I/O device.

$\overline{RFSH}$ (Refresh)
Output, active low. $\overline{RFSH}$ indicates that the lower 7 bits of the address bus contain a refresh address for dynamic memories and the current $\overline{MREQ}$ signal should be used to do a refresh read to all dynamic memories.

$\overline{HALT}$ (Halt state)
Output, active low. $\overline{HALT}$ indicates that the CPU has executed a HALT software instruction and is awaiting either a non-maskable or a maskable interrupt (with the mask enabled) before operation can resume. While halted, the CPU executes NOP's to maintain memory refresh activity.

$\overline{WAIT}$ (Wait)
Input, active low. $\overline{WAIT}$ indicates to the Z-80 CPU that the addressed memory or I/O devices are not ready for a data transfer. The CPU continues to enter wait states for as long as this signal is active.

$\overline{INT}$ (Interrupt Request)
Input, active low. The Interrupt Request signal is generated by I/O devices. A request will be honored at the end of the current instruction if the internal software controlled interrupt enable flip-flop (IFF) is enabled.

$\overline{NMI}$ (Non Maskable Interrupt)
Input, active low. The non-maskable nterrupt request line has a higher priority than $\overline{INT}$ and is always recognized at the end of the current instruction, independent of the status of the interrupt enable flip-flop. $\overline{NMI}$ automatically forces the Z-80 CPU to restart to location 0066_H.

$\overline{RESET}$
Input, active low. $\overline{RESET}$ initializes the CPU as follows: reset interrupt enable flip-flop, clear PC and registers I and R and set interrupt to 8080A mode. During reset time, the address and data bus go to a high impedance state and all control output signals go to the inactive state.

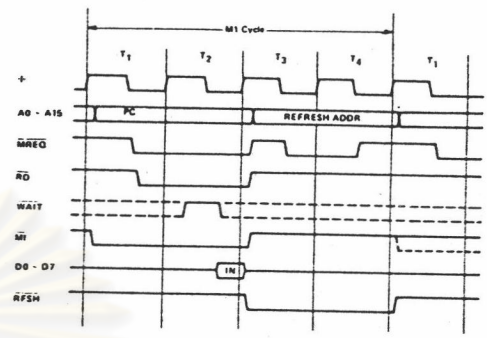
$\overline{BUSRQ}$ (Bus Request)
Input, active low. The bus request signal has a higher priority than $\overline{NMI}$ and is always recognized at the end of the current machine cycle and is used to request the CPU address bus, data bus and tri-state output control signals to go to a high impedance state so that other devices can control these busses.

$\overline{BUSAK}$ (Bus Acknowledge)
Output, active low. Bus acknowledge is used to indicate to the requesting device that the CPU address bus, data bus and tri-state control bus signals have been set to their high impedance state and the external device can now control these signals.

Timing Waveforms

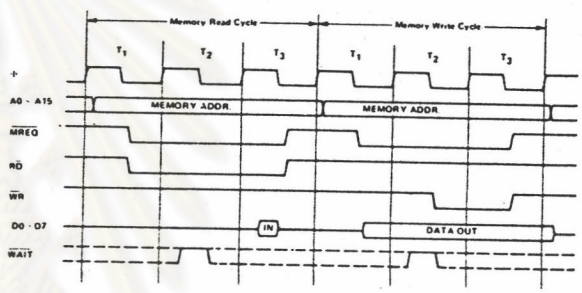
INSTRUCTION OP CODE FETCH

The program counter content (PC) is placed on the address bus immediately at the start of the cycle. One half clock time later $\overline{MREQ}$ goes active. The falling edge of $\overline{MREQ}$ can be used directly as a chip enable to dynamic memories. $\overline{RD}$ when active indicates that the memory data should be enabled onto the CPU data bus. The CPU samples data with the rising edge of the clock state T_3. Clock states T_3 and T_4 of a fetch cycle are used to refresh dynamic memories while the CPU is internally decoding and executing the instruction. The refresh control signal $\overline{RFSH}$ indicates that a refresh read of all dynamic memories should be accomplished.



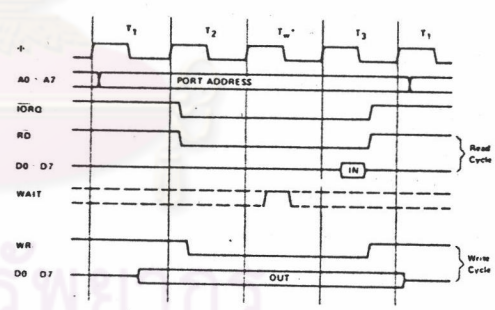
MEMORY READ OR WRITE CYCLES

Illustrated here is the timing of memory read or write cycles other than an OP code fetch (M_1 cycle). The $\overline{MREQ}$ and $\overline{RD}$ signals are used exactly as in the fetch cycle. In the case of a memory write cycle, the $\overline{MREQ}$ also becomes active when the address bus is stable so that it can be used directly as a chip enable for dynamic memories. The $\overline{WR}$ line is active when data on the data bus is stable so that it can be used directly as a R/W pulse to virtually any type of semiconductor memory.



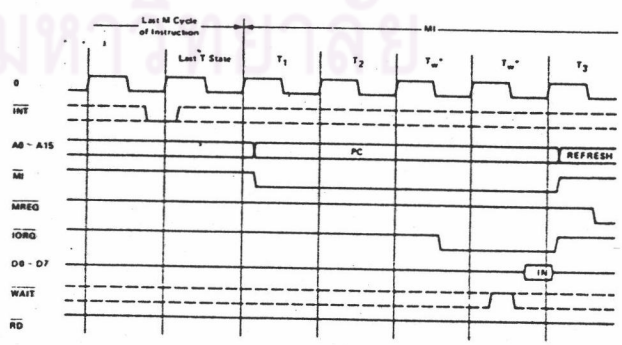
INPUT OR OUTPUT CYCLES

Illustrated here is the timing for an I/O read or I/O write operation. Notice that during I/O operations a single wait state is automatically inserted (Tw*). The reason for this is that during I/O operations this extra state allows sufficient time for an I/O port to decode its address and activate the $\overline{WAIT}$ line if a wait is required.



INTERRUPT REQUEST/ACKNOWLEDGE CYCLE

The interrupt signal is sampled by the CPU with the rising edge of the last clock at the end of any instruction. When an interrupt is accepted, a special M_1 cycle is generated. During this M_1 cycle, the $\overline{IORQ}$ signal becomes active (instead of $\overline{MREQ}$) to indicate that the interrupting device can place an 8-bit vector on the data bus. Two wait states (Tw*) are automatically added to this cycle so that a ripple priority interrupt scheme, such as the one used in the Z80 peripheral controllers, can be easily implemented.



Z80, Z80A Instruction Set

The following is a summary of the Z80, Z80A instruction set showing the assembly language mnemonic and the symbolic operation performed by the instruction. A more detailed listing appears in the Z80-CPU technical manual, and assembly language programming manual. The instructions are divided into the following categories:

8-bit loads	Miscellaneous Group
16-bit loads	Rotates and Shifts
Exchanges	Bit Set, Reset and Test
Memory Block Moves	Input and Output
Memory Block Searches	Jumps
8-bit arithmetic and logic	Calls
16-bit arithmetic	Restarts
General purpose Accumulator & Flag Operations	Returns

In the table the following terminology is used.

b ≡ a bit number in any 8-bit register or memory location

cc ≡ flag condition code
- NZ ≡ non zero
- Z ≡ zero
- NC ≡ non carry
- C ≡ carry
- PO ≡ Parity odd or no over flow
- PE ≡ Parity even or over flow
- P ≡ Positive
- M ≡ Negative (minus)

d ≡ any 8-bit destination register or memory location

dd ≡ any 16-bit destination register or memory location

e ≡ 8-bit signed 2's complement displacement used in relative jumps and indexed addressing

L ≡ 8 special call locations in page zero. In decimal notation these are 0, 8, 16, 24, 32, 40, 48 and 56

n ≡ any 8-bit binary number

nn ≡ any 16-bit binary number

r ≡ any 8-bit general purpose register (A, B, C, D, E, H, or L)

s ≡ any 8-bit source register or memory location

s_b ≡ a bit in a specific 8-bit register or memory location

ss ≡ any 16-bit source register or memory location

subscript "L" ≡ the low order 8 bits of a 16-bit register

subscript "H" ≡ the high order 8 bits of a 16-bit register

( ) ≡ the contents within the ( ) are to be used as a pointer to a memory location or I/O port number

8-bit registers are A, B, C, D, E, H, L, I and R

16-bit register pairs are AF, BC, DE and HL

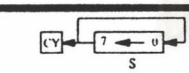
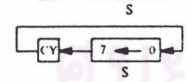
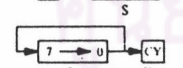
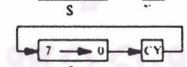
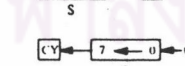
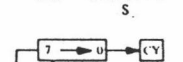
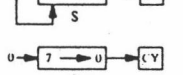
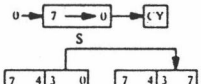
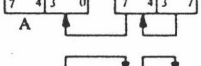
16-bit registers are SP, PC, IX and IY

Addressing Modes implemented include combinations of the following:

Immediate	Indexed
Immediate extended	Register
Modified Page Zero	Implied
Relative	Register Indirect
Extended	Bit

	Mnemonic	Symbolic Operation	Comments
8-BIT LOADS	LD r, s	r ← s	s ≡ r, n, (HL), (IX+e), (IY+e)
	LD d, r	d ← r	d ≡ (HL), r (IX+e), (IY+e)
	LD d, n	d ← n	d ≡ (HL), (IX+e), (IY+e)
	LD A, s	A ← s	s ≡ (BC), (DE), (nn), I, R
	LD d, A	d ← A	d ≡ (BC), (DE), (nn), I, R
16-BIT LOADS	LD dd, nn	dd ← nn	dd ≡ BC, DE, HL, SP, IX, IY
	LD dd, (nn)	dd ← (nn)	dd ≡ BC, DE, HL, SP, IX, IY
	LD (nn), ss	(nn) ← ss	ss ≡ BC, DE, HL, SP, IX, IY
	LD SP, ss	SP ← ss	ss = HL, IX, IY
	PUSH ss	$(SP-1) \leftarrow ss_H$; $(SP-2) \leftarrow ss_L$	ss = BC, DE, HL, AF, IX, IY
	POP dd	$dd_L \leftarrow (SP)$; $dd_H \leftarrow (SP+1)$	dd = BC, DE, HL, AF, IX, IY
EXCHANGES	EX DE, HL	DE ↔ HL	
	EX AF, AF'	AF ↔ AF'	
	EXX	$\begin{pmatrix} BC \\ DE \\ HL \end{pmatrix} \leftrightarrow \begin{pmatrix} BC' \\ DE' \\ HL' \end{pmatrix}$	
	EX (SP), ss	$(SP) \leftrightarrow ss_L$, $(SP+1) \leftrightarrow ss_H$	ss ≡ HL, IX, IY

	Mnemonic	Symbolic Operation	Comments
MEMORY BLOCK MOVES	LDI	(DE) ← (HL), DE ← DE+1 HL ← HL+1, BC ← BC-1	
	LDIR	(DE) ← (HL), DE ← DE+1 HL ← HL+1, BC ← BC-1 Repeat until BC = 0	
	LDD	(DE) ← (HL), DE ← DE-1 HL ← HL-1, BC ← BC-1	
	LDDR	(DE) ← (HL), DE ← DE-1 HL ← HL-1, BC ← BC-1 Repeat until BC = 0	
MEMORY BLOCK SEARCHES	CPI	A-(HL), HL ← HL+1 BC ← BC-1	
	CPIR	A-(HL), HL ← HL+1 BC ← BC-1, Repeat until BC = 0 or A = (HL)	A-(HL) sets the flags only. A is not affected
	CPD	A-(HL), HL ← HL-1 BC ← BC-1	
	CPDR	A-(HL), HL ← HL-1 BC ← BC-1, Repeat until BC= 0 or A = (HL)	
8-BIT ALU	ADD s	A ← A + s	
	ADC s	A ← A + s + CY	CY is the carry flag
	SUB s	A ← A - s	
	SBC s	A ← A - s - CY	s ≡ r, n, (HL) (IX+e), (IY+e)
	AND s	A ← A ∧ s	
	OR s	A ← A ∨ s	
	XOR s	A ← A ⊕ s	

	Mnemonic	Symbolic Operation	Comments
8-BIT ALU	CP s	A - s	s = r, n (HL) (IX+e), (IY+e)
	INC d	d ← d + 1	d = r, (HL) (IX+e), (IY+e)
	DEC d	d ← d - 1	
16-BIT ARITHMETIC	ADD HL, ss	HL ← HL + ss	ss ≡ BC, DE HL, SP
	ADC HL, ss	HL ← HL + ss + CY	
	SBC HL, ss	HL ← HL - ss - CY	
	ADD IX, ss	IX ← IX + ss	ss ≡ BC, DE, IX, SP
	ADD IY, ss	IY ← IY + ss	ss ≡ BC, DE, IY, SP
	INC dd	dd ← dd + 1	dd ≡ BC, DE, HL, SP, IX, IY
	DEC dd	dd ← dd - 1	dd ≡ BC, DE, HL, SP, IX, IY
GP ACC. & FLAG	DAA	Converts A contents into packed BCD following add or subtract.	Operands must be in packed BCD format
	CPL	$A \leftarrow \overline{A}$	
	NEG	A ← 00 - A	
	CCF	$CY \leftarrow \overline{CY}$	
	SCF	CY ← 1	
MISCELLANEOUS	NOP	No operation	
	HALT	Halt CPU	
	DI	Disable Interrupts	
	EI	Enable Interrupts	
	IM 0	Set interrupt mode 0	8080A mode
	IM 1	Set interrupt mode 1	Call to 0038_H
	IM 2	Set interrupt mode 2	Indirect Call
ROTATES AND SHIFTS	RLC s		s ≡ r, (HL) (IX+e), (IY+e)
	RL s		
	RRC s		
	RR s		
	SLA s		
	SRA s		
	SRL s		
	RLD		
	RRD		

	Mnemonic	Symbolic Operation	Comments
BIT S. R. & T	BIT b, s	$Z \leftarrow \overline{s_b}$	Z is zero flag
	SET b, s	$s_b \leftarrow 1$	s ≡ r, (HL) (IX+e), (IY+e)
	RES b, s	$s_b \leftarrow 0$	
INPUT AND OUTPUT	IN A, (n)	A ← (n)	
	IN r, (C)	r ← (C)	Set flags
	INI	(HL) ← (C), HL ← HL + 1 B ← B - 1	
	INIR	(HL) ← (C), HL ← HL + 1 B ← B - 1 Repeat until B = 0	
	IND	(HL) ← (C), HL ← HL - 1 B ← B - 1	
	INDR	(HL) ← (C). HL ← HL - 1 B ← B - 1 Repeat until B = 0	
	OUT(n), A	(n) ← A	
	OUT(C), r	(C) ← r	
	OUTI	(C) ← (HL), HL ← HL + 1 B ← B - 1	
	OTIR	(C) ← (HL). HL ← HL + 1 B ← B - 1 Repeat until B = 0	
	OUTD	(C) ← (HL), HL ← HL - 1 B ← B - 1	
	OTDR	(C) ← (HL), HL ← HL - 1 B ← B - 1 Repeat until B = 0	
JUMPS	JP nn	PC ← nn	cc { NZ PO; Z PE; NC P; C M
	JP cc, nn	If condition cc is true PC ← nn, else continue	
	JR e	PC ← PC + e	
	JR kk, e	If condition kk is true PC ← PC + e, else continue	kk { NZ NC; Z C
	JP (ss)	PC ← ss	ss = HL, IX, IY
	DJNZ e	B ← B - 1, if B = 0 continue, else PC ← PC + e	
CALLS	CALL nn	$(SP-1) \leftarrow PC_H$ $(SP-2) \leftarrow PC_L$, PC ← nn	cc { NZ PO; Z PE; NC P; C M
	CALL cc, nn	If condition cc is false continue, else same as CALL nn	
RESTARTS	RST L	$(SP-1) \leftarrow PC_H$ $(SP-2) \leftarrow PC_L$, $PC_H \leftarrow 0$ $PC_L \leftarrow L$	
RETURNS	RET	$PC_L \leftarrow (SP)$, $PC_H \leftarrow (SP+1)$	cc { NZ PO; Z PE; NC P; C M
	RET cc	If condition cc is false continue, else same as RET	
	RETI	Return from interrupt, same as RET	
	RETN	Return from non-maskable interrupt	

A.C. Characteristics Z80-CPU

T_A = 0°C to 70°C, Vcc = +5V ± 5%, Unless Otherwise Noted.

Signal	Symbol	Parameter	Min	Max	Unit	Test Condition
Φ	t_c	Clock Period	4	[12]	μsec	
	$t_{w(\Phi H)}$	Clock Pulse Width, Clock High	180	[E]	nsec	
	$t_{w(\Phi L)}$	Clock Pulse Width, Clock Low	180	2000	nsec	
	$t_{r,f}$	Clock Rise and Fall Time		30	nsec	
A_{0-15}	$t_{D(AD)}$	Address Output Delay		145	nsec	C_L = 50pF
	$t_{F(AD)}$	Delay to Float		110	nsec	
	t_{acm}	Address Stable Prior to $\overline{MREQ}$ (Memory Cycle)	[1]		nsec	
	t_{aci}	Address Stable Prior to $\overline{IORQ}$, $\overline{RD}$ or $\overline{WR}$ (I/O Cycle)	[2]		nsec	
	t_{ca}	Address Stable from $\overline{RD}$, $\overline{WR}$, $\overline{IORQ}$ or $\overline{MREQ}$	[3]		nsec	
	t_{caf}	Address Stable From $\overline{RD}$ or $\overline{WR}$ During Float	[4]		nsec	
D_{0-7}	$t_{D(D)}$	Data Output Delay		230	nsec	C_L = 50pF
	$t_{F(D)}$	Delay to Float During Write Cycle		90	nsec	
	$t_{S\Phi(D)}$	Data Setup Time to Rising Edge of Clock During M1 Cycle	50		nsec	
	$t_{S\overline{\Phi}(D)}$	Data Setup Time to Falling Edge of Clock During M2 to M5	60		nsec	
	t_{dcm}	Data Stable Prior to $\overline{WR}$ (Memory Cycle)	[5]		nsec	
	t_{dci}	Data Stable Prior to $\overline{WR}$ (I/O Cycle)	[6]		nsec	
	t_{cdf}	Data Stable From $\overline{WR}$	[7]			
	t_H	Any Hold Time for Setup Time	0		nsec	
$\overline{MREQ}$	$t_{DL\overline{\Phi}(MR)}$	$\overline{MREQ}$ Delay From Falling Edge of Clock, $\overline{MREQ}$ Low		100	nsec	C_L = 50pF
	$t_{DH\Phi(MR)}$	$\overline{MREQ}$ Delay From Rising Edge of Clock, $\overline{MREQ}$ High		100	nsec	
	$t_{DH\overline{\Phi}(MR)}$	$\overline{MREQ}$ Delay From Falling Edge of Clock, $\overline{MREQ}$ High		100	nsec	
	$t_{w(\overline{MRL})}$	Pulse Width, $\overline{MREQ}$ Low	[8]		nsec	
	$t_{w(\overline{MRH})}$	Pulse Width, $\overline{MREQ}$ High	[9]		nsec	
$\overline{IORQ}$	$t_{DL\Phi(IR)}$	$\overline{IORQ}$ Delay From Rising Edge of Clock, $\overline{IORQ}$ Low		90	nsec	C_L = 50pF
	$t_{DL\overline{\Phi}(IR)}$	$\overline{IORQ}$ Delay From Falling Edge of Clock, $\overline{IORQ}$ Low		110	nsec	
	$t_{DH\Phi(IR)}$	$\overline{IORQ}$ Delay From Rising Edge of Clock, $\overline{IORQ}$ High		100	nsec	
	$t_{DH\overline{\Phi}(IR)}$	$\overline{IORQ}$ Delay From Falling Edge of Clock, $\overline{IORQ}$ High		110	nsec	
$\overline{RD}$	$t_{DL\Phi(RD)}$	$\overline{RD}$ Delay From Rising Edge of Clock, $\overline{RD}$ Low		100	nsec	C_L = 50pF
	$t_{DL\overline{\Phi}(RD)}$	$\overline{RD}$ Delay From Falling Edge of Clock, $\overline{RD}$ Low		130	nsec	
	$t_{DH\Phi(RD)}$	$\overline{RD}$ Delay From Rising Edge of Clock, $\overline{RD}$ High		100	nsec	
	$t_{DH\overline{\Phi}(RD)}$	$\overline{RD}$ Delay From Falling Edge of Clock, $\overline{RD}$ High		110	nsec	
$\overline{WR}$	$t_{DL\Phi(WR)}$	$\overline{WR}$ Delay From Rising Edge of Clock, $\overline{WR}$ Low		80	nsec	C_L = 50pF
	$t_{DL\overline{\Phi}(WR)}$	$\overline{WR}$ Delay From Falling Edge of Clock, $\overline{WR}$ Low		90	nsec	
	$t_{DH\overline{\Phi}(WR)}$	$\overline{WR}$ Delay From Falling Edge of Clock, $\overline{WR}$ High		100	nsec	
	$t_{w(\overline{WRL})}$	Pulse Width, $\overline{WR}$ Low	[10]		nsec	
$\overline{M1}$	$t_{DL(M1)}$	$\overline{M1}$ Delay From Rising Edge of Clock, $\overline{M1}$ Low		130	nsec	C_L = 50pF
	$t_{DH(M1)}$	$\overline{M1}$ Delay From Rising Edge of Clock, $\overline{M1}$ High		130	nsec	
$\overline{RFSH}$	$t_{DL(RF)}$	$\overline{RFSH}$ Delay From Rising Edge of Clock, $\overline{RFSH}$ Low		180	nsec	C_L = 50pF
	$t_{DH(RF)}$	$\overline{RFSH}$ Delay From Rising Edge of Clock, $\overline{RFSH}$ High		150	nsec	
$\overline{WAIT}$	$t_{s(WT)}$	$\overline{WAIT}$ Setup Time to Falling Edge of Clock	70		nsec	
$\overline{HALT}$	$t_{D(HT)}$	$\overline{HALT}$ Delay Time From Falling Edge of Clock		300	nsec	C_L = 50pF
$\overline{INT}$	$t_{s(IT)}$	$\overline{INT}$ Setup Time to Rising Edge of Clock	80		nsec	
$\overline{NMI}$	$t_{w(\overline{NML})}$	Pulse Width, $\overline{NMI}$ Low	80		nsec	
$\overline{BUSRQ}$	$t_{s(BQ)}$	$\overline{BUSRQ}$ Setup Time to Rising Edge of Clock	80		nsec	
$\overline{BUSAK}$	$t_{DL(BA)}$	$\overline{BUSAK}$ Delay From Rising Edge of Clock, $\overline{BUSAK}$ Low		120	nsec	C_L = 50pF
	$t_{DH(BA)}$	$\overline{BUSAK}$ Delay From Falling Edge of Clock, $\overline{BUSAK}$ High		110	nsec	
$\overline{RESET}$	$t_{s(RS)}$	$\overline{RESET}$ Setup Time to Rising Edge of Clock	90		nsec	
	$t_{F(C)}$	Delay to Float ($\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$ and $\overline{WR}$)		100	nsec	
	t_{mr}	$\overline{M1}$ Stable Prior to $\overline{IORQ}$ (Interrupt Ack.)	[11]		nsec	

[12] $t_c = t_{w(\Phi H)} + t_{w(\Phi L)} + t_r + t_f$

[1] $t_{acm} = t_{w(\Phi H)} + t_f - 75$

[2] $t_{aci} = t_c - 80$

[3] $t_{ca} = t_{w(\Phi L)} + t_r - 40$

[4] $t_{caf} = t_{w(\Phi L)} + t_r - 60$

[5] $t_{dcm} = t_c - 210$

[6] $t_{dci} = t_{w(\Phi L)} + t_r - 210$

[7] $t_{cdf} = t_{w(\Phi L)} + t_r - 80$

[8] $t_{w(MRL)} = t_c - 40$

[9] $t_{w(MRH)} = t_{w(\Phi H)} + t_f - 30$

[10] $t_{w(\overline{WRL})} = t_c - 40$

[11] $t_{mr} = 2t_c + t_{w(\Phi H)} + t_f - 80$

NOTES:

A. Data should be enabled onto the CPU data bus when $\overline{RD}$ is active. During interrupt acknowledge data should be enabled when $\overline{M1}$ and $\overline{IORQ}$ are both active.

B. All control signals are internally synchronized, so they may be totally asynchronous with respect to the clock.

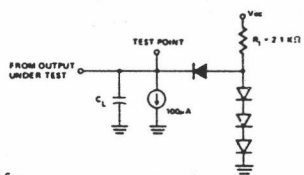
C. The $\overline{RESET}$ signal must be active for a minimum of 3 clock cycles.

D. Output Delay vs. Loaded Capacitance

TA = 70°C Vcc = +5V ±5%

Add 10nsec delay for each 50pf increase in load up to a maximum of 200pf for the data bus & 100pf for address & control lines

E. Although static by design, testing guarantees $t_{w(\Phi H)}$ of 200 μsec maximum

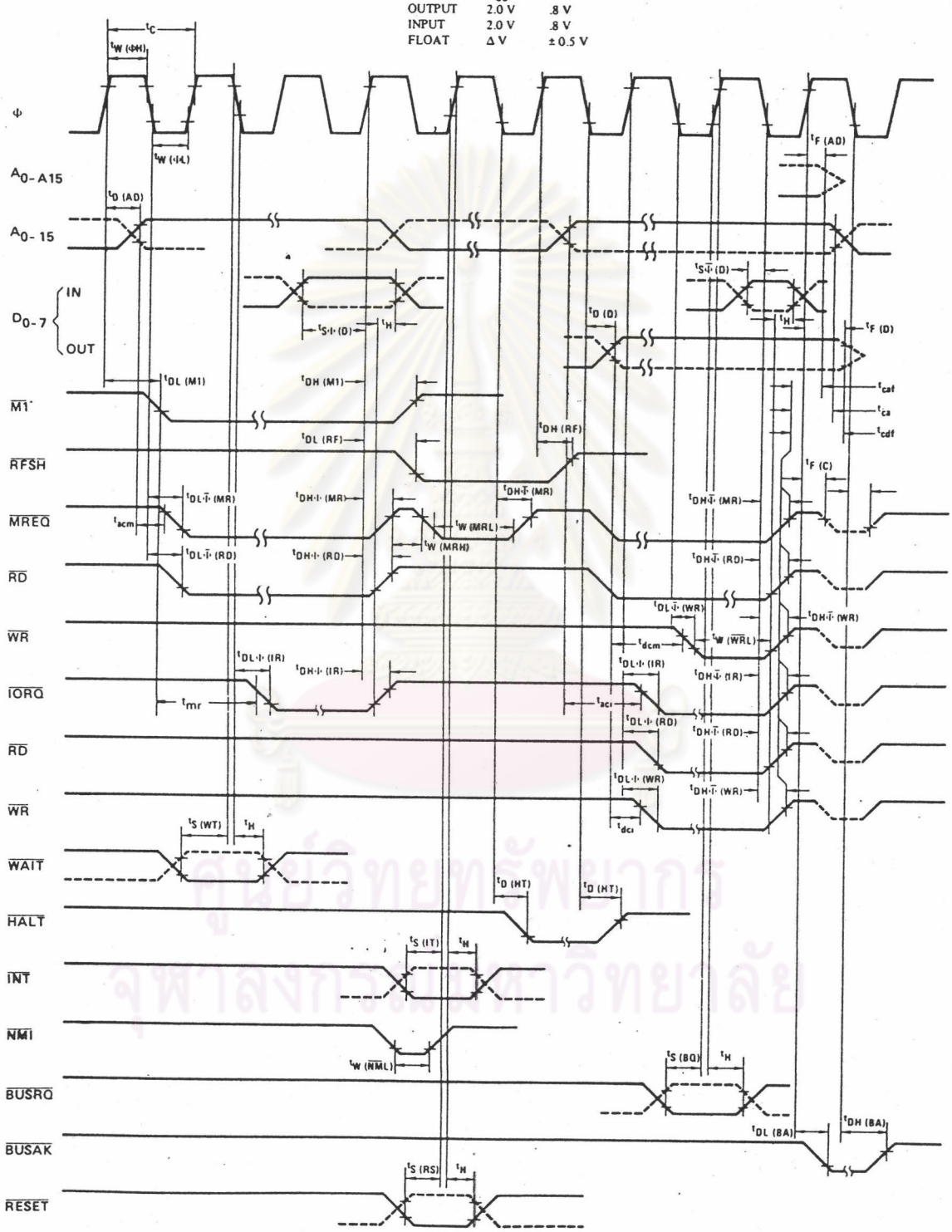


Load circuit for Output

A.C. Timing Diagram

Timing measurements are made at the following voltages, unless otherwise specified:

	"1"	"0"
CLOCK	V_{CC} -.6V	.45V
OUTPUT	2.0 V	.8 V
INPUT	2.0 V	.8 V
FLOAT	Δ V	± 0.5 V



Absolute Maximum Ratings

Temperature Under Bias	Specified operating range.
Storage Temperature	-65°C to +150°C
Voltage On Any Pin with Respect to Ground	-0.3V to +7V
Power Dissipation	1.5W

*Comment

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: For Z80-CPU all AC and DC characteristics remain the same for the military grade parts except I_{cc}.

I_{cc} = 200 mA

Z80-CPU D.C. Characteristics

T_A = 0°C to 70°C, V_{cc} = 5V ± 5% unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Condition
V_{ILC}	Clock Input Low Voltage	-0.3		0.45	V	
V_{IHC}	Clock Input High Voltage	V_{cc} -.6		V_{cc}+.3	V	
V_{IL}	Input Low Voltage	-0.3		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{cc}	V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL}=1.8mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -250μA
I_{CC}	Power Supply Current			150	mA	
I_{LI}	Input Leakage Current			10	μA	V_{IN}=0 to V_{cc}
I_{LOH}	Tri-State Output Leakage Current in Float			10	μA	V_{OUT}=2.4 to V_{cc}
I_{LOL}	Tri-State Output Leakage Current in Float			-10	μA	V_{OUT}=0.4V
I_{LD}	Data Bus Leakage Current in Input Mode			±10	μA	$0 \leq V_{IN} \leq V_{cc}$

Capacitance

T_A = 25°C, f = 1 MHz,
unmeasured pins returned to ground

Symbol	Parameter	Max.	Unit
C_Φ	Clock Capacitance	35	pF
C_{IN}	Input Capacitance	5	pF
C_{OUT}	Output Capacitance	10	pF

Z80-CPU Ordering Information

C – Ceramic
P – Plastic
S – Standard 5V ±5% 0° to 70°C
E – Extended 5V ±5% -40° to 85°C
M – Military 5V ±10% -55° to 125°C

Z80A-CPU D.C. Characteristics

T_A = 0°C to 70°C, V_{cc} = 5V ± 5% unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Condition
V_{ILC}	Clock Input Low Voltage	-0.3		0.45	V	
V_{IHC}	Clock Input High Voltage	V_{cc} -.6		V_{cc}+.3	V	
V_{IL}	Input Low Voltage	-0.3		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{cc}	V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL}=1.8mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -250μA
I_{CC}	Power Supply Current		90	200	mA	
I_{LI}	Input Leakage Current			10	μA	V_{IN}=0 to V_{cc}
I_{LOH}	Tri-State Output Leakage Current in Float			10	μA	V_{OUT}=2.4 to V_{cc}
I_{LOL}	Tri-State Output Leakage Current in Float			-10	μA	V_{OUT}=0.4V
I_{LD}	Data Bus Leakage Current in Input Mode			±10	μA	$0 \leq V_{IN} \leq V_{cc}$

Capacitance

T_A = 25°C, f = 1 MHz
unmeasured pins returned to ground

Symbol	Parameter	Max.	Unit
C_Φ	Clock Capacitance	35	pF
C_{IN}	Input Capacitance	5	pF
C_{OUT}	Output Capacitance	10	pF

Z80A-CPU Ordering Information

C – Ceramic
P – Plastic
S – Standard 5V ±5% 0° to 70°C

A.C. Characteristics Z80A-CPU

T_A = 0°C to 70°C, Vcc = +5V ± 5%, Unless Otherwise Noted.

Signal	Symbol	Parameter	Min	Max	Unit	Test Condition
Φ	t_c	Clock Period	.25	[12]	μsec	
	$t_{w(\Phi H)}$	Clock Pulse Width, Clock High	110	[E]	nsec	
	$t_{w(\Phi L)}$	Clock Pulse Width, Clock Low	110	2000	nsec	
	$t_{r,f}$	Clock Rise and Fall Time		30	nsec	
A_{0-15}	$t_{D(AD)}$	Address Output Delay		110	nsec	C_L = 50pF
	$t_{F(AD)}$	Delay to Float		90	nsec	
	t_{acm}	Address Stable Prior to $\overline{MREQ}$ (Memory Cycle)	[1]		nsec	
	t_{aci}	Address Stable Prior to $\overline{IORQ}$, $\overline{RD}$ or $\overline{WR}$ (I/O Cycle)	[2]		nsec	
	t_{ca}	Address Stable from $\overline{RD}$, $\overline{WR}$, $\overline{IORQ}$ or $\overline{MREQ}$	[3]		nsec	
	t_{caf}	Address Stable From $\overline{RD}$ or $\overline{WR}$ During Float	[4]		nsec	
D_{0-7}	$t_{D(D)}$	Data Output Delay		150	nsec	C_L = 50pF
	$t_{F(D)}$	Delay to Float During Write Cycle		90	nsec	
	$t_{S\Phi(D)}$	Data Setup Time to Rising Edge of Clock During M1 Cycle	35		nsec	
	$t_{S\overline{\Phi}(D)}$	Data Setup Time to Falling Edge of Clock During M2 to M5	50		nsec	
	t_{dcm}	Data Stable Prior to $\overline{WR}$ (Memory Cycle)	[5]		nsec	
	t_{dci}	Data Stable Prior to $\overline{WR}$ (I/O Cycle)	[6]		nsec	
	t_{cdf}	Data Stable From $\overline{WR}$	[7]			
	t_H	Any Hold Time for Setup Time		0	nsec	
$\overline{MREQ}$	$t_{DL\overline{\Phi}(MR)}$	$\overline{MREQ}$ Delay From Falling Edge of Clock, $\overline{MREQ}$ Low		85	nsec	C_L = 50pF
	$t_{DH\Phi(MR)}$	$\overline{MREQ}$ Delay From Rising Edge of Clock, $\overline{MREQ}$ High		85	nsec	
	$t_{DH\overline{\Phi}(MR)}$	$\overline{MREQ}$ Delay From Falling Edge of Clock, $\overline{MREQ}$ High		85	nsec	
	$t_{w(\overline{MRL})}$	Pulse Width, $\overline{MREQ}$ Low	[8]		nsec	
	$t_{w(\overline{MRH})}$	Pulse Width, $\overline{MREQ}$ High	[9]		nsec	
$\overline{IORQ}$	$t_{DL\Phi(IR)}$	$\overline{IORQ}$ Delay From Rising Edge of Clock, $\overline{IORQ}$ Low		75	nsec	C_L = 50pF
	$t_{DL\overline{\Phi}(IR)}$	$\overline{IORQ}$ Delay From Falling Edge of Clock, $\overline{IORQ}$ Low		85	nsec	
	$t_{DH\Phi(IR)}$	$\overline{IORQ}$ Delay From Rising Edge of Clock, $\overline{IORQ}$ High		85	nsec	
	$t_{DH\overline{\Phi}(IR)}$	$\overline{IORQ}$ Delay From Falling Edge of Clock, $\overline{IORQ}$ High		85	nsec	
$\overline{RD}$	$t_{DL\Phi(RD)}$	$\overline{RD}$ Delay From Rising Edge of Clock, $\overline{RD}$ Low		85	nsec	C_L = 50pF
	$t_{DL\overline{\Phi}(RD)}$	$\overline{RD}$ Delay From Falling Edge of Clock, $\overline{RD}$ Low		95	nsec	
	$t_{DH\Phi(RD)}$	$\overline{RD}$ Delay From Rising Edge of Clock, $\overline{RD}$ High		85	nsec	
	$t_{DH\overline{\Phi}(RD)}$	$\overline{RD}$ Delay From Falling Edge of Clock, $\overline{RD}$ High		85	nsec	
$\overline{WR}$	$t_{DL\Phi(WR)}$	$\overline{WR}$ Delay From Rising Edge of Clock, $\overline{WR}$ Low		65	nsec	C_L = 50pF
	$t_{DL\overline{\Phi}(WR)}$	$\overline{WR}$ Delay From Falling Edge of Clock, $\overline{WR}$ Low		80	nsec	
	$t_{DH\overline{\Phi}(WR)}$	$\overline{WR}$ Delay From Falling Edge of Clock, $\overline{WR}$ High		80	nsec	
	$t_{w(\overline{WRL})}$	Pulse Width, $\overline{WR}$ Low	[10]		nsec	
$\overline{M1}$	$t_{DL(M1)}$	$\overline{M1}$ Delay From Rising Edge of Clock, $\overline{M1}$ Low		100	nsec	C_L = 50pF
	$t_{DH(M1)}$	$\overline{M1}$ Delay From Rising Edge of Clock, $\overline{M1}$ High		100	nsec	
$\overline{RFSH}$	$t_{DL(RF)}$	$\overline{RFSH}$ Delay From Rising Edge of Clock, $\overline{RFSH}$ Low		130	nsec	C_L = 50pF
	$t_{DH(RF)}$	$\overline{RFSH}$ Delay From Rising Edge of Clock, $\overline{RFSH}$ High		120	nsec	
$\overline{WAIT}$	$t_{s(WT)}$	$\overline{WAIT}$ Setup Time to Falling Edge of Clock	70		nsec	
$\overline{HALT}$	$t_{D(HT)}$	$\overline{HALT}$ Delay Time From Falling Edge of Clock		300	nsec	C_L = 50pF
$\overline{INT}$	$t_{s(IT)}$	$\overline{INT}$ Setup Time to Rising Edge of Clock	80		nsec	
$\overline{NMI}$	$t_{w(\overline{NML})}$	Pulse Width, $\overline{NMI}$ Low	80		nsec	
$\overline{BUSRQ}$	$t_{s(BQ)}$	$\overline{BUSRQ}$ Setup Time to Rising Edge of Clock	50		nsec	
$\overline{BUSAK}$	$t_{DL(BA)}$	$\overline{BUSAK}$ Delay From Rising Edge of Clock, $\overline{BUSAK}$ Low		100	nsec	C_L = 50pF
	$t_{DH(BA)}$	$\overline{BUSAK}$ Delay From Falling Edge of Clock, $\overline{BUSAK}$ High		100	nsec	
$\overline{RESET}$	$t_{s(RS)}$	$\overline{RESET}$ Setup Time to Rising Edge of Clock	60		nsec	
	$t_{F(C)}$	Delay to Float ($\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$ and $\overline{WR}$)		80	nsec	
	t_{mr}	M1 Stable Prior to IORQ (Interrupt Ack.)	[11]		nsec	

[1] $t_{acm} = t_{w(\Phi H)} + t_f - 65$

[2] $t_{aci} = t_c - 70$

[3] $t_{ca} = t_{w(\Phi L)} + t_r - 50$

[4] $t_{caf} = t_{w(\Phi L)} + t_r - 45$

[5] $t_{dcm} = t_c - 170$

[6] $t_{dci} = t_{w(\Phi L)} + t_r - 170$

[7] $t_{cdf} = t_{w(\Phi L)} + t_r - 70$

[8] $t_{w(\overline{MRL})} = t_c - 30$

[9] $t_{w(\overline{MRH})} = t_{w(\Phi H)} + t_f - 20$

[10] $t_{w(\overline{WRL})} = t_c - 30$

[11] $t_{mr} = 2t_c + t_{w(\Phi H)} + t_f - 65$

[12] $t_c = t_{w(\Phi H)} + t_{w(\Phi L)} + t_r + t_f$

NOTES:

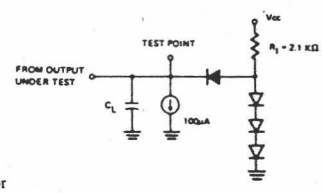
A. Data should be enabled onto the CPU data bus when $\overline{RD}$ is active. During interrupt acknowledge data should be enabled when $\overline{M1}$ and $\overline{IORQ}$ are both active.

B. All control signals are internally synchronized, so they may be totally asynchronous with respect to the clock.

C. The $\overline{RESET}$ signal must be active for a minimum of 3 clock cycles.

D. Output Delay vs. Loaded Capacitance
TA = 70°C Vcc = +5V ±5%
Add 10nsec delay for each 50pf increase in load up to maximum of 200pf for data bus and 100pf for address & control lines.

E. Although static by design, testing guarantees $t_{w(\Phi H)}$ of 200 μsec maximum



Load circuit for Output

ภาคผนวก ข

ข้อมูลของไอซีหมายเลข 2732

intel®

2732
32K (4K x 8) UV ERASABLE PROM

- **Fast Access Time:**
  - **— 450 ns Max. 2732**
  - **— 550 ns Max. 2732-6**
- **Single +5V ± 5% Power Supply**
- **Output Enable for MCS-85™ and MCS-86™ Compatibility**
- **Low Power Dissipation:**
  150mA Max. Active Current
  30mA Max. Standby Current
- **Pin Compatible to Intel® 2716 EPROM**
- **Completely Static**
- **Simple Programming Requirements**
  - **— Single Location Programming**
  - **— Programs with One 50ms Pulse**
- **Three-State Output for Direct Bus Interface**

The Intel® 2732 is a 32,768-bit ultraviolet erasable and electrically programmable read-only memory (EPROM). The 2732 operates from a single 5-volt power supply, has a standby mode, and features an output enable control. The total programming time for all bits is three and a half minutes. All these features make designing with the 2732 in microcomputer systems faster, easier, and more economical.

An important 2732 feature is the separate output control, Output Enable ($\overline{OE}$) from the Chip Enable control ($\overline{CE}$). The OE control eliminates bus contention in multiple bus microprocessor systems. Intel's Application Note AP-72 describes the microprocessor system implementation of the $\overline{OE}$ and $\overline{CE}$ controls on Intel's 2716 and 2732 EPROMs. AP-72 is available from Intel's Literature Department.

The 2732 has a standby mode which reduces the power dissipation without increasing access time. The maximum active current is 150mA, while the maximum standby current is only 30mA, an 80% savings. The standby mode is achieved by applying a TTL-high signal to the $\overline{CE}$ input.

PIN CONFIGURATION

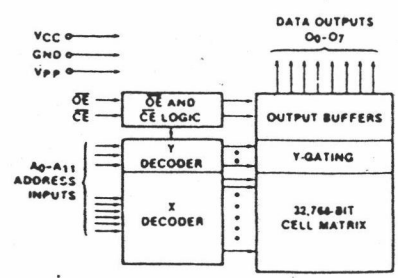
PIN NAMES

A_0-A_{11}	ADDRESSES
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
O_0-O_7	OUTPUTS

MODE SELECTION

MODE \ PINS	$\overline{CE}$ (18)	$\overline{OE}/V_{PP}$ (20)	V_{CC} (24)	OUTPUTS (9-11,13-17)
Read	V_{IL}	V_{IL}	+5	D_{OUT}
Standby	V_{IH}	Don't Care	+5	High Z
Program	V_{IL}	Vpp	+5	D_{IN}
Program Verify	V_{IL}	V_{IL}	+5	D_{OUT}
Program Inhibit	V_{IH}	Vpp	+5	High Z

BLOCK DIAGRAM



ภาคผนวก ค

ข้อมูลของไอซีหมายเลข 6116

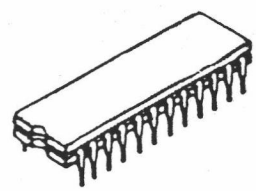
HM6116-2,HM6116-3,HM6116-4,HM6116P-2,HM6116P-3,HM6116P-4

2048-word × 8-bit High Speed Static CMOS RAM

■FEATURES

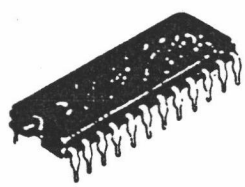
- Single 5V Supply and High Density 24 Pin Package
- High speed: Fast Access Time 120ns/150ns/200ns (max.)
- Low Power Standby and Low Power Operation — Standby: 100μW (typ.), Operation: 180mW (typ.)
- Completely Static RAM: No clock or Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Pin Out Compatible with Standard 16K EPROM/MASK ROM
- Equal Access and Cycle Time

HM6116-2, HM6116-3, HM6116-4



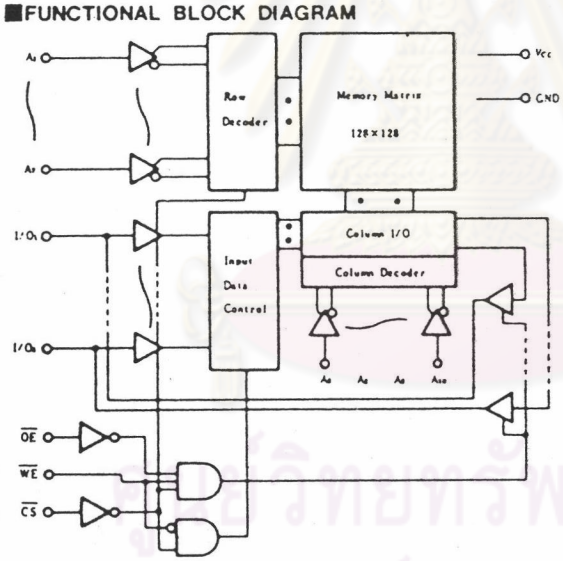
(DG-24)

HM6116P-2, HM6116P-3, HM6116P-4



(DP-24)

■FUNCTIONAL BLOCK DIAGRAM



■PIN ARRANGEMENT

■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to GND	V_T	−0.5* to +7.0	V
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature (Plastic)	T_{stg}	−55 to +125	°C
Storage Temperature (Ceramic)	T_{stg}	−65 to +150	°C
Temperature Under Bias	T_{bias}	−10 to +85	°C
Power Dissipation	P_T	1.0	W

* Pulse Width 50ns : −1.5 V

■TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	×	×	Not Selected	I_{SB}, I_{SB1}	High Z	
L	L	H	Read	I_{CC}	Dout	Read Cycle (1)~(3)
L	H	L	Write	I_{CC}	Din	Write Cycle (1)
L	L	L	Write	I_{CC}	Din	Write Cycle (2)

ภาคผนวก ง

ข้อมูลของไอซีหมายเลข 8255

intel®

8255A/8255A-5
PROGRAMMABLE PERIPHERAL INTERFACE

- MCS-85™ Compatible 8255A-5
- 24 Programmable I/O Pins
- Completely TTL Compatible
- Fully Compatible with Intel Microprocessor Families
- Improved Timing Characteristics
- Direct Bit Set/Reset Capability Easing Control Application Interface
- Reduces System Package Count
- Improved DC Driving Capability
- Available in EXPRESS
  - Standard Temperature Range
  - Extended Temperature Range
- 40 Pin DIP Package or 44 Lead PLCC
  (See Intel Packaging: Order Number: 231369)

The Intel 8255A is a general purpose programmable I/O device designed for use with Intel microprocessors. It has 24 I/O pins which may be individually programmed in 2 groups of 12 and used in 3 major modes of operation. In the first mode (MODE 0), each group of 12 I/O pins may be programmed in sets of 4 to be input or output. In MODE 1, the second mode, each group may be programmed to have 8 lines of input or output. Of the remaining 4 pins, 3 are used for handshaking and interrupt control signals. The third mode of operation (MODE 2) is a bidirectional bus mode which uses 8 lines for a bidirectional bus, and 5 lines, borrowing one from the other group, for handshaking.

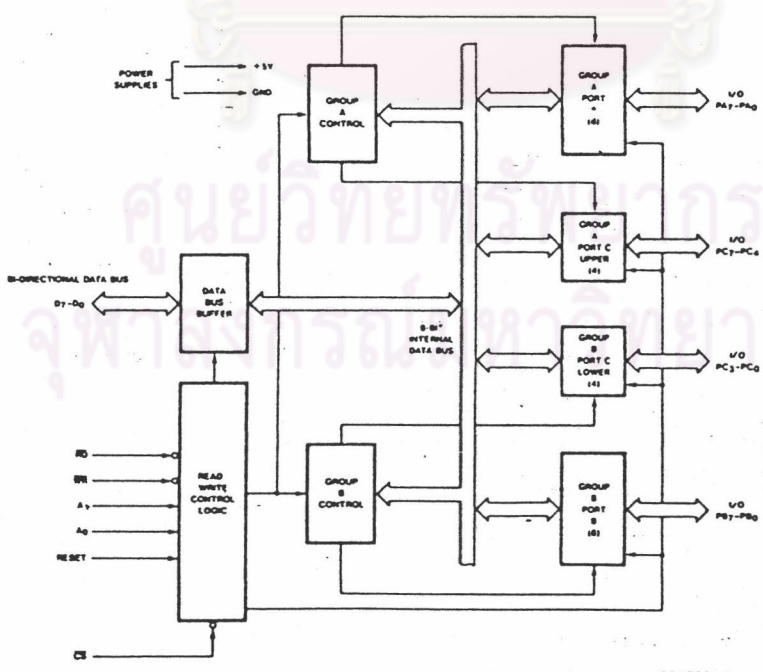


Figure 1. 8255A Block Diagram

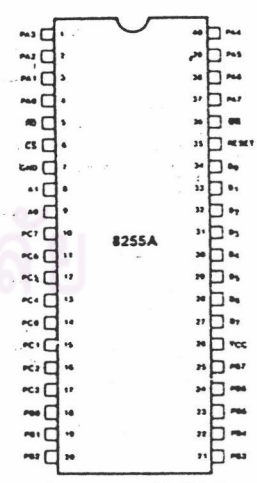


Figure 2. Pin Configuration

September 1987
Order Number: 231308-002

8255A FUNCTIONAL DESCRIPTION

General

The 8255A is a programmable peripheral interface (PPI) device designed for use in Intel microcomputer systems. Its function is that of a general purpose I/O component to interface peripheral equipment to the microcomputer system bus. The functional configuration of the 8255A is programmed by the system software so that normally no external logic is necessary to interface peripheral devices or structures.

Data Bus Buffer

This 3-state bidirectional 8-bit buffer is used to interface the 8255A to the system data bus. Data is transmitted or received by the buffer upon execution of input or output instructions by the CPU. Control words and status information are also transferred through the data bus buffer.

Read/Write and Control Logic

The function of this block is to manage all of the internal and external transfers of both Data and Control or Status words. It accepts inputs from the CPU Address and Control busses and in turn, issues commands to both of the Control Groups.

($\overline{CS}$)

Chip Select. A "low" on this input pin enables the communication between the 8255A and the CPU.

($\overline{RD}$)

Read. A "low" on this input pin enables the 8255A to send the data or status information to the CPU on the data bus. In essence, it allows the CPU to "read from" the 8255A.

($\overline{WR}$)

Write. A "low" on this input pin enables the CPU to write data or control words into the 8255A.

(A_0 and A_1)

Port Select 0 and Port Select 1. These input signals, in conjunction with the RD and WR inputs, control the selection of one of the three ports or the control word registers. They are normally connected to the least significant bits of the address bus (A_0 and A_1).

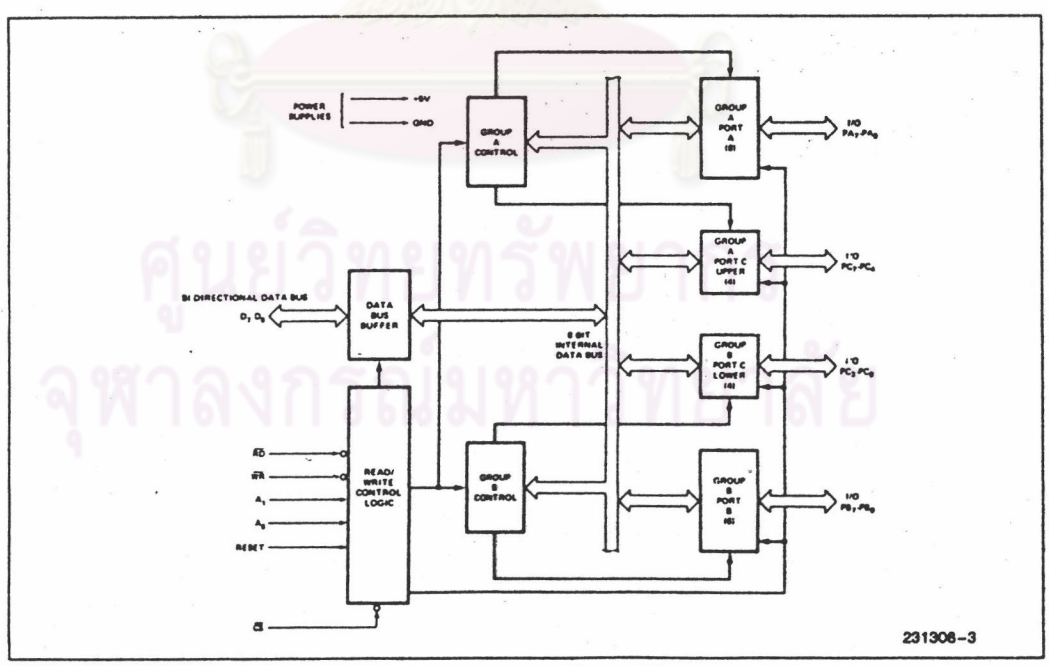


Figure 3. 8255A Block Diagram Showing Data Bus Buffer and Read/Write Control Logic Functions

8255A BASIC OPERATION

A_1	A_0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	Input Operation (READ)
0	0	0	1	0	Port A → Data Bus
0	1	0	1	0	Port B → Data Bus
1	0	0	1	0	Port C → Data Bus
					Output Operation (WRITE)
0	0	1	0	0	Data Bus → Port A
0	1	1	0	0	Data Bus → Port B
1	0	1	0	0	Data Bus → Port C
1	1	1	0	0	Data Bus → Control
					Disable Function
X	X	X	X	1	Data Bus → 3-State
1	1	0	1	0	Illegal Condition
X	X	1	1	0	Data Bus → 3-State

(RESET)

Reset. A "high" on this input clears the control register and all ports (A, B, C) are set to the input mode.

Group A and Group B Controls

The functional configuration of each port is programmed by the systems software. In essence, the CPU "outputs" a control word to the 8255A. The control word contains information such as "mode", "bit set", "bit reset", etc., that initializes the functional configuration of the 8255A.

Each of the Control blocks (Group A and Group B) accepts "commands" from the Read/Write Control Logic, receives "control words" from the internal data bus and issues the proper commands to its associated ports.

Control Group A—Port A and Port C upper (C7–C4)

Control Group B—Port B and Port C lower (C3–C0)

The Control Word Register can **Only** be written into. No Read operation of the Control Word Register is allowed.

Ports A, B, and C

The 8255A contains three 8-bit ports (A, B, and C). All can be configured in a wide variety of functional characteristics by the system software but each has its own special features or "personality" to further enhance the power and flexibility of the 8255A.

Port A. One 8-bit data output latch/buffer and one 8-bit data input latch.

Port B. One 8-bit data input/output latch/buffer and one 8-bit data input buffer.

Port C. One 8-bit data output latch/buffer and one 8-bit data input buffer (no latch for input). This port can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and it can be used for the control signal outputs and status signal inputs in conjunction with ports A and B.

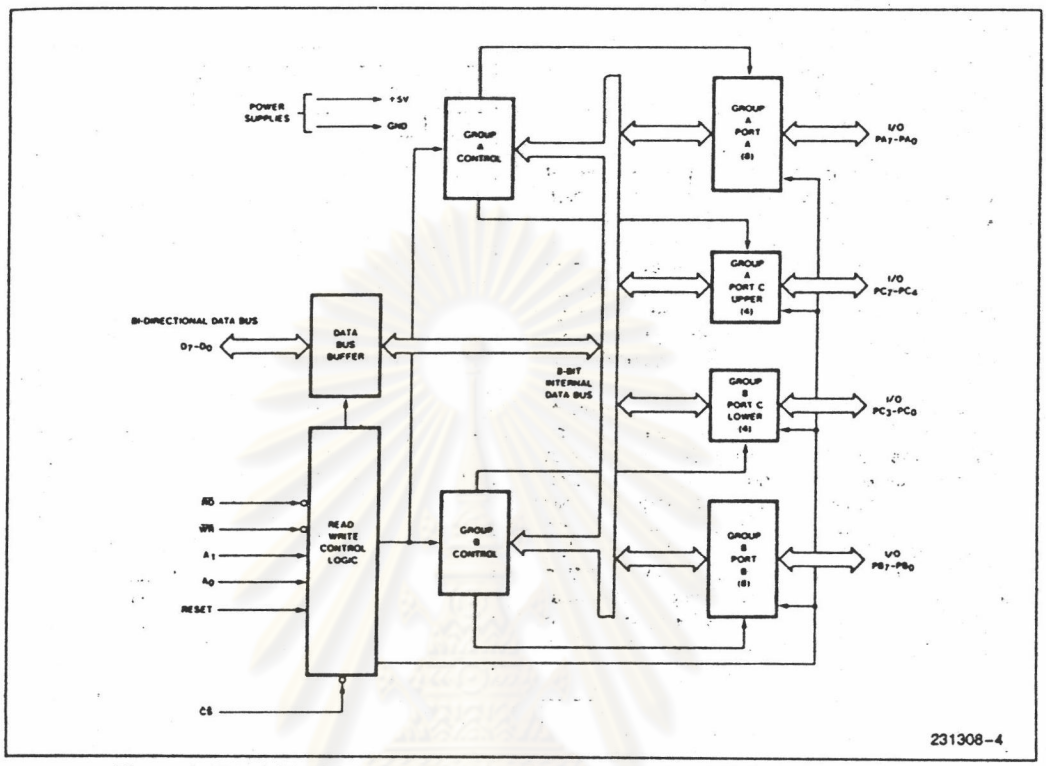
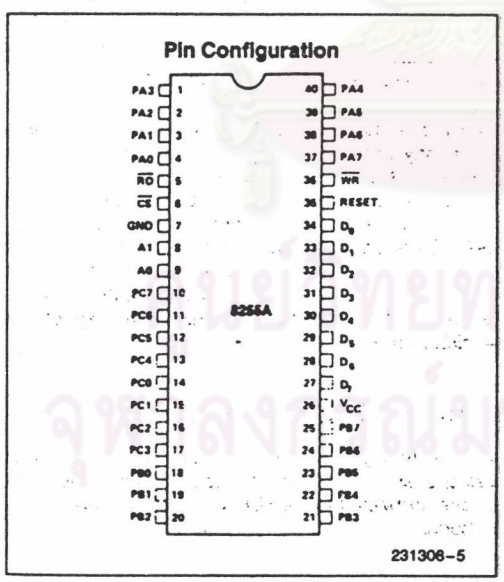


Figure 4. 8225A Block Diagram Showing Group A and Group B Control Functions



Pin Names

D_7–D_0	Data Bus (Bi-Directional)
RESET	Reset Input
$\overline{CS}$	Chip Select
$\overline{RD}$	Read Input
$\overline{WR}$	Write Input
A0, A1	Port Address
PA7–PA0	Port A (BIT)
PB7–PB0	Port B (BIT)
PC7–PC0	Port C (BIT)
V_{CC}	+5 Volts
GND	0 Volts

8255A OPERATIONAL DESCRIPTION

Mode Selection

There are three basic modes of operation that can be selected by the system software:

Mode 0—Basic Input/Output

Mode 1—Strobed Input/Output

Mode 2—Bi-Directional Bus

When the reset input goes "high" all ports will be set to the input mode (i.e., all 24 lines will be in the high impedance state). After the reset is removed the 8255A can remain in the input mode with no additional initialization required. During the execution of the system program any of the other modes may be selected using a single output instruction. This allows a single 8255A to service a variety of peripheral devices with a simple software maintenance routine.

The modes for Port A and Port B can be separately defined, while Port C is divided into two portions as required by the Port A and Port B definitions. All of the output registers, including the status flip-flops, will be reset whenever the mode is changed. Modes may be combined so that their functional definition can be "tailored" to almost any I/O structure. For instance; Group B can be programmed in Mode 0 to monitor simple switch closings or display computational results, Group A could be programmed in Mode 1 to monitor a keyboard or tape reader on an interrupt-driven basis.

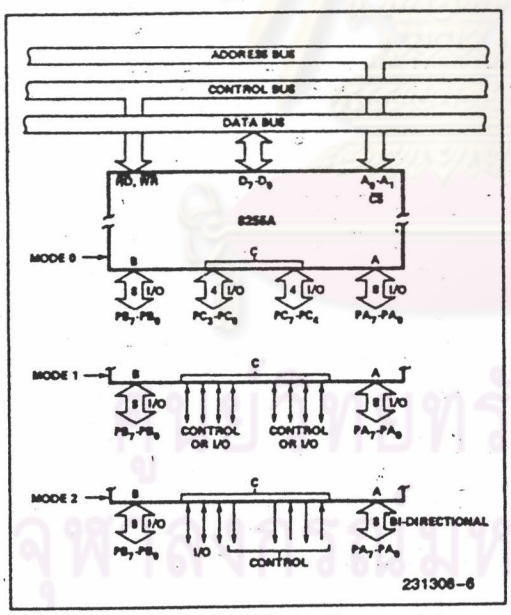


Figure 5. Basic Mode Definitions and Bus Interface

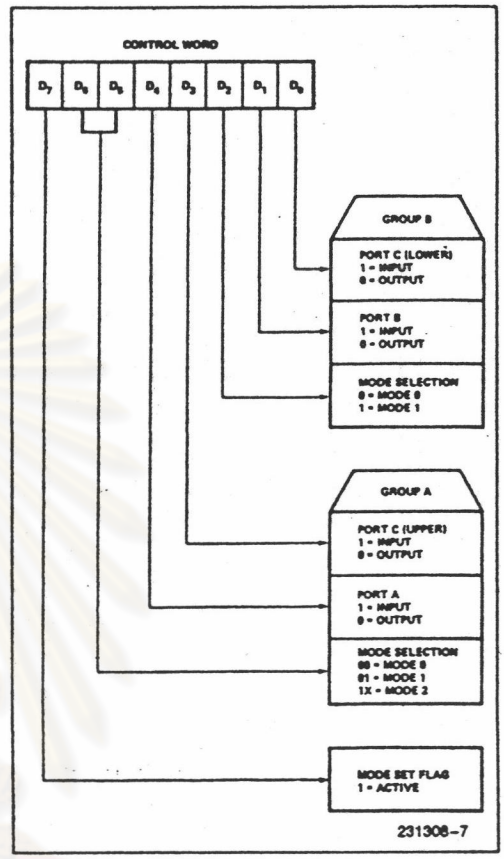


Figure 6. Mode Definition Format

The mode definitions and possible mode combinations may seem confusing at first but after a cursory review of the complete device operation a simple, logical I/O approach will surface. The design of the 8255A has taken into account things such as efficient PC board layout, control signal definition vs PC layout and complete functional flexibility to support almost any peripheral device with no external logic. Such design represents the maximum use of the available pins.

Single Bit Set/Reset Feature

Any of the eight bits of Port C can be Set or Reset using a single OUTput instruction. This feature reduces software requirements in Control-based applications.

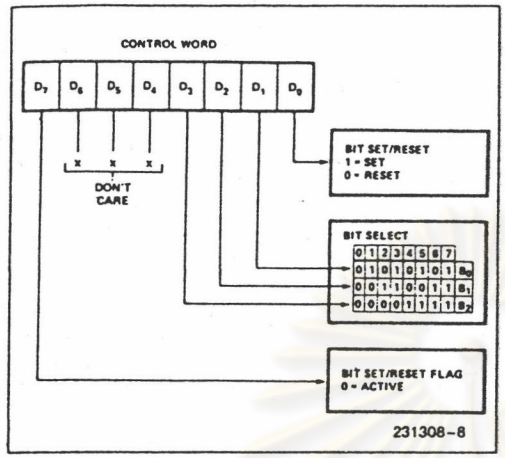


Figure 7. Bit Set/Reset Format

When Port C is being used as status/control for Port A or B, these bits can be set or reset by using the Bit Set/Reset operation just as if they were data output ports.

Interrupt Control Functions

When the 8255A is programmed to operate in mode 1 or mode 2, control signals are provided that can be used as interrupt request inputs to the CPU. The interrupt request signals, generated from port C, can be inhibited or enabled by setting or resetting the associated INTE flip-flop, using the bit set/reset function of port C.

This function allows the Programmer to disallow or allow a specific I/O device to interrupt the CPU without affecting any other device in the interrupt structure.

INTE flip-flop definition:

(BIT-SET)—INTE is set—Interrupt enable

(BIT-RESET)—INTE is RESET—Interrupt disable

NOTE:
All Mask flip-flops are automatically reset during mode selection and device Reset.

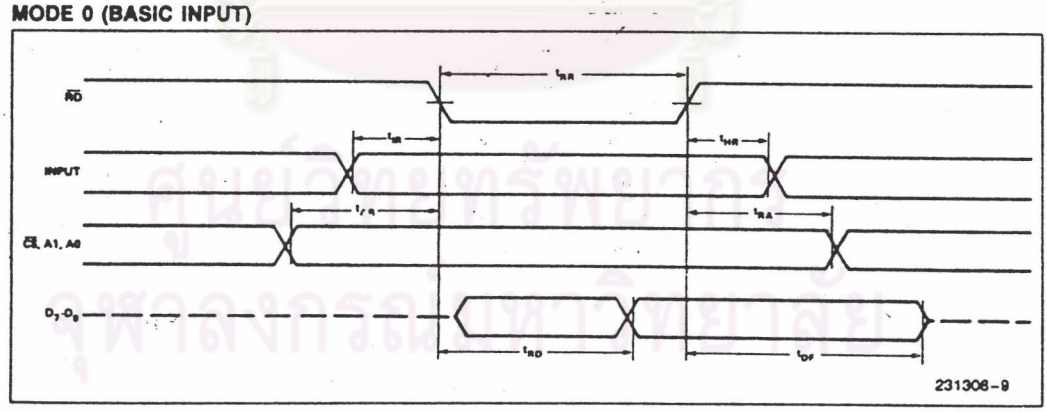
Operating Modes

MODE 0 (Basic Input/Output). This functional configuration provides simple input and output operations for each of the three ports. No "handshaking" is required, data is simply written to or read from a specified port.

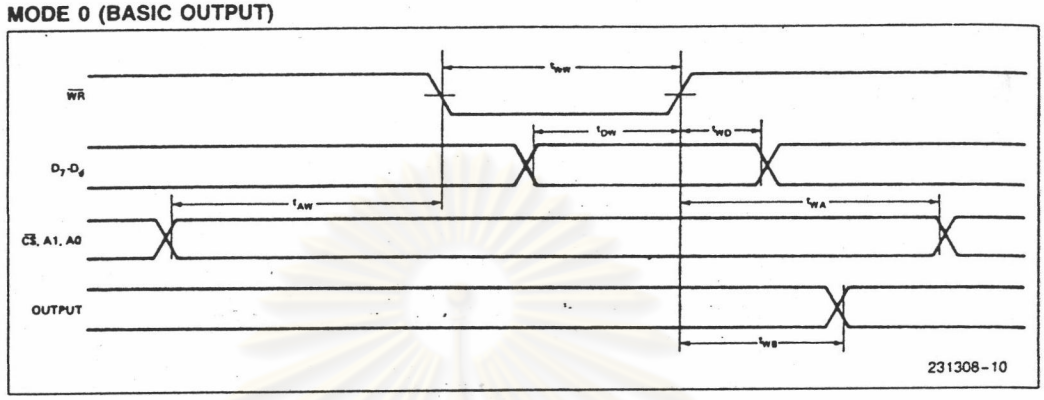
Mode 0 Basic Functional Definitions:

- Two 8-bit ports and two 4-bit ports.
- Any port can be input or output.
- Outputs are latched.
- Inputs are not latched.
- 16 different Input/Output configurations are possible in this Mode.

MODE 0 (BASIC INPUT)



MODE 0 (BASIC OUTPUT)



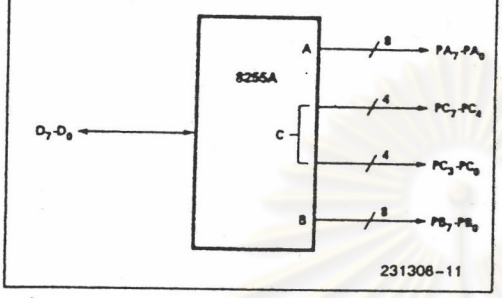
MODE 0 PORT DEFINITION

A		B		Group A			Group B	
D_4	D_3	D_1	D_0	Port A	Port C (Upper)	#	Port B	Port C (Lower)
0	0	0	0	OUTPUT	OUTPUT	0	OUTPUT	OUTPUT
0	0	0	1	OUTPUT	OUTPUT	1	OUTPUT	INPUT
0	0	1	0	OUTPUT	OUTPUT	2	INPUT	OUTPUT
0	0	1	1	OUTPUT	OUTPUT	3	INPUT	INPUT
0	1	0	0	OUTPUT	INPUT	4	OUTPUT	OUTPUT
0	1	0	1	OUTPUT	INPUT	5	OUTPUT	INPUT
0	1	1	0	OUTPUT	INPUT	6	INPUT	OUTPUT
0	1	1	1	OUTPUT	INPUT	7	INPUT	INPUT
1	0	0	0	INPUT	OUTPUT	8	OUTPUT	OUTPUT
1	0	0	1	INPUT	OUTPUT	9	OUTPUT	INPUT
1	0	1	0	INPUT	OUTPUT	10	INPUT	OUTPUT
1	0	1	1	INPUT	OUTPUT	11	INPUT	INPUT
1	1	0	0	INPUT	INPUT	12	OUTPUT	OUTPUT
1	1	0	1	INPUT	INPUT	13	OUTPUT	INPUT
1	1	1	0	INPUT	INPUT	14	INPUT	OUTPUT
1	1	1	1	INPUT	INPUT	15	INPUT	INPUT

MODE CONFIGURATIONS

CONTROL WORD #0

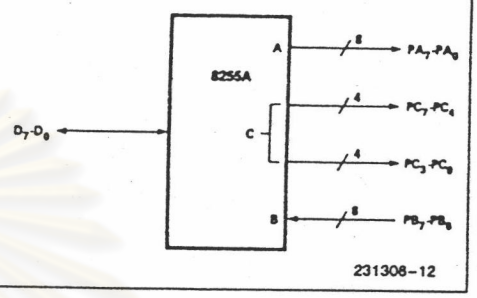
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	0	0	0	0



231308-11

CONTROL WORD #2

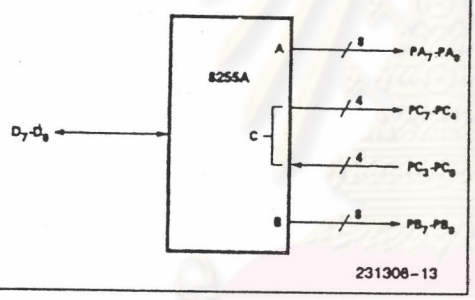
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	0	0	1	0



231308-12

CONTROL WORD #1

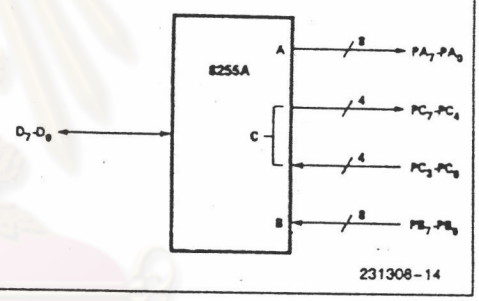
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	0	0	0	1



231308-13

CONTROL WORD #3

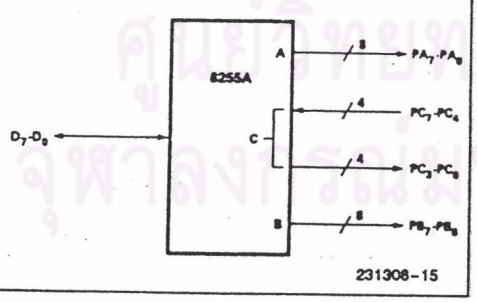
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	0	0	1	1



231308-14

CONTROL WORD #4

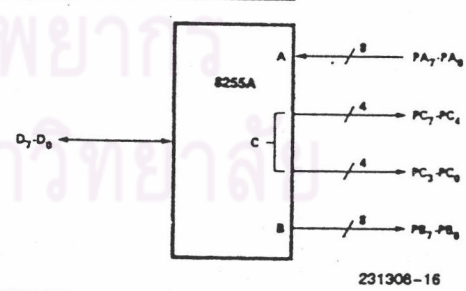
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	1	0	0	0



231308-15

CONTROL WORD #8

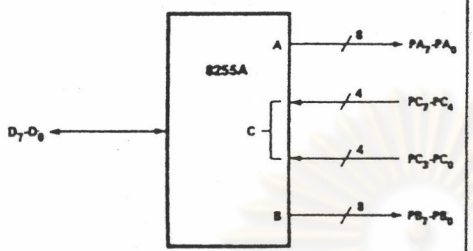
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	0	0	0	0



231308-16

CONTROL WORD #5

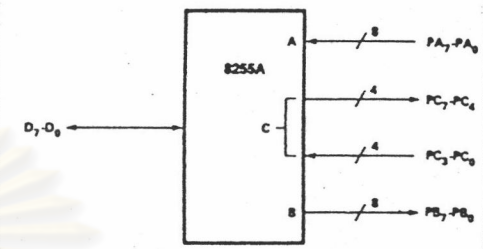
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	1	0	0	1



231308-17

CONTROL WORD #9

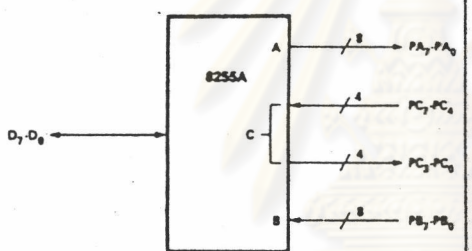
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	0	0	0	1



231308-18

CONTROL WORD #6

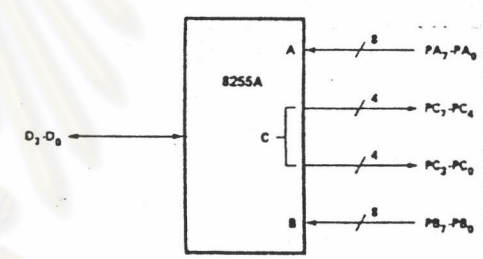
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	1	0	1	0



231308-19

CONTROL WORD #10

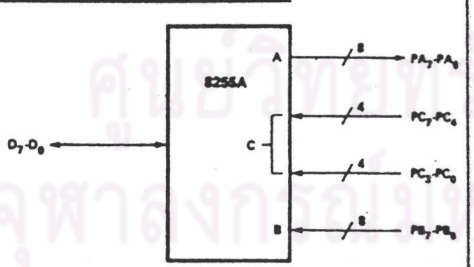
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	0	0	1	0



231308-20

CONTROL WORD #7

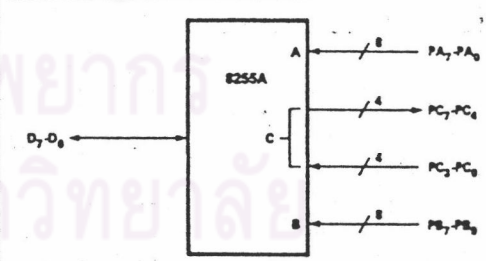
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	1	0	1	1



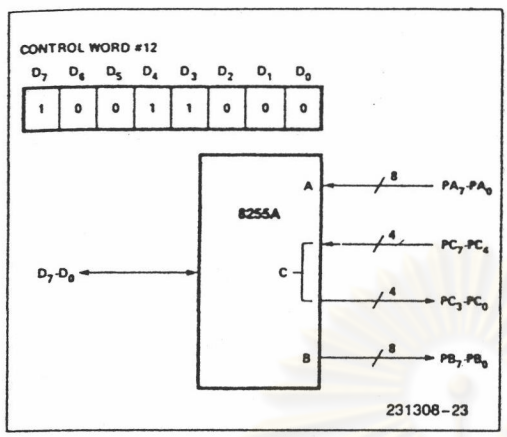
231308-21

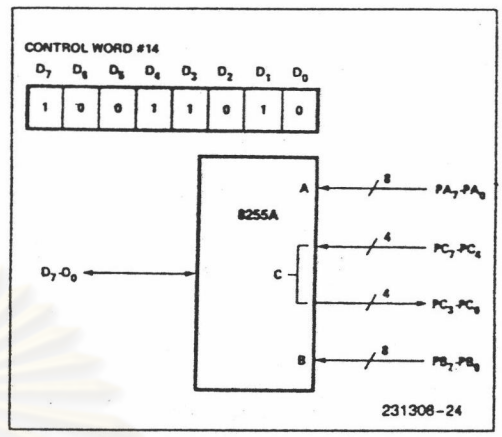
CONTROL WORD #11

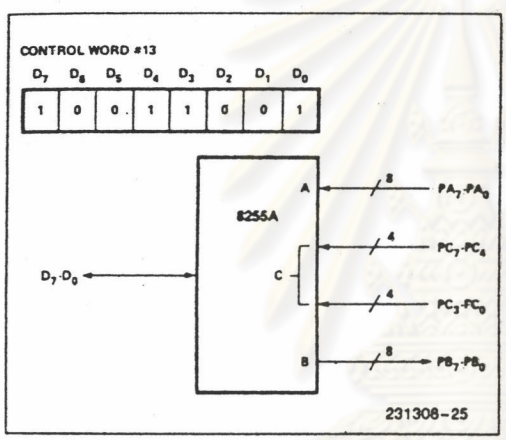
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	0	0	1	1

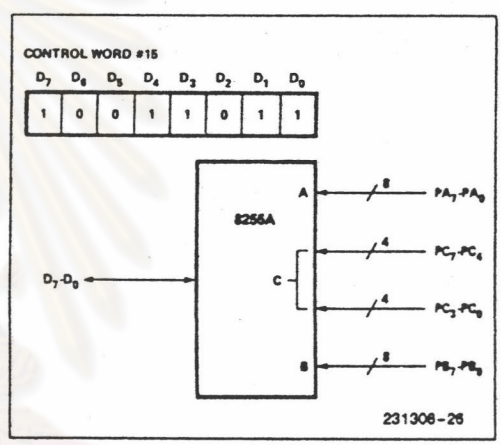


231308-22









Operating Modes

MODE 1 (Strobed Input/Output). This functional configuration provides a means for transferring I/O data to or from a specified port in conjunction with strobes or "handshaking" signals. In mode 1, port A and port B use the lines on port C to generate or accept these "handshaking" signals.

Mode 1 Basic Functional Definitions:

- Two Groups (Group A and Group B)
- Each group contains one 8-bit data port and one 4-bit control/data port.
- The 8-bit data port can be either input or output. Both inputs and outputs are latched.
- The 4-bit port is used for control and status of the 8-bit data port.

Input Control Signal Definition

$\overline{\text{STB}}$ (Strobe Input). A "low" on this input loads data into the input latch.

IBF (Input Buffer Full F/F)

A "high" on this output indicates that the data has been loaded into the input latch; in-essence, an acknowledgement. IBF is set by STB input being low and is reset by the rising edge of the RD input.

INTR (Interrupt Request)

A "high" on this output can be used to interrupt the CPU when an input device is requesting service. INTR is set by the $\overline{\text{STB}}$ is a "one", IBF is a "one" and INTE is a "one". It is reset by the falling edge of $\overline{\text{RD}}$. This procedure allows an input device to request service from the CPU by simply strobing its data into the port.

INTE A

Controlled by bit set/reset of PC_4.

INTE B

Controlled by bit set/reset of PC_2.

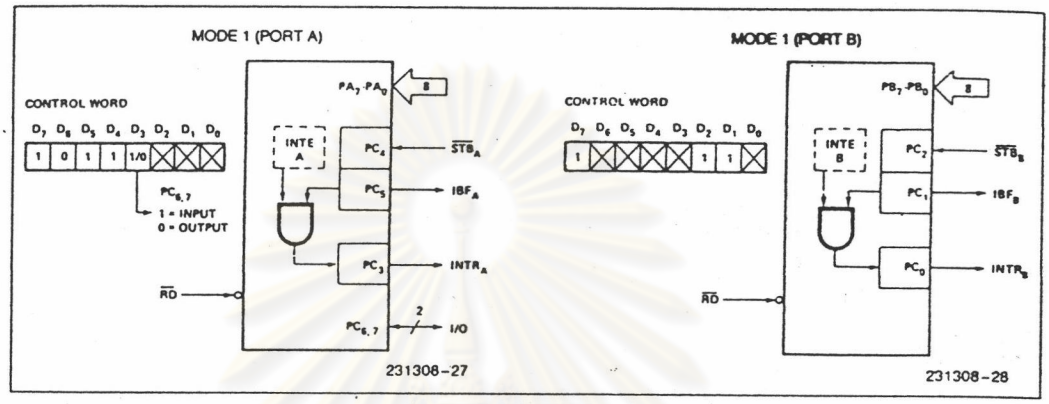


Figure 8. MODE 1 Input

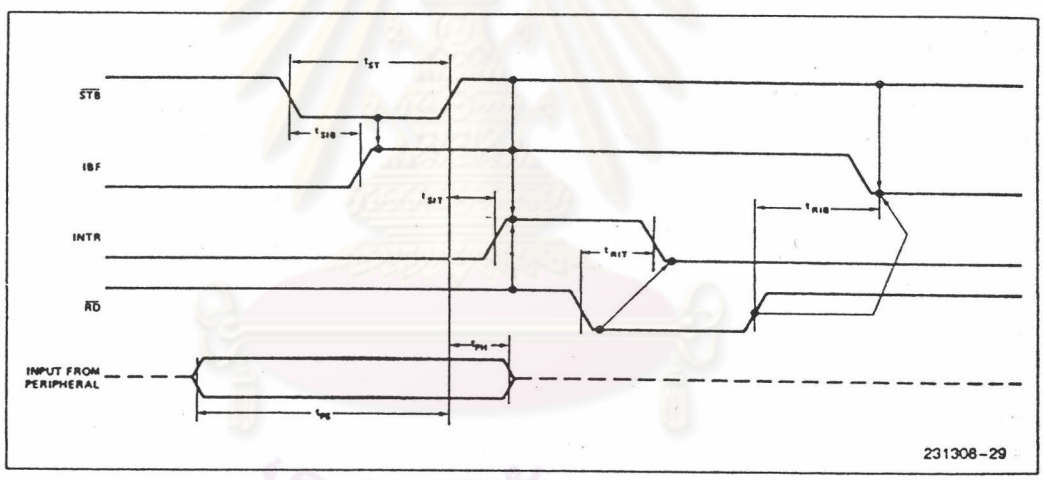


Figure 9. MODE 1 (Strobed Input)

Output Control Signal Definition

$\overline{OBF}$ (Output Buffer Full F/F). The $\overline{OBF}$ output will go "low" to indicate that the CPU has written data out to the specified port. The $\overline{OBF}$ F/F will be set by the rising edge of the $\overline{WR}$ input and reset by $\overline{ACK}$ input being low.

$\overline{ACK}$ (Acknowledge Input). A "low" on this input informs the 8255A that the data from port A or port B has been accepted. In essence, a response from the peripheral device indicating that it has received the data output by the CPU.

INTR (Interrupt Request). A "high" on this output can be used to interrupt the CPU when an output device has accepted data transmitted by the CPU. INTR is set when $\overline{ACK}$ is a "one", $\overline{OBF}$ is a "one", and INTE is a "one". It is reset by the falling edge of $\overline{WR}$.

INTE A

Controlled by bit set/reset of PC_6.

INTE B

Controlled by bit set/reset of PC_2.

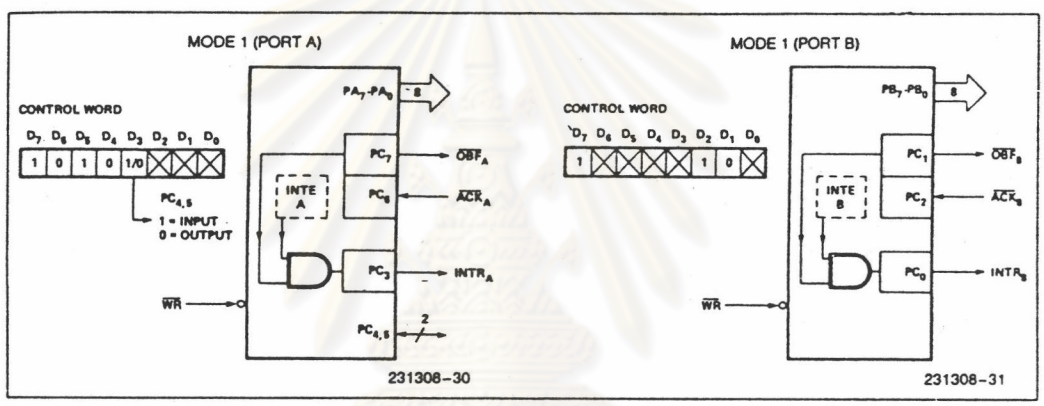


Figure 10. MODE 1 Output

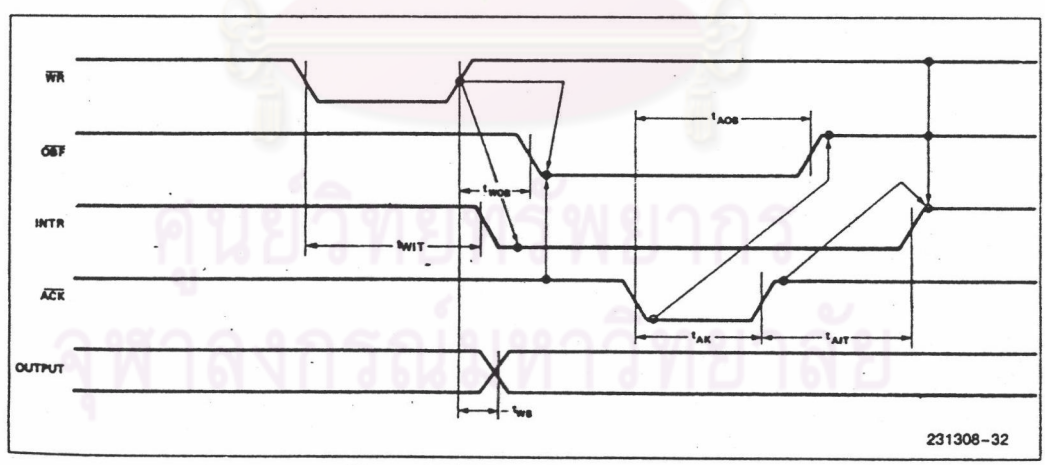


Figure 11. MODE 1 (Strobed Output)

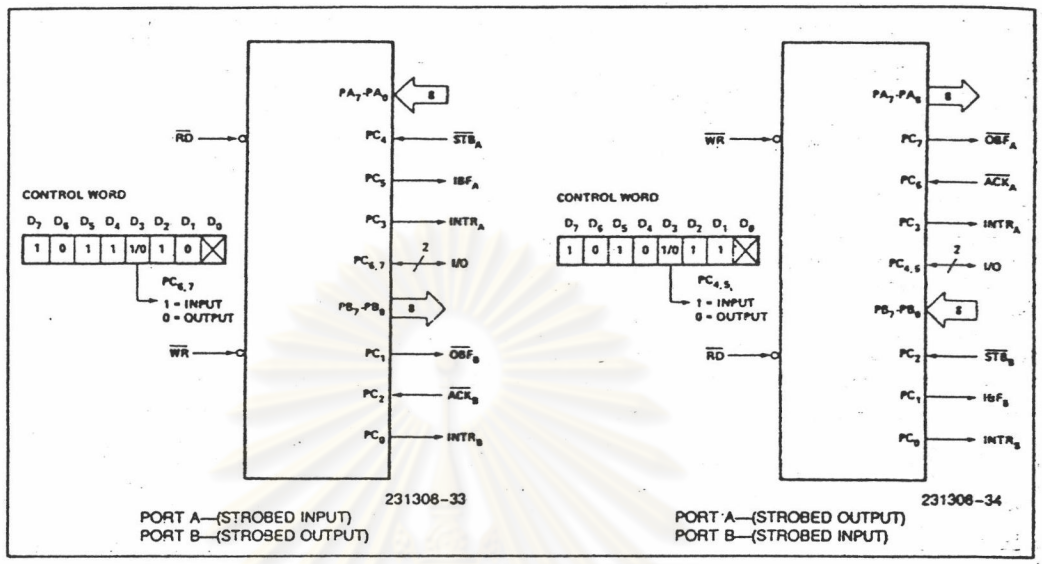


Figure 12. Combinations of MODE 1

Combinations of MODE 1

Port A and Port B can be individually defined as input or output in MODE 1 to support a wide variety of strobed I/O applications.

Operating Modes

MODE 2 (Strobed Bidirectional Bus I/O). This functional configuration provides a means for communicating with a peripheral device or structure on a single 8-bit bus for both transmitting and receiving data (bidirectional bus I/O). "Handshaking" signals are provided to maintain proper bus flow discipline in a similar manner to MODE 1. Interrupt generation and enable/disable functions are also available.

MODE 2 Basic Functional Definitions:

- Used in Group A only.
- One 8-bit, bi-directional bus Port (Port A) and a 5-bit control Port (Port C).
- Both inputs and outputs are latched.
- The 5-bit control port (Port C) is used for control and status for the 8-bit, bi-directional bus port (Port A).

Bidirectional Bus I/O Control Signal Definition

INTR (Interrupt Request). A high on this output can be used to interrupt the CPU for both input or output operations.

Output Operations

$\overline{OBF}$ (Output Buffer Full). The $\overline{OBF}$ output will go "low" to indicate that the CPU has written data out to port A.

$\overline{ACK}$ (Acknowledge). A "low" on this input enables the tri-state output buffer of port A to send out the data. Otherwise, the output buffer will be in the high impedance state.

INTE 1 (The INTE Flip-Flop Associated with OBF). Controlled by bit set/reset of PC_6.

Input Operations

$\overline{STB}$ (Strobe Input). A "low" on this input loads data into the input latch.

IBF (Input Buffer Full F/F). A "high" on this output indicates that data has been loaded into the input latch.

INTE 2 (The INTE Flip-Flop Associated with IBF). Controlled by bit set/reset of PC_4.

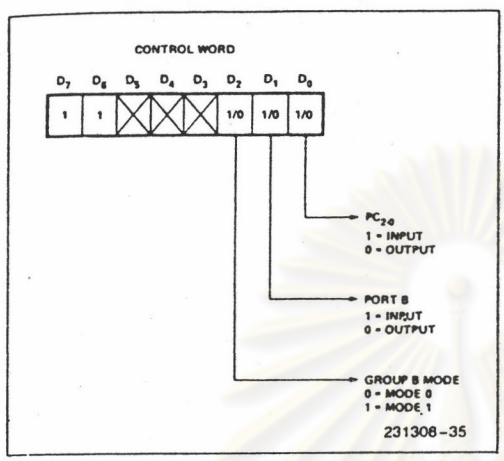


Figure 13. MODE Control Word

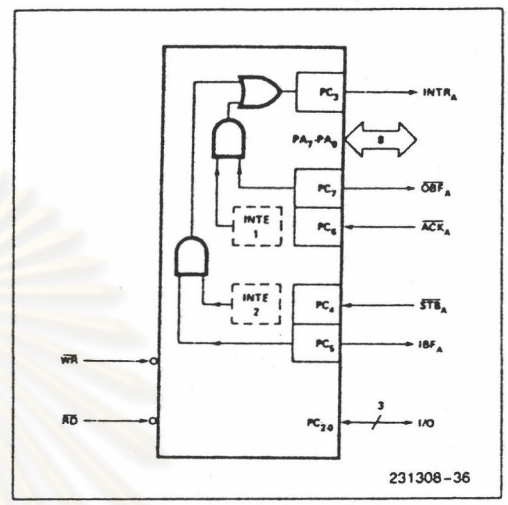
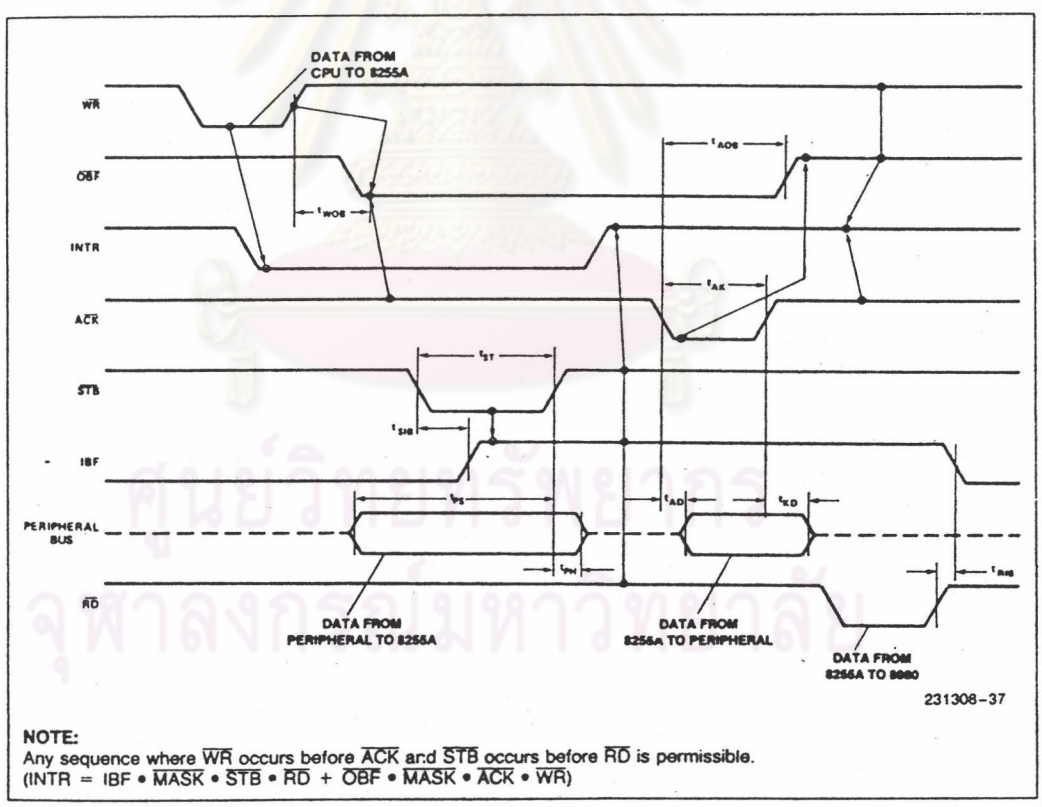


Figure 14. MODE 2



NOTE:
Any sequence where $\overline{WR}$ occurs before $\overline{ACK}$ and $\overline{STB}$ occurs before $\overline{RD}$ is permissible.
($INTR = IBF \bullet \overline{MASK} \bullet \overline{STB} \bullet \overline{RD} + \overline{OBF} \bullet \overline{MASK} \bullet \overline{ACK} \bullet \overline{WR}$)

Figure 15. MODE 2 (Bidirectional)

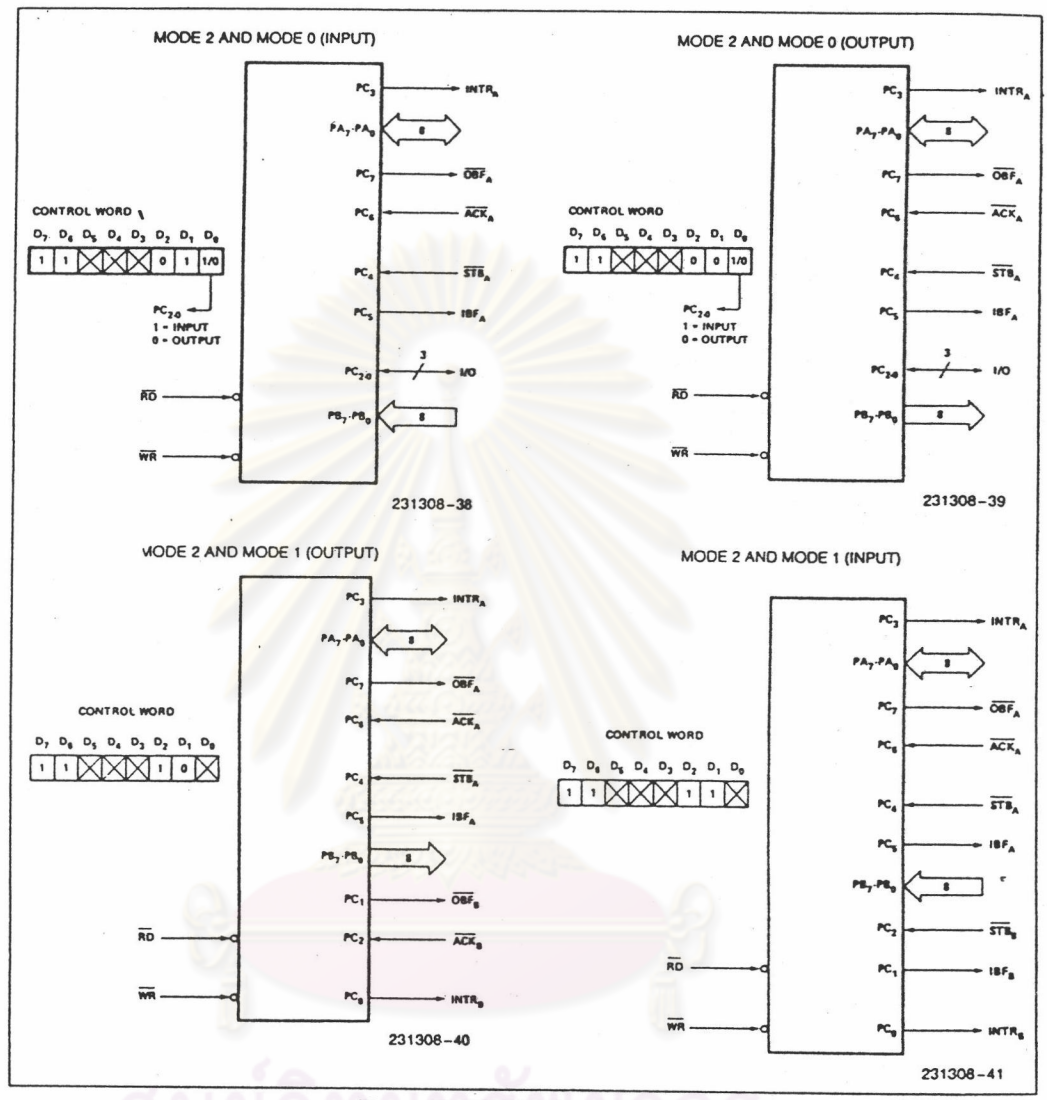


Figure 16. MODE 1/4 Combinations

Mode Definition Summary

	MODE 0		MODE 1		MODE 2	
	IN	OUT	IN	OUT	GROUP A ONLY	
PA_0	IN	OUT	IN	OUT	⟷	
PA_1	IN	OUT	IN	OUT	⟷	
PA_2	IN	OUT	IN	OUT	⟷	
PA_3	IN	OUT	IN	OUT	⟷	
PA_4	IN	OUT	IN	OUT	⟷	
PA_5	IN	OUT	IN	OUT	⟷	
PA_6	IN	OUT	IN	OUT	⟷	
PA_7	IN	OUT	IN	OUT	⟷	
PB_0	IN	OUT	IN	OUT	—	MODE 0 OR MODE 1 ONLY
PB_1	IN	OUT	IN	OUT	—	
PB_2	IN	OUT	IN	OUT	—	
PB_3	IN	OUT	IN	OUT	—	
PB_4	IN	OUT	IN	OUT	—	
PB_5	IN	OUT	IN	OUT	—	
PB_6	IN	OUT	IN	OUT	—	
PB_7	IN	OUT	IN	OUT	—	
PC_0	IN	OUT	$INTR_B$	$INTR_B$	I/O	
PC_1	IN	OUT	IBF_B	$\overline{OBF}_B$	I/O	
PC_2	IN	OUT	$\overline{STB}_B$	$\overline{ACK}_B$	I/O	
PC_3	IN	OUT	$INTR_A$	$INTR_A$	$INTR_A$	
PC_4	IN	OUT	$\overline{STB}_A$	I/O	$\overline{STB}_A$	
PC_5	IN	OUT	IBF_A	I/O	IBF_A	
PC_6	IN	OUT	I/O	$\overline{ACK}_A$	$\overline{ACK}_A$	
PC_7	IN	OUT	I/O	$\overline{OBF}_A$	$\overline{OBF}_A$	

Special Mode Combination Considerations

There are several combinations of modes when not all of the bits in Port C are used for control or status. The remaining bits can be used as follows:

If Programmed as Inputs—

All input lines can be accessed during a normal Port C read.

If Programmed as Outputs—

Bits in C upper (PC_7–PC_4) must be individually accessed using the bit set/reset function.

Bits in C lower (PC_3–PC_0) can be accessed using the bit set/reset function or accessed as a threesome by writing into Port C.

Source Current Capability on Port B and Port C

Any set of **eight** output buffers, selected randomly from Ports B and C can source 1 mA at 1.5 volts.

This feature allows the 8255 to directly drive Darlington type drivers and high-voltage displays that require such source current.

Reading Port C Status

In Mode 0, Port C transfers data to or from the peripheral device. When the 8255 is programmed to function in Modes 1 or 2, Port C generates or accepts "hand-shaking" signals with the peripheral device. Reading the contents of Port C allows the programmer to test or verify the "status" of each peripheral device and change the program flow accordingly.

There is no special instruction to read the status information from Port C. A normal read operation of Port C is executed to perform this function.

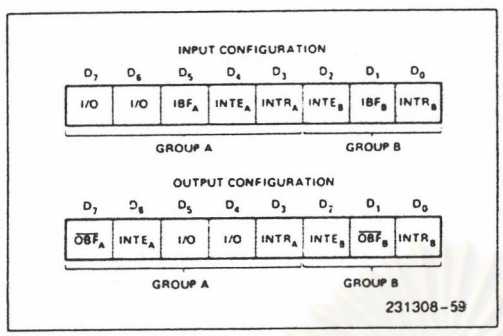


Figure 17. MODE 1 Status Word Format

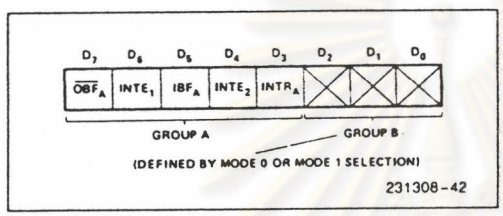


Figure 18. MODE 2 Status Word Format

APPLICATIONS OF THE 8255A

The 8255A is a very powerful tool for interfacing peripheral equipment to the microcomputer system. It represents the optimum use of available pins and is flexible enough to interface almost any I/O device without the need for additional external logic.

Each peripheral device in a microcomputer system usually has a "service routine" associated with it. The routine manages the software interface between the device and the CPU. The functional definition of the 8255A is programmed by the I/O service routine and becomes an extension of the system software. By examining the I/O devices interface characteristics for both data transfer and timing, and matching this information to the examples and tables in the detailed operational description, a control word can easily be developed to initialize the 8255A to exactly "fit" the application. Figures 19 through 25 represent a few examples of typical applications of the 8255A.

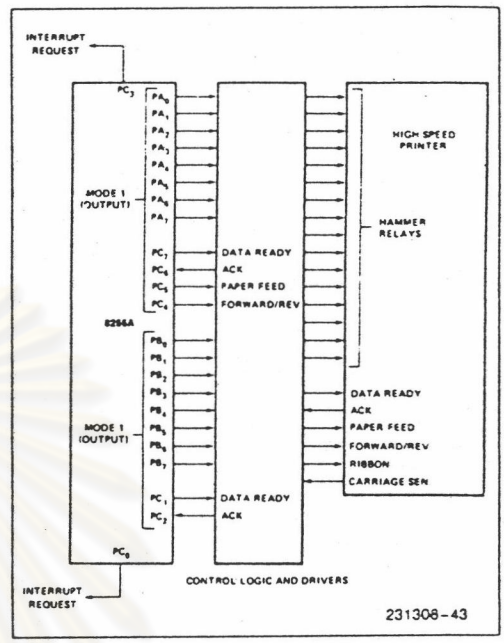


Figure 19. Printer Interface

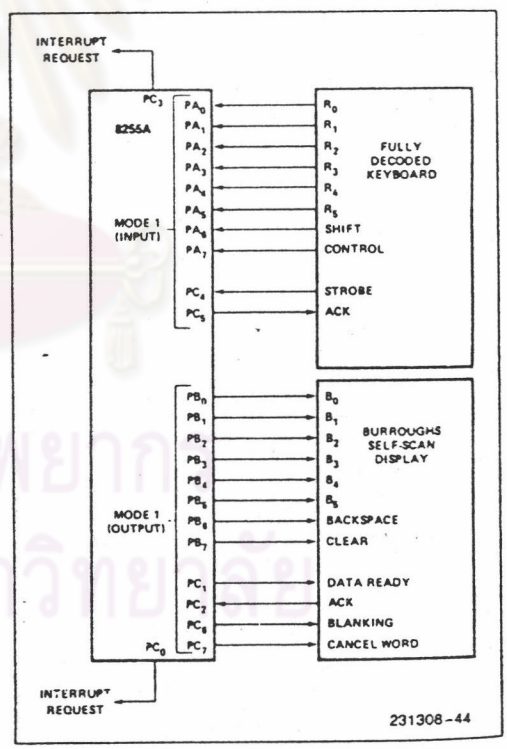


Figure 20. Keyboard and Display Interface

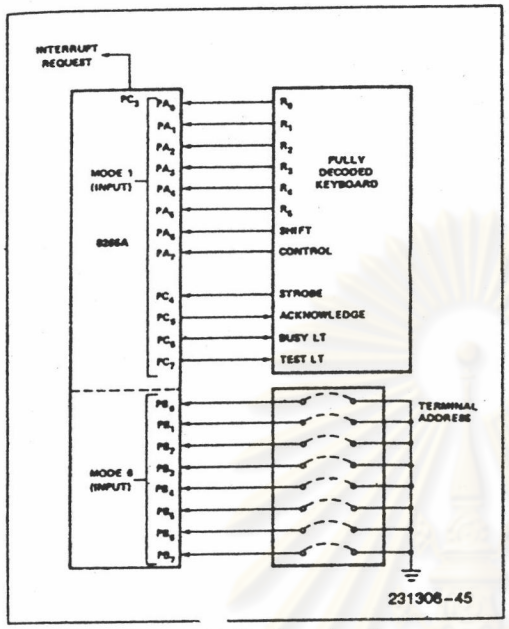


Figure 21. Keyboard and Terminal Address Interface

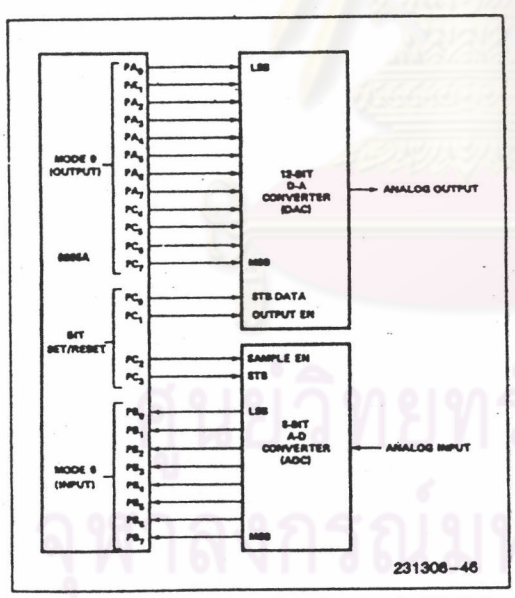


Figure 22. Digital to Analog, Analog to Digital

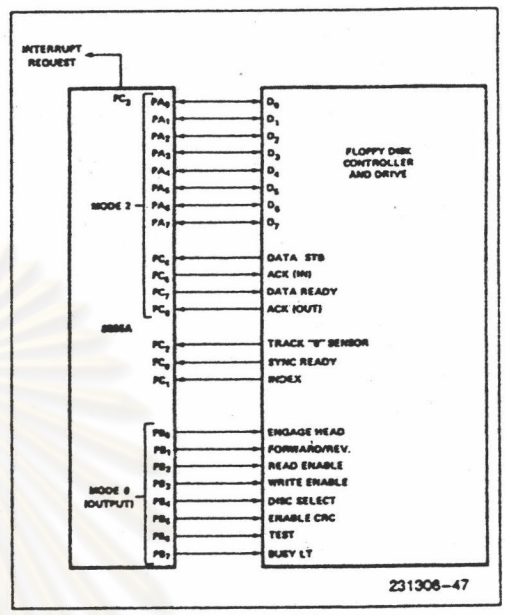


Figure 23. Basic Floppy Disk Interface

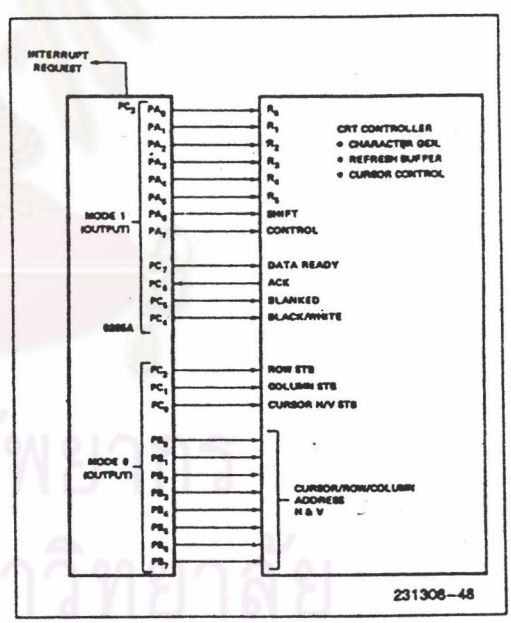


Figure 24. Basic CRT Controller Interface

ภาคผนวก จ

ข้อมูลของไอซี ADC หมายเลข 574A

BURR-BROWN®

ADC574A

Microprocessor-Compatible ANALOG-TO-DIGITAL CONVERTER

FEATURES

- COMPLETE 12-BIT A/D CONVERTER WITH REFERENCE, CLOCK, AND 8-, 12-, OR 16-BIT MICROPROCESSOR BUS INTERFACE
- IMPROVED PERFORMANCE SECOND SOURCE FOR 574A-TYPE A/D CONVERTERS
  - 25μs Maximum Conversion Time
  - 150ns Bus Access Time
  - A_0 Input: Bus Contention During Read Operation Eliminated
- FULLY SPECIFIED FOR OPERATION ON ±12V OR ±15V SUPPLIES
- NO MISSING CODES OVER TEMPERATURE
  - 0°C to +75°C: ADC574AJH, KH Grades
  - −55°C to +125°C: ADC574ASH, TH Grades

DESCRIPTION

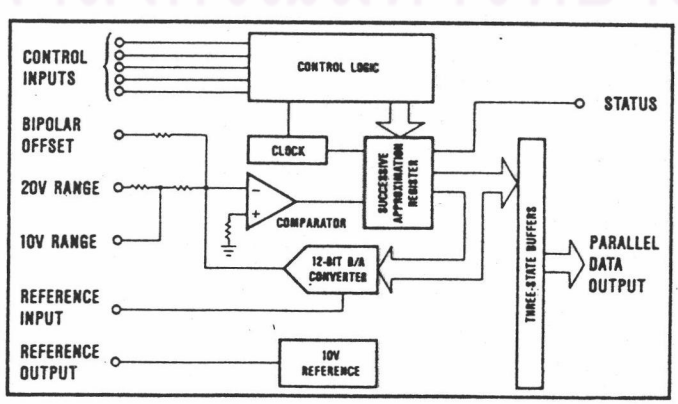
The ADC574A is a 12-bit successive approximation analog-to-digital converter, utilizing state-of-the-art CMOS and laser-trimmed bipolar die custom-designed for freedom from latch-up and for optimum AC performance. It is complete with a self-contained +10V reference, internal clock, digital interface for microprocessor control, and three-state outputs.

The reference circuit, containing a buried zener, is laser-trimmed for minimum temperature coefficient. The clock oscillator is current-controlled for excellent stability over temperature. Full-scale and offset errors may be externally-trimmed to zero. Internal scaling resistors are provided for the selection of analog input signal ranges of 0V to +10V, 0V to +20V, ±5V, and ±10V.

The converter may be externally programmed to provide 8- or 12-bit resolution. The conversion time for 12 bits is factory set for 20μs typical.

Output data are available in a parallel format from TTL-compatible three-state output buffers. Output data are coded in straight binary for unipolar input signals and bipolar offset binary for bipolar input signals.

The ADC574A, available in both industrial and military temperature ranges, requires supply voltages of +5V and ±12V or ±15V. It is packaged in a hermetic 28-pin side-brazed ceramic DIP.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

T_A = +25°C, V_{CC} = +12V or +15V, V_{EE} = −12V or −15V, V_{LOGIC} = +5V unless otherwise specified.

MODEL	ADC574AJH, ADC574ASH			ADC574AKH, ADC574ATH			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
RESOLUTION			12			•	Bits
INPUT							
ANALOG							
Voltage Ranges: Unipolar		0 to +10, 0 to +20			•		V
Bipolar		±5, ±10			•		V
Impedance: 0 to +10V, ±5V	3.7	5	6.3	•	•	•	kΩ
±10V, 0V to +20V	7.5	10	12.5	•	•	•	kΩ
DIGITAL (CE, $\overline{CS}$, R/$\overline{C}$, A_0, 12/$\overline{8}$)							
Over Temperature Range							
Voltages: Logic 1	+2.4[1]		+5.5	•		•	V
Logic 0	−0.5		+0.8	•	•	•	V
Current, 0.0V ≤ V_{IN} ≤ 5.0V	−5	0.1	+5	•	•	•	µA
Capacitance		5			•		pF
TRANSFER CHARACTERISTICS							
ACCURACY							
At +25°C							
Linearity Error			±1			±1/2	LSB
Unipolar Offset Error (adjustable to zero)			±2			•	LSB
Bipolar Offset Error (adjustable to zero)			±10			±4	LSB
Full-Scale Calibration Error[2]							
(adjustable to zero)			±0.3			•	% of FS[3]
No Missing Codes Resolution	11			12			Bits
Inherent Quantization Error		±1/2			•		LSB
T_{MIN} to T_{MAX}							
Linearity Error: J, K Grades			±1			±1/2	% of FS
S, T Grades			±1			•	% of FS
Full-Scale Calibration Error							
Without Initial adjustment[2]: J, K Grades			±0.5			±0.4	% of FS
S, T Grades			±0.8			±0.6	% of FS
Adjusted to zero at +25°C: J, K Grades			±0.22			±0.12	% of FS
S, T Grades			±0.5			±0.25	% of FS
No Missing Codes Resolution	11			12			Bits
POWER SUPPLY SENSITIVITY							
Change in Full-Scale Calibration							
+13.5V < V_{CC} < +16.5V or +11.4V < V_{CC} < +12.6V			±2			±1	LSB
−16.5V < V_{EE} < −13.5V or −12.6V < V_{EE} < −11.4V			±2			±1	LSB
+4.5V < V_{LOGIC} < +5.5V			±1/2			•	LSB
CONVERSION TIME[4]							
8-Bit Cycle	10	13	17	•	•	•	µs
12-Bit Cycle	15	20	25	•	•	•	µs
DRIFT							
Unipolar Offset: J, K Grades			±10			±5	ppm/°C
S, T Grades			±5			±2.5	ppm/°C
Change over Temperature Range, All Grades			±2			±1	LSB
Bipolar Offset, All Grades			±10			±5	ppm/°C
Change over Temperature Range: J, K Grades			±2			±1	LSB
S, T Grades			±4			±2	LSB
Full-Scale Calibration: J, K Grades			±45			±25	ppm/°C
S, T Grades			±50			±25	ppm/°C
Change over Temperature Range: J, K Grades			±9			±5	LSB
S, T Grades			±20			±10	LSB
OUTPUT							
DIGITAL (DB_{11} – DB_0, STATUS)							
Over Temperature Range							
Output Codes: Unipolar			Unipolar Straight Binary (USB)				
Bipolar			Bipolar Offset Binary (BOB)				
Logic Levels: Logic 0 (I_{sink} = 1.6mA)			+0.4			•	V
Logic 1 (I_{source} = 500µA)	+2.4			•			V
Leakage, Data Bits Only, High-Z State	−5	0.1	+5	•	•	•	µA
Capacitance		5			•		pF
INTERNAL REFERENCE VOLTAGE							
Voltage	+9.9	+10.0	+10.1	•	•	•	V
Source Current Available for External Loads[5]	2.0			•			mA

ELECTRICAL (CONT)

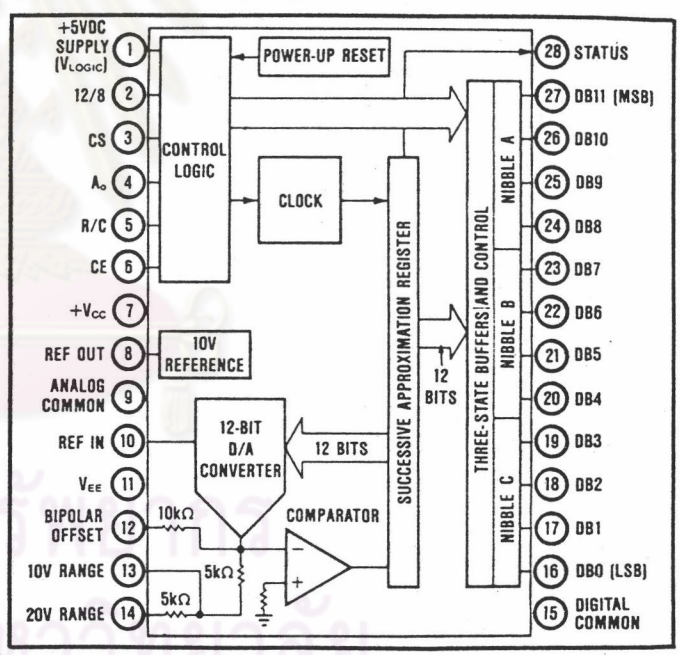
T_A = +25°C, V_{CC} = +12V or +15V, V_{EE} = −12V or −15V, V_{LOGIC} = +5V unless otherwise specified.

MODEL	ADC574AJH, ADC574ASH			ADC574AKH, ADC574ATH			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY REQUIREMENTS							
Voltage: V_{CC}	+11.4		+16.5	•		•	V
V_{EE}	−11.4		−16.5	•		•	V
V_{LOGIC}	+4.5		+5.5	•		•	V
Current: I_{CC}		11	15		•	•	mA
I_{EE}		21	28		•	•	mA
I_{LOGIC}		7	15		•	•	mA
Power Dissipation (±15V Supplies)		515	720		•	•	mW
TEMPERATURE RANGE (Ambient)							
Specification: J, K Grades	0		+75	•		•	°C
S, T Grades	−55		+125	•		•	°C
Storage	−65		+150	•		•	°C

*Same specification as grade to the immediate left.

NOTES: (1) Although this guaranteed threshold is higher than the standard TTL guaranteed level (+2.0V), bus loading is much less. Typical input current is only 0.25% of a standard TTL load. (2) With fixed 50Ω resistor from REF OUT to REF IN. This parameter is also adjustable to zero at +25°C (see "Optional External Full Scale and Offset Adjustments" section). (3) FS in this specification table means Full-Scale Range. That is, for a ±10V input range, FS means 20V; for a 0 to +10V range, FS means 10V. Use of the term Full Scale for these specifications instead of Full-Scale Range is consistent with other vendors' 574 and 574A specification tables. (4) See "Controlling the ADC574A" section for detailed information concerning digital timing. (5) External loading must be constant during conversion. When supplying an external load and operating on ±12V supplies, a buffer amplifier must be provided for the reference output.

CONNECTION DIAGRAM



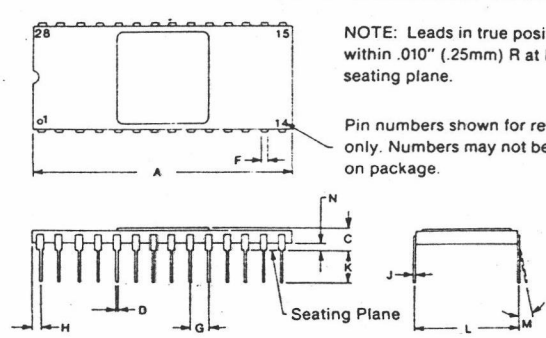
ABSOLUTE MAXIMUM RATINGS

V_{CC} to Digital Common	0 to +16.5V
V_{EE} to Digital Common	0 to −16.5V
V_{LOGIC} to Digital Common	0 to +7V
Analog Common to Digital Common	±1V
Control Inputs (CE, $\overline{CS}$, A_0, 12/8, R/C) to Digital Common	−0.5V to V_{LOGIC} +0.5V
Analog Inputs (REF IN, BIP OFF, $10V_{IN}$) to Analog Common	±16.5V
$20V_{IN}$ to Analog Common	±24V
REF OUT	Indefinite Short to Common, Momentary Short to V_{CC}
Chip Temperature: J, K, L Grades	+100°C
S, T, U Grades	+150°C
Power Dissipation	1000mW
Lead Temperature, Soldering	+300°C, 10sec
Thermal Resistance, θ_{JA}	48°C/W

CAUTION: These devices are sensitive to electrostatic discharge. Appropriate I.C. handling procedures should be followed.

MECHANICAL

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.386	1.414	35.20	35.92
C	.108	.166	2.74	4.22
D	.015	.021	0.38	0.53
F	.035	.060	0.89	1.52
G	.100 BASIC		2.54 BASIC	
H	.036	.064	0.91	1.63
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.600 BASIC		15.24 BASIC	
M	– –	10°	– –	10°
N	.025	.060	0.64	1.52



NOTE: Leads in true position within .010" (.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

CASE: Ceramic, hermetic
MATING CONNECTOR: 2803MC
WEIGHT: 4.8 grams (0.17oz.)

DISCUSSION OF SPECIFICATIONS

LINEARITY ERROR

Linearity error is defined as the deviation of actual code transition values from the ideal transition values. Ideal transition values lie on a line drawn through zero (or minus full scale for bipolar operation) and plus full scale. The zero value is located at an analog input value 1/2LSB before the first code transition (000_H to 001_H). The full-scale value is located at an analog value 3/2LSB beyond the last code transition (FFE_H to FFF_H) (see Figure 1).

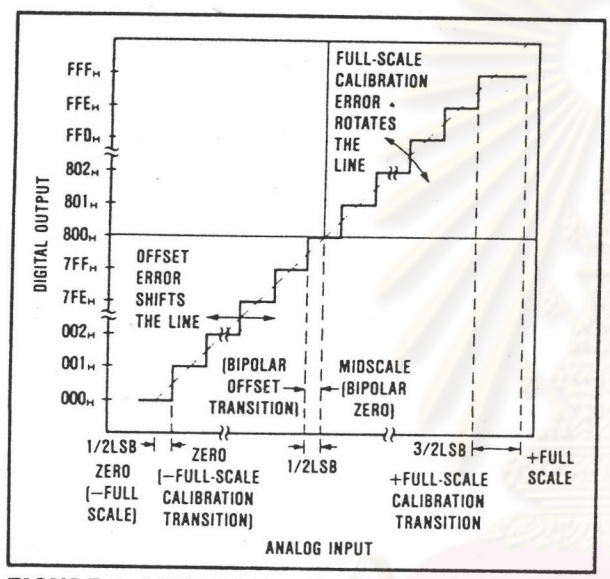


FIGURE 1. ADC574A Transfer Characteristic Terminology.

Thus, for a converter connected for bipolar operation and with a full-scale range (or span) of 20V (±10V), the zero value of −10V is 2.44mV below the first code transition (000_H to 001_H at −9.99756V) and the plus full-scale value of +10V is 7.32mV above the last code transition (FFE_H to FFF_H at +9.99268) (see Table I).

NO MISSING CODES (DIFFERENTIAL LINEARITY ERROR)

A specification which guarantees no missing codes requires that every code combination appear in a monotonically-increasing sequence as the analog input is increased throughout the range. Thus, every input code width (quantum) must have a finite width. If an input quantum has a value of zero (a differential linearity error of −1LSB), a missing code will occur.

ADC57A KH and TH grades are guaranteed to have no missing codes to 12-bit resolution over their respective specification temperature ranges.

UNIPOLAR OFFSET ERROR

An ADC574A connected for unipolar operation has an analog input range of 0V to plus full scale. The first output code transition should occur at an analog input value 1/2LSB above 0V. Unipolar offset error is defined as the deviation of the actual transition value from the ideal value. The unipolar offset temperature coefficient specifies the change of this transition value versus a change in ambient temperature.

BIPOLAR OFFSET ERROR

A/D converter specifications have historically defined bipolar offset as the first transition value above the minus full-scale value. The ADC574A specification, however, follows the terminology defined for the 574 converter several years ago. Thus, bipolar offset is located near the midscale value of 0V (bipolar zero) at the output code transition $7FF_H$ to 800_H.

Bipolar offset error for the ADC574A is defined as the deviation of the actual transition value from the ideal transition value located 1/2LSB below 0V. The bipolar offset temperature coefficient specifies the maximum change of the code transition value versus a change in ambient temperature.

FULL SCALE CALIBRATION ERROR

The last output code transition (FFE_H to FFF_H) occurs for an analog input value 3/2LSB below the nominal full-scale value. The full scale calibration error is the deviation of the actual analog value at the last transition point from the ideal value. The full-scale calibration temperature coefficient specifies the maximum change of the code transition value versus a change in ambient temperature.

POWER SUPPLY SENSITIVITY

Electrical specifications for the ADC574A assume the application of the rated power supply voltages of +5V and ±12V or ±15V. The major effect of power supply

TABLE I. Input Voltages, Transition Values, and LSB Values.

Binary (BIN) Output	Input Voltage Range and LSB Values				
Analog Input Voltage Range	Defined As:	±10V	±5V	0 to +10V	0 to +20V
One Least Significant Bit (LSB)	$\frac{FSR}{2^n}$ n = 8 n = 12	$\frac{20V}{2^n}$ 78.13mV 4.88mV	$\frac{10V}{2^n}$ 39.06mV 2.44mV	$\frac{10V}{2^n}$ 39.06mV 2.44mV	$\frac{20V}{2^n}$ 78.13mV 4.88mV
Output Transition Values FFE_H to FFF_H $7FFF_H$ to 800_H 000_H to 001_H	+ Full-Scale Calibration Midscale Calibration (Bipolar Offset) Zero Calibration (− Full-Scale Calibration)	+10V − 3/2LSB 0 − 1/2LSB −10V + 1/2LSB	+5V − 3/2LSB 0 − 1/2LSB −5V + 1/2LSB	+10V − 3/2LSB +5V − 1/2LSB 0 + 1/2LSB	+20V − 3/2LSB +10V − 1/2LSB 0 + 1/2LSB

voltage deviations from the rated values will be a small change in the full-scale calibration value. This change, of course, results in a proportional change in all code transition values (i.e. a gain error). The specification describes the maximum change in the full-scale calibration value from the initial value for a change in each power supply voltage.

TEMPERATURE COEFFICIENTS

The temperature coefficients for full-scale calibration, unipolar offset and bipolar offset specify the maximum change from the +25°C value to the value at T_{MIN} or T_{MAX}.

QUANTIZATION UNCERTAINTY

Analog-to-digital converters have an inherent quantization error of ±1/2LSB. This error is a fundamental property of the quantization process and cannot be eliminated.

CODE WIDTH (QUANTUM)

Code width, or quantum, is defined as the range of analog input values for which a given otuput code will occur. The ideal code width is 1LSB.

INSTALLATION

LAYOUT PRECAUTIONS

Analog (pin 9) and digital (pin 15) commons are not connected together internally in the ADC574A, but should be connected together as close to the unit as possible and to an analog common ground plane beneath the converter on the component side of the board. In addition, a wide conductor pattern should run directly from pin 9 to the analog supply common, and a separate wide conductor pattern from pin 15 to the digital supply common.

If the single-point system common cannot be established directly at the converter, pin 9 and pin 15 should still be connected together at the converter; a single wide conductor pattern then connects these two pins to the system common. This single common path will typically carry about 1.5mA of current out of the converter. Code-dependent currents do not flow in analog (pin 9) or digital (pin 15) commons. DC currents that flow are typically +7mA in pin 9 and −5.5mA in pin 15.

Coupling between analog input and digital lines should be minimized by careful layout. For instance, if the lines must cross, they should do so at right angles. Parallel analog and digital lines should be separated from each other by a pattern connected to common.

If external full scale and offset potentiometers are used, the potentiometers and associated resistors should be located as close to the ADC574A as possible. If no trim adjustments are used, the fixed resistors should likewise be as close as possible.

POWER SUPPLY DECOUPLING

The power supplies should be bypassed with 10μF tantalum bypass capacitors located close to the converter to obtain noise-free operation. Noise on the power supply lines can degrade the converter's performance. Noise and spikes from a switching power supply are especially troublesome.

ANALOG SIGNAL SOURCE IMPEDANCE

The signal source supplying the analog input signal to the ADC574A will be driving into a nominal DC input impedance of either 5kΩ or 10kΩ. However, the output impedance of the driving source should be very low, such as the output impedance provided by a wideband, fast-settling operational amplifier. Transients in A/D input current are caused by the changes in output current of the internal D/A converter as it tests the various bits. The output voltage of the driving source must remain constant while furnishing these fast current changes. If the application requires a sample/hold, select a sample/hold with sufficient bandwidth to preserve the accuracy or use a separate wideband buffer amplifier to lower the output impedance.

RANGE CONNECTIONS

The ADC574A offers four standard input ranges: 0V to +10V, 0V to +20V, ±5V, and ±10V. If a 10V input range is required, the analog input signal should be connected to pin 13 of the converter. A signal requiring a 20V range is connected to pin 14. In either case the other pin of the two is left unconnected. Full-scale and offset adjustments are described below.

To operate the converter with a 10.24V (2.5mV LSB) or 20.48V (5mV LSB) input range, insert a 200Ω potentiometer in series with pin 13 for the 10.24V range, or a 500Ω potentiometer in series with pin 14 for the 20.48V range. Use a fixed 50Ω, 1% resistor for R_2 (Figures 2 and 3). Offset adjustment is still performed as described below. Full-scale adjustment is performed as described below but with adjustment performed using the input potentiometer instead of R_2.

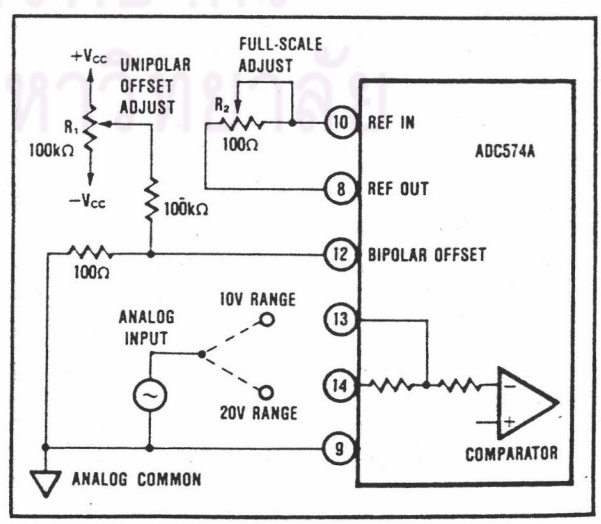


FIGURE 2. Unipolar Configuration.

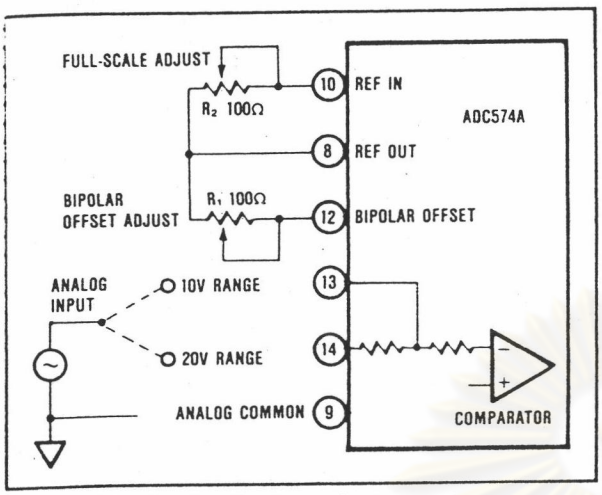


FIGURE 3. Bipolar Configuration.

CALIBRATION

OPTIONAL EXTERNAL FULL-SCALE AND OFFSET ADJUSTMENTS

Offset and full-scale errors may be trimmed to zero using external offset and full-scale trim potentiometers connected to the ADC574A as shown in Figures 2 and 3 for unipolar and bipolar operation.

CALIBRATION PROCEDURE—UNIPOLAR RANGES

If adjustment of unipolar offset and full scale is not required, replace R_2 with a 50Ω, 1% metal film resistor and connect pin 12 to pin 9, omitting the adjustment network.

If adjustment is required, connect the converter as shown in Figure 2. Sweep the input through the end-point transition voltage (0V + 1/2LSB; +1.22mV for the 10V range, +2.44mV for the 20V range) that causes the output code to be DBO ON (high). Adjust potentiometer R_1 until DBO is alternately toggling ON and OFF with all other bits OFF. Then adjust full scale by applying an input voltage of nominal full-scale value minus 3/2LSB, the value which should cause all bits to be ON. This value is +9.9963V for the 10V range and +19.9927V for the 20V range. Adjust potentiometer R_2 until bits DB1–DB11 are ON and DBO is toggling ON and OFF.

CALIBRATION PROCEDURE—BIPOLAR RANGES

If external adjustments of full-scale and bipolar offset are not required, the potentiometers may be replaced by 50Ω, 1% metal film resistors.

If adjustments are required, connect the converter as shown in Figure 3. The calibration procedure is similar to that described above for unipolar operation, except that the offset adjustment is performed with an input voltage which is 1/2LSB above the minus full-scale value (−4.9988V for the ±5V range, −9.9976V for the ±10V range). Adjust R_1 for DB0 to toggle ON and OFF with all other bits OFF. To adjust full-scale, apply a DC input signal which is 3/2LSB below the nominal plus full-scale value (+4.9963V for ±5V range, +9.9927V for ±10V range) and adjust R_2 for DB0 to toggle ON and OFF with all other bits ON.

CONTROLLING THE ADC574A

The Burr-Brown ADC574A can be easily interfaced to most microprocessor systems and other digital systems. The microprocessor may take full control of each conversion, or the converter may operate in a stand-alone mode, controlled only by the $R/\overline{C}$ input. Full control consists of selecting an 8- or 12-bit conversion cycle, initiating the conversion, and reading the ouptut data when ready—choosing either 12 bits all at once, or 8 bits followed by 4 bits in a left-justified format. The five control inputs (12/8, $\overline{CS}$, A_0, $R/\overline{C}$, and CE) are all TTL/CMOS-compatible. The functions of the control inputs are described in Table II. The control function truth table is listed in Table III.

STAND-ALONE OPERATION

For stand-alone operation, control of the converter is accomplished by a single control line connected to $R/\overline{C}$. In this mode $\overline{CS}$ and A_0 are connected to digital common and CE and $12/\overline{8}$ are connected to V_{LOGIC} (+5V). The output data are presented as 12-bit words. The

TABLE II. ADC574A Control Line Functions.

Pin Designation	Definition	Function
CE (Pin 6)	Chip Enable (active high)	Must be high ("1") to either initiate a conversion or read output data. 0-1 edge may be used to initiate a conversion
$\overline{CS}$ (Pin 3)	Chip Select (active low)	Must be low ("0") to either initiate a conversion or read output data. 1-0 edge may be used to initiate a conversion
$R/\overline{C}$ (Pin 5)	Read/Convert ("1" = read) ("0" = convert)	Must be low ("0") to initiate either 8 or 12-bit conversions. 1-0 edge may be used to initiate a conversion. Must be high ("1") to read output data. 0-1 edge may be used to initiate a read operation.
A_0 (Pin 4)	Byte Address Short Cycle	In the start-convert mode, A_0 selects 8-bit (A_0 = "1") or 12-bit (A_0 = "0") conversion mode. When reading output data in 2 8-bit bytes, A_0 = "0" accesses 8 MSBs (high byte) and A_0 = "1" accesses 4 LSBs and trailing "0s" (low byte).
$12/\overline{8}$ (Pin 2)	Data Mode Select ("1" = 12 bits) ("0" = 8 bits)	When reading output data; $12/\overline{8}$ = "1" enables all 12 output bits simultaneously. $12/\overline{8}$ = "0" will enable the MSB's or LSB's as determined by the A_0 line.

TABLE III. Control Input Truth Table.

CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	A_0	Operation
0	X	X	X	X	None
X	1	X	X	X	None
↑	0	0	X	0	Initiate 12-bit conversion
↑	0	0	X	1	Initiate 8-bit conversion
1	↓	0	X	0	Initiate 12-bit conversion
1	↓	0	X	1	Initiate 8-bit conversion
1	0	↓	X	0	Initiate 12-bit conversion
1	0	↓	X	1	Initiate 8-bit conversion
1	0	1	1	X	Enable 12-bit output
1	0	1	0	0	Enable 8 MSBs only
1	0	1	0	1	Enable 4 LSBs plus 4 trailing zeros

stand-alone mode is used in systems containing dedicated input ports which do not require full bus interface capability.

Conversion is initiated by a high-to-low transition of R/$\overline{C}$. The three-state data output buffers are enabled when R/$\overline{C}$ is high and STATUS is low. Thus, there are two possible modes of operation; conversion can be initiated with either positive or negative pulses. In either case the R/$\overline{C}$ pulse must remain low for a minimum of 50nsec.

Figure 4 illustrates timing when conversion is initiated by an R/$\overline{C}$ pulse which goes low and returns to the high state during the conversion. In this case, the three-state outputs go to the high-impedance state in response to the falling edge of R/$\overline{C}$ and are enabled for external access of the data after completion of the conversion. Figure 5 illustrates the timing when conversion is initiated by a positive R/$\overline{C}$ pulse. In this mode the ouptut data from the previous conversion is enabled during the positive portion of R/$\overline{C}$. A new conversion is started on the falling edge of R/$\overline{C}$, and the three-state outputs return to the high-impedance state until the next occurrence of a high R/$\overline{C}$ pulse. Table IV lists timing specifications for stand-alone operation.

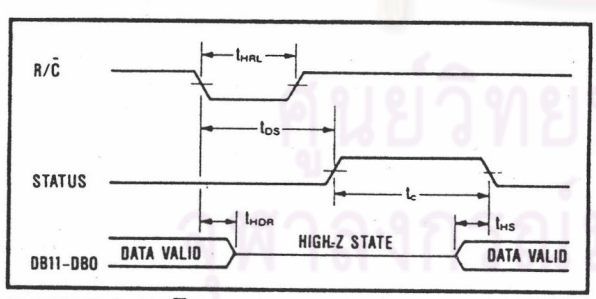


FIGURE 4. R/$\overline{C}$ Pulse Low — Outputs Enabled After Conversion.

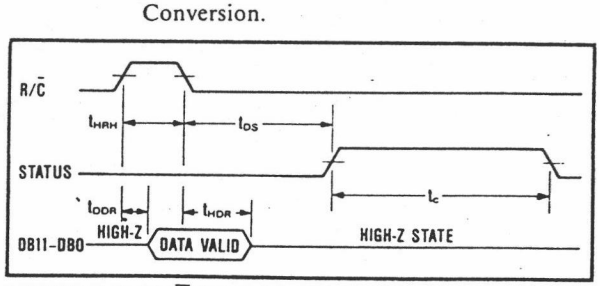


FIGURE 5. R/$\overline{C}$ Pulse High — Outputs Enabled Only While R/$\overline{C}$ Is High.

TABLE IV. Stand-Alone Mode Timing.

Symbol	Parameter	Min	Typ	Max	Units
t_{HRL}	Low R/$\overline{C}$ Pulse Width	50			ns
t_{DS}	STS Delay from R/$\overline{C}$			200	ns
t_{HDR}	Data Valid After R/$\overline{C}$ Low	25			ns
t_{HS}	STS Delay After Data Valid	300	500	1000	ns
t_{HRH}	High R/$\overline{C}$ Pulse Width	150			ns
t_{DDR}	Data Access Time			150	ns

FULLY CONTROLLED OPERATION

Conversion Length

Conversion length (8-bit or 12-bit) is determined by the state of the A_0 input, which is latched upon receipt of a conversion start transition (described below). If A_0 is latched high, the conversion continues for 8 bits. The full 12-bit conversion will occur if A_0 is low. If all 12 bits are read following an 8-bit conversion, the 3LSBs (DB0 - DB2) will be low (logic 0) and DB3 will be high (logic 1). A_0 is latched because it is also involved in enabling the output buffers. No other control inputs are latched.

CONVERSION START

The converter is commanded to initiate conversion by a transition occurring on any of three logic inputs (CE, $\overline{CS}$, and R/$\overline{C}$) as shown in Table III. Conversion is initiated by the last of the three to reach the required state and thus all three may be dynamically controlled. If necessary, all three may change states simultaneously, and the nominal delay time is the same regardless of which input actually starts conversion. If it is desired that a particular input establish the actual start of conversion, the other two should be stable a minimum of 50nsec prior to the transition of that input. Timing relationships for start of conversion timing are illustrated in Figure 6. The specifications for timing are contained in Table V.

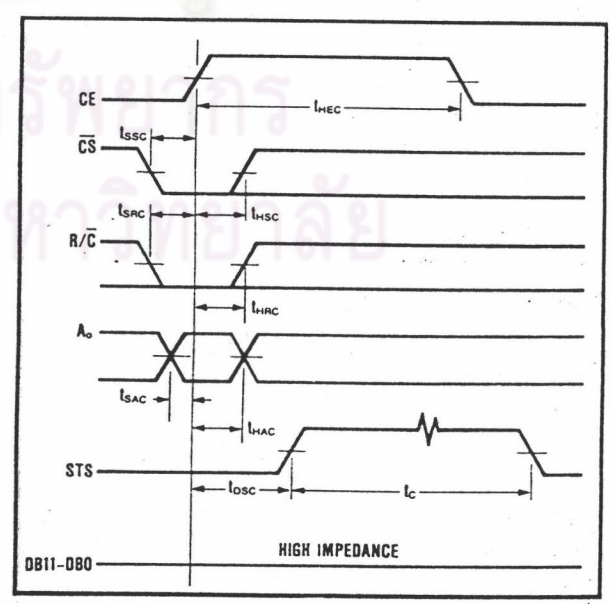


FIGURE 6. Conversion Cycle Timing.

TABLE V. Timing Specifications.

Symbol	Parameter	Min	Typ	Max	Units
Convert Mode					
t_{DSC}	STS delay from CE		100	200	ns
t_{HEC}	CE Pulse width	50	30		ns
t_{SSC}	$\overline{CS}$ to CE setup	50	20		ns
t_{HSC}	$\overline{CS}$ low during CE high	50	20		ns
t_{SRC}	R/$\overline{C}$ to CE setup	50	0		ns
t_{HRC}	R/$\overline{C}$ low during CE high	50	20		ns
t_{SAC}	A_0 to CE setup	0	0		ns
t_{HAC}	A_0 valid during CE high	50	20		ns
t_C	Conversion time, 12 bit cycle	15	20	25	μs
	8 bit cycle	10	13	17	μs
Read Mode					
t_{DD}	Access time from CE		75	150	ns
t_{HD}	Data valid after CE low	25	35		ns
t_{HL}	Output float delay		100	150	ns
t_{SSR}	$\overline{CS}$ to CE setup	50	0		ns
t_{SRR}	R/$\overline{C}$ to CE setup	0	0		ns
t_{SAR}	A_0 to CE setup	50	25		ns
t_{HSR}	$\overline{CS}$ valid after CE low	0	0		ns
t_{HRR}	R/$\overline{C}$ high after CE low	0	0		ns
t_{HAR}	A_0 valid after CE low	50	25		ns
t_{HS}	STS delay after data valid	300	500	1000	ns

NOTE: Specifications are at +25°C and measured at 50% level of transitions.

The STATUS output indicates the current state of the converter by being in a high state only during conversion. During this time the three state output buffers remain in a high-impedance state, and therefore data cannot be read during conversion. During this period additional transitions of the three digital inputs which control conversion will be ignored, so that conversion cannot be prematurely terminated or restarted. However, if A_0 changes state after the beginning of conversion, any additional start conversion transition will latch the new state of A_0, possibly resulting in an incorrect conversion length (8 bits vs 12 bits) for that conversion.

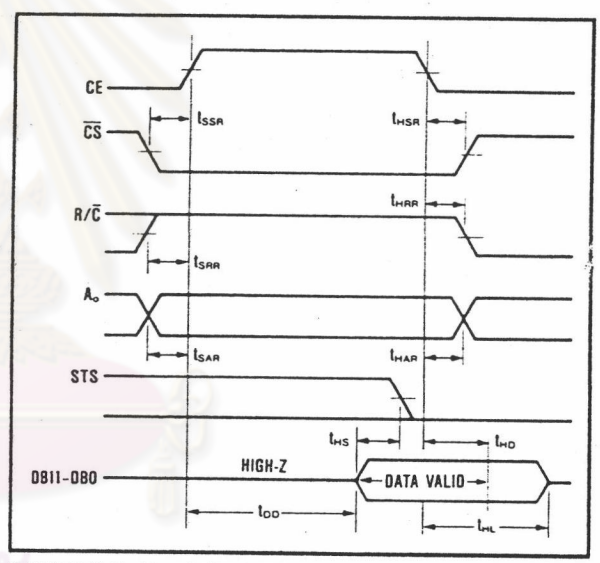


FIGURE 7. Read Cycle Timing.

READING OUTPUT DATA

After conversion is initiated, the output data buffers remain in a high-impedance state until the following four logic conditions are simultaneously met: R/$\overline{C}$ high, STATUS low, CE high, and $\overline{CS}$ low. Upon satisfaction of these conditions the data lines are enabled according to the state of inputs 12/$\overline{8}$ and A_0. See Figure 7 and Table V for timing relationships and specifications.

In most applications the 12/$\overline{8}$ input will be hard-wired in either the high or low condition, although it is fully TTL- and CMOS-compatible and may be actively driven if desired. When 12/$\overline{8}$ is high, all 12 output lines (DB0-DB11) are enabled simultaneously for full data word transfer to a 12-bit or 16-bit bus. In this situation the A_0 state is ignored.

When 12/$\overline{8}$ is low, the data is presented in the form of two 8-bit bytes, with selection of the byte of interest accomplished by the state of A_0 during the read cycle. Connection of the ADC574A to an 8-bit bus for transfer of left-justified data is illustrated in Figure 8. The A_0 input is usually driven by the least significant bit of the address bus, allowing storage of the output data word in two consecutive memory locations.

When A_0 is low, the byte addressed contains the 8MSBs. When A_0 is high, the byte addressed contains the 4LSBs from the conversion followed by four logic zeros which have been forced by the control logic. The left-justified

	Word 1								Word 2							
Processor	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Converter	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	0	0	0	0

FIGURE 8. 12-Bit Data Format for 8-Bit Systems.

formats of the two 8-bit bytes are shown in Figure 8. The design of the ADC574A guarantees that the A_0 input may be toggled at any time with no damage to the converter; the outputs which are tied together as illustrated in Figure 9 cannot be enabled at the same time.

In the majority of applications the read operation will be attempted only after the conversion is complete and the STATUS output has gone low. In those situations requiring the earliest possible access to the data, the read may be started as much as 1.15μsec (t_{DD} max + t_{HS} max) before STATUS goes low. Refer to Figure 7 for these timing relationships.

ORDERING INFORMATION

Model	Temperature Range	Linearity Error, max (T_{MIN} to T_{MAX})	Resolution, No Missing Codes (T_{MIN} to T_{MAX})	Full-Scale TC, max (ppm/°C)
ADC574AJH	0°C to +75°C	±1LSB	11 Bits	±45
ADC574AKH	0°C to +75°C	±1/2LSB	12 Bits	±25
ADC574ASH	−55°C to +125°C	±1LSB	11 Bits	±50
ADC574ATH	−55°C to +125°C	±1LSB	12 Bits	±25

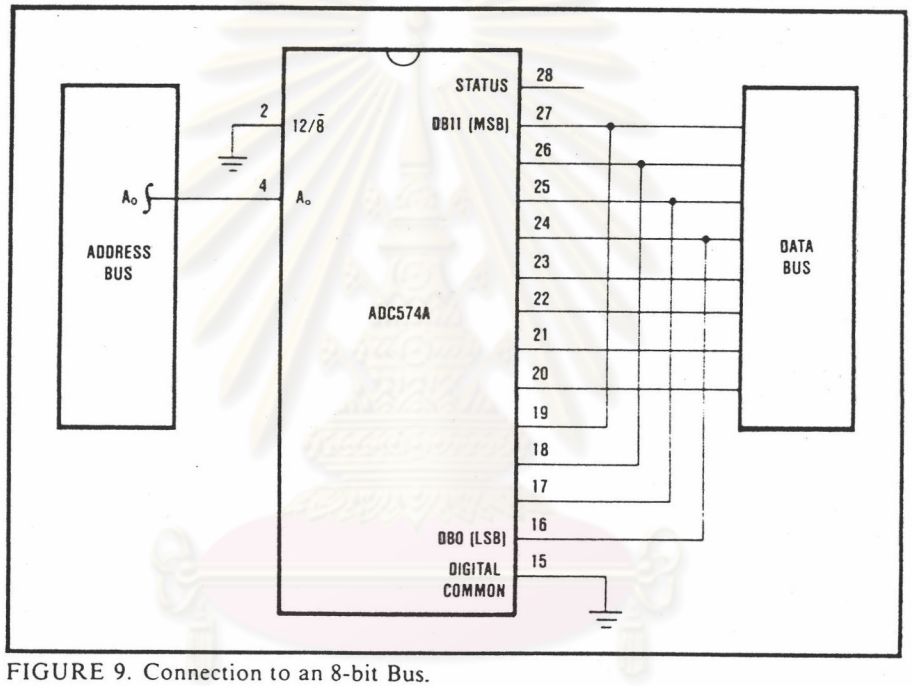


FIGURE 9. Connection to an 8-bit Bus.

ภาคผนวก ฉ

ข้อมูลของจอแสดงผลแบบ LCD ชนิดจุดและรหัสตัวอักษร

DV series

DV-16100

16 chars × 1 line **TN/STN** Reflective/EL/LED Backlight

■ ABSOLUTELY MAXIMUM RATINGS

Item	Symbol	Standard Value			Unit
		Min	Typ.	Max.	
Supply Voltage for Logic	V_{DD}-V_{SS}	0	-	7.0	V
Supply Voltage for LCD Drive	V_{DD}-V_{EE}	-	-	13.5	V
Input Voltage	V_I	V_{SS}	-	V_{DD}	V
Operature Temp	T_{OPR}	0	-	50	°C
Storage Temp	T_{STG}	-20	-	70	°C

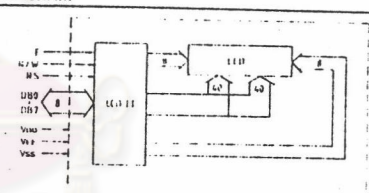
■ ELECTRICAL CHARACTERISTIC (REFLECTIVE TYPE)

Item	Symbol	Test Condition	Standard Value			Unit
			Min.	Typ.	Max.	
Input "High" Voltage	V_{IH}		2.2	-	V_{DD}	V
Input "Low" Voltage	V_{IL}		-	-	0.6	V
Output "High" Voltage	V_{OH}	for 0.2mA	2.2	-	-	V
Output "Low" Voltage	V_{OL}	for 1.2mA	-	-	0.4	V
Supply Current	I_{DD}	V_{DD} 5.0V	-	1.0	3.0	mA

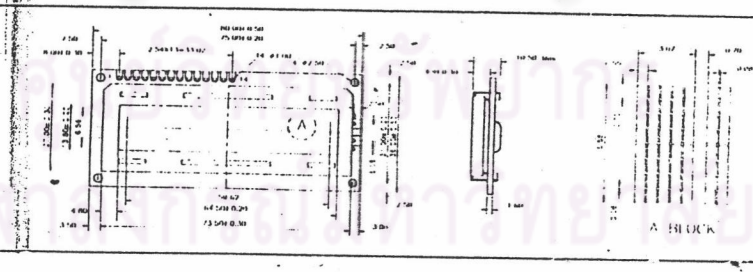
■ PIN FUNCTIONS

No	Symbol	Function	No	Symbol	Function
1	V_{SS}	GND, 0V	8	DB1	Data Bus
2	V_{DD}	+5V	9	DB2	
3	V_{EE}	for LCD Drive	10	DB3	—
4	RS	Function Select	11	DB4	
5	R/W	Read/Write	12	DB5	
6	E	Enable Signal	13	DB6	
7	DB0	Data Bus Line	14	DB7	

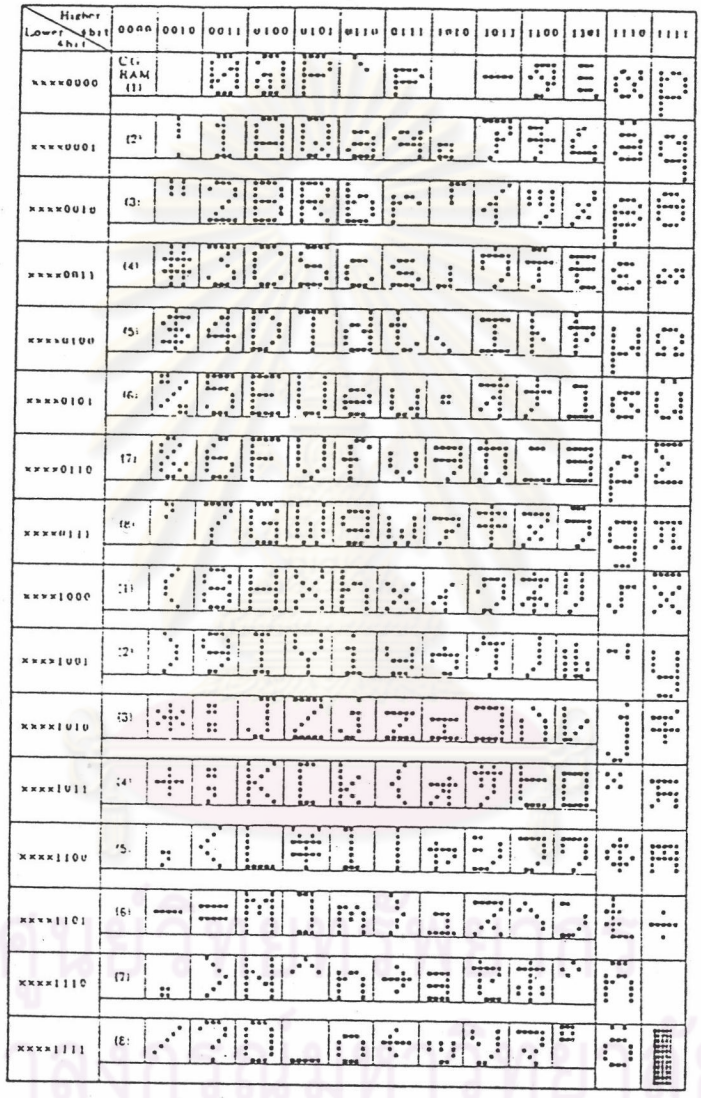
■ BLOCK DIAGRAM



■ DIMENSION OUTLINE



CHARACTER FONT TABLE



NOTE: CGRAM is a CHARACTER GENERATOR RAM having a storage function of character pattern which enable to change freely by user's program.

ภาคผนวก ช

ชุดคำสั่งดูแลระบบ

```
 1  0000  PORT_A      .EQU  00000000B  ; รหัสคุมพอร์ท A ของ 8255
 2  0001  PORT_B      .EQU  00000001B  ; รหัสคุมพอร์ท B ของ 8255
 3  0002  PORT_C      .EQU  00000010B  ; รหัสคุมพอร์ท C ของ 8255
 4  0003  PORT_CTRL   .EQU  00000011B  ; รหัสควบคุม 8255 ให้ทำงาน
 5  0004  LCD_CTRL    .EQU  00000100B  ; รหัสควบคุม LCD ให้ทำงาน
 6  0005  LCD_WRI     .EQU  00000101B  ; รหัสเขียน DD RAM ของ LCD
 7  0081  CTRL_8255   .EQU  10000001B  ; รหัสกำหนดหน้าที่ของพอร์ทใน 8255
 8  0008  ADC_CON     .EQU  00001000B  ; รหัสสั่งให้ ADC แปลงสัญญาณ
 9  000A  ADC_READH   .EQU  00001010B  ; รหัสอ่านค่าดิจิตอล 8 บิตบนของ ADC
10  000B  ADC_READL   .EQU  00001011B  ; รหัสอ่านค่าดิจิตอล 4 บิตล่างของ ADC
11  0080  CK_MD1      .EQU  10000000B  ; รหัสเปิดสวิทช์ตรวจสอบ MODE 1
12  0081  CK_MD2      .EQU  10000001B  ; รหัสเปิดสวิทช์ตรวจสอบ MODE 2
13  0082  CK_MD3      .EQU  10000010B  ; รหัสเปิดสวิทช์ตรวจสอบ MODE 3
14  0080  CK_T1       .EQU  10000000B  ; รหัสเปิดสวิทช์ตรวจสอบ T1
15  0081  CK_T2       .EQU  10000001B  ; รหัสเปิดสวิทช์ตรวจสอบ T2
16  0082  CK_U1       .EQU  10000010B  ; รหัสเปิดสวิทช์ตรวจสอบ U1
17  0083  CK_U2       .EQU  10000011B  ; รหัสเปิดสวิทช์ตรวจสอบ U2
18  0084  CK_U3       .EQU  10000100B  ; รหัสเปิดสวิทช์ตรวจสอบ U3
19  0085  CK_U4       .EQU  10000101B  ; รหัสเปิดสวิทช์ตรวจสอบ U4
20  0086  CK_U5       .EQU  10000110B  ; รหัสเปิดสวิทช์ตรวจสอบ U5
21  0087  CK_U6       .EQU  10000111B  ; รหัสเปิดสวิทช์ตรวจสอบ U6
22  000C  OP_T1       .EQU  00001100B  ; รหัสเปิดสวิทช์เปิดช่องรับสัญญาณ T1
23  001C  OP_T2       .EQU  00011100B  ; รหัสเปิดสวิทช์เปิดช่องรับสัญญาณ T2
24  002C  OP_U1       .EQU  00101100B  ; รหัสเปิดสวิทช์เปิดช่องรับสัญญาณ U1
25  003C  OP_U2       .EQU  00111100B  ; รหัสเปิดสวิทช์เปิดช่องรับสัญญาณ U2
26  004C  OP_U3       .EQU  01001100B  ; รหัสเปิดสวิทช์เปิดช่องรับสัญญาณ U3
27  005C  OP_U4       .EQU  01011100B  ; รหัสเปิดสวิทช์เปิดช่องรับสัญญาณ U4
28  006C  OP_U5       .EQU  01101100B  ; รหัสเปิดสวิทช์เปิดช่องรับสัญญาณ U5
29  007C  OP_U6       .EQU  01111100B  ; รหัสเปิดสวิทช์เปิดช่องรับสัญญาณ U6
30  17FF  STK_TOP     .EQU  17FFH ; กำหนดตำแหน่งบนสุดของ STRACK
```

```
31                          ; ชุดคำสั่งหลัก
32  0000                    .ORG    0000H
33  0000   31 FF 17                 LD SP,STK_TOP ; กำหนด STRACK TOP
34  0003   C3 6E 00                 JP SETPORT
35                          ; กับดักสัญญาณ INTERRUPT ทุกชนิด
36  0008                    .ORG    0008H
37  0008   C3 69 00                 JP IGNORE
38  0010                    .ORG    0010H
39  0010   C3 69 00                 JP IGNORE
40  0018                    .ORG    0018H
41  0018   C3 69 00                 JP IGNORE
42  0020                    .ORG    0020H
43  0020   C3 69 00                 JP IGNORE
44  0028                    .ORG    0028H
45  0028   C3 69 00                 JP IGNORE
46  0030                    .ORG    0030H
47  0030   C3 69 00                 JP IGNORE
48                          ; สำหรับ INT MODEL
49  0038                    .ORG    0038H
50  0038   C3 6A 00                 JP IGNORI
51                          ; สำหรับ NMI MODEL
52  0066                    .ORG    0066H
53  0066   C3 6C 00                 JP IGNORN
54                          ; หยุดการ INTERRUPT ด้วยการสั่งย้อนกลับ (RETURN)
55  0069   C9              IGNORE:  RET
56  006A   ED 4D           IGNORI:  RETI
57  006C   ED 45           IGNORN:  RETN
58                          ; กำหนดให้ 8255 พอร์ท A เป็น OUTPUT    (MODE0)
59                          ;                พอร์ท B เป็น OUTPUT    (MODE0)
60                          ;                พอร์ท C บนเป็น OUTPUT (MODE0)
61                          ;                พอร์ท C ล่างเป็น INPUT    (MODE0)
62  006E   3E 81            SETPORT: LD A,CTRL_8255
63  0070   D3 03                     OUT (PORT_CTRL),A
64  0072   CD 76 0B                  CALL INITLCD ; ลบหน้าจอ LCD
65  0075   CD 97 0B                  CALL CLSLCD
66  0078   CD 10 0B                  CALL CLRDLCD
67  007B   3E 4D                     LD A,4DH ; ใส่รหัสแสดง "M"
68  007D   32 4F 10                  LD (DPLYDATA1),A
```

```
 69  0080  3E 3A          LD A,3AH ; ใส่รหัสแสดง ":"
 70  0082  32 51 10       LD (DPLYDATA1+2),A
 71  0085  3E 2E          LD A,2EH ; ใส่รหัสแสดง "."
 72  0087  32 5A 10       LD (DPLYDATA2+3),A
 73                ; ตรวจสอบ MODE โดยทดสอบบิต PC0 (0 เลือก,1 ไม่เลือก)
 74  008A  3E 80    CK_MD: LD A,CK_MD1
 75  008C  D3 01          OUT (PORT_B),A
 76  008E  CD BC 0B       CALL DELAY2
 77  0091  DB 02          IN A,(PORT_C)
 78  0093  CB 47          BIT 0,A
 79  0095  CA BC 00       JP Z,MODE1
 80  0098  3E 81          LD A,CK_MD2
 81  009A  D3 01          OUT (PORT_B),A
 82  009C  CD BC 0B       CALL DELAY2
 83  009F  DB 02          IN A,(PORT_C)
 84  00A1  CB 47          BIT 0,A
 85  00A3  CA 10 02       JP Z,MODE2
 86  00A6  3E 82          LD A,CK_MD3
 87  00A8  D3 01          OUT (PORT_B),A
 88  00AA  CD BC 0B       CALL DELAY2
 89  00AD  DB 02          IN A,(PORT_C)
 90  00AF  CB 47          BIT 0,A
 91  00B1  CA 1F 03       JP Z,MODE3
 92  00B4  21 E5 0B       LD HL,SMODE ; ถ้าไม่เลือกสวิทช์ MODE ให้
 93  00B7  CD 41 0B       CALL SCAN1 ; แสดง "SELECT MODE!!"
 94  00BA  18 CE          JR CK_MD
 95                ; ชุดคำสั่งย่อย "MODE 1"
 96  00BC  21 D5 0B MODE1: LD HL,MODE ; แสดงคำว่า "MODE 1"
 97  00BF  CD 41 0B       CALL SCAN1
 98  00C2  3E 42          LD A,42H ; ให้ตำแหน่ง 42 ของ LCD แสดงผล
 99  00C4  CD 60 0B       CALL GOTO
100  00C7  16 31          LD D,31H ; รหัสแสดง "1"
101  00C9  CD A3 0B       CALL WRBYTE
102  00CC  CD B7 05       CALL CK_CH ; ตรวจสอบการเลือกช่องสัญญาณ
103  00CF  CB 40          BIT 0,B ; ถ้าไม่เลือก T1 แสดง "ERROR"
104  00D1  C2 E8 00       JP NZ,M1_10 ; สลับกับ "SELECT T1"
105  00D4  21 F5 0B ERDPLY: LD HL,ERROR
106  00D7  CD 41 0B       CALL SCAN1
```

```
107  00DA  CD BC 0B          CALL DELAY2
108  00DD  21 05 0C          LD HL,T12
109  00E0  CD 41 0B          CALL SCAN1
110  00E3  CD BC 0B          CALL DELAY2
111  00E6  18 EC             JR ERDPLY
112  00E8  21 55 0C  M1_10:  LD HL,CHDT ; แสดง "CHOOSE Del_T"
113  00EB  CD 41 0B          CALL SCAN1
114  00EE  3E 45             LD A,45H ; ให้ตำแหน่ง 45 ของ LCD แสดงผล
115  00F0  CD 60 0B          CALL GOTO
116  00F3  16 54             LD D,54H ; รหัสแสดง "T"
117  00F5  CD A3 0B          CALL WRBYTE
118  00F8  CD BC 0B          CALL DELAY2
119  00FB  CD C3 03  M1_1:   CALL SET_DT1 ; รับค่า Del_T จากผู้ใช้
120  00FE  CD BC 0B          CALL DELAY2
121  0101  21 65 0C  M1_2:   LD HL,STB ; แสดง "STANDBY"
122  0104  CD 41 0B          CALL SCAN1
123  0107  CD 9F 0A  M1_3:    CALL SW3
124  010A  28 02              JR Z,M1_4
125  010C  18 F9              JR M1_3
126  010E  CD BC 0B  M1_4:   CALL DELAY2
127  0111  21 61 10          LD HL,REC_START ; ตำแหน่งเริ่มเก็บข้อมูล
128  0114  22 32 10          LD (REC_ADDR),HL
129  0117  21 00 00          LD HL,0000H
130  011A  22 34 10          LD (COUNT_NO),HL
131  011D  21 05 0C          LD HL,T12
132  0120  CD 41 0B          CALL SCAN1
133  0123  CD BC 0B          CALL DELAY2
134  0126  3E 31             LD A,31H ; รหัสแสดง "1"
135  0128  32 53 10          LD (DPLYDATA1+4),A
136  012B  32 50 10          LD (DPLYDATA1+1),A
137  012E  3E 54             LD A,54H ; รหัสแสดง "T"
138  0130  32 52 10          LD (DPLYDATA1+3),A
139  0133  3E 20             LD A,20H ; รหัสแสดง " "
140  0135  32 5D 10          LD (DPLYDATA2+6),A
141  0138  3E 4B             LD A,4BH ; รหัสแสดง "K"
142  013A  32 5E 10          LD (DPLYDATA2+7),A
143  013D  FD 21 3C 10  M1_5: LD IY,TEMP_1 ; รับค่าอุณหภูมิเริ่มต้น
144  0141  97                SUB A ; เริ่มเปิดช่องรับสัญญาณ T1
```

```
145  0142  D3 02          OUT (PORT_C),A
146  0144  3E 0C          LD A,OP_T1
147  0146  D3 01          OUT (PORT_B),A
148  0148  CD E3 0A       CALL RADC16 ; อ่านค่าความต่างศักย์จาก T1
149  014B  01 A5 0C       LD BC,N_TD1
150  014E  CD DF 04       CALL N_VT ; แปลงค่าความต่างศักย์เป็นอุณหภูมิ
151  0151  FD 75 00       LD (IY),L
152  0154  FD 74 01       LD (IY+1),H
153  0157  22 40 10       LD (H_BCD),HL
154  015A  CD 52 05       CALL HEX_BCD ; แปลงเลขฐาน 16 เป็นฐาน 10
155  015D  21 42 10       LD HL,H_BCD+2
156  0160  CD 87 09       CALL DPLY_VT ; แสดงค่าอุณหภูมิ T1
157  0163  CD 9F 0A       CALL SW3
158  0166  28 02          JR Z,M1_6
159  0168  18 D3          JR M1_5
160  016A  CD BC 0B  M1_6: CALL DELAY2
161  016D  21 15 0C       LD HL,REC
162  0170  CD 41 0B       CALL SCAN1
163  0173  2A 3C 10       LD HL,(TEMP_1)
164  0176  CD 00 10       CALL MEM_REC ; เริ่มบันทึกค่าสัญญาณที่เลือก
165  0179  FD 21 3E 10 M1_7: LD IY,TEMP_2 ; อ่านค่าอุณหภูมิเพื่อเปรียบเทียบ
166  017D  97             SUB A
167  017E  D3 02          OUT (PORT_C),A
168  0180  3E 0C          LD A,OP_T1
169  0182  D3 01          OUT (PORT_B),A
170  0184  CD E3 0A       CALL RADC16 ; อ่านค่าความต่างศักย์จาก T1
171  0187  01 A5 0C       LD BC,N_TD1
172  018A  CD DF 04       CALL N_VT ; แปลงค่าความต่างศักย์เป็นอุณหภูมิ
173  018D  FD 75 00       LD (IY),L
174  0190  FD 74 01       LD (IY+1),H
175  0193  22 40 10       LD (H_BCD),HL
176  0196  CD 52 05       CALL HEX_BCD ; แปลงค่าฐาน 16 เป็นฐาน 10
177  0199  21 42 10       LD HL,H_BCD+2
178  019C  CD 87 09       CALL DPLY_VT ; แสดงค่าอุณหภูมิ T1
179  019F  CD 9F 0A       CALL SW3
180  01A2  28 28          JR Z,M1_9
181  01A4  CD B9 0A       CALL SW4
182  01A7  C2 AD 01       JP NZ,M1_8
```

```
183  01AA  C3 01 01          JP M1_2
184  01AD  CD 81 05  M1_8:   CALL CP_T12 ; เปรียบเทียบอุณหภูมิ
185  01B0  38 C7             JR C,M1_7
186  01B2  21 15 0C          LD HL,REC
187  01B5  CD 41 0B          CALL SCAN1
188  01B8  2A 3E 10          LD HL,(TEMP_2)
189  01BB  E5                PUSH HL
190  01BC  CD 00 10          CALL MEM_REC ; บันทึกค่าสัญญาณที่เลือก
191  01BF  E1                POP HL
192  01C0  00                NOP
193  01C1  22 3C 10          LD (TEMP_1),HL
194  01C4  38 B3             JR C,M1_7
195  01C6  DD 21 01 01       LD IX,M1_2
196  01CA  18 06             JR DMF_TILL_SEL
197  01CC  DD 21 01 01  M1_9:LD IX,M1_2
198  01D0  18 0F             JR D_TILL_SEL
199                     ; ชุดคำสั่งย่อยแสดง "MEMORY FULL" จนกระทั่งกดสวิทช์
200  01D2  21 25 0C     DMF_TILL_SEL: LD HL,OL
201  01D5  CD 41 0B          CALL SCAN1
202  01D8  CD D3 0A          CALL SW34
203  01DB  CB 47             BIT 0,A
204  01DD  20 02             JR NZ,D_TILL_SEL
205  01DF  DD E9             JP (IX)
206                     ; ชุดคำสั่งย่อยแสดง "DISPLAY DATA" จนกระทั่งกดสวิทช์
207  01E1  CD BC 0B     D_TILL_SEL:  DELAY2
208  01E4  21 35 0C          LD HL,DPLY
209  01E7  CD 41 0B          CALL SCAN1
210  01EA  CD D3 0A          CALL SW34
211  01ED  CB 47             BIT 0,A
212  01EF  20 02             JR NZ,DO1
213  01F1  DD E9             JP (IX)
214  01F3  CD BC 0B  DO1:    CALL DELAY2
215  01F6  2A 36 10          LD HL,(COUNT_NO2)
216  01F9  22 34 10          LD (COUNT_NO),HL
217  01FC  21 61 10          LD HL,REC_START
218  01FF  22 32 10          LD (REC_ADDR),HL
219  0202  97                SUB A
220  0203  CD 19 10  DO2:    CALL MEM_DPLY ; แสดงค่าที่บันทึกไว้
```

```
221  0206  CB 57                    BIT 2,A
222  0208  28 F9                    JR Z,DO2
223  020A  CB 4F                    BIT 1,A
224  020C  20 E5                    JR NZ,DO1
225  020E  DD E9                    JP (IX)
226                 ; ชุดคำสั่งย่อย "MODE 2"
227  0210  21 D5 0B  MODE2:         LD HL,MODE ; แสดง "MODE 2"
228  0213  CD 41 0B                 CALL SCAN1
229  0216  3E 42                    LD A,42H ; ให้แสดงที่ตำแหน่ง 42 ของ LCD
230  0218  CD 60 0B                 CALL GOTO
231  021B  16 32                    LD D,32H ; รหัสแสดง "2"
232  021D  CD A3 0B                 CALL WRBYTE
233  0220  CD B7 05                 CALL CK_CH ; ตรวจสอบช่องรับสัญญาณ
234  0223  21 3C 10                 LD HL,TEMP_1
235  0226  70                       LD (HL),B
236  0227  21 55 0C                 LD HL,CHDT ; แสดง "CHOOSE Del_t"
237  022A  CD 41 0B                 CALL SCAN1
238  022D  3E 45                    LD A,45H ; ให้แสดงที่ตำแหน่ง 45 ของ LCD
239  022F  CD 60 0B                 CALL GOTO
240  0232  16 74                    LD D,74H ; รหัสแสดง "t"
241  0234  CD A3 0B                 CALL WRBYTE
242  0237  CD BC 0B                 CALL DELAY2
243  023A  3E 32                    LD A,32H ; รหัสแสดง "2"
244  023C  32 50 10                 LD (DPLYDATA1+1),A
245  023F  CD FB 03                 CALL SET_Dt ; รับค่า Del_t
246  0242  CD BC 0B                 CALL DELAY2
247  0245  3A 3E 10                 LD A,(TEMP_2) ; ปรับค่า Del_t ให้ตรงตามที่ตั้ง
248  0248  2A 3A 10                 LD HL,(N_D)
249  024B  0E 10                    LD C,10H
250  024D  32 3E 10  M2_7:          LD (TEMP_2),A
251  0250  91                       SUB C
252  0251  23                       INC HL
253  0252  30 F9                    JR NC,M2_7
254  0254  3A 3E 10                 LD A,(TEMP_2)
255  0257  FE 00                    CP 00H
256  0259  20 01                    JR NZ,M2_8
257  025B  2B                       DEC HL
258  025C  22 3A 10  M2_8:          LD (N_D),HL
```

```
259  025F   ED 5B 3A 10          LD DE,(N_D)
260  0263   2A 38 10             LD HL,(NUM_DATA)
261  0266   97                   SUB A
262  0267   ED 52                SBC HL,DE
263  0269   30 03                JR NC,M2_9
264  026B   21 00 00             LD HL,0000H
265  026E   22 38 10    M2_9:    LD (NUM_DATA),HL ; เก็บค่า Del_t ที่ปรับแล้ว
266  0271   21 65 0C    M2_1:    LD HL,STB ; แสดง "STANDBY"
267  0274   CD 41 0B             CALL SCAN1
268  0277   CD 9F 0A    M2_2:    CALL SW3
269  027A   28 02                JR Z,M2_3
270  027C   18 F9                JR M2_2
271  027E   CD BC 0B    M2_3:    CALL DELAY2
272  0281   21 61 10             LD HL,REC_START ; ตำแหน่งบันทึกเริ่มต้น
273  0284   22 32 10             LD (REC_ADDR),HL
274  0287   21 00 00             LD HL,0000H
275  028A   22 34 10             LD (COUNT_NO),HL
276  028D   21 15 0C    M2_4:    LD HL,REC
277  0290   CD 41 0B             CALL SCAN1
278  0293   21 3C 10             LD HL,TEMP_1
279  0296   46                   LD B,(HL)
280  0297   CB 40                BIT 0,B
281  0299   28 10                JR Z,M2_5
282  029B   97                   SUB A ; เปิดช่องรับสัญญาณ T1
283  29C    D3 02                OUT (PORT_C),A
284  029E   3E 0C                LD A,OP_T1
285  02A0   D3 01                OUT (PORT_B),A
286  02A2   CD E3 0A             CALL RADC16 ; อ่านค่าความต่างศักย์ T1
287  02A5   01 A5 0C             LD BC,N_TD1
288  02A8   CD DF 04             CALL N_VT ; แปลงค่าความต่างศักย์เป็นอุณหภูมิ
289  02AB   11 00 00    M2_5:    LD DE,0000H
290  02AE   ED 53 3A 10          LD (N_D),DE
291  02B2   97                   SUB A
292  02B3   32 3F 10             LD (TEMP_2+1),A
293  02B6   CD 00 10             CALL MEM_REC ; บันทึกค่าสัญญาณที่เลือกไว้
294  02B9   DD 21 71 02          LD IX,M2_1
295  02BD   D2 D2 01             JP NC,D_MF_TILL_SEL
296  02C0   3A 3F 10             LD A,(TEMP_2+1)
```

```
297  02C3  4F                  LD C,A
298  02C4  3A 3E 10            LD A,(TEMP_2)
299  02C7  81                  ADD A,C
300  02C8  27                  DAA
301  02C9  2A 3A 10            LD HL,(N_D)
302  02CC  0E 10               LD C,10H
303  02CE  32 3F 10  M2_10:    LD (TEMP_2+1),A
304  02D1  91                  SUB C
305  02D2  23                  INC HL
306  02D3  30 F9               JR NC,M2_10
307  02D5  3A 3F 10            LD A,(TEMP_2+1)
308  02D8  4F                  LD C,A
309  02D9  3E 0A               LD A,0AH
310  02DB  91                  SUB C
311  02DC  32 3F 10            LD (TEMP_2+1),A
312  02DF  22 3A 10            LD (N_D),HL
313  02E2  ED 5B 3A 10         LD DE,(N_D)
314  02E6  2A 38 10            LD HL,(NUM_DATA)
315  02E9  97                  SUB A
316  02EA  ED 52               SBC HL,DE
317  02EC  30 0B               JR NC,M2_14
318  02EE  21 00 00            LD HL,0000H
319  02F1  32 3F 10            LD (TEMP_2+1),A
320  02F4  CD 97 0B            CALL CLSLCD
321  02F7  18 0F               JR M2_13
322  02F9  CD 97 0B  M2_14:    CALL CLSLCD
323  02FC  7C                  LD A,H
324  02FD  B5                  OR L
325  02FE  28 08               JR Z,M2_13
326  0300  3E 0A               LD A,0AH
327  0302  CD 9E 04            CALL TIMER_SEL ; เข้าการหน่วงเวลา
328  0305  21 00 00            LD HL,0000H
329  0308  3A 3F 10  M2_13:    LD A,(TEMP_2+1)
330  030B  CD 9E 04            CALL TIMER_SEL ; เข้าการหน่วงเวลา
331  030E  CB 67               BIT 4,A
332  0310  CA 8D 02            JP Z,M2_4
333  0313  CB 5F               BIT 3,A
334  0315  CA 71 02            JP Z,M2_1
```

```
335  0318  DD 21 71 02  M2_6:      LD IX,M2_1
336  031C  C3 E1 01                JP D_TILL_SEL
337                     ; ชุดคำสั่งย่อย "MODE 3"
338  031F  21 D5 0B     MODE3:     LD HL,MODE ; แสดง "MODE 3"
339  0322  CD 41 0B                CALL SCAN1
340  0325  3E 42                   LD A,42H ; ให้แสดงที่ตำแหน่ง 42 ของ LCD
341  0327  CD 60 0B                CALL GOTO
342  032A  16 33                   LD D,33H ; รหัสแสดง "3"
343  032C  CD A3 0B                CALL WRBYTE
344  032F  CD BC 0B                CALL DELAY2
345  0332  CD BC 0B                CALL DELAY2
346  0335  3E 2C                   LD A,OP_U1 ; เปิดช่องสัญญาณ U1
347  0337  D3 01                   OUT (PORT_B),A
348  0339  3E 10                   LD A,00010000B
349  033B  D3 02                   OUT (PORT_C),A
350  033D  CD C9 0B                CALL DELAY3
351  0340  21 65 0C     M3_1:      LD HL,STB ; แสดง "STANDBY"
352  0343  CD 41 0B                CALL SCAN1
353  0346  CD AE 03     M3_2:      CALL DM3_2
354  0349  38 FB                   JR C,M3_2
355  034B  CD AE 03                CALL DM3_2
356  034E  38 F6                   JR C,M3_2
357  0350  CD C9 0B                CALL DELAY3 ; หน่วงเวลากัน DEBOUND
358  0353  11 00 00                LD DE,0000H
359  0356  CD 97 0B                CALL CLSLCD
360  0359  CD D4 04     M3_5:      CALL SEC_01
361  035C  13                      INC DE
362  035D  CD AE 03                CALL DM3_2
363  0360  30 FB                   JR C,M3_5
364  0362  21 27 00                LD HL,0027H ;ADD DELAY3
365  0365  19                      ADD HL,DE
366  0366  22 40 10                LD (H_BCD),HL
367  0369  CD 52 05                CALL HEX_BCD
368  036C  21 95 0C                LD HL,DM3 ; แสดงผลการจับเวลาที่ได้
369  036F  CD 41 0B                CALL SCAN1
370  0372  DD 21 43 10             LD IX,H_BCD+3
371  0376  21 55 10                LD HL,DPLYDATA1+6
372  0379  DD 56 00                LD D,(IX)
```

```
373  037C  CD 20 0B          CALL ASCII
374  037F  DD 2B             DEC IX
375  0381  DD 56 00          LD D,(IX)
376  0384  CD 20 0B          CALL ASCII
377  0387  21 54 10          LD HL,DPLYDATA1+5
378  038A  3E 40             LD A,40H ; ให้แสดงที่ตำแหน่ง 40 ของ LCD
379  038C  CD 60 0B          CALL GOTO
380  038F  CD A8 03          CALL DM3_1
381  0392  CD A8 03          CALL DM3_1
382  0395  3E 43             LD A,43H ; ให้แสดงที่ตำแหน่ง 43 ของ LCD
383  0397  CD 60 0B          CALL GOTO
384  039A  CD A8 03          CALL DM3_1
385  039D  CD A8 03          CALL DM3_1
386  03A0  CD 9F 0A  M3_6:   CALL SW3
387  03A3  CA 1F 03          JP Z,MODE3
388  03A6  18 F8             JR M3_6
389  03A8  23        DM3_1:  INC HL ; ชุดคำสั่งย่อยแสดงค่าสำหรับ MODE 3
390  03A9  56                LD D,(HL)
391  03AA  CD A3 0B          CALL WRBYTE
392  03AD  C9                RET
393  03AE  D5        DM3_2:  PUSH DE ; ชุดคำสั่งย่อยอ่านค่าสัญญาณและ
394  03AF  DB 08             IN A,(ADC_CON) ; ตรวจสอบสัญญาณ MODE3
395  03B1  06 10             LD B,10H
396  03B3  10 FE     M3_3:   DJNZ M3_3
397  03B5  DB 0A             IN A,(ADC_READH)
398  03B7  57                LD D,A
399  03B8  DB 0B             IN A,(ADC_READL)
400  03BA  5F                LD E,A
401  03BB  21 00 E0          LD HL,E000H
402  03BE  97                SUB A
403  03BF  ED 52             SBC HL,DE
404  03C1  D1                POP DE
405  03C2  C9                RET
406                  ; ชุดคำสั่งย่อยตั้งค่า "DELTA T"
407  03C3  21 75 0C  SET_DT1:  LD HL,DE_T
408  03C6  CD 41 0B          CALL SCAN1
409  03C9  3E 43     SET_DT11: LD A,43H ; ให้แสดงที่ตำแหน่ง 43 ของ LCD
410  03CB  CD 50 0A          CALL CYCLE ; แสดงค่า 0-9 สลับกันไป
```

```
411  03CE  97                    SUB A
412  03CF  BA                    CP D
413  03D0  38 F1                 JR C,SET_DT1
414  03D2  7B                    LD A,E
415  03D3  32 38 10              LD (NUM_DATA),A
416  03D6  3E 42                 LD A,42H ; ให้แสดงที่ตำแหน่ง 42 ของ LCD
417  03D8  CD 50 0A              CALL CYCLE ; แสดง 0-9 สลับกันไป
418  03DB  97                    SUB A
419  03DC  BA                    CP D
420  03DD  38 0F                 JR C,SET_DT12
421  03DF  7B                    LD A,E ; แปลงค่า Del_T ให้อยู่ในฐาน 16
422  3E0   87                    ADD A,A
423  03E1  47                    LD B,A
424  03E2  87                    ADD A,A
425  03E3  87                    ADD A,A
426  03E4  80                    ADD A,B
427  03E5  47                    LD B,A
428  03E6  3A 38 10              LD A,(NUM_DATA)
429  03E9  80                    ADD A,B
430  03EA  32 39 10              LD (NUM_DATA+1),A
431  03ED  C9                    RET
432  03EE  3E 42       SET_DT12: LD A,42H ; ให้แสดงที่ตำแหน่ง 42 ของ LCD
433  03F0  CD 60 0B              CALL GOTO
434  03F3  16 2A                 LD D,2AH ; รหัสแสดง "*"
435  03F5  CD A3 0B              CALL WRBYTE
436  03F8  C3 C9 03              JP SET_DT11
437                 ; ชุดคำสั่งย่อยตั้งค่า "DELTA t"
438  03FB  21 85 0C    SET_Dt:   LD HL,DE_t
439  03FE  CD 41 0B              CALL SCAN1
440  0401  21 44 10              LD HL,DIV_DATA-1
441  0404  06 05                 LD B,05H
442  0406  97                    SUB A
443  0407  23          SET_Dt1:  INC HL
444  0408  77                    LD (HL),A
445  0409  10 FC                 DJNZ SET_Dt1
446  040B  3E 45       SET_Dt2:  LD A,45H ; ให้แสดงที่ตำแหน่ง 45 ของ LCD
447  040D  CD 50 0A              CALL CYCLE ; แสดง 0-9 สลับกันไป
448  0410  97                    SUB A
```

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449  0411  BA                CP D
450  0412  DA FB 03          JP C,SET_Dt
451  0415  21 45 10          LD HL,DIV_DATA
452  0418  73                LD (HL),E
453  0419  3E 43    SET_Dt4:  LD A,43H ; ให้แสดงที่ตำแหน่ง 43 ของ LCD
454  041B  CD 50 0A          CALL CYCLE ; แสดง 0-9 สลับกันไป
455  041E  97                SUB A
456  041F  BA                CP D
457  0420  3E 43             LD A,43H
458  0422  DD 21 0B 04       LD IX,SET_Dt2
459  0426  38 5E             JR C,SET_Dt3
460  0428  23                INC HL
461  0429  73                LD (HL),E
462  042A  3E 42    SET_Dt5:  LD A,42H ; ให้แสดงที่ตำแหน่ง 42 ของ LCD
463  042C  CD 50 0A          CALL CYCLE ; แสดง 0-9 สลับกันไป
464  042F  97                SUB A
465  0430  BA                CP D
466  0431  3E 42             LD A,42H
467  0433  DD 21 19 04       LD IX,SET_Dt4
468  0437  38 4D             JR C,SET_Dt3
469  0439  23                INC HL
470  043A  73                LD (HL),E
471  043B  3E 41    SET_Dt6:  LD A,41H ; ให้แสดงที่ตำแหน่ง 41 ของ LCD
472  043D  CD 50 0A          CALL CYCLE ; แสดง 0-9 สลับกันไป
473  0440  97                SUB A
474  0441  BA                CP D
475  0442  3E 41             LD A,41H
476  0444  DD 21 2A 04       LD IX,SET_Dt5
477  0448  38 3C             JR C,SET_Dt3
478  044A  23                INC HL
479  044B  73                LD (HL),E
480  044C  3E 40             LD A,40H ; ให้แสดงที่ตำแหน่ง 40 ของ LCD
481  044E  CD 50 0A          CALL CYCLE ; แสดง 0-9 สลับกันไป
482  0451  97                SUB A
483  0452  BA                CP D
484  0453  3E 40             LD A,40H
485  0455  DD 21 3B 04       LD IX,SET_Dt6
486  0459  38 2B             JR C,SET_Dt3
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487  045B  23              INC HL
488  045C  73              LD (HL),E
489  045D  21 44 10        LD HL,DIV_DATA-1
490  0460  11 00 00        LD DE,0000H ; แปลงค่า Del_t เป็นฐาน 16
491  0463  01 01 00        LD BC,0001H
492  0466  CD 91 04        CALL G
493  0469  01 0A 00        LD BC,000AH
494  046C  CD 91 04        CALL G
495  046F  01 64 00        LD BC,0064H
496  0472  CD 91 04        CALL G
497  0475  01 E8 03        LD BC,03E8H
498  0478  CD 91 04        CALL G
499  047B  01 10 27        LD BC,2710H
500  047E  CD 91 04        CALL G
501  0481  ED 53 38 10     LD (NUM_DATA),DE
502  0485  C9              RET
503  0486  CD 60 0B  SET_Dt3:  CALL GOTO
504  0489  16 2A           LD D,2AH
505  048B  CD A3 0B        CALL WRBYTE
506  048E  2B              DEC HL
507  048F  DD E9           JP (IX)
508  0491  23        G:    INC HL ; ชุดคำสั่งย่อยแปลงค่า Del_t
509  0492  7E              LD A,(HL)
510  0493  FE 00           CP 0
511  0495  28 06           JR Z, G_END
512  0497  EB              EX DE,HL
513  0498  09        G1:   ADD HL,BC
514  0499  3D              DEC A
515  049A  20 FC           JR NZ,G1
516  049C  EB              EX DE,HL
517  049D  C9        G_END:  RET
518                   ; ชุดคำสั่งย่อยหน่วงเวลาสำหรับ MODE 2,3
519  049E  4F        TIMER_SEL:  LD C,A
520  049F  79        SEC_10:  LD A,C
521  04A0  47              LD B,A
522  04A1  CD 9F 0A        CALL SW3
523  04A4  28 21           JR Z,TS2
524  04A6  CD B9 0A        CALL SW4
```

```
525  04A9  28 21          JR Z,TS3
526  04AB  E5             PUSH HL
527  04AC  7C             LD A,H
528  04AD  B5             OR L
529  04AE  20 0A          JR NZ,TS4
530  04B0  E1             POP HL
531  04B1  97             SUB A
532  04B2  B8             CP B
533  04B3  30 1C          JR NC,TIMER_END
534  04B5  21 01 00       LD HL,0001H
535  04B8  18 01          JR TS1
536  04BA  E1       TS4:  POP HL
537  04BB  CD D4 04 TS1:  CALL SEC_01
538  04BE  10 FB          DJNZ TS1
539  04C0  2B             DEC HL
540  04C1  7C             LD A,H
541  04C2  B5             OR L
542  04C3  20 DA          JR NZ,SEC_10
543  04C5  18 0A          JR TIMER_END
544  04C7  CB DF    TS2:  SET 3,A
545  04C9  CB E7          SET 4,A
546  04CB  C9             RET
547  04CC  CB 9F    TS3:  RES 3,A
548  04CE  CB E7          SET 4,A
549  04D0  C9             RET
550  04D1  CB A7 TIMER_END: RES 4,A
551  04D3  C9             RET
552  04D4  C5       SEC_01: PUSH BC ; ชุดคำสั่งย่อย
553  04D5  01 FF 02       LD BC,02FFH ; หน่วงเวลา 0.01 วินาที
554  04D8  0B       SEC_011: DEC BC
555  04D9  78             LD A,B
556  04DA  B1             OR C
557  04DB  20 FB          JR NZ,SEC_011
558  04DD  C1             POP BC
559  04DE  C9             RET
560                  ; ชุดคำสั่งย่อยแปลงค่าดิจิตอลเป็นค่าอุณหภูมิและความต่างศักย์
561  04DF  D5       N_VT: PUSH DE
562  04E0  62             LD H,D
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```
563  04E1  6B                      LD L,E
564  04E2  CD 01 05                CALL HLXDE
565  04E5  ED 5B 4D 10             LD DE,(DIV_DATA+8)
566  04E9  CD FB 04                CALL BC_1XBCXDE
567  04EC  D1                      POP DE
568  04ED  E5            MULTI_N:  PUSH HL
569  04EE  CD FB 04                CALL BC_1XBCXDE
570  04F1  EB                      EX DE,HL
571  04F2  E1                      POP HL
572  04F3  19                      ADD HL,DE
573  04F4  0A            ADD_A1:   LD A,(BC)
574  04F5  57                      LD D,A
575  04F6  03                      INC BC
576  04F7  0A                      LD A,(BC)
577  04F8  5F                      LD E,A
578  04F9  19                      ADD HL,DE
579  04FA  C9                      RET
580  04FB  0A            BC_1XBCXDE: LD A,(BC)
581  04FC  67                      LD H,A
582  04FD  03                      INC BC
583  04FE  0A                      LD A,(BC)
584  04FF  6F                      LD L,A
585  0500  03                      INC BC
586  0501  ED 53 45 10   HLXDE:    LD (DIV_DATA),DE
587  0505  22 47 10                LD (DIV_DATA+2),HL
588  0508  CD 0F 05                CALL X
589  050B  2A 4D 10                LD HL,(DIV_DATA+8)
590  050E  C9                      RET
591  050F  D9            X:        EXX
592  0510  97                      SUB A
593  0511  21 49 10                LD HL,DIV_DATA+4
594  0514  06 06                   LD B,06H
595  0516  77            X1:       LD (HL),A
596  0517  23                      INC HL
597  0518  10 FC                   DJNZ X1
598  051A  06 10                   LD B,10H
599  051C  CD 2B 05      X2:       CALL XSLR
600  051F  CD 38 05                CALL XSLA
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601  0522  30 03          JR NC,X3
602  0524  CD 40 05       CALL B_R
603  0527  10 F3    X3:   DJNZ X2
604  0529  D9             EXX
605  052A  C9             RET
606  052B  97        XSLR: SUB A
607  052C  21 4A 10       LD HL,DIV_DATA+5
608  052F  0E 04          LD C,04H
609  0531  23        XSLR1: INC HL
610  0532  CB 16          RL (HL)
611  0534  0D             DEC C
612  0535  20 FA          JR NZ,XSLR1
613  0537  C9             RET
614  0538  97        XSLA: SUB A
615  0539  21 44 10       LD HL,DIV_DATA-1
616  053C  0E 02          LD C,02H
617  053E  18 F1          JR XSLR1
618  0540  97        B_R:  SUB A
619  0541  0E 04          LD C,04H
620  0543  21 4B 10       LD HL,DIV_DATA+6
621  0546  11 47 10       LD DE,DIV_DATA+2
622  0549  1A        B_R1: LD A,(DE)
623  054A  8E             ADC A,(HL)
624  054B  77             LD (HL),A
625  054C  23             INC HL
626  054D  13             INC DE
627  054E  0D             DEC C
628  054F  20 F8          JR NZ,B_R1
629  0551  C9             RET
630  0552  AF        HEX_BCD: XOR A ; ชุดคำสั่งย่อยแปลงฐาน 16 เป็นฐาน 10
631  0553  32 42 10       LD (H_BCD+2),A
632  0556  32 43 10       LD (H_BCD+3),A
633  0559  32 44 10       LD (H_BCD+4),A
634  055C  06 10          LD B,10H
635  055E  21 40 10  HEX_BCD1: LD HL,H_BCD
636  0561  CB 16          RL (HL)
637  0563  23             INC HL
638  0564  CB 16          RL (HL)
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```
639  0566  3A 42 10                    LD A,(H_BCD+2)
640  0569  8F                          ADC A,A
641  056A  27                          DAA
642  056B  32 42 10                    LD (H_BCD+2),A
643  056E  3A 43 10                    LD A,(H_BCD+3)
644  0571  8F                          ADC A,A
645  0572  27                          DAA
646  0573  32 43 10                    LD (H_BCD+3),A
647  0576  3A 44 10                    LD A,(H_BCD+4)
648  0579  8F                          ADC A,A
649  057A  27                          DAA
650  057B  32 44 10                    LD (H_BCD+4),A
651  057E  10 DE                       DJNZ HEX_BCD1
652  0580  C9                          RET
653                    ; ชุดคำสั่งย่อยเปรียบเทียบอุณหภูมิ
654  0581  ED 5B 3E 10  CP_T12:        LD DE,(TEMP_2)
655  0585  2A 3C 10                    LD HL,(TEMP_1)
656  0588  3A 39 10                    LD A,(NUM_DATA+1)
657  058B  4F                          LD C,A
658  058C  06 00                       LD B,00H
659  058E  3E 03                       LD A,03H
660  0590  CB 21        RL_BC:         SLA C
661  0592  CB 10                       RL B
662  0594  3D                          DEC A
663  0595  20 F9                       JR NZ,RL_BC
664  0597  3A 39 10                    LD A,(NUM_DATA+1)
665  059A  87                          ADD A,A
666  059B  81                          ADD A,C
667  059C  4F                          LD C,A
668  059D  3E 00                       LD A,00
669  059F  88                          ADC A,B
670  05A0  47                          LD B,A
671  05A1  97                          SUB A
672  05A2  ED 52                       SBC HL,DE
673  05A4  38 03                       JR C,CONV_HL_DE
674  05A6  ED 42                       SBC HL,BC
675  05A8  C9           CPEND:         RET
676  05A9  ED 5B 3C 10  CONV_HL_DE:    LD DE,(TEMP_1)
```

```
677  05AD  2A 3E 10          LD HL,(TEMP_2)
678  05B0  97                SUB A
679  05B1  ED 52             SBC HL,DE
680  05B3  ED 42             SBC HL,BC
681  05B5  18 F1             JR CPEND
682                ; ชุดคำสั่งย่อยตรวจช่องสัญญาณด้วย PC1(=0เลือก,=1ไม่เลือก)
683  05B7  21 00 00  CK_CH:  LD HL,0000H
684  05BA  22 3A 10          LD (N_D),HL
685  05BD  97                SUB A
686  05BE  32 3E 10          LD (TEMP_2),A
687  05C1  DD 21 00 10       LD IX,MEM_REC
688  05C5  FD 21 19 10       LD IY,MEM_DPLY
689  05C9  3E 80             LD A,CK_T1
690  05CB  D3 01             OUT (PORT_B),A ; ส่งรหัสตรวจสอบ T1
691  05CD  CD C9 0B          CALL DELAY3
692  05D0  DB 02             IN A,(PORT_C)
693  05D2  CB 4F             BIT 1,A
694  05D4  CB 80             RES 0,B
695  05D6  C2 EB 05          JP NZ,CK_CH2
696  05D9  CB C0             SET 0,B
697  05DB  11 18 07          LD DE,MT1
698  05DE  21 FD 07          LD HL,DT1
699  05E1  3E 02             LD A,02H
700  05E3  CD E9 06          CALL CK_CH1
701  05E6  3E 00             LD A,00H
702  05E8  32 3E 10          LD (TEMP_2),A
703  05EB  3E 81     CK_CH2: LD A,CK_T2
704  05ED  D3 01             OUT (PORT_B),A ; ส่งรหัสตรวจสอบ T2
705  05EF  CD C9 0B          CALL DELAY3
706  05F2  DB 02             IN A,(PORT_C)
707  05F4  CB 4F             BIT 1,A
708  05F6  C2 0E 06          JP NZ,CK_CH3
709  05F9  11 1E 07          LD DE,MT2
710  05FC  21 31 08          LD HL,DT2
711  05FF  3E 02             LD A,02H
712  0601  CD E9 06          CALL CK_CH1
713  0604  0E 00             LD C,00H
714  0606  3A 3E 10          LD A,(TEMP_2)
```

```
715  0609  81                ADD A,C
716  060A  27                DAA
717  060B  32 3E 10           LD (TEMP_2),A
718  060E  3E 82     CK_CH3:  LD A,CK_U1
719  0610  D3 01              OUT (PORT_B),A ; ส่งรหัสตรวจสอบ U1
720  0612  CD C9 0B           CALL DELAY3
721  0615  DB 02              IN A,(PORT_C)
722  0617  CB 4F              BIT 1,A
723  0619  C2 31 06           JP NZ,CK_CH4
724  061C  11 34 07           LD DE,MU1
725  061F  21 65 08           LD HL,DU1
726  0622  3E 01              LD A,01H
727  0624  CD E9 06           CALL CK_CH1
728  0627  0E 01              LD C,01H
729  0629  3A 3E 10           LD A,(TEMP_2)
730  062C  81                ADD A,C
731  062D  27                DAA
732  062E  32 3E 10           LD (TEMP_2),A
733  0631  3E 83     CK_CH4:  LD A,CK_U2
734  0633  D3 01              OUT (PORT_B),A ; ส่งรหัสตรวจสอบ U2
735  0635  CD C9 0B           CALL DELAY3
736  0638  DB 02              IN A,(PORT_C)
737  063A  CB 4F              BIT 1,A
738  063C  C2 54 06           JP NZ,CK_CH5
739  063F  11 38 07           LD DE,MU2
740  0642  21 88 08           LD HL,DU2
741  0645  3E 01              LD A,01H
742  0647  CD E9 06           CALL CK_CH1
743  064A  0E 01              LD C,01H
744  064C  3A 3E 10           LD A,(TEMP_2)
745  064F  81                ADD A,C
746  0650  27                DAA
747  0651  32 3E 10           LD (TEMP_2),A
748  0654  3E 84     CK_CH5:  LD A,CK_U3
749  0656  D3 01              OUT (PORT_B),A ; ส่งรหัสตรวจสอบ U3
750  0658  CD C9 0B           CALL DELAY3
751  065B  DB 02              IN A,(PORT_C)
752  065D  CB 4F              BIT 1,A
```

```
753  065F  C2 77 06          JP NZ,CK_CH6
754  0662  11 3C 07          LD DE,MU3
755  0665  21 AB 08          LD HL,DU3
756  0668  3E 01             LD A,01H
757  066A  CD E9 06          CALL CK_CH1
758  066D  0E 00             LD C,00H
759  066F  3A 3E 10          LD A,(TEMP_2)
760  0672  81                ADD A,C
761  0673  27                DAA
762  0674  32 3E 10          LD (TEMP_2),A
763  0677  3E 85    CK_CH6:  LD A,CK_U4
764  0679  D3 01             OUT (PORT_B),A ; ส่งรหัสตรวจสอบ U4
765  067B  CD C9 0B          CALL DELAY3
766  067E  DB 02             IN A,(PORT_C)
767  0680  CB 4F             BIT 1,A
768  0682  C2 9A 06          JP NZ,CK_CH7
769  0685  11 40 07          LD DE,MU4
770  0688  21 CD 08          LD HL,DU4
771  068B  3E 01             LD A,01H
772  068D  CD E9 06          CALL CK_CH1
773  0690  0E 00             LD C,00H
774  0692  3A 3E 10          LD A,(TEMP_2)
775  0695  81                ADD A,C
776  0696  27                DAA
777  0697  32 3E 10          LD (TEMP_2),A
778  069A  3E 86    CK_CH7:  LD A,CK_U5
779  069C  D3 01             OUT (PORT_B),A ; ส่งรหัสตรวจสอบ U5
780  069E  CD C9 0B          CALL DELAY3
781  06A1  DB 02             IN A,(PORT_C)
782  06A3  CB 4F             BIT 1,A
783  06A5  C2 BD 06          JP NZ,CK_CH8
784  06A8  11 44 07          LD DE,MU5
785  06AB  21 EF 08          LD HL,DU5
786  06AE  3E 01             LD A,01H
787  06B0  CD E9 06          CALL CK_CH1
788  06B3  0E 00             LD C,00H
789  06B5  3A 3E 10          LD A,(TEMP_2)
790  06B8  81                ADD A,C
```

```
791  06B9  27              DAA
792  06BA  32 3E 10        LD (TEMP_2),A
793  06BD  3E 87   CK_CH8: LD A,CK_U6
794  06BF  D3 01           OUT (PORT_B),A ; ส่งรหัสตรวจสอบ U6
795  06C1  CD C9 0B        CALL DELAY3
796  06C4  DB 02           IN A,(PORT_C)
797  06C6  CB 4F           BIT 1,A
798  06C8  C2 E0 06        JP NZ,CK_CH9
799  06CB  11 48 07        LD DE,MU6
800  06CE  21 11 09        LD HL,DU6
801  06D1  3E 01           LD A,01H
802  06D3  CD E9 06        CALL CK_CH1
803  06D6  0E 00           LD C,00H
804  06D8  3A 3E 10        LD A,(TEMP_2)
805  06DB  81              ADD A,C
806  06DC  27              DAA
807  06DD  32 3E 10        LD (TEMP_2),A
808  06E0  3E C9   CK_CH9: LD A,C9H
809  06E2  DD 77 00        LD (IX),A
810  06E5  FD 77 00        LD (IY),A
811  06E8  C9              RET
812  06E9  E5      CK_CH1: PUSH HL
813  06EA  2A 3A 10        LD HL,(N_D)
814  06ED  85              ADD A,L
815  06EE  6F              LD L,A
816  06EF  3E 00           LD A,00H
817  06F1  8C              ADC A,H
818  06F2  67              LD H,A
819  06F3  22 3A 10        LD (N_D),HL
820  06F6  E1              POP HL
821  06F7  3E CD           LD A,CDH
822  06F9  DD 77 00        LD (IX),A
823  06FC  FD 77 00        LD (IY),A
824  06FF  DD 73 01        LD (IX+1),E
825  0702  DD 72 02        LD (IX+2),D
826  0705  FD 75 01        LD (IY+1),L
827  0708  FD 74 02        LD (IY+2),H
828  070B  DD 23           INC IX
```

```
829  070D  DD 23          INC IX
830  070F  DD 23          INC IX
831  0711  FD 23          INC IY
832  0713  FD 23          INC IY
833  0715  FD 23          INC IY
834  0717  C9             RET
835                ; ชุดคำสั่งย่อยบันทึกค่าของสัญญาณที่อ่านได้ในหน่วยความจำ
836  0718  54       MT1:  LD D,H
837  0719  5D             LD E,L
838  071A  06 00           LD B,00H
839  071C  18 31           JR REC_NO_CMS
840  071E  97       MT2:  SUB A ; ส่งรหัสอ่านสัญญาณ T2
841  071F  D3 02           OUT (PORT_C),A
842  0721  3E 1C           LD A,OP_T2
843  0723  D3 01           OUT (PORT_B),A
844  0725  CD E3 0A        CALL RADC16
845  0728  01 AB 0C        LD BC,N_TD2
846  072B  CD DF 04        CALL N_VT
847  072E  54              LD D,H
848  072F  5D              LD E,L
849  0730  06 00           LD B,00H
850  0732  18 1B           JR REC_NO_CMS
851  0734  0E 2C    MU1:   LD C,OP_U1; ส่งรหัสอ่านสัญญาณ U1
852  0736  18 14           JR MV
853  0738  0E 3C    MU2:   LD C,OP_U2 ; ส่งรหัสอ่านสัญญาณ U2
854  073A  18 10           JR MV
855  073C  0E 4C    MU3:   LD C,OP_U3 ; ส่งรหัสอ่านสัญญาณ U3
856  073E  18 0C           JR MV
857  0740  0E 5C    MU4:   LD C,OP_U4 ; ส่งรหัสอ่านสัญญาณ U4
858  0742  18 08           JR MV
859  0744  0E 6C    MU5:   LD C,OP_U5 ; ส่งรหัสอ่านสัญญาณ U5
860  0746  18 04           JR MV
861  0748  0E 7C    MU6:   LD C,OP_U6 ; ส่งรหัสอ่านสัญญาณ U6
862  074A  18 00           JR MV
863  074C  CD 72 07  MV:   CALL RV ; ชุดคำสั่งย่อยอ่านค่าสัญญาณ
864  074F  2A 32 10  REC_NO_CMS: LD HL,(REC_ADDR)
865  0752  73              LD (HL),E
866  0753  23              INC HL
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```
867  0754   72                    LD (HL),D
868  0755   23                    INC HL
869  0756   70                    LD (HL),B
870  0757   23                    INC HL
871  0758   22 32 10              LD (REC_ADDR),HL
872  075B   ED 5B 34 10           LD DE,(COUNT_NO)
873  075F   13                    INC DE
874  0760   13                    INC DE
875  0761   13                    INC DE
876  0762   ED 53 34 10           LD (COUNT_NO),DE
877  0766   ED 53 36 10           LD (COUNT_NO2),DE
878  076A   ED 4B D3 0B           LD BC,(REC_END)
879  076E   97                    SUB A
880  076F   ED 42                 SBC HL,BC
881  0771   C9                    RET
882                  ; ชุดคำสั่งย่อยอ่านค่าความต่างศักย์
883  0772   3E 10        RV:     LD A,00010000B
884  0774   D3 02                OUT (PORT_C),A
885  0776   79                    LD A,C
886  0777   D3 01                OUT (PORT_B),A
887  0779   21 00 00              LD HL,0000H
888  077C   CD E3 0A              CALL RADC16
889  077F   06 01                 LD B,01H
890  0781   CD D4 04     RV3:     CALL SEC_01
891  0784   10 FB                 DJNZ RV3
892  0786   06 00                 LD B,00H
893  0788   3E F0                 LD A,F0H
894  078A   BB                    CP E
895  078B   20 6F                 JR NZ,RV_END2
896  078D   3E FF                 LD A,FFH
897  078F   BA                    CP D
898  0790   20 6A                 JR NZ,RV_END2
899  0792   3E F0                 LD A,F0H ; ส่งรหัสเปิดความต่างศักย์อ้างอิงขนาด
900  0794   A1                    AND C    ; 400 mV
901  795    4F                    LD C,A
902  0796   3E 03                 LD A,00000011B
903  0798   81                    ADD A,C
904  0799   D3 01                 OUT (PORT_B),A
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```
905  079B  CD E3 0A   CALL RADC16
906  079E  23         INC HL
907  079F  06 01      LD B,01H
908  07A1  3E F0      LD A,F0H
909  07A3  BB         CP E
910  07A4  20 38      JR NZ,RV_END
911  07A6  3E FF      LD A,FFH
912  07A8  BA         CP D
913  07A9  20 33      JR NZ,RV_END
914  07AB  3E 02      LD A,00000010B
915  07AD  81         ADD A,C ; ส่งรหัสเปิดความต่างศักย์อ้างอิงขนาด
916  07AE  D3 01      OUT (PORT_B),A ; 800 mV
917  07B0  CD E3 0A   CALL RADC16
918  07B3  23         INC HL
919  07B4  06 02      LD B,02H
920  07B6  3E F0      LD A,F0H
921  07B8  BB         CP E
922  07B9  20 23      JR NZ,RV_END
923  07BB  3E FF      LD A,FFH
924  07BD  BA         CP D
925  07BE  20 1E      JR NZ,RV_END
926  07C0  3E 01      LD A,00000001B
927  07C2  81         ADD A,C ; ส่งรหัสเปิดความต่างศักย์อ้างอิงขนาด
928  07C3  D3 01      OUT (PORT_B),A ; 1200 mV
929  07C5  CD E3 0A   CALL RADC16
930  07C8  23         INC HL
931  07C9  06 03      LD B,03H
932  07CB  3E F0      LD A,F0H
933  07CD  BB         CP E
934  07CE  20 0E      JR NZ,RV_END
935  07D0  3E FF      LD A,FFH
936  07D2  BA         CP D
937  07D3  20 09      JR NZ,RV_END
938  07D5  79         LD A,C ; ส่งรหัสเปิดความต่างศักย์อ้างอิงขนาด
939  07D6  D3 01      OUT (PORT_B),A ; 1600 mV
940  07D8  CD E3 0A   CALL RADC16
941  07DB  23         INC HL
942  07DC  06 04      LD B,04H
```

```
943  07DE  7D          RV_END:   LD A,L
944  07DF  D5          RV1:      PUSH DE
945  07E0  2A 3A 10              LD HL,(N_D)
946  07E3  11 01 00              LD DE,0001H
947  07E6  19                    ADD HL,DE
948  07E7  22 3A 10              LD (N_D),HL
949  07EA  C5                    PUSH BC
950  07EB  F5                    PUSH AF
951  07EC  3A 3F 10              LD A,(TEMP_2+1)
952  07EF  0E 07                 LD C,07H
953  07F1  81                    ADD A,C
954  07F2  27                    DAA
955  07F3  32 3F 10              LD (TEMP_2+1),A
956  07F6  F1                    POP AF
957  07F7  C1                    POP BC
958  07F8  D1                    POP DE
959  07F9  3D                    DEC A
960  07FA  20 E3                 JR NZ,RV1
961  07FC  C9          RV_END2:  RET
962                    ; ชุดคำสั่งย่อยแสดงค่าสัญญาณในหน่วยความจำ
963  07FD  CB 57       DT1:      BIT 2,A
964  07FF  28 01                 JR Z,DT1_1
965  0801  C9                    RET
966  0802  CD 97 0B    DT1_1:    CALL CLSLCD
967  0805  CD BC 0B              CALL DELAY2
968  0808  2A 32 10              LD HL,(REC_ADDR)
969  080B  F5                    PUSH AF
970  080C  3E 54                 LD A,54H ; รหัสแสดง "T"
971  080E  32 52 10              LD (DPLYDATA1+3),A
972  0811  3E 31                 LD A,31H ; รหัสแสดง "1"
973  0813  32 53 10              LD (DPLYDATA1+4),A
974  0816  3E 20                 LD A,20H ; รหัสแสดง " "
975  0818  32 5D 10              LD (DPLYDATA2+6),A
976  081B  3E 4B                 LD A,4BH ; รหัสแสดง "K"
977  081D  32 5E 10              LD (DPLYDATA2+7),A
978  0820  CD 75 09              CALL DPLY_T
979  0823  F1                    POP AF
980  0824  CD D3 0A              CALL SW34
```

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 981  0827  CB 47                    BIT 0,A
 982  0829  20 03                    JR NZ,DT1_2
 983  082B  C3 68 09                 JP CK_COUNT2
 984  082E  C3 40 09     DT1_2:      JP CK_COUNT
 985  0831  CB 57        DT2:        BIT 2,A
 986  0833  28 01                    JR Z,DT2_1
 987  0835  C9                       RET
 988  0836  CD 97 0B     DT2_1:      CALL CLSLCD
 989  0839  CD BC 0B                 CALL DELAY2
 990  083C  2A 32 10                 LD HL,(REC_ADDR)
 991  083F  F5                       PUSH AF
 992  0840  3E 54                    LD A,54H ; รหัสแสดง "T"
 993  0842  32 52 10                 LD (DPLYDATA1+3),A
 994  0845  3E 32                    LD A,32H ; รหัสแสดง "2"
 995  847   32 53 10                 LD (DPLYDATA1+4),A
 996  084A  3E 20                    LD A,20H ; รหัสแสดง " "
 997  084C  32 5D 10                 LD (DPLYDATA2+6),A
 998  084F  3E 4B                    LD A,4BH ; รหัสแสดง "K"
 999  0851  32 5E 10                 LD (DPLYDATA2+7),A
1000  0854  CD 75 09                 CALL DPLY_T
1001  0857  F1                       POP AF
1002  0858  CD D3 0A                 CALL SW34
1003  085B  CB 47                    BIT 0,A
1004  085D  20 03                    JR NZ,DT2_2
1005  085F  C3 68 09                 JP CK_COUNT2
1006  0862  C3 40 09     DT2_2:      JP CK_COUNT
1007  0865  CB 57        DU1:        BIT 2,A
1008  0867  28 01                    JR Z,DU1_1
1009  0869  C9                       RET
1010  086A  CD 97 0B     DU1_1:      CALL CLSLCD
1011  086D  CD BC 0B                 CALL DELAY2
1012  0870  F5                       PUSH AF
1013  0871  3E 55                    LD A,55H ; รหัสแสดง "U"
1014  0873  32 52 10                 LD (DPLYDATA1+3),A
1015  0876  3E 31                    LD A,31H ; รหัสแสดง "1"
1016  0878  32 53 10                 LD (DPLYDATA1+4),A
1017  087B  3E 6D                    LD A,6DH ; รหัสแสดง "m"
1018  087D  32 5D 10                 LD (DPLYDATA2+6),A
```

```
1019  0880  3E 56          LD A,56H ; รหัสแสดง “V”
1020  0882  32 5E 10       LD (DPLYDATA2+7),A
1021  0885  C3 33 09       JP DP_V
1022  0888  CB 57    DU2:  BIT 2,A
1023  088A  28 01          JR Z,DU2_1
1024  088C  C9             RET
1025  088D  CD 97 0B  DU2_1: CALL CLSLCD
1026  0890  CD BC 0B       CALL DELAY2
1027  0893  F5             PUSH AF
1028  0894  3E 55          LD A,55H ; รหัสแสดง “U”
1029  0896  32 52 10       LD (DPLYDATA1+3),A
1030  0899  3E 32          LD A,32H ; รหัสแสดง “2”
1031  089B  32 53 10       LD (DPLYDATA1+4),A
1032  089E  3E 6D          LD A,6DH ; รหัสแสดง “m”
1033  08A0  32 5D 10       LD (DPLYDATA2+6),A
1034  08A3  3E 56          LD A,56H ; รหัสแสดง “V”
1035  08A5  32 5E 10       LD (DPLYDATA2+7),A
1036  08A8  C3 33 09       JP DP_V
1037  08AB  CB 57    DU3:  BIT 2,A
1038  08AD  28 01          JR Z,DU3_1
1039  08AF  C9             RET
1040  08B0  CD 97 0B  DU3_1: CALL CLSLCD
1041  08B3  CD BC 0B       CALL DELAY2
1042  08B6  F5             PUSH AF
1043  08B7  3E 55          LD A,55H ; รหัสแสดง “U”
1044  08B9  32 52 10       LD (DPLYDATA1+3),A
1045  08BC  3E 33          LD A,33H ; รหัสแสดง “3”
1046  08BE  32 53 10       LD (DPLYDATA1+4),A
1047  08C1  3E 6D          LD A,6DH ; รหัสแสดง “m”
1048  08C3  32 5D 10       LD (DPLYDATA2+6),A
1049  08C6  3E 56          LD A,56H ; รหัสแสดง “V”
1050  08C8  32 5E 10       LD (DPLYDATA2+7),A
1051  08CB  18 66          JR DP_V
1052  08CD  CB 57    DU4:  BIT 2,A
1053  08CF  28 01          JR Z,DU4_1
1054  08D1  C9             RET
1055  08D2  CD 97 0B  DU4_1: CALL CLSLCD
1056  08D5  CD BC 0B       CALL DELAY2
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1057  08D8  F5           PUSH AF
1058  08D9  3E 55        LD A,55H ; รหัสแสดง “U”
1059  08DB  32 52 10     LD (DPLYDATA1+3),A
1060  08DE  3E 34        LD A,34H ; รหัสแสดง “4”
1061  08E0  32 53 10     LD (DPLYDATA1+4),A
1062  08E3  3E 6D        LD A,6DH ; รหัสแสดง “m”
1063  08E5  32 5D 10     LD (DPLYDATA2+6),A
1064  08E8  3E 56        LD A,56H ; รหัสแสดง “V”
1065  08EA  32 5E 10     LD (DPLYDATA2+7),A
1066  08ED  18 44        JR DP_V
1067  08EF  CB 57  DU5:  BIT 2,A
1068  08F1  28 01        JR Z,DU5_1
1069  08F3  C9           RET
1070  08F4  CD 97 0B  DU5_1:  CALL CLSLCD
1071  08F7  CD BC 0B     CALL DELAY2
1072  08FA  F5           PUSH AF
1073  08FB  3E 55        LD A,55H ; รหัสแสดง “U”
1074  08FD  32 52 10     LD (DPLYDATA1+3),A
1075  0900  3E 35        LD A,35H ; รหัสแสดง “5”
1076  0902  32 53 10     LD (DPLYDATA1+4),A
1077  0905  3E 6D        LD A,6DH ; รหัสแสดง “m”
1078  0907  32 5D 10     LD (DPLYDATA2+6),A
1079  090A  3E 56        LD A,56H ; รหัสแสดง “V”
1080  090C  32 5E 10     LD (DPLYDATA2+7),A
1081  090F  18 22        JR DP_V
1082  0911  CB 57  DU6:  BIT 2,A
1083  0913  28 01        JR Z,DU6_1
1084  0915  C9           RET
1085  0916  CD 97 0B  DU6_1:  CALL CLSLCD
1086  0919  CD BC 0B     CALL DELAY2
1087  091C  F5           PUSH AF
1088  091D  3E 55        LD A,55H ; รหัสแสดง “U”
1089  091F  32 52 10     LD (DPLYDATA1+3),A
1090  0922  3E 36        LD A,36H ; รหัสแสดง “6”
1091  0924  32 53 10     LD (DPLYDATA1+4),A
1092  0927  3E 6D        LD A,6DH ; รหัสแสดง “m”
1093  0929  32 5D 10     LD (DPLYDATA2+6),A
1094  092C  3E 56        LD A,56H ; รหัสแสดง “V”
```

```
1095  092E  32 5E 10          LD (DPLYDATA2+7),A
1096  0931  18 00             JR DP_V
1097  0933  CD DF 09  DP_V:   CALL DPLY_V ; ชุดคำสั่งย่อยแสดงผล
1098  0936  F1                POP AF
1099  0937  CD D3 0A          CALL SW34
1100  093A  CB 47             BIT 0,A
1101  093C  20 02             JR NZ,CK_COUNT
1102  093E  18 28             JR CK_COUNT2
1103  0940  CD BC 0B  CK_COUNT: CALL DELAY2
1104  0943  ED 5B 34 10       LD DE,(COUNT_NO)
1105  0947  1B                DEC DE
1106  0948  1B                DEC DE
1107  0949  1B                DEC DE
1108  094A  ED 53 34 10       LD (COUNT_NO),DE
1109  094E  3E FF             LD A,FFH
1110  0950  A3                AND E
1111  0951  20 1F             JR NZ,CKC_END
1112  0953  3E FF             LD A,FFH
1113  0955  A2                AND D
1114  0956  20 1A             JR NZ,CKC_END
1115  0958  CD BC 0B          CALL DELAY2
1116  095B  21 45 0C          LD HL,END
1117  095E  CD 41 0B          CALL SCAN1
1118  0961  CD D3 0A          CALL SW34
1119  0964  CB 47             BIT 0,A
1120  0966  20 05             JR NZ,CK_COUNT1
1121  0968  CB D7  CK_COUNT2: SET 2,A
1122  096A  CB 8F             RES 1,A
1123  096C  C9                RET
1124  096D  CB CF  CK_COUNT1: SET 1,A
1125  096F  CB D7             SET 2,A
1126  0971  C9                RET
1127  0972  CB 97  CKC_END:   RES 2,A
1128  0974  C9                RET
1129                  ; ชุดคำสั่งย่อยแสดงอุณหภูมิ
1130  0975  5E      DPLY_T:   LD E,(HL)
1131  0976  23                INC HL
1132  0977  56                LD D,(HL)
```

```
1133  0978  23              INC HL
1134  0979  23              INC HL
1135  097A  22 32 10        LD (REC_ADDR),HL
1136  097D  EB              EX DE,HL
1137  097E  22 40 10        LD (H_BCD),HL
1138  0981  CD 52 05        CALL HEX_BCD
1139  0984  21 42 10        LD HL,H_BCD+2
1140                  ; ชุดคำสั่งย่อยแสดงค่าความต่างศักย์
1141  0987  4E        DPLY_VT:  LD C,(HL)
1142  0988  23              INC HL
1143  0989  5E              LD E,(HL)
1144  098A  23              INC HL
1145  098B  56              LD D,(HL)
1146  098C  DD E5           PUSH IX
1147  098E  FD E5           PUSH IY
1148  0990  E5              PUSH HL
1149  0991  21 55 10        LD HL,DPLYDATA1+6
1150  0994  CD 20 0B        CALL ASCII
1151  0997  53              LD D,E
1152  0998  CD 20 0B        CALL ASCII
1153  099B  21 5F 10        LD HL,SDATA
1154  099E  51              LD D,C
1155  099F  CD 20 0B        CALL ASCII
1156  09A2  DD 21 5F 10     LD IX,SDATA
1157  09A6  FD 21 59 10     LD IY,DPLYDATA2+2
1158  09AA  DD 4E 00        LD C,(IX)
1159  09AD  FD 71 00        LD (IY),C
1160  09B0  DD 23           INC IX
1161  09B2  FD 23           INC IY
1162  09B4  FD 23           INC IY
1163  09B6  DD 4E 00        LD C,(IX)
1164  09B9  FD 71 00        LD (IY),C
1165  09BC  06 04           LD B,04H
1166  09BE  DD 21 55 10     LD IX,DPLYDATA1+6
1167  09C2  DD 4E 00  DPLY_TT4: LD C,(IX)
1168  09C5  3E 30           LD A,30H
1169  09C7  91              SUB C
1170  09C8  20 09           JR NZ,DPLY_TT1
```

```
1171  09CA  3E 20          LD A,20H
1172  09CC  DD 77 00       LD (IX),A
1173  09CF  DD 23          INC IX
1174  09D1  10 EF          DJNZ DPLY_TT4
1175  09D3  21 4F 10  DPLY_TT1:  LD HL,DPLYDATA1
1176  09D6  CD 41 0B       CALL SCAN1
1177  09D9  E1             POP HL
1178  09DA  FD E1          POP IY
1179  09DC  DD E1          POP IX
1180  09DE  C9             RET
1181  09DF  2A 32 10  DPLY_V:  LD HL,(REC_ADDR)
1182  09E2  5E             LD E,(HL)
1183  09E3  23             INC HL
1184  09E4  56             LD D,(HL)
1185  09E5  23             INC HL
1186  09E6  46             LD B,(HL)
1187  09E7  23             INC HL
1188  09E8  22 32 10       LD (REC_ADDR),HL
1189  09EB  3E 00          LD A,00H
1190  09ED  90             SUB B
1191  09EE  30 1C          JR NC,DPLY_V0
1192  09F0  3E 01          LD A,01H
1193  09F2  90             SUB B
1194  09F3  30 24          JR NC,DPLY_V1
1195  09F5  3E 02          LD A,02H
1196  09F7  90             SUB B
1197  09F8  30 2A          JR NC,DPLY_V2
1198  09FA  3E 03          LD A,03H
1199  09FC  90             SUB B
1200  09FD  30 30          JR NC,DPLY_V3
1201  09FF  21 A2 3F       LD HL,3FA2H
1202  0A02  97             SUB A
1203  0A03  BB             CP E
1204  0A04  20 34          JR NZ,DPLY_V4
1205  0A06  97             SUB A
1206  0A07  BA             CP D
1207  0A08  20 30          JR NZ,DPLY_V4
1208  0A0A  18 38          JR DPLY_V5
```

```
1209  0A0C  21 00 00     DPLY_V0:    LD HL,0000H
1210  0A0F  97                        SUB A
1211  0A10  BB                        CP E
1212  0A11  20 27                     JR NZ,DPLY_V4
1213  0A13  97                        SUB A
1214  0A14  BA                        CP D
1215  0A15  20 23                     JR NZ,DPLY_V4
1216  0A17  18 2B                     JR DPLY_V5
1217  0A19  21 FF 0F     DPLY_V1:    LD HL,0FFFH
1218  0A1C  97                        SUB A
1219  0A1D  BB                        CP E
1220  0A1E  20 1A                     JR NZ,DPLY_V4
1221  0A20  97                        SUB A
1222  0A21  BA                        CP D
1223  0A22  20 16                     JR NZ,DPLY_V4
1224  0A24  21 C7 1F     DPLY_V2:    LD HL,1FC7H
1225  0A27  97                        SUB A
1226  0A28  BB                        CP E
1227  0A29  20 0F                     JR NZ,DPLY_V4
1228  0A2B  97                        SUB A
1229  0A2C  BA                        CP D
1230  0A2D  20 0B                     JR NZ,DPLY_V4
1231  0A2F  21 BC 2F     DPLY_V3:    LD HL,2FBCH
1232  0A32  97                        SUB A
1233  0A33  BB                        CP E
1234  0A34  20 04                     JR NZ,DPLY_V4
1235  0A36  97                        SUB A
1236  0A37  BA                        CP D
1237  0A38  20 00                     JR NZ,DPLY_V4
1238  0A3A  E5           DPLY_V4:    PUSH HL
1239  0A3B  01 B1 0C                  LD BC,N_V
1240  0A3E  CD DF 04                  CALL N_VT
1241  0A41  EB                        EX DE,HL
1242  0A42  E1                        POP HL
1243  0A43  19                        ADD HL,DE
1244  0A44  22 40 10     DPLY_V5:    LD (H_BCD),HL
1245  0A47  CD 52 05                  CALL HEX_BCD
1246  0A4A  21 42 10                  LD HL,H_BCD+2
```

```
1247  0A4D  C3 87 09          JP DPLY_VT
1248                  ; ชุดคำสั่งย่อยแสดง0-9เก็บค่าในREG.Eและแสดงที่ตำแหน่งREG.A
1249  0A50  C5        CYCLE: PUSH BC
1250  0A51  16 FF            LD D,FFH
1251  0A53  1E 00            LD E,00H
1252  0A55  F5                PUSH AF
1253  0A56  CD 60 0B          CALL GOTO
1254  0A59  CD A3 0B          CALL WRBYTE
1255  0A5C  F1                POP AF
1256  0A5D  CD BC 0B          CALL DELAY2
1257  0A60  CD 9F 0A          CALL SW3
1258  0A63  20 0C             JR NZ,CYCLE3
1259  0A65  16 30             LD D,30H
1260  0A67  F5                PUSH AF
1261  0A68  CD 60 0B          CALL GOTO
1262  0A6B  CD A3 0B          CALL WRBYTE
1263  0A6E  F1                POP AF
1264  0A6F  18 2A             JR CYCLE_END
1265  0A71  CD B9 0A  CYCLE3: CALL SW4
1266  0A74  28 21             JR Z,CYCLE_END2
1267  0A76  1E FF     CYCLE2: LD E,FFH
1268  0A78  16 2F             LD D,2FH
1269  0A7A  06 0A             LD B,0AH
1270  0A7C  1C        CYCLE1: INC E
1271  0A7D  14                INC D
1272  0A7E  F5                PUSH AF
1273  0A7F  CD 60 0B          CALL GOTO
1274  0A82  CD A3 0B          CALL WRBYTE
1275  0A85  F1                POP AF
1276  0A86  CD BC 0B          CALL DELAY2
1277  0A89  CD 9F 0A          CALL SW3
1278  0A8C  28 0D             JR Z,CYCLE_END
1279  0A8E  CD B9 0A          CALL SW4
1280  0A91  28 04             JR Z,CYCLE_END2
1281  0A93  10 E7             DJNZ CYCLE1
1282  0A95  18 DF             JR CYCLE2
1283  0A97  16 08  CYCLE_END2: LD D,08H
1284  0A99  C1                POP BC
```

```
1285  0A9A  C9                    RET
1286  0A9B  16 00       CYCLE_END: LD D,00H
1287  0A9D  C1                    POP BC
1288  0A9E  C9                    RET
1289                    ; ชุดคำสั่งย่อยตรวจสอบSW3ถ้ากด(PC2=0)ถ้าไม่กด(PC2=1)
1290  0A9F  C5          SW3:      PUSH BC
1291  0AA0  0E 02                 LD C,PORT_C
1292  0AA2  ED 40                 IN B,(C)
1293  0AA4  CB 50                 BIT 2,B
1294  0AA6  28 02                 JR Z,SW31
1295  0AA8  C1          SW3END:   POP BC
1296  0AA9  C9                    RET
1297  0AAA  CD AC 0B    SW31:     CALL DLY ; ป้องกันการ DEBOUNCE
1298  0AAD  ED 40                 IN B,(C)
1299  0AAF  CB 50                 BIT 2,B
1300  0AB1  28 F5                 JR Z,SW3END
1301  0AB3  C1                    POP BC
1302  0AB4  CD AC 0B              CALL DLY ; ป้องกันการ DEBOUNCE
1303  0AB7  18 E6                 JR SW3
1304                    ; ชุดคำสั่งย่อยตรวจสอบSW4ถ้ากด(PC3=0)ถ้าไม่กด(PC3=1)
1305  0AB9  C5          SW4:      PUSH BC
1306  0ABA  0E 02                 LD C,PORT_C
1307  0ABC  ED 40                 IN B,(C)
1308  0ABE  CB 58                 BIT 3,B
1309  0AC0  28 02                 JR Z,SW41
1310  0AC2  C1          SW4END:   POP BC
1311  0AC3  C9                    RET
1312  0AC4  CD AC 0B    SW41:     CALL DLY ; ป้องกันการ DEBOUNCE
1313  0AC7  ED 40                 IN B,(C)
1314  0AC9  CB 58                 BIT 3,B
1315  0ACB  28 F5                 JR Z,SW4END
1316  0ACD  C1                    POP BC
1317  0ACE  CD AC 0B              CALL DLY ; ป้องกันการ DEBOUNCE
1318  0AD1  18 E6                 JR SW4
1319                    ; ชุดคำสั่งย่อยรับค่าการกดSW3(A.BIT0=1)และSW4(A.BIT0=0)
1320  0AD3  CD 9F 0A    SW34:     CALL SW3
1321  0AD6  20 03                 JR NZ,SW34_1
1322  0AD8  CB C7                 SET 0,A
```

```
1323  0ADA  C9              RET
1324  0ADB  CD B9 0A  SW34_1:  CALL SW4
1325  0ADE  20 F3           JR NZ,SW34
1326  0AE0  CB 87           RES 0,A
1327  0AE2  C9              RET
1328                        ; ชุดคำสั่งย่อยอ่านค่าจาก ADC 16 ครั้งไว้ใน RES. DE
1329  0AE3  F5        RADC16:  PUSH AF
1330  0AE4  C5                 PUSH BC
1331  0AE5  E5                 PUSH HL
1332  0AE6  06 C0              LD B,C0H
1333  0AE8  CD B5 0B  RADC164:  CALL DELAY1
1334  0AEB  10 FB              DJNZ RADC164
1335  0AED  21 00 00           LD HL,0000H
1336  0AF0  0E 10              LD C,10H
1337  0AF2  97        RADC161:  SUB A
1338  0AF3  DB 08              IN A,(ADC_CON)
1339  0AF5  06 10              LD B,10H
1340  0AF7  10 FE     RADC163:  DJNZ RADC163 ; หน่วงเวลา > 25 µs
1341  0AF9  DB 0A              IN A,(ADC_READH)
1342  0AFB  57                 LD D,A
1343  0AFC  DB 0B              IN A,(ADC_READL)
1344  0AFE  5F                 LD E,A
1345  0AFF  06 04              LD B,04H
1346  0B01  CB 3A     RADC162:  SRL D
1347  0B03  CB 1B               RR E
1348  0B05  10 FA               DJNZ RADC162
1349  0B07  19                  ADD HL,DE
1350  0B08  0D                  DEC C
1351  0B09  20 E7               JR NZ,RADC161
1352  0B0B  EB                  EX DE,HL
1353  0B0C  E1                  POP HL
1354  0B0D  C1                  POP BC
1355  0B0E  F1                  POP AF
1356  0B0F  C9                  RET
1357                        ; ชุดคำสั่งย่อยลบ DISPLAY DATA
1358  0B10  F5        CLRDLCD:  PUSH AF
1359  0B11  C5                  PUSH BC
1360  0B12  3E 20               LD A,20H
```

```
1361  0B14  21 4F 10          LD HL,DPLYDATA1
1362  0B17  06 10             LD B,10H
1363  0B19  77          CLRDLCD1:  LD (HL),A
1364  0B1A  23                INC HL
1365  0B1B  10 FC             DJNZ CLRDLCD1
1366  0B1D  C1                POP BC
1367  0B1E  F1                POP AF
1368  0B1F  C9                RET
1369                ; ชุดคำสั่งย่อยเปลี่ยนเลขHEXเป็นรหัสASCIIจากRES.Dเก็บที่(HL)
1370  0B20  C5          ASCII:     PUSH BC
1371  0B21  F5                PUSH AF
1372  0B22  0E 02              LD C,02H
1373  0B24  3E 00       ASCII2:    LD A,00H
1374  0B26  06 04              LD B,04H
1375  0B28  CB 22       ASCII1:    SLA D
1376  0B2A  17                 RLA
1377  0B2B  10 FB              DJNZ ASCII1
1378  0B2D  CD 38 0B           CALL HEXAS
1379  0B30  77                 LD (HL),A
1380  0B31  23                 INC HL
1381  0B32  0D                 DEC C
1382  0B33  20 EF              JR NZ,ASCII2
1383  0B35  F1                 POP AF
1384  0B36  C1                 POP BC
1385  0B37  C9                 RET
1386  0B38  C6 30       HEXAS:     ADD A,30H
1387  0B3A  FE 3A              CP 3AH
1388  0B3C  38 02              JR C,HEXAS1
1389  0B3E  C6 07              ADD A,07H
1390  0B40  C9          HEXAS1:    RET
1391                ; ชุดคำสั่งย่อยแสดงค่าจากตำแหน่งเริ่มต้น (HL) ทั้งแถว
1392  0B41  D5          SCAN1:     PUSH DE
1393  0B42  CD 76 0B           CALL INITLCD
1394  0B45  CD 97 0B           CALL CLSLCD
1395  0B48  CD 4D 0B           CALL WRP
1396  0B4B  D1                 POP DE
1397  0B4C  C9                 RET
1398  0B4D  F5          WRP:       PUSH AF
```

```
1399  0B4E  3E 00          LD A,00H
1400  0B50  CD 60 0B       CALL GOTO
1401  0B53  CD 6A 0B       CALL WRLINE
1402  0B56  3E 40          LD A,40H
1403  0B58  CD 60 0B       CALL GOTO
1404  0B5B  CD 6A 0B       CALL WRLINE
1405  0B5E  F1             POP AF
1406  0B5F  C9             RET
1407  0B60  CB FF    GOTO:  SET 7,A
1408  0B62  D3 00          OUT (PORT_A),A
1409  0B64  D3 04          OUT (LCD_CTRL),A
1410  0B66  CD B5 0B       CALL DELAY1
1411  0B69  C9             RET
1412  0B6A  C5       WRLINE: PUSH BC
1413  0B6B  06 08          LD B,08H
1414  0B6D  56       TEST11: LD D,(HL)
1415  0B6E  CD A3 0B       CALL WRBYTE
1416  0B71  23             INC HL
1417  0B72  10 F9          DJNZ TEST11
1418  0B74  C1             POP BC
1419  0B75  C9             RET
1420                 ; ชุดคำสั่งย่อยเริ่มต้นสั่งงาน LCD
1421  0B76  F5       INITLCD: PUSH AF
1422  0B77  3E 38          LD A,00111000B
1423  0B79  D3 00          OUT (PORT_A),A
1424  0B7B  D3 04          OUT (LCD_CTRL),A
1425  0B7D  CD B5 0B       CALL DELAY1
1426  0B80  CD B5 0B       CALL DELAY1 ; หน่วงเวลา > 4.1 ms
1427  0B83  3E 0C          LD A,00001100B
1428  0B85  D3 00          OUT (PORT_A),A
1429  0B87  D3 04          OUT (LCD_CTRL),A
1430  0B89  CD B5 0B       CALL DELAY1
1431  0B8C  3E 06          LD A,00000110B
1432  0B8E  D3 00          OUT (PORT_A),A
1433  0B90  D3 04          OUT (LCD_CTRL),A
1434  0B92  CD B5 0B       CALL DELAY1
1435  0B95  F1             POP AF
1436  0B96  C9             RET
```

```
1437  0B97  F5          CLSLCD:   PUSH AF
1438  0B98  3E 01                LD A,00000001B ; ลบ DISPLAY ทั้งหมด
1439  0B9A  D3 00                OUT (PORT_A),A
1440  0B9C  D3 04                OUT (LCD_CTRL),A
1441  0B9E  CD B5 0B             CALL DELAY1
1442  0BA1  F1                   POP AF
1443  0BA2  C9                   RET
1444                      ; ชุดคำสั่งย่อยเขียน BYTE
1445  0BA3  7A          WRBYTE:   LD A,D
1446  0BA4  D3 00                OUT (PORT_A),A
1447  0BA6  D3 05                OUT (LCD_WRI),A
1448  0BA8  CD B5 0B             CALL DELAY1
1449  0BAB  C9                   RET
1450                      ; ชุดคำสั่งย่อยหน่วงเวลา
1451  0BAC  C5          DLY:      PUSH BC
1452  0BAD  06 40                LD B,40H
1453  0BAF  00          DLY1:     NOP
1454  0BB0  00                   NOP
1455  0BB1  10 FC                DJNZ DLY1
1456  0BB3  C1                   POP BC
1457  0BB4  C9                   RET
1458                      ;
1459  0BB5  C5          DELAY1:   PUSH BC
1460  0BB6  06 80                LD B,80H
1461  0BB8  10 FE       DELAY12:  DJNZ DELAY12
1462  0BBA  C1                   POP BC
1463  0BBB  C9                   RET
1464                      ;
1465  0BBC  C5          DELAY2:   PUSH BC
1466  0BBD  06 FF                LD B,FFH
1467  0BBF  CD B5 0B    DELAY21:  CALL DELAY1
1468  0BC2  CD B5 0B             CALL DELAY1
1469  0BC5  10 F8                DJNZ DELAY21
1470  0BC7  C1                   POP BC
1471  0BC8  C9                   RET
1472                      ;
1473  0BC9  C5          DELAY3:   PUSH BC
1474  0BCA  06 FF                LD B,FFH
```

```
1475  0BCC  CD B5 0B      DELAY31:    CALL DELAY1
1476  0BCF  10 FB                    DJNZ DELAY31
1477  0BD1  C1                       POP BC
1478  0BD2  C9                       RET
1479                      ;
1480                      ; พื้นที่หน่วยความจำ ROM
1481  0BD3  5017                REC_END     .DEFW  1750H
1482  0BD5  3D 3D 3D 3D 20      MODE        .DB    "==== MODE   ===="
      0BDA  4D 4F 44 45 20
      0BDF  20 20 3D 3D 3D
      0BE4  3D
1483  0BE5  20 53 45 4C 45      SMODE       .DB    " SELECT MODE !! "
      0BEA  43 54 20 4D 4F
      0BEF  44 45 20 21 21
      0BF4  20
1484  0BF5  3C 3C 3C 3C 20      ERROR       .DB    "<<<< ERROR >>>>>"
      0BFA  45 52 52 4F 52
      0BFF  20 3E 3E 3E 3E
      0C04  3E
1485  0C05  3C 3C 20 20 53      T12         .DB    "<<  SELECT T1 >>"
      0C0A  45 4C 45 43 54
      0C0F  20 54 31 20 3E
      0C14  3E
1486  0C15  3C 3C 3C 20 52      REC         .DB    "<<< RECORDED >>>"
      0C1A  45 43 4F 52 44
      0C1F  45 44 20 3E 3E
      0C24  3E
1487  0C25  3C 20 4D 45 4D      OL          .DB    "< MEMORY FULL  >"
      0C2A  4F 52 59 20 46
      0C2F  55 4C 4C 20 20
      0C34  3E
1488  0C35  3C 20 44 49 53      DPLY        .DB    "< DISPLAY DATA >"
      0C3A  50 4C 41 59 20
      0C3F  44 41 54 41 20
      0C44  3E
1489  0C45  3C 20 20 45 4E      END         .DB    "<  END OF DATA >"
      0C4A  44 20 4F 46 20
      0C4F  44 41 54 41 20
```

```
        0C54   3E
1490    0C55   20 20 43 48 4F      CHDT        .DB   "  CHOOSE Del_  ?"
        0C5A   4F 53 45 20 44
        0C5F   65 6C 5F 20 20
        0C64   3F
1491    0C65   23 23 23 20 20      STB         .DB   "###  STANDBY ###"
        0C6A   53 54 41 4E 44
        0C6F   42 59 20 23 23
        0C74   23
1492    0C75   20 20 44 65 6C      DE_T        .DB   "  Del-T = ** K  "
        0C7A   2D 54 20 3D 20
        0C7F   2A 2A 20 4B 20
        0C84   20
1493    0C85   44 65 6C 2D 74      DE_t        .DB   "Del-t = ****.* s"
        0C8A   20 3D 20 2A 2A
        0C8F   2A 2A 2E 2A 20
        0C94   73
1494    0C95   4D 33 3A 20 74      DM3         .DB   "M3: t =   .   s "
        0C9A   20 3D 20 20 20
        0C9F   2E 20 20 20 73
        0CA4   20
1495    0CA5   01 B3 0A 16 03      N_TD1       .DEFB  01H,B3H,0AH,16H,03H,02H
        0CAA   02
1496    0CAB   01 B3 0A 16 02      N_TD2       .DEFB  01H,B3H,0AH,16H,02H,C0H
        0CB0   C0
1497    0CB1   00 00 0F 7A 00      N_V         .DEFB  00H,00H,0FH,7AH,00H,0CH
        0CB6   0C
```

```
1498                    ; พื้นที่หน่วยความจำ RAM
1499    1000            .ORG    1000H
1500    1000   CD 18 07 MEM_REC:     CALL MT1
1501    1003   CD 1E 07              CALL MT2
1502    1006   CD 34 07              CALL MU1
1503    1009   CD 38 07              CALL MU2
1504    100C   CD 3C 07              CALL MU3
1505    100F   CD 40 07              CALL MU4
1506    1012   CD 44 07              CALL MU5
```

```
1507  1015  CD 48 07                    CALL MU6
1508  1018  C9                          RET
1509  1019  CD FD 07      MEM_DPLY:     CALL DT1
1510  101C  CD 31 08                    CALL DT2
1511  101F  CD 65 08                    CALL DU1
1512  1022  CD 88 08                    CALL DU2
1513  1025  CD AB 08                    CALL DU3
1514  1028  CD CD 08                    CALL DU4
1515  102B  CD EF 08                    CALL DU5
1516  102E  CD 11 09                    CALL DU6
1517  1031  C9                          RET
1518  1032  0000              REC_ADDR    .DEFW  0000H
1519  1034  0000              COUNT_NO    .DEFW  0000H
1520  1036  0000              COUNT_NO2   .DEFW  0000H
1521  1038  0000              NUM_DATA    .DEFW  0000H
1522  103A  0000              N_D         .DEFW  0000H
1523  103C  0000              TEMP_1      .DEFW  0000H
1524  103E  0000              TEMP_2      .DEFW  0000H
1525  1040  00 00 00 00 00    H_BCD       .DEFB  00H,00H,00H,00H,00H
1526  1045  00 00 00 00 00    DIV_DATA    .DEFB  00H,00H,00H,00H,00H,00H,
      104A  00 00 00 00 00                       00H,00H,00H,00H
1527  104F  0000 0000 0000    DPLYDATA1   .DEFW  0000H,0000H,0000H,0000H
      1055  0000
1528  1057  0000 0000 0000    DPLYDATA2   .DEFW  0000H,0000H,0000H,0000H
      105D  0000
1529  105F  0000              SDATA       .DEFW  0000H
1530  1061  00          REC_START:  NOP   ; กำหนดตำแหน่ง REC_START
```


ประวัติผู้เขียน

นายมนต์เทียน เทียนประทีป เกิดวันที่ 14 เมษายน พ.ศ. 2513 สำเร็จการศึกษาระดับปริญญาตรีวิทยาศาสตรบัณฑิต สาขาวิชาฟิสิกส์ ภาควิชาฟิสิกส์ คณะวิทยาศาสตร์ จุฬาลงกรณ์มหาวิทยาลัย ในปีการศึกษา 2535 แล้วเข้าศึกษาต่อในหลักสูตรวิทยาศาสตรมหาบัณฑิต สาขาวิชาฟิสิกส์ ที่ภาควิชาฟิสิกส์ คณะวิทยาศาสตร์ จุฬาลงกรณ์มหาวิทยาลัย เมื่อปีการศึกษา 2536