เอกสารอ้างอิง

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ภาคผนวก ก

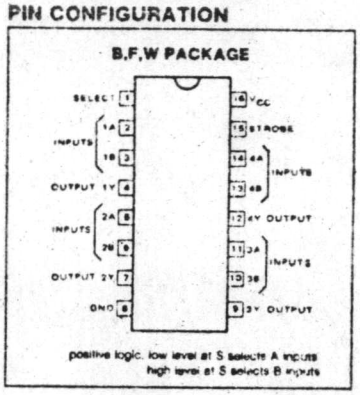
รายละเอียดของไอซีต่าง ๆ ที่ใช้ในวงจร

QUAD 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER (NON-INV.) 54/74157

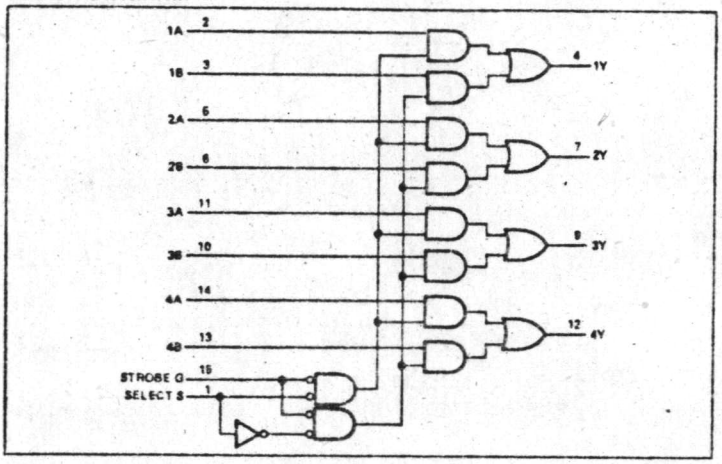
SPEED/PACKAGE AVAILABILITY

54	F,W	74	B,F
54LS	F,W	74LS	B,F
54S	F,W	74S	B,F

PIN CONFIGURATION



BLOCK DIAGRAM



TRUTH TABLE

INPUTS				OUTPUT Y
STROBE	SELECT	A	B	
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

H = high level, L = low level, X = irrelevant

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS				54/74 C_L = 15pF, R_L = 400Ω			54/74LS C_L = 15pF, R_L = 2kΩ			54/74S C_L = 15pF, R_L = 280Ω			
PARAMETER		FROM INPUT	TO OUTPUT	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
Propagation delay time													
t_{PLH}	Low-to-high	Data	Any		9	14		9	14		5	7.5	ns
t_{PHL}	High-to-low				9	14		9	14		4.5	6.5	
t_{PLH}	Low-to-high	Enable	Any		13	20							
t_{PHL}	High-to-low				14	21							
t_{PLH}	Low-to-high	Select	Any		15	23		15	23		9.5	15	
t_{PHL}	High-to-low				18	27		8	27		9.5	15	
t_{PLH}	Low-to-high	Strobe	Any					13	20		8.5	12.5	
t_{PHL}	High-to-low							14	21		7.5	12	

Load circuit and typical waveforms are shown at the front of section.

QUAD D-TYPE EDGE-TRIGGERED FLIP-FLOP 54/74175

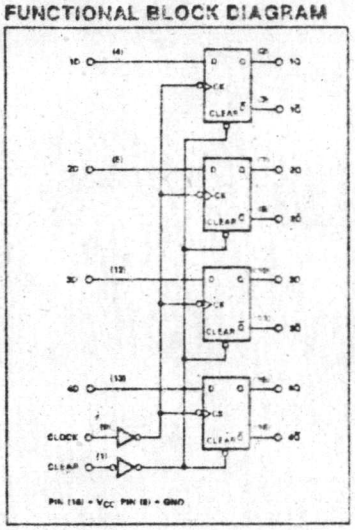
SPEED/PACKAGE AVAILABILITY

54	F,W	74	B
54LS	F,W	74LS	B
		74S	B

DESCRIPTION

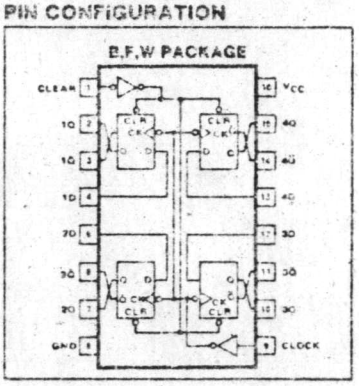
Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION

B,F,W PACKAGE



TRUTH TABLE (EACH FLIP-FLOP)

INPUTS			OUTPUTS	
CLEAR	CLOCK	D	Q	$\overline{Q}$
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q}_0$

H = high level (steady state)
L = low level (steady state)
X = irrelevant
↑ = transition from low to high level
Q_0 = the level of Q before the indicated steady-state input conditions were established

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS				54/74 C_L = 15pF, R_L = 400Ω			54/74LS C_L = 15pF, R_L = 2kΩ			54/74S C_L = 15pF, R_L = 280Ω			
PARAMETER		FROM INPUT	TO OUTPUT	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
f_{Clock}	Clock frequency			25	35		30	40		75	110		MHz
t_w	Width of pulse Clock			20			20			12			ns
	Clear												
t_{Setup}	Input setup time Data			20			20			8			ns
	Clear inactive			25			25			15			
t_{Hold}	Input hold time			0			5			2			ns
Propagation delay time													
t_{PLH}	Low-to-high	Clear			16	25		16	25				ns
t_{PHL}	High-to-low				23	35		23	35				
t_{PLH}	Low-to-high	Clock			20	30		20	30		9	12	
t_{PHL}	High-to-low				21	30		21	35		11	17	
t_{PLH}	Low-to-high	Clear	$\overline{Q}$								13	15	
t_{PHL}	High-to-low	Clear	Q								13	22	

Load circuit and typical waveforms are shown at the front of section.

intel

2102A, 2102AL

1K (1K x 1) STATIC RAM

P/N	Standby Pwr. (mW)	Operating Pwr. (mW)	Access (ns)
2102AL-4	35	174	450
2102AL	35	174	350
2102AL-2	42	342	250
2102A-2	—	342	250
2102A	—	289	350
2102A-4	—	289	450
2102A-6	—	289	650

- Single +5 Volts Supply Voltage
- Directly TTL Compatible: All Inputs and Output
- Standby Power Mode (2102AL)
- Three-State Output: OR-Tie Capability
- Inputs Protected: All Inputs Have Protection Against Static Charge
- Low Cost Packaging: 16 Pin Dual-In-Line Configuration

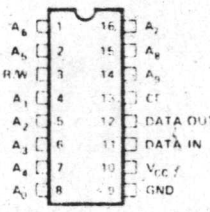
The Intel® 2102A is a high speed 1024 word by one bit static random access memory element using N-channel MOS devices integrated on a monolithic array. It uses fully DC stable (static) circuitry and therefore requires no clocks or refreshing to operated. The data is read out nondestructively and has the same polarity as the input data.

The 2102A is designed for memory applications where high performance, low cost, large bit storage, and simple interfacing are important design objectives. *A low standby power version (2102AL) is also available. It has all the same operating characteristics of the 2102A with the added feature of 35mW maximum power dissipation in standby and 174mW in operations.*

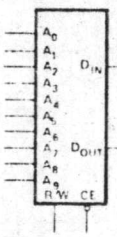
It is directly TTL compatible in all respects: inputs, output, and a single +5 volt supply. A separate chip enable ($\overline{CE}$) lead allows easy selection of an individual package when outputs are OR-tied.

The Intel® 2102A is fabricated with N-channel silicon gate technology. This technology allows the design and production of high performance easy to use MOS circuits and provides a higher functional density on a monolithic chip than either conventional MOS technology or P-channel silicon gate technology.

PIN CONFIGURATION



LOGIC SYMBOL



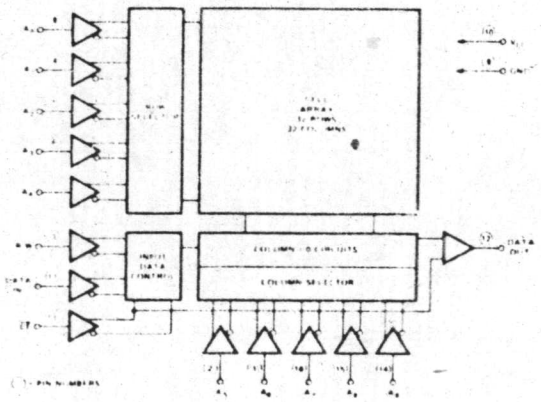
PIN NAMES

D_{IN}	DATA INPUT
A_0-A_9	ADDRESS INPUTS
R/$\overline{W}$	READ/WRITE INPUT
$\overline{CE}$	CHIP ENABLE
D_{OUT}	DATA OUTPUT
V_{CC}	POWER (+5V)

TRUTH TABLE

$\overline{CE}$	R/W	D_{IN}	D_{OUT}	MODE
H	X	X	HIGH Z	NOT SELECTED
L	L	L	L	WRITE "0"
L	L	H	H	WRITE "1"
L	H	X	D_{OUT}	READ

BLOCK DIAGRAM



Absolute Maximum Ratings*

Ambient Temperature Under Bias	−10°C to 80°C
Storage Temperature	−65°C to +150°C
Voltage On Any Pin With Respect To Ground	−0.5V to +7V
Power Dissipation	1 Watt

*COMMENT:

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D. C. and Operating Characteristics

T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified.

Symbol	Parameter	2102A, 2102A-4, 2102AL, 2102AL-4 Limits Min.	Typ.[1]	Max.	2102A-2, 2102AL-2 Limits Min.	Typ.[1]	Max.	2101A-6 Limits Min.	Typ.[1]	Max.	Unit	Test Conditions
I_{LI}	Input Load Current		1	10		1	10		1	10	µA	V_{IN} = 0 to 5.25V
I_{LOH}	Output Leakage Current		1	5		1	5		1	5	µA	$\overline{CE}$ = 2.0V, V_{OUT} = V_{OH}
I_{LOL}	Output Leakage Current		-1	-10		-1	-10		-1	-10	µA	$\overline{CE}$ = 2.0V, V_{OUT} = 0.4V
I_{CC}	Power Supply Current		33	Note 2		45	65		33	55	mA	All Inputs = 5.25V, Data Out Open, T_A = 0°C
V_{IL}	Input Low Voltage	-0.5		0.8	-0.5		0.8	-0.5		0.65	V	
V_{IH}	Input High Voltage	2.0		V_{CC}	2.0		V_{CC}	2.2		V_{CC}	V	
V_{OL}	Output Low Voltage			0.4			0.4			0.45	V	I_{OL} = 2.1mA
V_{OH}	Output High Voltage	2.4			2.4			2.2			V	I_{OH} = -100µA

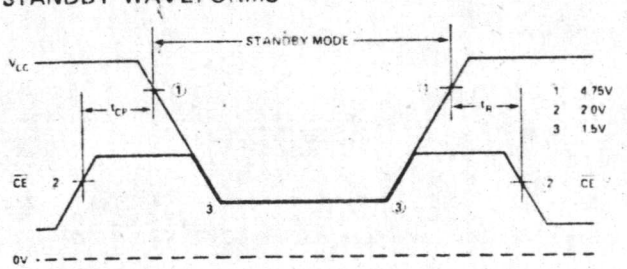
Notes: 1. Typical values are for T_A = 25°C and nominal supply voltage.
2. The maximum I_{CC} value is 55mA for the 2102A and 2102A-4, and 33mA for the 2102AL and 2102AL-4.

Standby Characteristics 2102AL, 2102AL-2, and 2102AL-4

T_A = 0°C to 70°C

Symbol	Parameter	2102AL, 2102AL-4 Limits Min.	Typ.[1]	Max.	2102AL-2 Limits Min.	Typ.[1]	Max.	Unit	Test Conditions
V_{PD}	V_{CC} in Standby	1.5			1.5			V	
V_{CES}[2]	$\overline{CE}$ Bias in Standby	2.0			2.0			V	2.0V ≤ V_{PD} ≤ V_{CC} Max.
		V_{PD}			V_{PD}			V	1.5V ≤ V_{PD} < 2.0V
I_{PD1}	Standby Current		15	23		20	28	mA	All Inputs = V_{PD1} = 1.5V
I_{PD2}	Standby Current		20	30		25	38	mA	All Inputs = V_{PD2} = 2.0V
t_{CP}	Chip Deselect to Standby Time	0			0			ns	
t_R[3]	Standby Recovery Time	t_{RC}			t_{RC}			ns	

STANDBY WAVEFORMS



NOTES:
1. Typical values are for T_A = 25°C.
2. Consider the test conditions as shown: If the standby voltage (V_{PD}) is between 5.25V (V_{CC} Max.) and 2.0V, then $\overline{CE}$ must be held at 2.0V Min. (V_{IH}). If the standby voltage is less than 2.0V but greater than 1.5V (V_{PD} Min.), then $\overline{CE}$ and standby voltage must be at least the same value or, if they are different, $\overline{CE}$ must be the more positive of the two.
3. t_R = t_{RC} (READ CYCLE TIME)

A. C. Characteristics T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified

READ CYCLE

Symbol	Parameter	2102A-2, 2102AL-2 Limits (ns) Min.	Max.	2102A, 2102AL Limits (ns) Min.	Max.	2102A-4, 2102AL-4 Limits (ns) Min.	Max.	2102A-6 Limits (ns) Min.	Max.
t_{RC}	Read Cycle	250		350		450		650	
t_A	Access Time		250		350		450		650
t_{CO}	Chip Enable to Output Time		130		180		230		400
t_{OH1}	Previous Read Data Valid with Respect to Address	40		40		40		50	
t_{OH2}	Previous Read Data Valid with Respect to Chip Enable	0		0		0		0	

WRITE CYCLE

t_{WC}	Write Cycle	250	350	450	650
t_{AW}	Address to Write Setup Time	20	20	20	200
t_{WP}	Write Pulse Width	180	250	300	400
t_{WR}	Write Recovery Time	0	0	0	50
t_{DW}	Data Setup Time	180	250	300	450
t_{DH}	Data Hold Time	0	0	0	20
t_{CW}	Chip Enable to Write Setup Time	180	250	300	550

A. C. CONDITIONS OF TEST

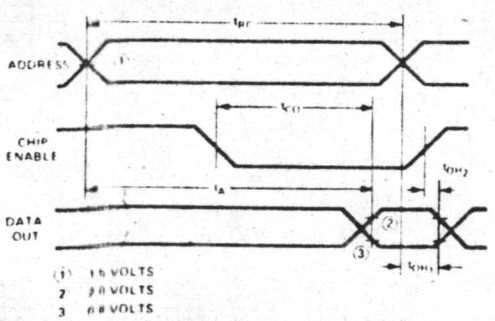
Input Pulse Levels		0.8 Volt to 2.0 Volt
Input Rise and Fall Times		10nsec
Timing Measurement Reference Levels	Inputs:	1.5 Volts
	Output:	0.8 and 2.0 Volts
Output Load		1 TTL Gate and C_L = 100 pF

Capacitance [2] T_A = 25°C, f = 1MHz

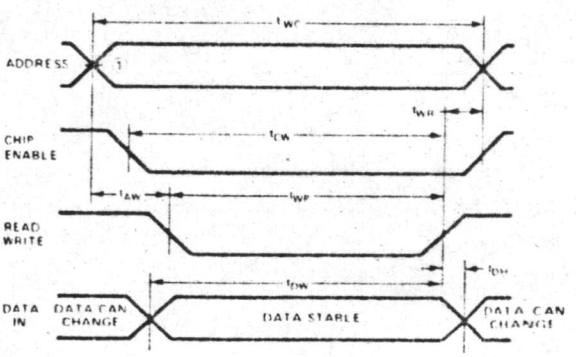
SYMBOL	TEST	LIMITS (pF) TYP. [1]	MAX.
C_{IN}	INPUT CAPACITANCE (ALL INPUT PINS) V_{IN} = 0V	3	5
C_{OUT}	OUTPUT CAPACITANCE V_{OUT} = 0V	7	10

Waveforms

READ CYCLE



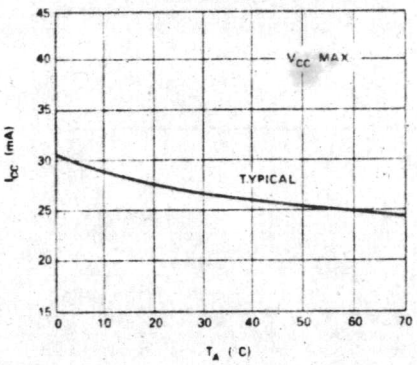
WRITE CYCLE



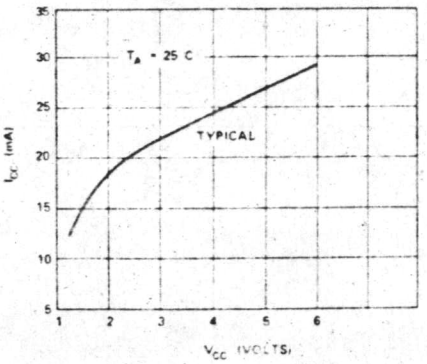
NOTES: 1. Typical values are for T_A = 25°C and nominal supply voltage.
2. This parameter is periodically sampled and is not 100% tested.

Typical D. C. and A. C. Characteristics

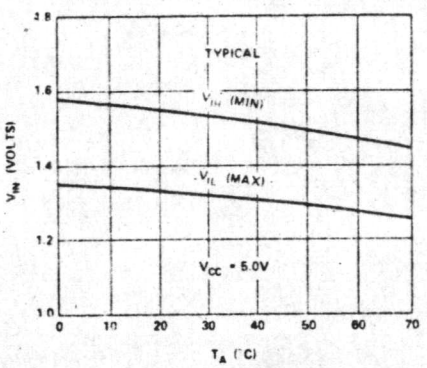
POWER SUPPLY CURRENT VS.
AMBIENT TEMPERATURE



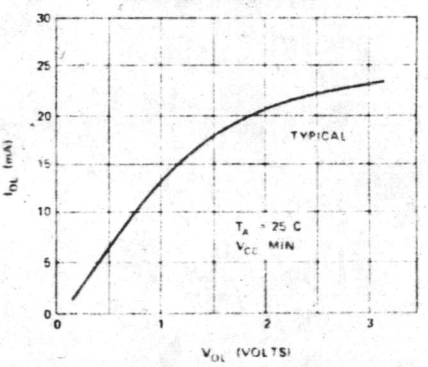
POWER SUPPLY CURRENT VS.
SUPPLY VOLTAGE



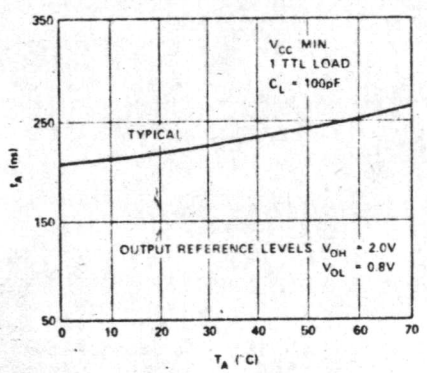
V_{IN} LIMITS VS. TEMPERATURE



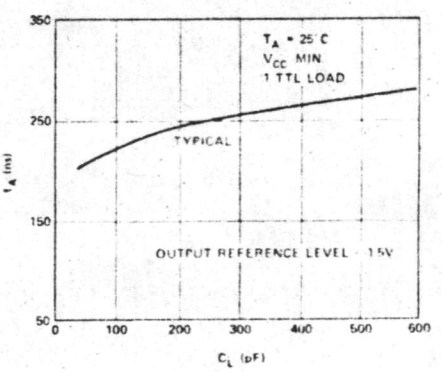
OUTPUT SINK CURRENT VS.
OUTPUT VOLTAGE



ACCESS TIME VS.
AMBIENT TEMPERATURE



ACCESS TIME VS.
LOAD CAPACITANCE



intel

1702A

2K (256 x 8) UV ERASABLE PROM

1702A-2	0.65 us Max.
1702A	1.0 us Max.
1702A-6	1.5 us Max.

- **Fast Access Time: Max. 650 ns (1702A-2)**
- **Fast Programming: 2 Minutes for all 2048 Bits**
- **All 2048 Bits Guaranteed* Programmable: 100% Factory Tested**
- **Static MOS: No Clocks Required**
- **Inputs and Outputs DTL and TTL Compatible**
- **Three-State Output: OR-tie Capability**

The 1702A is a 256 word by 8-bit electrically programmable ROM ideally suited for uses where fast turn-around and pattern experimentation are important. The 1702A undergoes complete programming and functional testing prior to shipment, thus insuring 100% programmability.

Initially all 2048 bits of the 1702A are in the "0" state (output low). Information is introduced by selectively programming "1"s (output high) in the proper bit location. The 1702A is packaged in a 24 pin dual in-line package with a transparent lid. The transparent lid allows the user to expose the 1702A to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device.

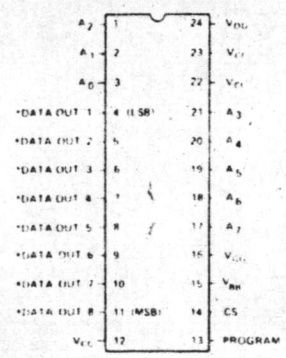
The circuitry of the 1702A is completely static. No clocks are required. Access times from 650ns to 1.5μs are available. A 1702AL family is available (see 1702AL data sheets for specifications) for those systems requiring lower power dissipation than the 1702A.

A pin-for-pin metal mask programmed ROM, the Intel 1302, is also available for large volume production runs of systems initially using the 1702A.

The 1702A is fabricated with silicon gate technology. This low threshold technology allows the design and production of higher performance MOS circuits and provides a higher functional density on a monolithic chip than conventional MOS technologies.

*Intel's liability shall be limited to replacing any unit which fails to program as desired.

PIN CONFIGURATION

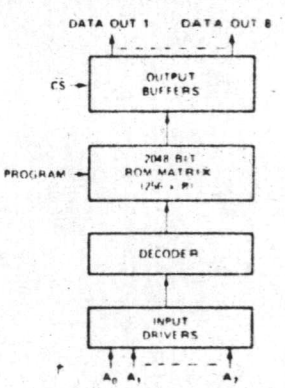


*THIS PIN IS THE DATA INPUT LEAD DURING PROGRAMMING

PIN NAMES

A_0–A_7	Address Inputs
$\overline{CS}$	Chip Select Input
D_{OUT1}–D_{OUT8}	Data Outputs

BLOCK DIAGRAM



NOTE: In the read mode a logic 1 at the address inputs and data outputs is a high and logic 0 is a low.

U.S. Patent No. 3660819

PIN CONNECTIONS

The external lead connections to the 1702A differ, depending on whether the device is being programmed or used in read mode (see following table). In the programming mode, the data inputs 1-8 are pins 4-11 respectively. *The programming voltages and timing are shown in the ROM and PROM Programming instructions section, pages 3-57.*

MODE \ PIN	12 (V_{CC})	13 (Program)	14 ($\overline{CS}$)	15 (V_{BB})	16 (V_{GG})	22 (V_{CC})	23 (V_{CC})	24 (V_{DD})
Read	V_{CC}	V_{CC}	GND	V_{CC}	V_{GG}	V_{CC}	V_{CC}	V_{DD}
Programming	GND	Program Pulse	GND	V_{BB}	Pulsed V_{GG}	GND	GND	Pulsed V_{DD}

Absolute Maximum Ratings*

Ambient Temperature Under Bias . . . . . -10°C to +80°C
Storage Temperature . . . . . −65°C to +125°C
Soldering Temperature of Leads (10 sec) . . . . . +300°C
Power Dissipation . . . . . 2 Watts
Read Operation: Input Voltages and Supply Voltages with respect to V_{CC} . . . . . +0.5V to −20V
Program Operation: Input Voltages and Supply Voltages with respect to V_{CC} . . . . . −48V

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

D.C. and Operating Characteristics

T_A = 0°C to 70°C, V_{CC} = +5V ±5%, V_{DD} = -9V ±5%, V_{GG} = -9V ±5%, unless otherwise noted.

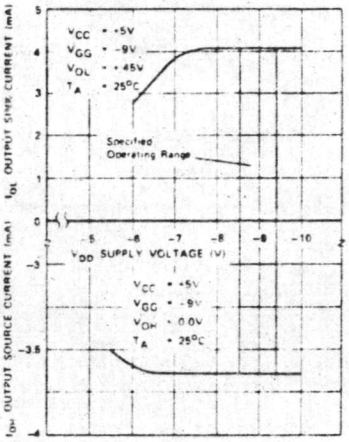
READ OPERATION

Symbol	Test	1702A, 1702A-6 Limits Min.	Typ.[1]	Max.	1702A-2 Limits Min.	Typ.[1]	Max.	Unit	Conditions
I_{LI}	Address and Chip Select Input Load Current			1			1	μA	V_{IN} = 0.0V
I_{LO}	Output Leakage Current			1			1	μA	V_{OUT} = 0.0V, $\overline{CS}$ = V_{IH2}
I_{DD1}[1]	Power Supply Current		35	50		40	60	mA	$\overline{CS}$ = V_{IH2}, I_{OL} = 0.0mA, T_A = 25°C, Continuous
I_{DD2}	Power Supply Current		32	46		37	55	mA	$\overline{CS}$ = 0.0V, I_{OL} = 0.0mA, T_A = 25°C, Continuous
I_{DD3}	Power Supply Current		38	60		43	65	mA	$\overline{CS}$ = V_{IH2}, I_{OL} = 0.0mA, T_A = 0°C, Continuous
I_{CF1}	Output Clamp Current		8	14		7	13	mA	V_{OUT} = -1.0V, T_A = 0°C, Continuous
I_{CF2}	Output Clamp Current		7	13		6	12	mA	V_{OUT} = -1.0V, T_A = 25°C, Continuous
I_{GG}	Gate Supply Current			1			1	μA	
V_{IL1}	Input Low Voltage for TTL Interface	-1		0.65	-1		0.65	V	
V_{IL2}	Input Low Voltage for MOS Interface	V_{DD}		V_{CC}-6	V_{DD}		V_{CC}-6	V	
V_{IH1}	Addr. Input High Voltage	V_{CC}-2		V_{CC}+0.3	V_{CC}-2		V_{CC}+0.3	V	
V_{IH2}	Chip Sel. Input High Volt.	V_{CC}-2		V_{CC}+0.3	V_{CC}-1.5		V_{CC}+0.3	V	
I_{OL}	Output Sink Current	1.6	4		1.6	4		mA	V_{OUT} = 0.45V
I_{OH}	Output Source Current	-2.0			-2.0			mA	V_{OUT} = 0.0V
V_{OL}	Output Low Voltage		-3	0.45		-3	0.45	V	I_{OL} = 1.6mA
V_{OH}	Output High Voltage	3.5	4.5		3.5	4.5		V	I_{OH} = -200μA

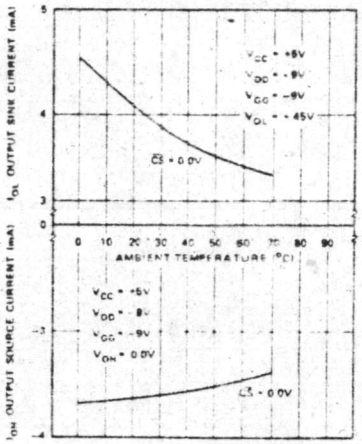
Note 1: Typical values are at nominal voltages and T_A = 25°C.

Typical Characteristics

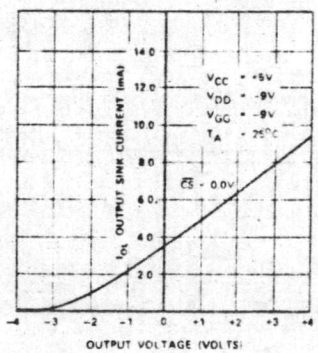
OUTPUT CURRENT VS. V_{DD} SUPPLY VOLTAGE



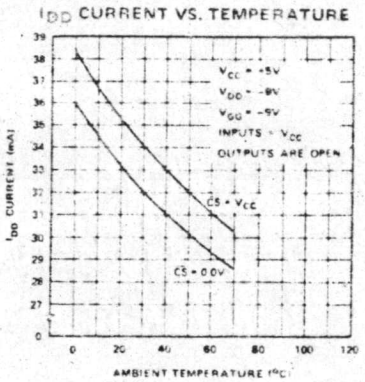
OUTPUT CURRENT VS. TEMPERATURE



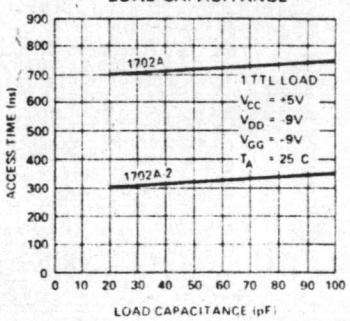
OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE



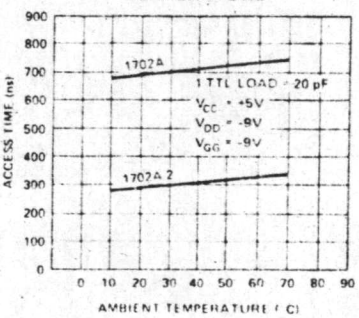
I_{DD} CURRENT VS. TEMPERATURE



ACCESS TIME VS. LOAD CAPACITANCE



ACCESS TIME VS. TEMPERATURE



A.C. Characteristics

T_A = 0° C to +70° C, V_{CC} = +5V ±5%, V_{DD} = −9V ±5%, V_{GG} = −9V ±5% unless otherwise noted

Symbol	Test	1702A Limits Min.	1702A Limits Max.	1702A-2 Limits Min.	1702A-2 Limits Max.	1702A-6 Limits Min.	1702A-6 Limits Max.	Unit
Freq.	Repetition Rate		1		1.6		0.66	MHz
t_{OH}	Previous Read Data Valid		0.1		0.1		0.1	μs
t_{ACC}	Address to Output Delay		1		0.65		1.5	μs
t_{CS}	Chip Select Delay		0.1		0.3		0.6	μs
t_{CO}	Output Delay From $\overline{CS}$		0.9		0.35		0.9	μs
t_{OD}	Output Deselect		0.3		0.3		0.3	μs

Capacitance* T_A = 25°C

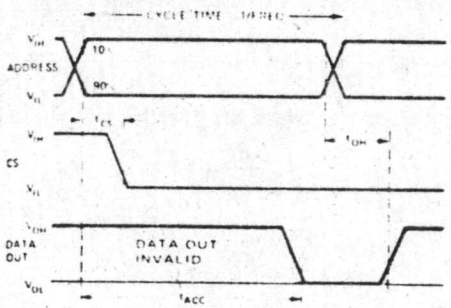
SYMBOL	TEST	TYPICAL	MAXIMUM	UNIT	CONDITIONS
C_{IN}	Input Capacitance	8	15	pF	$V_{IN} = V_{CC}$, $\overline{CS} = V_{CC}$, All unused pins
C_{OUT}	Output Capacitance	10	15	pF	$V_{OUT} = V_{CC}$, $V_{GG} = V_{CC}$, are at A.C. ground

*This parameter is periodically sampled and is not 100% tested.

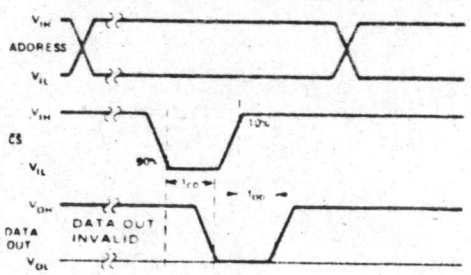
Switching Characteristics

Conditions of Test:
Input pulse amplitudes: 0 to 4V; t_R, t_F ≤50 ns
Output load is 1 TTL gate; measurements made at output of TTL gate (t_{PD}≤15 ns), C_L = 15pF

A) READ OPERATION



B) DESELECTION OF DATA OUTPUT IN OR-TIE OPERATION



intel

2708, 2704

8K AND 4K UV ERASABLE PROM

- 2708 1024x8 Organization
- 2704 512x8 Organization

- **Fast Programming — Typ. 100 sec. For All 8K Bits**
- **Low Power During Programming**
- **Access Time — 450 ns Max.**
- **Standard Power Supplies — +12V, +5V, -5V**
- **Static — No Clocks Required**
- **Inputs and Outputs TTL Compatible During Both Read and Program Modes**
- **Three-State Output — OR-Tie Capability**

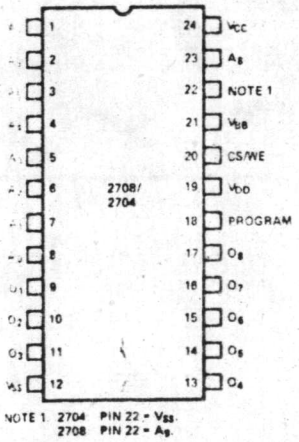
The Intel 2708/2704 are high speed 8192/4096 bit erasable and electrically reprogrammable ROM's (EPROM) ideally suited where fast turn around and pattern experimentation are important requirements.

The 2708/2704 are packaged in a 24 pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the devices.

A pin for pin mask programmed ROM, the Intel 2308, is available for large volume production runs of systems initially using the 2708.

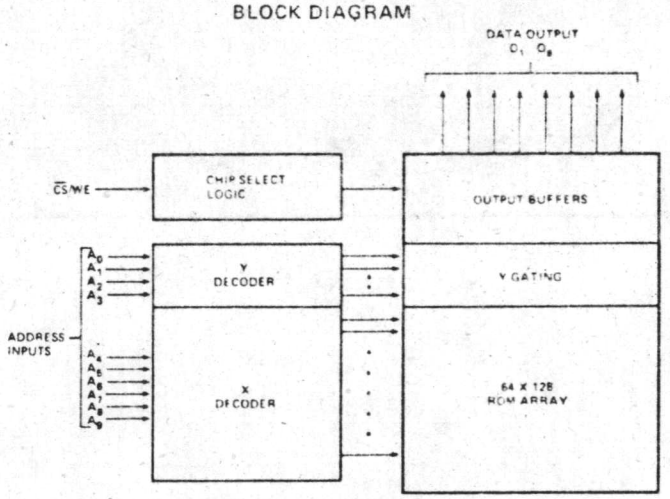
The 2708/2704 is fabricated with the time proven N-channel silicon gate technology.

PIN CONFIGURATIONS



NOTE 1: 2704 PIN 22 = V_{SS}.
2708 PIN 22 = A_8.

BLOCK DIAGRAM



PIN NAMES

A_0 A_9	ADDRESS INPUTS
O_1 O_8	DATA OUTPUTS
$\overline{CS}/\overline{WE}$	CHIP SELECT/WRITE ENABLE INPUT

PIN CONNECTION DURING READ OR PROGRAM

MODE	PIN NUMBER 9-11, 13-17	12	18	19	20	21	24
READ	D_{OUT}	V_{SS}	V_{SS}	V_{DD}	V_{IL}	V_{BB}	V_{CC}
PROGRAM	D_{IN}	V_{SS}	Pulsed V_{IHP}	V_{DD}	V_{IHW}	V_{BB}	V_{CC}

PROGRAMMING

The programming specifications are in the ROM and PROM Programming Instructions (see page 3-59).

Absolute Maximum Ratings*

Temperature Under Bias	-25°C to +85°C
Storage Temperature	-65°C to +125°C
V_{DD} With Respect to V_{BB}	+20V to -0.3V
V_{CC} and V_{SS} With Respect to V_{BB}	+15V to -0.3V
All Input or Output Voltages With Respect to V_{BB} During Read	+15V to -0.3V
$\overline{CS}$/WE Input With Respect to V_{BB} During Programming	+20V to -0.3V
Program Input With Respect to V_{BB}	+35V to -0.3V
Power Dissipation	1.5W

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

READ OPERATION

D.C. and Operating Characteristics

T_A = 0°C to 70°C, V_{CC} = +5V ±5%, V_{DD} = +12V ±5%, V_{BB} = -5V ±5%, V_{SS} = 0V, Unless Otherwise Noted.

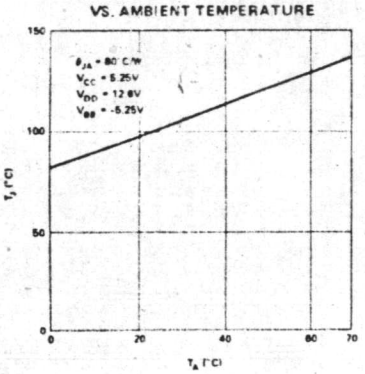
Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Conditions
I_{LI}	Address and Chip Select Input Sink Current		1	10	μA	V_{IN} = 5.25 V or V_{IN} = V_{IL}
I_{LO}	Output Leakage Current		1	10	μA	V_{OUT} = 5.25V, $\overline{CS}$/WE = 5V
I_{DD}[2]	V_{DD} Supply Current		50	65	mA	Worst Case Supply Currents:
I_{CC}[2]	V_{CC} Supply Current		6	10	mA	All Inputs High
I_{BB}[2]	V_{BB} Supply Current		30	45	mA	$\overline{CS}$/WE = 5V; T_A = 0°C
V_{IL}	Input Low Voltage	V_{SS}		0.65	V	
V_{IH}	Input High Voltage	3.0		V_{CC}+1	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 1.6mA
V_{OH1}	Output High Voltage	3.7			V	I_{OH} = -100μA
V_{OH2}	Output High Voltage	2.4			V	I_{OH} = -1mA
P_D	Power Dissipation			800	mW	T_A = 70°C

NOTES: 1. Typical values are for T_A = 25°C and nominal supply voltages.

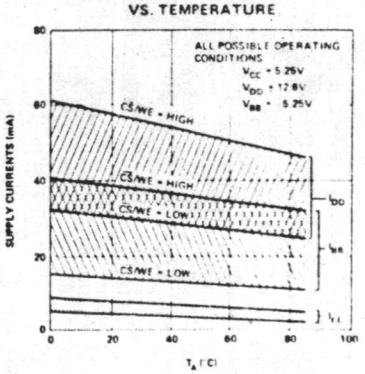
2. The total power dissipation of the 2704/2708 is specified at 800 mW. It is not calculable by summing the various currents (I_{DD}, I_{CC}, and I_{BB}) multiplied by their respective voltages since current paths exist between the various power supplies and V_{SS}. The I_{DD}, I_{CC}, and I_{BB} currents should be used to determine power supply capacity only.

Typical D.C. Characteristics

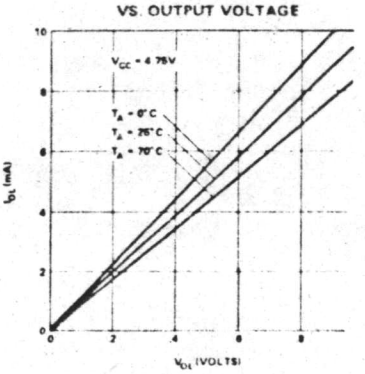
MAXIMUM JUNCTION TEMPERATURE VS. AMBIENT TEMPERATURE



RANGE OF SUPPLY CURRENTS VS. TEMPERATURE



OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE



A.C. Characteristics

T_A = 0°C to 70°C, V_{CC} = +5V ±5%, V_{DD} = +12V ±5%, V_{BB} = -5V ±5%, V_{SS} = 0V, Unless Otherwise Noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{ACC}	Address to Output Delay		280	450	ns
$t_{\overline{CO}}$	Chip Select to Output Delay		60	120	ns
t_{DF}	Chip De-Select to Output Float	0		120	ns
t_{OH}	Address to Output Hold	0			ns

Capacitance[1] T_A = 25°C, f = 1MHz

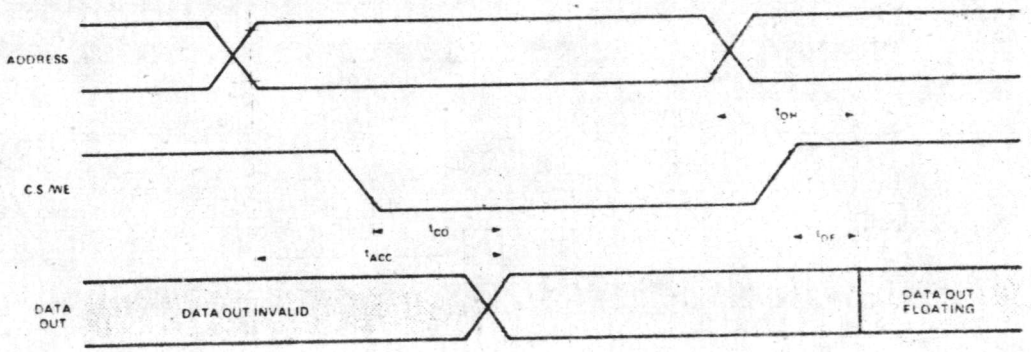
Symbol	Parameter	Typ.	Max.	Unit	Conditions
C_{IN}	Input Capacitance	4	6	pF	V_{IN}=0V
C_{OUT}	Output Capacitance	8	12	pF	V_{OUT}=0V

Note 1. This parameter is periodically sampled and not 100% tested.

A.C. Test Conditions:

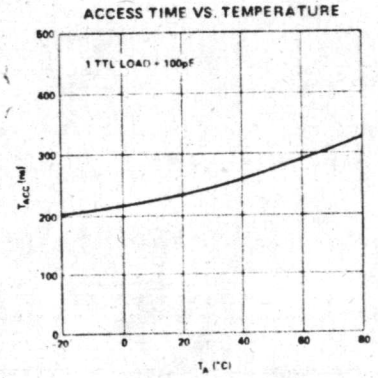
Output Load: 1 TTL gate and C_L = 100pF
Input Rise and Fall Times: ≤20ns
Timing Measurement Reference Levels: 0.8V and 2.8V for inputs; 0.8V and 2.4V for outputs
Input Pulse Levels: 0.65V to 3.0V

Waveforms

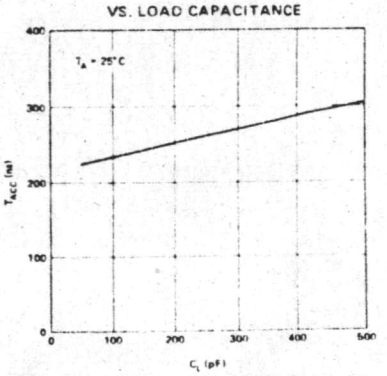


Typical A.C. Characteristics

ACCESS TIME VS. TEMPERATURE



ACCESS TIME VS. LOAD CAPACITANCE



UART — The UART is a universal, asynchronous, receiver/transmitter LSI circuit. It can simultaneously receive parallel data inputs, disassemble them, and transmit them as asynchronous serial data outputs, and receive asynchronous serial data inputs, assemble them, and gate them out as parallel data words. Additionally, it can add start, parity (even or odd), and stop bits to its transmit, serial-data outputs, and can check received serial data for word format and parity errors. Following is a list of the UART pin assignments for this application.

Pins 1 through 3 provide the required power and signal ground inputs to the UART.

Pin 4 (Enbl Rcvr Rgtr) is normally low to gate outputs from Rcvr Rgtr pins 5 through 12, but goes high to block the receiver register outputs when either a word format error (framing error indicated by missing stop bit) or a parity error occurs in a received word.

Pins 5 through 12 (Rcvr Rgtr) are the receiver register output pins.

Pin 13 (Parity Err) goes high to indicate a parity error in a received data word.

Pin 14 (Frame Err) goes high to indicate a framing error (format error) if a received word does not end with a stop bit (mark or logical 1 bit).

Pin 16 (Enbl Status Rgtrs) is tied low to enable status outputs from pins 13, 14, 19, and 22 (parity error, framing error, receiver register full, and transmit holding register empty).

Pin 17 (Rcvr Clk ÷ 16) accepts a receive clock signal that is 16 times the actual bit rate of received data inputs.

Pin 18 (Reset Rcvr Rgtr Full) goes low to reset pin 19 (Rcvr Rgtr Full) when the receive register is not full; pin 19 goes high when the receive register is full.

Pin 20 (Ser Rcvr Data) receives serial data inputs; reception starts with a high-to-low (marking to spacing) transition on this line.

Pin 21 (Reset) goes high to reset the UART when a master reset occurs.

Pin 22 (Bfr Rgtr Empty) goes high when transmit holding register is empty.

Pin 23 (Load Bfr Rgtr) goes low to load data on pins 26 through 33 into the UART transmit buffer register.

Pin 24 (Xmtr Shf-Rgtr Empty) goes high to indicate transmit shift register is empty.

Pin 25 (Ser Xmtr Data) is the output pin for serial transmit data; it is high when no data is being transmitted and shifts low (start bit) to indicate the start of transmission.

Pins 26 through 33 receive parallel data inputs.

Pin 34 (Load Mode Rgtr) is tied high to permit addition of control and parity bits to the parallel, transmit data inputs.

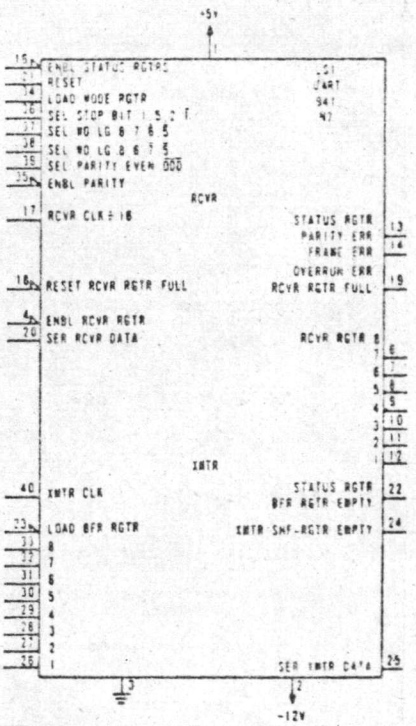
Pin 35 (Enbl Parity) is low to enable parity bit generation and checking, and is high to disable these functions.

Pin 36 (Sel Stop Bit) goes high when the display terminal is operating at 110 baud transmission rate to enable two stop bits to be added to transmitted words; it is low to enable only one stop bit at all other baud rates.

Pins 37 and 38 (Sel Wd Lg) are connected so as to enable eight data bits per transmitted word when no parity is selected (see pin 33, preceding) or to enable seven data bits and a parity bit per transmitted word when parity check/generation is enabled (see pin 35, preceding).

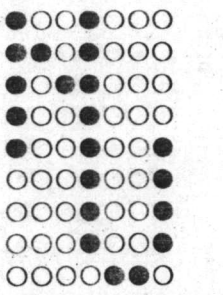
Pin 39 (Sel Parity Even/Odd) is high to select even parity checking and generation when these functions are enabled (see pin 35, preceding), and low to select odd parity checking and generation.

Pin 40 (Xmtr Clk) receives a clock signal that is 16 times the actual bit rate of transmitted data (see also pin 17, preceding).

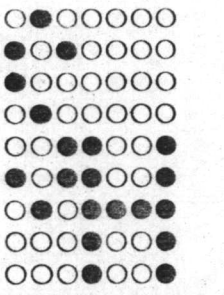


ภาคผนวก ข

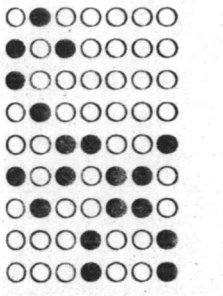
ตัวอักษรที่ออกแบบเพื่อแสดงบนจอภาพ



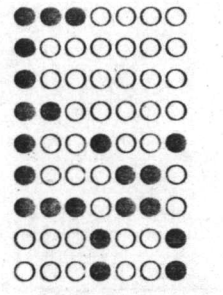
symbol NUL
code 00



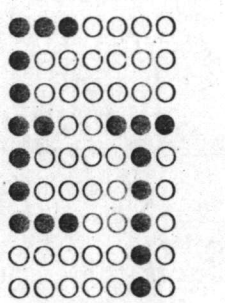
symbol SOH
code 01



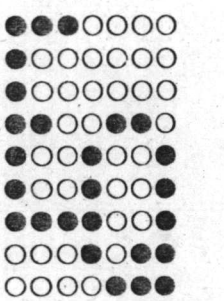
symbol STX
code 02



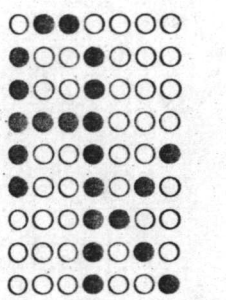
symbol ETX
code 03



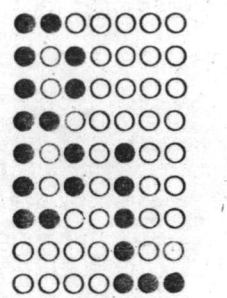
symbol EOT
code 04



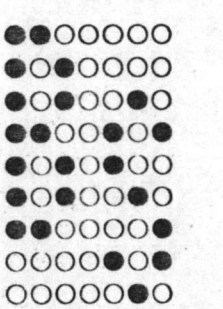
symbol ENQ
code 05



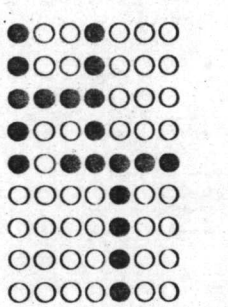
symbol ACK
code 06



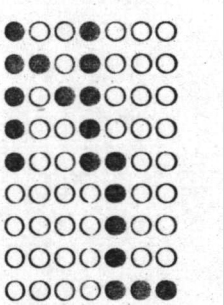
symbol BEL
code 07



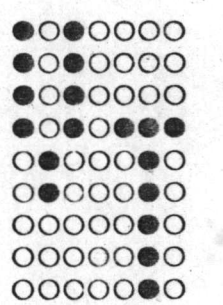
symbol BS
code 08



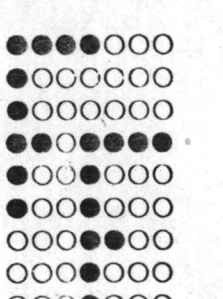
symbol HT
code 09



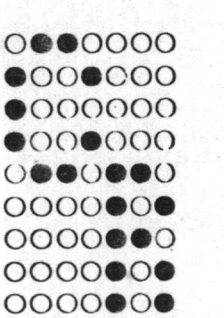
symbol NL
code 0A



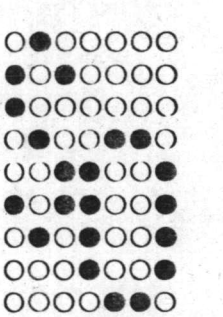
symbol VT
code 0B



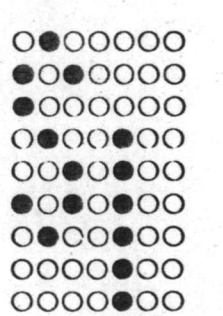
symbol FF
code 0C



symbol CR
code 0D



symbol SO
code 0E



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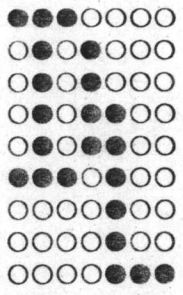
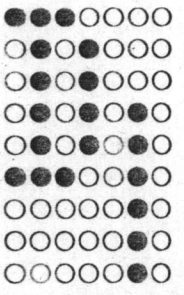


symbol DLE
code 10



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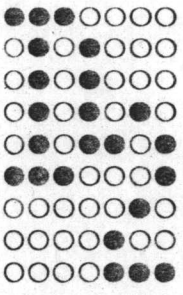
code 11



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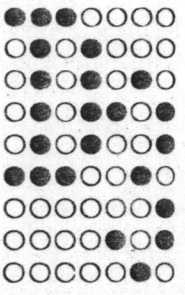

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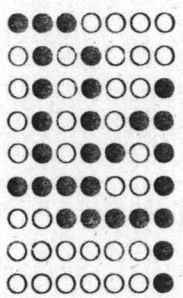

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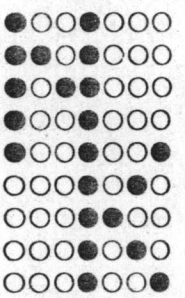

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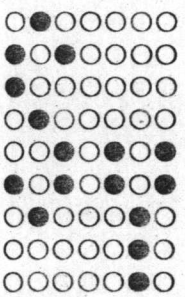

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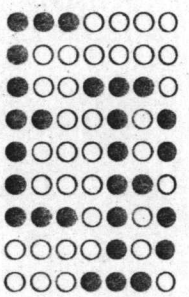

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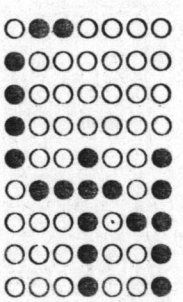

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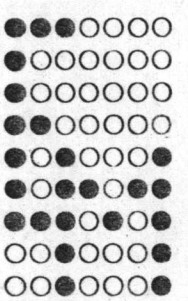

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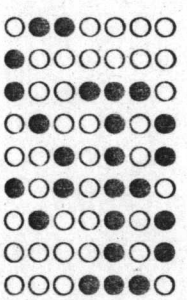

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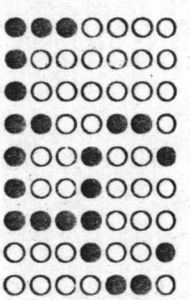

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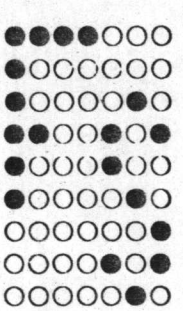

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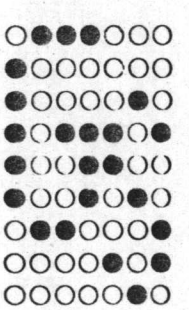
code 1C



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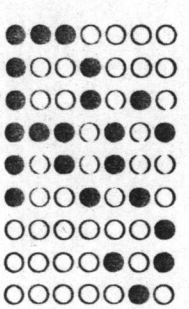

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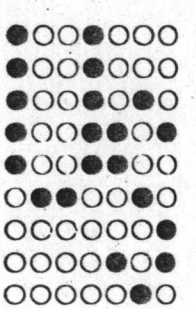

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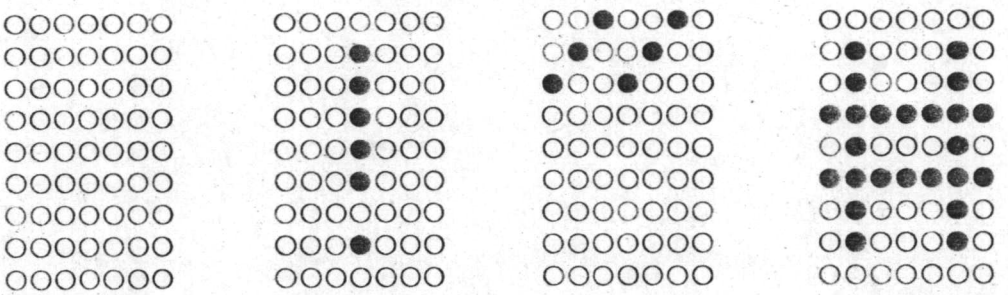
code 1F

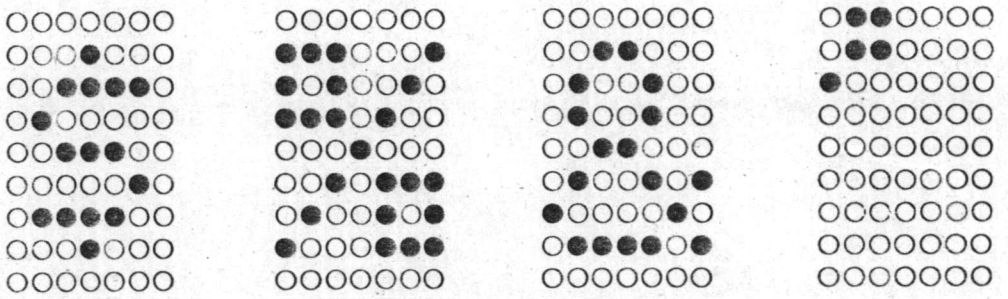


symbol SP
code 20

symbol !
code 21

symbol "
code 22

symbol #
code 23

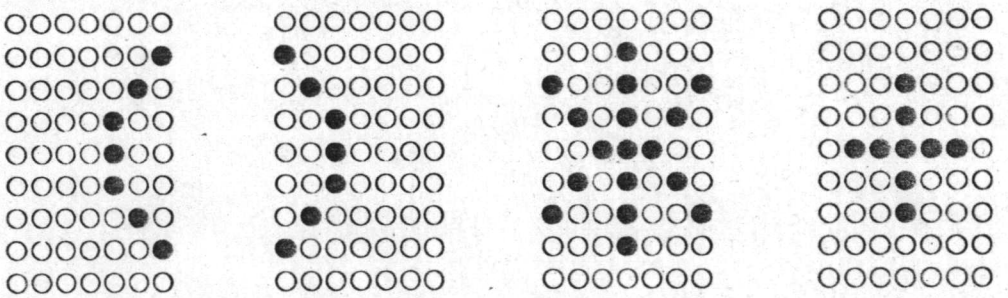


symbol $
code 24

symbol %
code 25

symbol &
code 26

symbol '
code 27

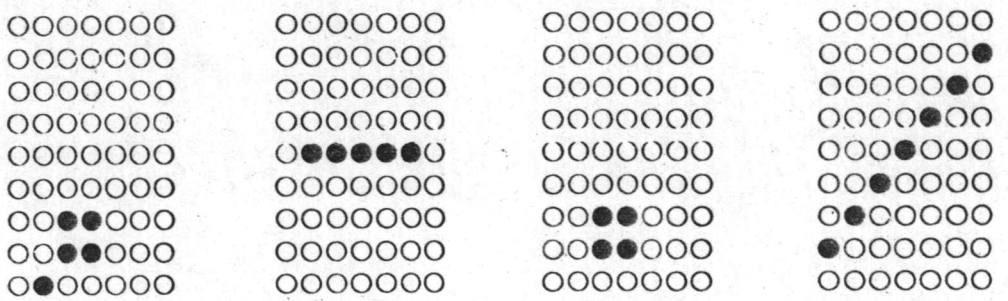


symbol (
code 28

symbol)
code 29

symbol *
code 2A

symbol +
code 2B

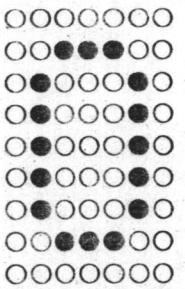


symbol ,
code 2C

symbol -
code 2D

symbol .
code 2E

symbol /
code 2F



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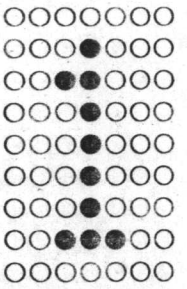
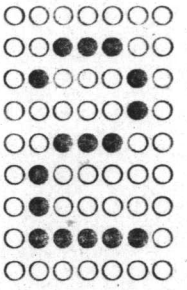
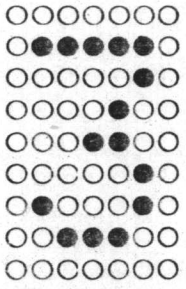
code 30



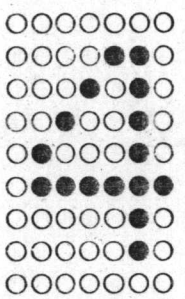
symbol 1
code 31



symbol 2
code 32



symbol 3
code 33



symbol 4
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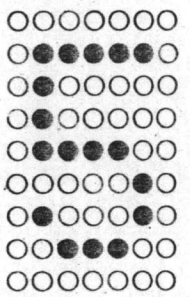

symbol 5
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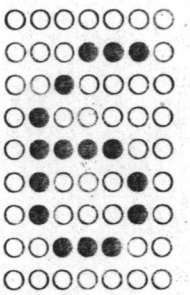
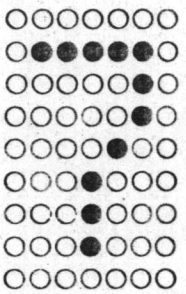


symbol 6
code 36



symbol 7
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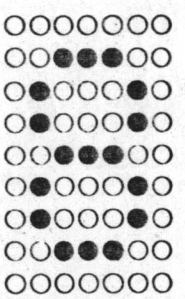
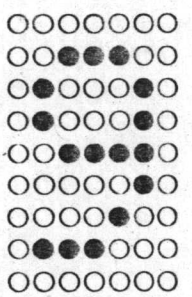
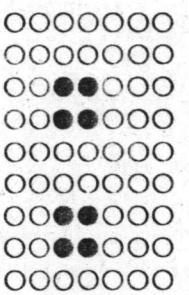


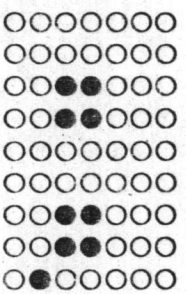
symbol 8
code 38



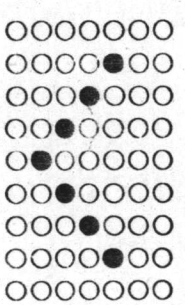
symbol 9
code 39



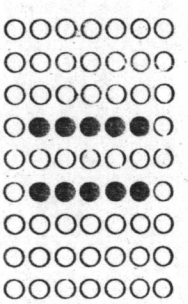
symbol :
code 3A



symbol ;
code 3B



symbol <
code 3C



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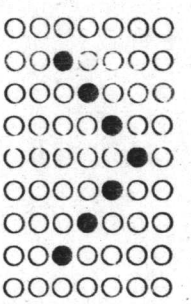
code 3D



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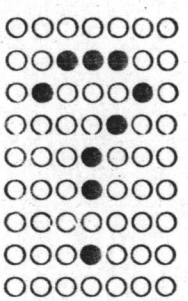
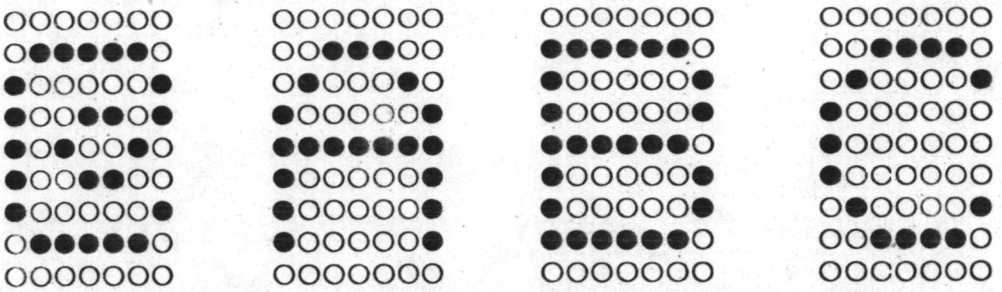
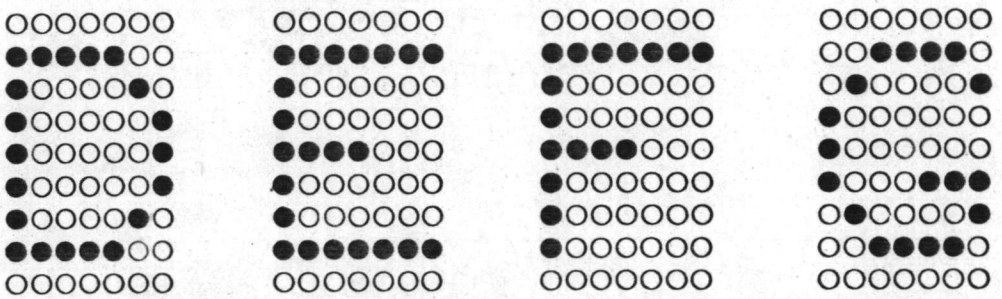
code 3E



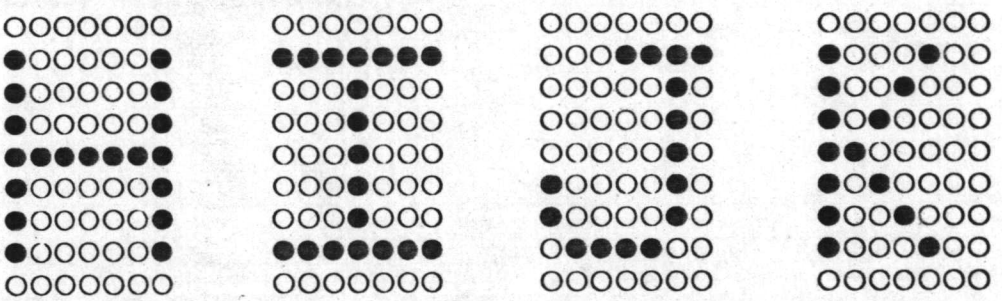
symbol ?
code 3F



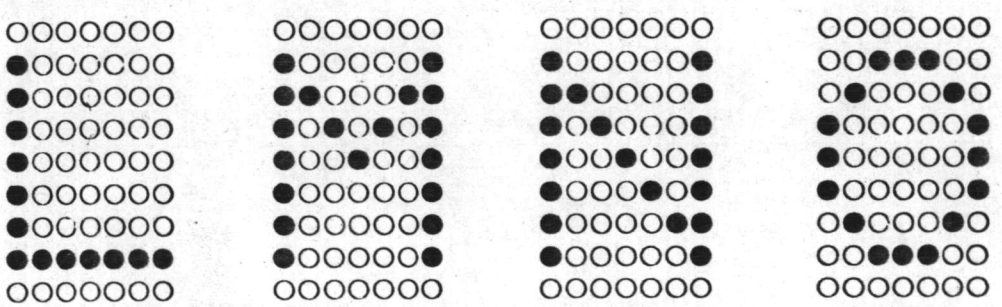
symbol @ code 40 | symbol A code 41 | symbol B code 42 | symbol C code 43



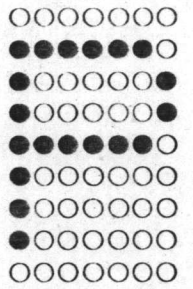
symbol D code 44 | symbol E code 45 | symbol F code 46 | symbol G code 47



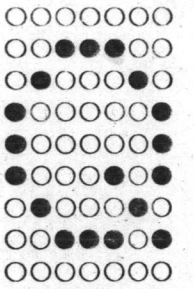
symbol H code 48 | symbol I code 49 | symbol J code 4A | symbol K code 4B



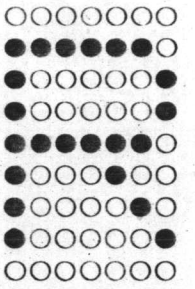
symbol L code 4C | symbol M code 4D | symbol N code 4E | symbol O code 4F



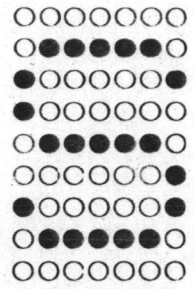
symbol P
code 50



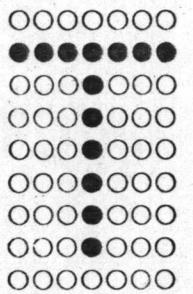
symbol Q
code 51



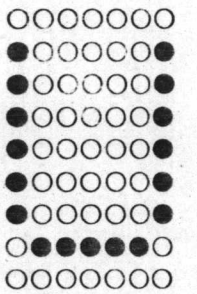
symbol R
code 52



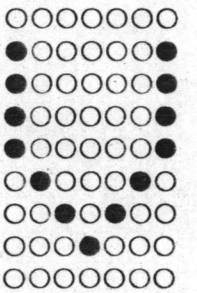
symbol S
code 53



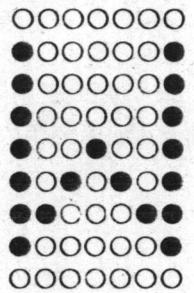
symbol T
code 54



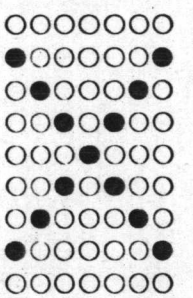
symbol U
code 55



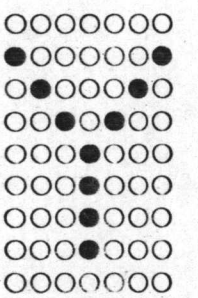
symbol V
code 56



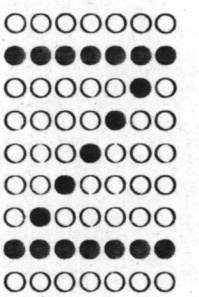
symbol W
code 57



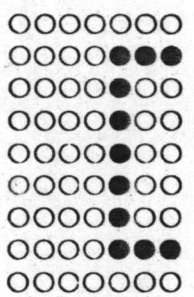
symbol X
code 58



symbol Y
code 59



symbol Z
code 5A



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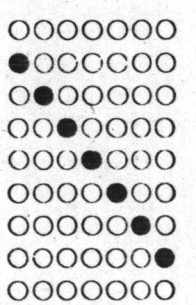
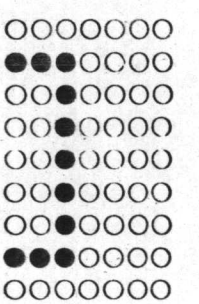
code 5B



symbol \
code 5C



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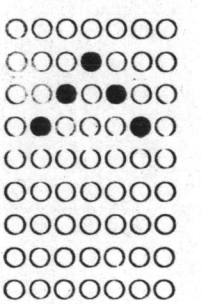

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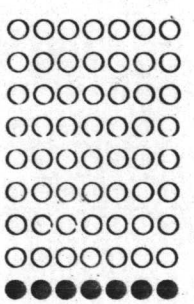

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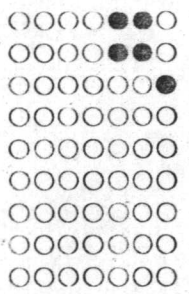
code 5F



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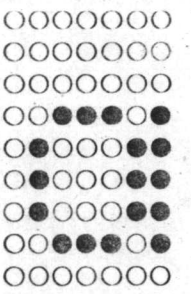

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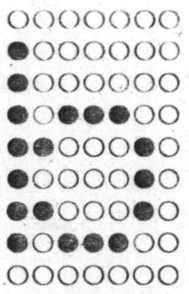

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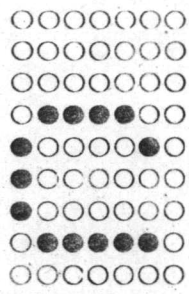

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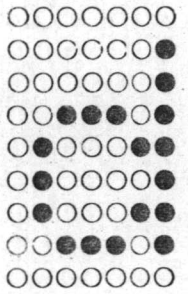
code 63



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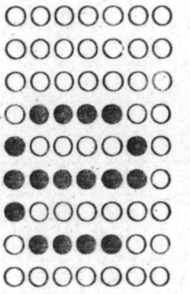
code 64



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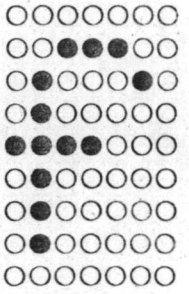

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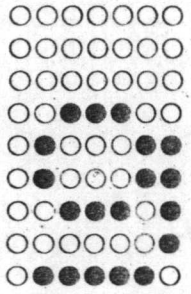

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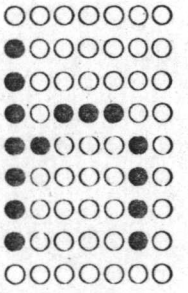

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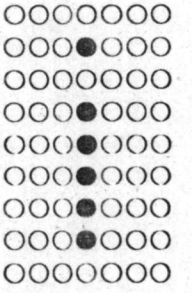

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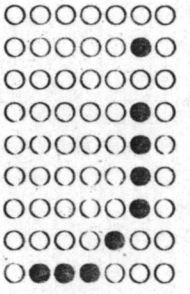

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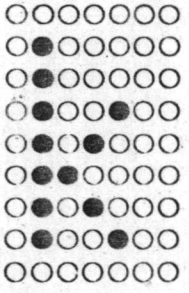

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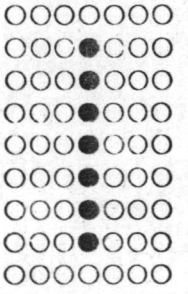

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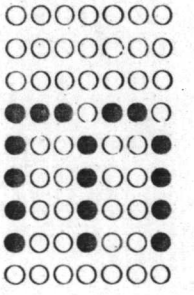

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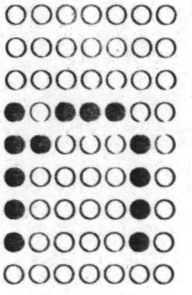

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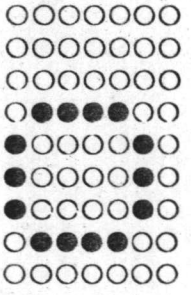

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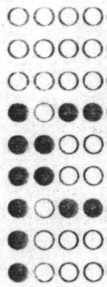

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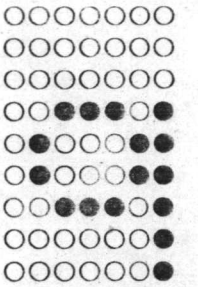

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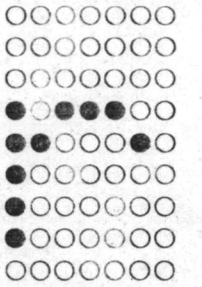
code 71



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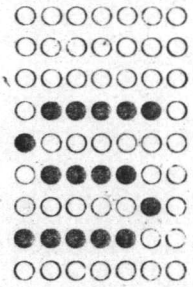

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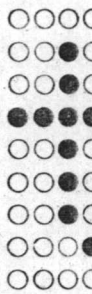

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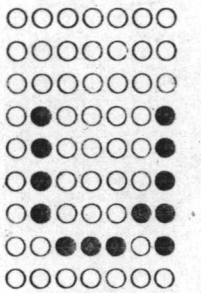

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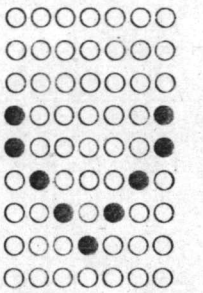

symbol v
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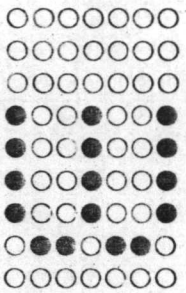

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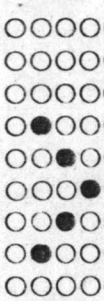

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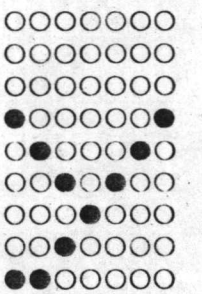

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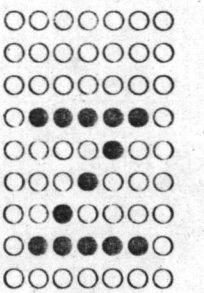

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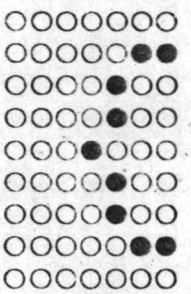
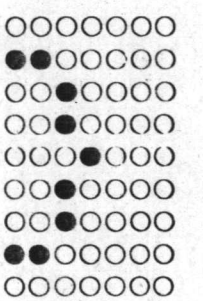


symbol {
code 7B

symbol |
code 7C



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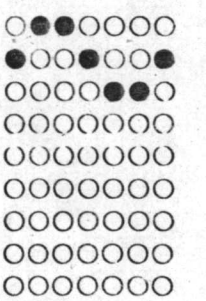

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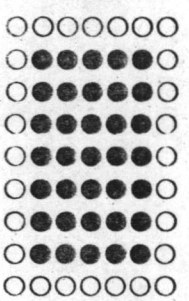

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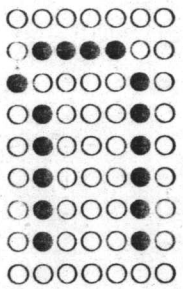

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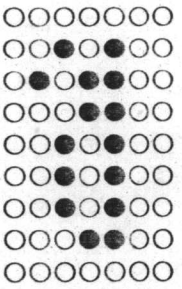

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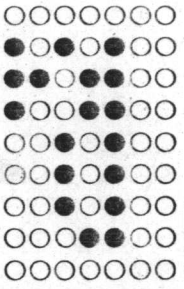

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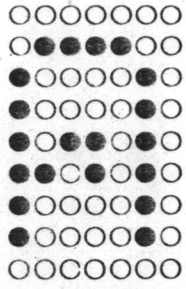

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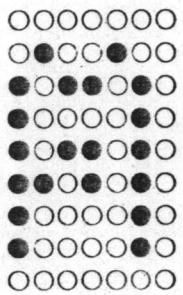

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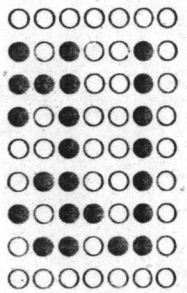

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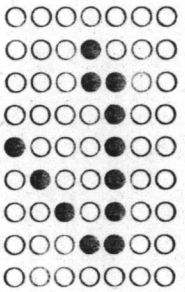

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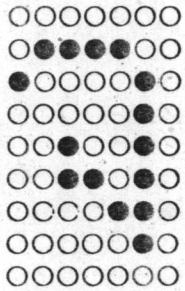

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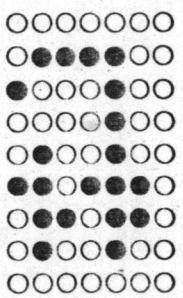

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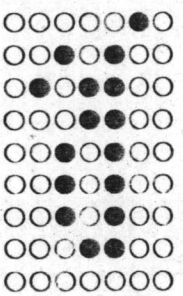

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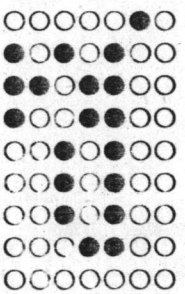

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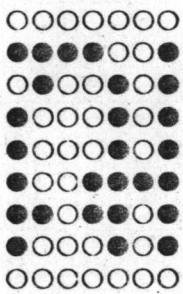

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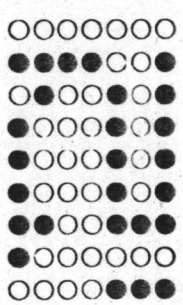

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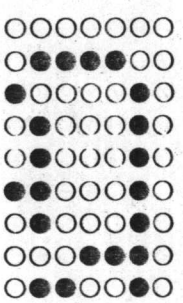

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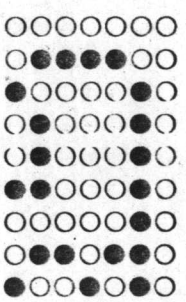

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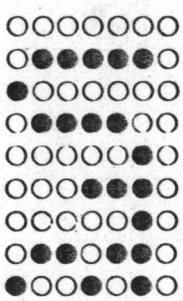

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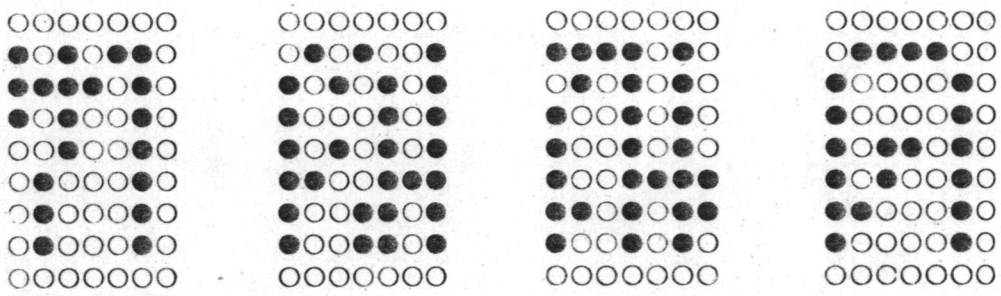

symbol ฑ
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symbol ฒ
code B1

symbol ณ
code B2

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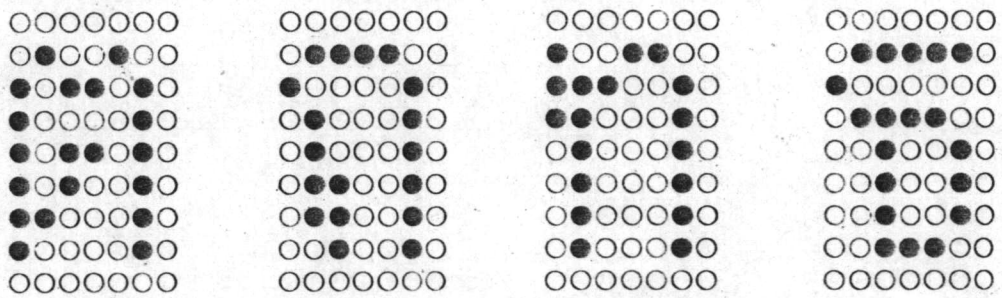
code B3



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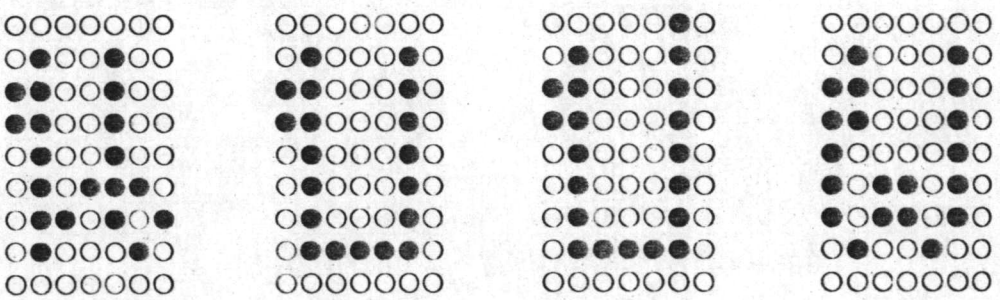
code B4

symbol ถ
code B5

symbol ท
code B6

symbol ธ
code B7



symbol น
code B8

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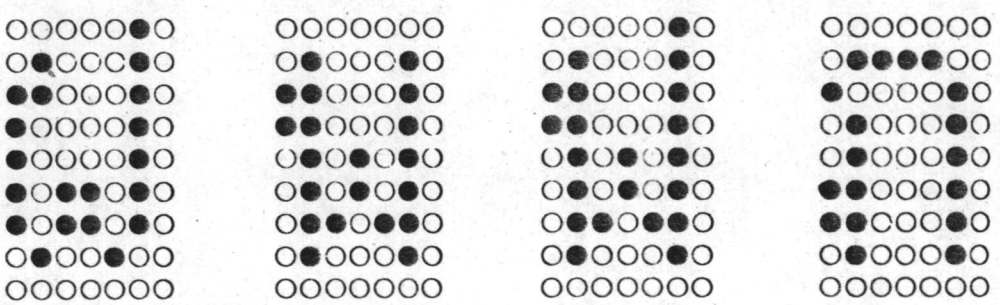
symbol ป
code BA

symbol ผ
code BB



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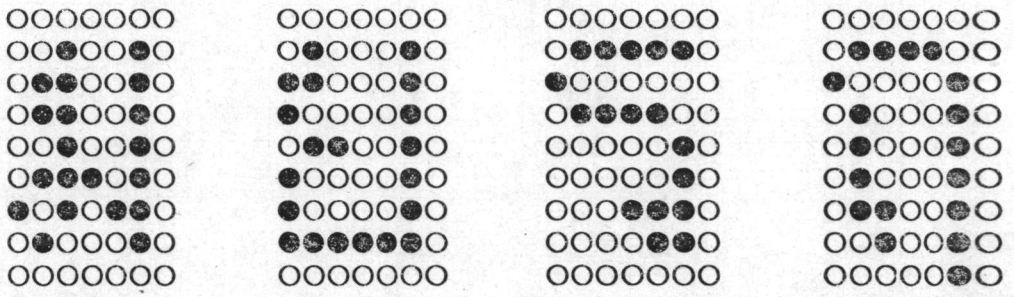
code BC

symbol พ
code BD

symbol ฟ
code BE

symbol ภ
code BF



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symbol ฝ code C1

symbol ฟ code C2

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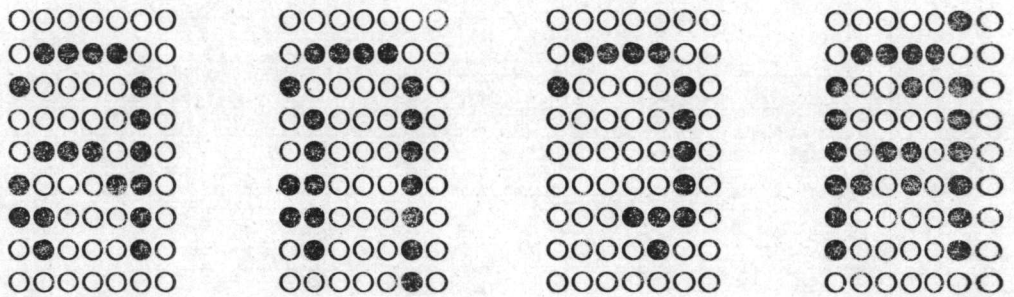

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symbol ฦ code C5

symbol ว code C6

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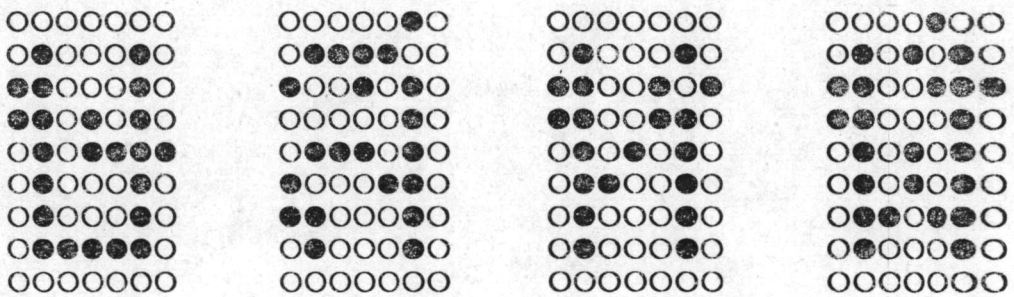

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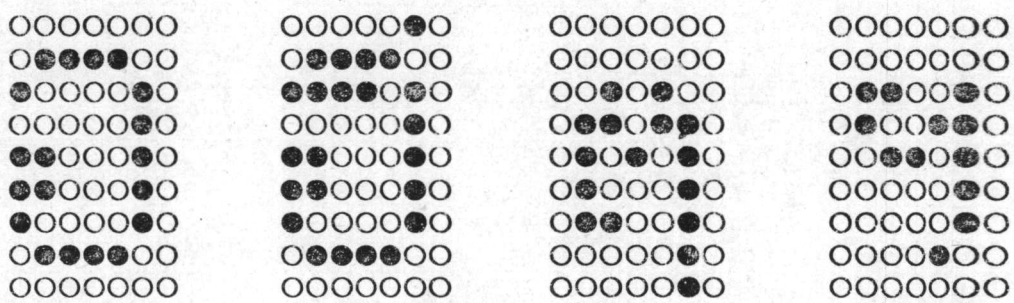
symbol ส code C9

symbol ห code CA

symbol ฬ code CB



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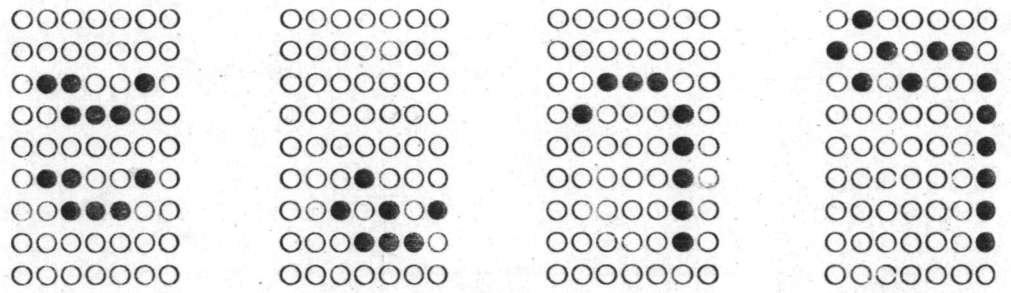
symbol ๆ code CE

symbol ๆ code CF



symbol ั
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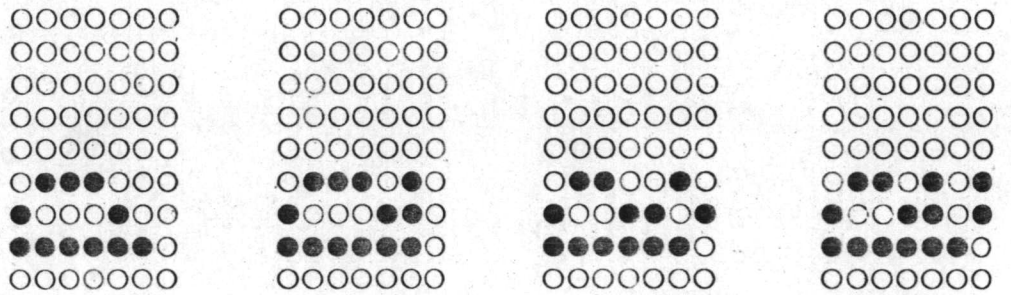
code D3



symbol ิ
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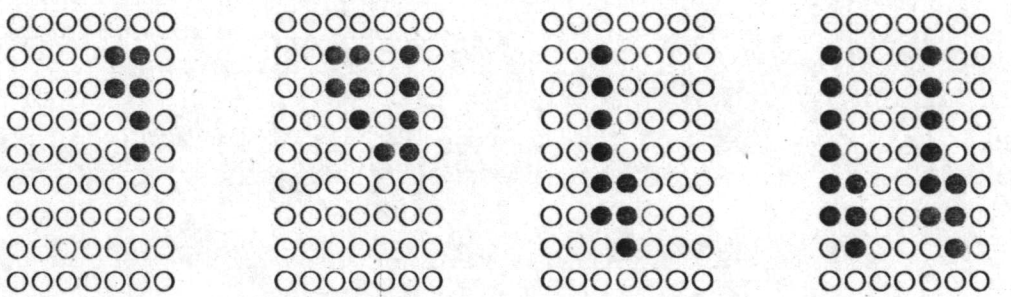
symbol ื
code D7

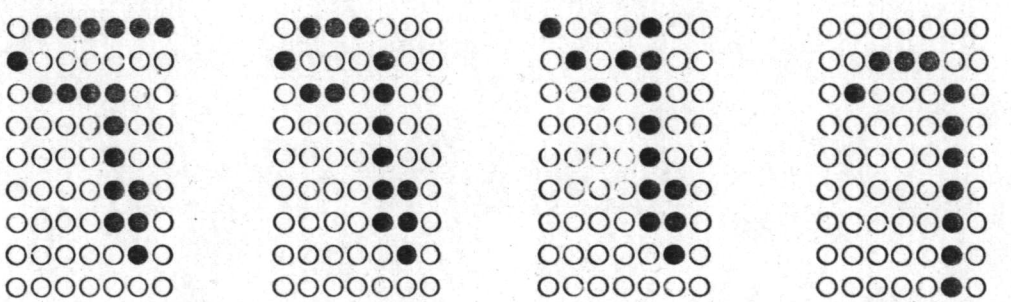


symbol ุ
code D8

symbol ู
code D9

symbol ฺ
code DA

symbol ฺ
code DB

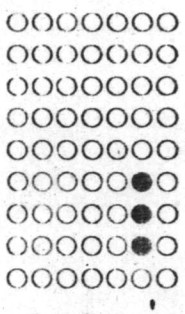


symbol ฺ
code DC

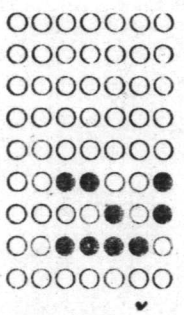
symbol ฺ
code DD

symbol ฺ
code DE

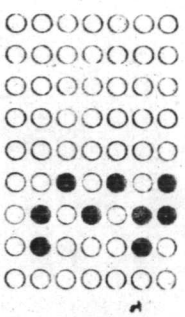
symbol ฺ
code DF



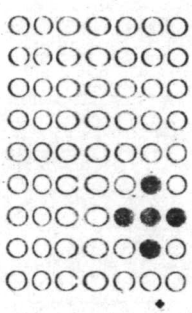
symbol code E0



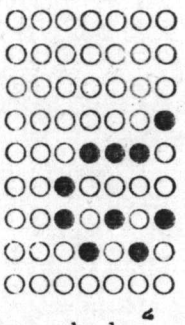
symbol code E1



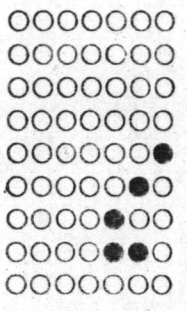
symbol code E2



symbol code E3



symbol code E4



symbol code E5

ภาคผนวก ค

ตารางคำศัพท์

A register	เอ รีจิสเตอร์
A/Q	เอ/คิว
A/Q-DMA	เอ/คิว-ดีเอ็มเอ
access	แอ็กเซส
access time	แอ็กเซสไทม์
address	แอ็กเดรส
ADT (Auto Data Transfer)	เอดีที
alarm driver	อลาร์มไดรเวอร์
alphabetic	ตัวอักษร
ALU (Arithmatic Logic Unit)	เอแอลยู
ANSI (American National Standard Institute)	เอเอ็นเอสไอ
ANSI x 3131/638	เอเอ็นเอสไอ เอ็กซ์ 3131 / 638
ASCII (American National Standard Code for Information Interchange)	เอเอสซีไอไอ (แอสกิ)
asynchronous	อซิงโครนัส
balanced line	บาลานซ์ลายน์
band	แบนด์
band detect register	แบนด์ดีเท็ครีจิสเตอร์
bank (memory)	แบ็งก์
baud rate	บ็อดเรท
binary	ไบนารี
bit	บิท
bit density	บิทเด็นซิตี
blanking	แบล็งกิง
blink (field)	กระพริบ

BPI (bit per inch)	บีพีไอ
BREAK key	แป้นเบรก
buffer	บัฟเฟอร์
byte	ไบท์
card reader	เครื่องอ่านบัตร
CARRIAGE RETURN key	แป้นคาริเอ็จรีเทอน
carrier on	แคร์เรียร์ออน
cassette tape transport	เครื่องบันทึกและอ่านเทปคาสเซท์
cathode ray tube	หลอดภาพ
central processing unit	หน่วยประมวลผลกลาง
channel	แชนแนล
character generator	คาแร็กเตอร์เจเนอเรเตอร์
character mark	คาแร็กเตอร์มาร์ก
character mark sensor	คาแร็กเตอร์มาร์กเซนเซอร์
character request	คาแร็กเตอร์รีเควส
character set	คาแร็กเตอร์เซท
chain (printer)	เชน
chip	ชิป
chip enable	ชิปเอเนเบิล
chip select	ชิปซีเล็กท์
CLA (Communication Line Adapter)	ซีแอลเอ
clear	เคลียร์
clear control (circuit)	เคลียร์คอนโทรล
CLEAR key	แป้นเคลียร์
clock (circuit, signal)	คล็อก

CO key (carrier on)	แป้นซีโอ
code	รหัส
combination	คอมบิเนชัน
communication control (code)	รหัสควบคุมการสื่อสาร
comparator (chip, circuit)	คอมแพเรเตอร์
compiler	คอมพายเลอร์
complement	คอมพลีเมนท์
computer	คอมพิวเตอร์
configuration	คอนฟิกูเรชัน
control bit	คอนโทรลบิท
control code	รหัสควบคุม
Control Data Corporation (CDC)	คอนโทรลดาตาคอร์ปอเรชัน
CONTROL key	แป้นคอนโทรล
controller/formatter	คอนโทรลเลอร์/ฟอร์แมตเตอร์
count	นับ
counter (circuit)	เคาน์เตอร์
CR/LP interface (Card Reader/Line Printer)	ซีอาร์/แอลพี อินเตอร์เฟส
crystal	คริสตัล
cursor	เคอร์เซอร์
cursor control (circuit)	เคอร์เซอร์คอนโทรล
cursor counter (circuit)	เคอร์เซอร์เคาน์เตอร์
cursor display (circuit)	เคอร์เซอร์ดิสเพลย์
cycle	ไซเกิล
Cyber 18-20	ไซเบอร์ 18-20
data	ข้อมูล

data decode (circuit)	ดาตาดีโคด
data strobe (signal)	ดาตาสโตรบ
delay time	ดีเลย์ไทม์
digital electronic	ดิจิตัลอีเล็คทรอนิคส์
diskette	ดิสเก็ตท์
DMA (Direct Memory Access)	ดีเอ็มเอ
driver (circuit, program)	ไดรเวอร์
duplex	ดูเพล็กซ์
EBCDIC	เอ็บซีดิก
ECMA-34	อีซีเอ็มเอ -34
edit	อีดิท
electron beam	ลำอีเล็คตรอน
emulate	อีมูเลท
ENTER+ key	แป้นเอ็นเตอร์ +
ENTER- key	แป้นเอ็นเตอร์ -
EPROM (Erasable - Programmable Read-Only Memory)	อีพร็อม
equipment number	อีควิปเมนท์นัมเบอร์
error voltage	เออเรอร์โวลเตจ
ESC key (Escape)	แป้นอีเอสซี
ETX key (End of Text)	แป้นอีทีเอ็กซ์
EVFU (Electronic Vertical Format Unit)	อีวีเอฟยู
execute	เอ็กซีคิวท์
field	ฟิลด์
filter (circuit)	ฟิลเตอร์

firmware	เฟิร์มแวร์
flexible disk (diskette,floppy disk)	เฟล็กซิเบิลดิสก์
flexible disk drive	เครื่องบันทึกและอ่านเฟล็กซิเบิลดิสก์
flip-flop (chip, circuit)	ฟลิป- ฟล็อป
font	ฟอนท์
format	ฟอร์แมท
format effector (code)	รหัสที่มีผลต่อฟอร์แมท
format register	ฟอร์แมทรีจิสเตอร์
format tape	ฟอร์แมทเทป
format tape reader	ฟอร์แมทเทปรีเดอร์
framing error	เฟรมมิงเออเรอร์
full duplex	ฟูลดูเพล็กซ์
function	ฟังก์ชัน
function decoder (circuit)	ฟังก์ชันดีโคเดอร์
function register	ฟังก์ชันรีจิสเตอร์
gate (chip, circuit)	เกท
half duplex	ฮาร์ฟดูเพล็กซ์
hammer	แฮมเมอร์
hammer driver (circuit)	แฮมเมอร์ไดรเวอร์
handshake	แฮนด์เชค
hardware	ฮาร์ดแวร์
high voltage	แรงดันไฟสูง
highlight control (circuit)	ไฮไลท์คอนโทรล
home (position)	โฮม
home mark	โฮมมาร์ก

home mark sensor	โฮมมาร์คเซนเซอร์
horizontal control (circuit)	ฮอริซอนทัลคอนโทรล
horizontal counter (circuit)	ฮอริซอนทัลเคาน์เตอร์
horizontal sync (signal)	ฮอริซอนทัลซิงค์
I/O port	ไอโอพอร์ท
IBM	ไอบีเอ็ม
IC (Integrated circuit)	ไอซี
information separator (code)	รหัสที่ใช้เป็นตัวแยกข้อมูล
input	อินพุท
instruction	คำสั่ง
Intel	อินเทล
interface	อินเตอร์เฟส
interlock	อินเตอร์ล็อก
interrupt	อินเตอร์รัป
jumper	จัมเปอร์
keyboard	คีย์บอร์ด
keyboard display terminal	ระบบจอภาพ
keyboard encoder (chip,circuit)	คีย์บอร์ดเอ็นโคเดอร์
kilobyte	กิโลไบท์
latch (chip, circuit)	แล็ทช์
level (signal)	ระดับ
line clear (circuit)	ลายน์เคลียร์
LINE FEED key	แป้นลายน์ฟีด
line printer	เครื่องพิมพ์บรรทัด
line ready (signal)	ลายน์เรดี

local	โลกัล
loop back	ลูปแบ็ก
lo intensity (field)	จาง
LSI (Large Scale Integrated Circuit)	แอลเอสไอ
macro memory	แมโครเมโมรี
magnetic tape transport	เครื่องบันทึกและอ่านเทปแม่เหล็ก
main timing counter (circuit)	เมนไทมิงเคาน์เตอร์
master clear	มาสเตอร์เคลียร์
master console	มาสเตอร์คอนโซล
matrix printer	เครื่องพิมพ์ระบบจุดแมทริกซ์
megabyte	ล้านไบท์
megahertz	เมกะเฮิตซ์
memory	หน่วยความจำ
memory address conversion (circuit)	เม โมรีแอ็ดเดรสคอนเวอชัน
micro memory	ไมโครเมโมรี
micro program	ไมโครโปรแกรม
microprocessor	ไมโครโปรเซสเซอร์
millisecond	มิลลิวินาที
minicomputer	คอมพิวเตอร์ขนาดเล็ก
modem	โมเด็ม
modem control (circuit)	โมเด็มคอนโทรล
monostable multivibrator	โมโนสเตเบิลมัลติไวเบรเตอร์
MOS (Metal Oxide Semiconductor)	มอส
multiplexer	มัลติเพล็กเซอร์
multivibrator	มัลติไวเบรเตอร์

N-key rollover	เอ็นคีย์โรลโอเวอร์
nanosecond	นาโนวินาที
NRZI (Non-return to Zero Inverted)	เอ็นอาร์แซดไอ
numeric	ตัวเลข
on-line	ออนลายน์
one's complement	วันส์คอมพลีเมนท์
operating system	โปรแกรมควบคุมการทำงาน
oscillator	ออสซิลเลเตอร์
overlap seek	โอเวอร์แล็บซีค
output	เอาท์พุท
pack	แพ็ก
page	เพจ
PAGE key	แป้นเพจ
parallel load	พาราลแลลโหลด
parity	พาริตี
parity bit	พาริตีบิท
pattern	แพ็ตเทอน
PE (Phase Encoded)	พีอี
period	คาบ
peripheral controller	เพอริเฟอรัลคอนโทรล์เลอร์
peripheral device	เพอริเฟอรัลดีไวซ์
phase lock	เฟสล็อค
power supply	แหล่งจ่ายไฟ
priority	ระดับความสำคัญ

printable code	ปรินเอเบิลโคด
printed wiring assembly	แผ่นวงจร
pulse	พัลซ์
Q register	คิวรีจิสเตอร์
RAM (Random-Accessed Memory)	แร็ม
read-write control (circuit)	รีดไรท์คอนโทรล
ready (signal)	เรดี
receiver (chip, circuit)	วงจรรับข้อมูล
rectifier(circuit)	เร็กติฟายเออร์
regulator (chip, circuit)	เรกูเลเตอร์
reject	รีเจ็กท์
REPEAT key	แป้นรีพีท
reply	รีพลาย
reset	รีเซท
RESET key	แป้นรีเซท
rewind	รีวายด์
ROM (Read-Only Memory)	รอม
RS-232C	อาร์เอส-232 ซี
scan	สแกน
scan counter (circuit)	สแกนเคาน์เตอร์
scroll	สโครล
scroll control (circuit)	สโครลคอนโทรล
sector	เซ็กเตอร์
serial (communication,load)	ซีเรียล

servo phase-lock loop	เซอร์โวเฟสล็อกลูป
SHIFT key	แป้นชิฟท์
SHIFT LOCK key	แป้นชิฟท์ล็อก
shift register	ชิฟท์รีจิสเตอร์
slot	สล็อต
software	ซอฟท์แวร์
solinoid	โซลีนอยด์
sort	ซอต
special character	ตัวอักษรพิเศษ
square wave	สแควร์เวฟ
stable	สเตเบิล
start bit	สตาร์ทบิท
static RAM	สแตติคแร็ม
status	สเตตัส
status register	สเตตัสรีจิสเตอร์
stop bit	สต็อปบิท
storage module drive	เครื่องบันทึกและอ่านจานแม่เหล็ก
strobe (signal)	สโตรบ
subroutine	ซับรูทีน
synchronize	ซิงโครไนซ์
teletypewriter	เครื่องโทรพิมพ์
terminator (code)	เทอร์มิเนเตอร์
timer (chip, circuit)	ไทเมอร์
timing	ไทมิง
track	แทร็ค

transfer rate	ความเร็วในการส่งผ่านข้อมูล
transform	ทรานสฟอร์ม
transmitter (chip, circuit)	วงจรส่งข้อมูล
tristate bus	ไตรสเตทบัส
TTL (Transistor - Transistor Logic)	ทีทีแอล
two's complement	ทูส์คอมพลีเมนท์
UART (Universal Asynchronous Receiver - Transmitter)	ยูอาร์ต
Unit	ยูนิต
Unit load	ยูนิตโหลด
utility program	ยูทิลิตี้โปรแกรม
verify	เวอร์ฟาย
version	เวอร์ชัน
vertical address counter (circuit)	เวอร์ติกัลแอ็ดเดรสเคาน์เตอร์
vertical control (circuit)	เวอร์ติกัลคอนโทรล
vertical counter (circuit)	เวอร์ติกัลเคาน์เตอร์
vertical motor	เวอร์ติกัลมอเตอร์
vertical reader	เวอร์ติกัลรีเดอร์
vertical sync (signal)	เวอร์ติกัลซิงค์
vertical tabulation	เวอร์ติกัลแทบูเลชัน
vidio display assembly	ส่วนแสดงภาพ
vidio display unit	หน่วยแสดงภาพ
vidio driver (circuit)	วิดีโอไดรเวอร์
Western Digital	เวสเทอนดิจิตัล
width (pulse)	ช่วงกว้าง
word length	ความยาวของข้อมูล
yoke	โยค

ประวัติผู้เขียน

นายไตรรัตน์ ใจสำราญ เกิดเมื่อวันที่ 12 พฤษภาคม พ.ศ.2497 ที่กรุงเทพฯ สำเร็จปริญญา B.S.E.E. จาก Mapua Institute of Technology กรุงมนิลา ประเทศฟิลิปปินส์ ในปี พ.ศ.2519 เคยเขียนบทความลงในวารสารอีเลคทรอนิคส์ ของชุมนุมวิชาการ คณะวิศวกรรมศาสตร์ จุฬาลงกรณ์มหาวิทยาลัย ฉบับที่ 1 ถึงฉบับที่ 4 เข้าศึกษาต่อในระดับปริญญามหาบัณฑิต ที่ภาควิชาวิศวกรรมคอมพิวเตอร์ คณะวิศวกรรมศาสตร์ จุฬาลงกรณ์มหาวิทยาลัย ในปี พ.ศ.2520 ปัจจุบันเป็นวิศวกรประจำระบบคอมพิวเตอร์ขนาดเล็ก ที่บริษัทคอนโทรลดาต้า (ประเทศไทย) จำกัด