เอกสารอ้างอิง

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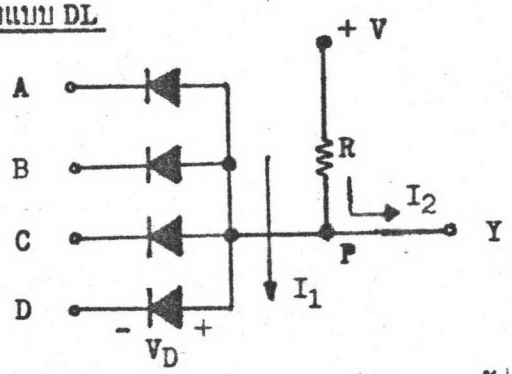
ภาคผนวก ก.

การคำนวนหาค่าความต้านทานโดยประมาณในวงจรลอจิคเกทแบบ

AND เกทแบบ DL



รูป ก.

วงจรพื้นฐานแสดงดังรูป ก. ในวงจรนี้ค่าความต้านทานสามารถหาได้โดยกำหนดให้

อินพุท D มีสัญญานลอจิคเป็น "0"

อินพุท A,B,C มีสัญญานลอจิคเป็น "1"

เพราะฉนั้นเอาท์พุทจะมีสัญญานลอจิคเป็น "0" ดังนั้นกระแสจะแยกไหลเป็นสองทางดังรูป และเนื่องจากอินพุทและเอาท์พุทของวงจรนี้ต่อร่วมกับวงจรไอซีเบอร์ 4040 ดังนั้นกระแส I และ I จะเป็นกระแสซิงค์(sink current)ที่ไหลเข้าไปยังไอซี

จากคู่มือการใช้งานของ 4040 กำหนดว่า

เมื่อ V_{DD} = 5 โวลท์

V_{OL} = 0.4โวลท์

I_{OL} = 0.5มิลลิแอมป์

แรงดันที่จุด P = $V_D + V_{OL}$

= 0.65 + 0.4

= 1.05โวลท์

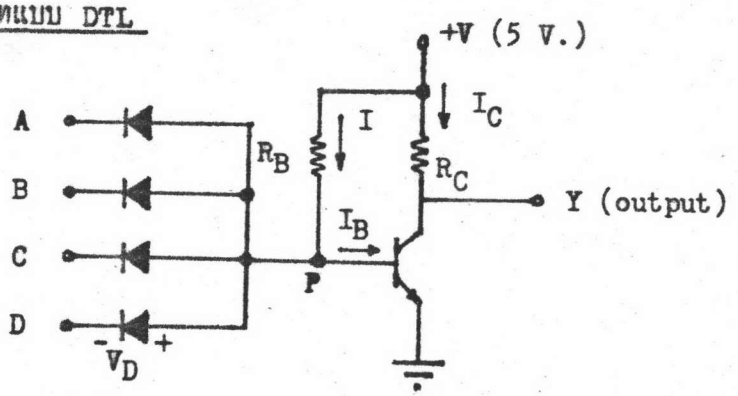
เพราะฉนั้นความต้านทานต่ำสุด (R_{min}) $= (V - V_P)/I$

$= (5 - 1.05)/I$

$= 3.95/0.5$ (กำหนด $I = 0.5$ mA)

$= 7.9$ กิโลโอห์ม

NAND เกทแบบ DTL



ค่า R_B และ R_C หาได้โดยกำหนดให้

อินพุท A,B,C มีลอจิคเป็น "1"

อินพุท D มีลอจิคเป็น "0"

เพราะฉนั้นเอาท์พุทจะมีลอจิคเป็น "1" นั่นคือทรานซิสเตอร์ OFF ($I_C = I_B = 0$) ดังนั้นกระแส I จะไหลผ่านไดโอดของอินพุท D ในกรณีนี้จะกำหนดให้ I_{OL} มีค่าต่ำกว่าในคู่มือการใช้งานเพื่อให้ค่า V_{OL} มีค่าเกือบเป็นศูนย์ เพราะฉนั้น $V_P = V_D = 0.65$ โวลท์ ($V_{OL} = 0$)

กำหนดให้ $I_{OL} = 0.1$ มิลลิแอมป์

เพราะฉนั้น $R_B(min.) = (V - V_P)/I_{OL}$

$.= (5 - 0.65)/0.1$

$= 43.5$ กิโลโอห์ม

เลือกใช้ $R_B = 47$ กิโลโอห์ม

ค่าต้านทาน R_C หาได้โดยเมื่อทรานซิสเตอร์ ON กระแส I_C (กระแส I_C เท่ากับกระแสที่ไหลมายังเอาท์พุทรวมกับกระแสไหลผ่านทรานซิสเตอร์) ควรมีค่าไม่เกิน

หนึ่งมิลลิแอมป์ ดังนั้น $R_C = (V - V_{CE(Sat.)})/I_C$

$R_{C(min)} = (5 - 0.2)/1\ mA$

$= 4.8$ กิโลโอห์ม

เลือกใช้ $= 5.6$ กิโลโอห์ม

เมื่อหาค่าความต้านทานทั้งสองได้แล้วจำเป็นต้องตรวจสอบดูว่า วงจรนี้สามารถทำงานได้จริง วิธีตรวจสอบทำโดยการสมมติเมื่อทรานซิสเตอร์อยู่ในสภาวะ ON ดังนั้น กระแส I_C จะเท่ากับ

$I_C = (5 - 0.2)/5.6k$

$= 0.857$ มิลลิแอมป์

$I_B = I_C/H_{FE(min)}$; $H_{FE} = 110$

$= 0.008$ มิลลิแอมป์

แต่ในวงจรที่ใช้ I_B มีค่า $= (5 - 0.8)/47k$

$= 0.089$ มิลลิแอมป์

เพราะฉนั้นจะเห็นว่าค่าของกระแส I_B ภายในวงจรมีค่ามากเกินกว่าค่าที่กำหนดไว้ สรุปได้ว่าทรานซิสเตอร์อยู่ในสภาวะ ON จริงและวงจรนี้สามารถทำงานได้จริง.

ภาคผนวก ข.

คู่มือการใช้งานของวงจรไอซีเบอร์ต่างๆที่ใช้ในการออกแบบ

SCL4001UB CMOS NOR GATE (Unbuffered)

FEATURES

- Unbuffered Outputs for Quasi-Linear Applications
- Quad 2-Input NOR Configuration
- Diode Protection on all Inputs
- Output Drive Current Compatible with "B" Series
- Pin Compatible with Buffered SCL4001B
- Balanced Output Drive Current Specifications

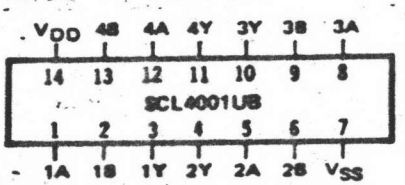
DESCRIPTION

The SCL4001UB consists of four positive-logic NOR gates. The outputs are unbuffered, making the device suitable for quasi-linear applications, such as gated oscillators, multivibrators, and pulse shaping circuits.

For digital applications, the buffered SCL4001B is recommended for its higher gain and input pattern insensitivity.

CONNECTION DIAGRAM

(all packages)



Add suffix for package:

C	14-pin Cerdip
D	14-pin Ceramic
E	14-pin Epoxy
F	14-pin Flat
H	Chip

TRUTH TABLE

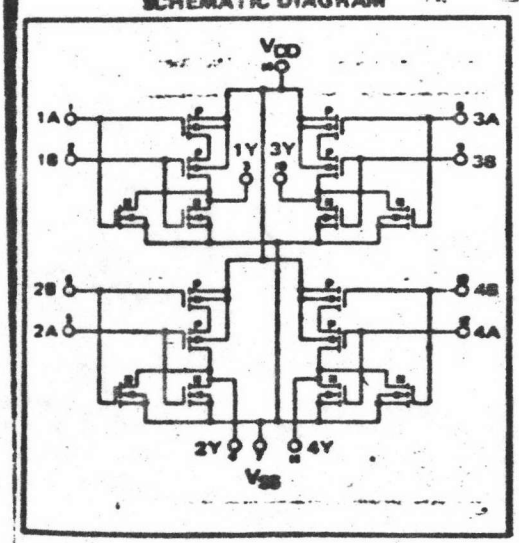
Inputs	Output
0 0	1
All other combinations	0

RECOMMENDED OPERATING CONDITIONS

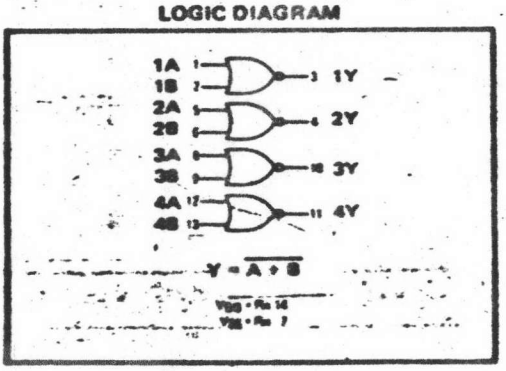
For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

SCHEMATIC DIAGRAM



LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS

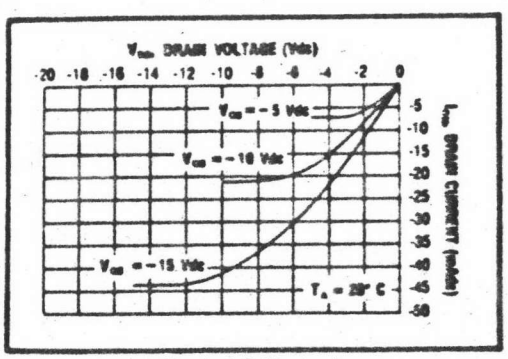
STATIC CHARACTERISTICS [1]

PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW} [2] Min.	T_{LOW} [2] Max.	+25°C Min.	+25°C Typ.	+25°C Max.	T_{HIGH} [2] Min.	T_{HIGH} [2] Max.	Units
QUIESCENT DEVICE CURRENT	I_{DD}	5	$V_{IN} = V_{SS}$ or V_{DD}	–	0.05	–	0.0005	0.05	–	1.5	μAdc
		10	All valid input	–	0.10	–	0.001	0.10	–	3.0	
		15	combinations	–	0.20	–	0.002	0.20	–	6.0	

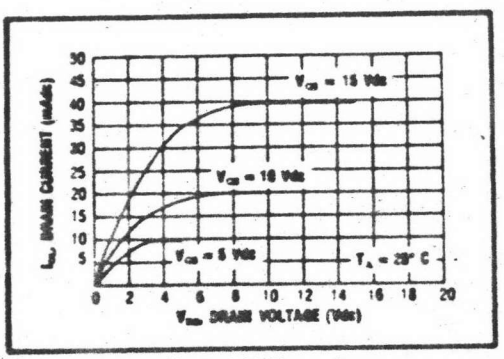
NOTES: [1] Remaining Static Electrical Characteristics are listed under "SCL4000B Series Family Specifications".
[2] T_{LOW} = -55°C for C, D, F, H device.
= -40°C for E device.
T_{HIGH} = +125°C for C, D, F, H device.
= + 85°C for E device.
[3] This device has been designed for balanced output drive current specifications. Consult Family Specifications.

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V_{DD} (Vdc)	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME	t_{PLH}, t_{PHL}	5	–	75	150	ns
		10	–	35	70	
		15	–	25	50	
OUTPUT TRANSITION TIME	t_{TLH}, t_{THL}	5	–	100	200	ns
		10	–	50	100	
		15	–	40	80	



Typical P-Channel
Source Current Characteristics



Typical N-Channel
Sink Current Characteristics

SCL4009UB Inverting
SCL4010B Non-Inverting

CMOS
HEX BUFFERS/CONVERTERS

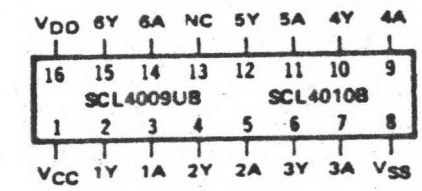
FEATURES

- Direct Drive of 2 TTL/DTL Loads
- Operation from Single or Dual Supplies
- All Inputs Diode-Protected

DESCRIPTION

The SCL4009UB and SCL4010B are single-chip monolithic silicon integrated circuits containing eighteen N-Channel and twelve P-Channel enhancement-mode MOS transistors connected to form six independent buffer/converter configurations. These devices are designed for use as hex CMOS-to-DTL or TTL logic level converters or hex CMOS current drivers. Conversion ranges are from CMOS logic operating at 3Vdc to 18Vdc supply levels to DTL or TTL logic operating at 3Vdc to 6Vdc supply levels. Conversion to logic output levels greater than 6Vdc is permitted proving $V_{CC} \leq V_{DD}$.

CONNECTION DIAGRAM
(all packages)



Add Suffix for Package:

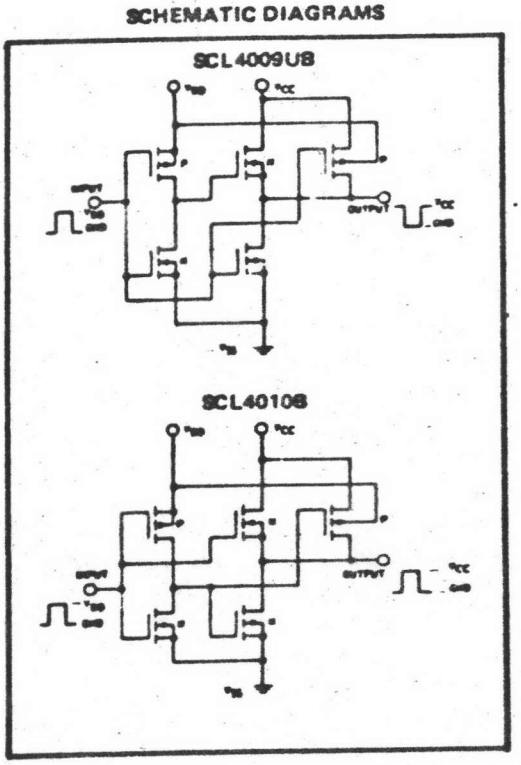
- C 16-pin Cerdip
- D 16-pin Ceramic
- E 16-pin Epoxy
- F 16-pin Flat
- H Chip

RECOMMENDED OPERATING CONDITIONS

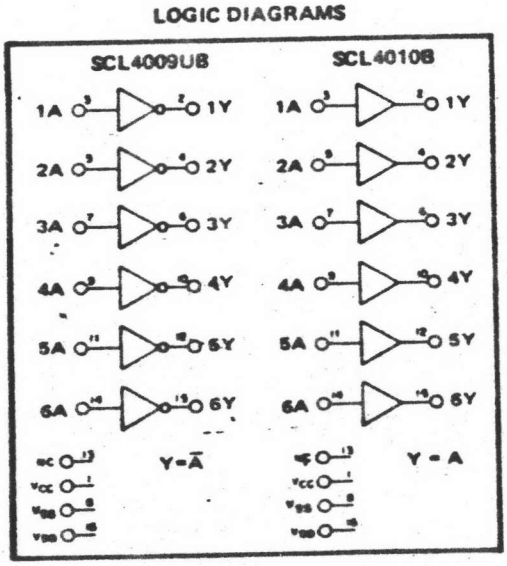
For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
	$V_{CC} - V_{SS}$	3 to 15	Vdc
	$V_{CC} \leq V_{DD}$		
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

SCHEMATIC DIAGRAMS



LOGIC DIAGRAMS



ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS [1,3]

PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW}[2]		+25°C			T_{HIGH}[2]		Units
				Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I_{DD}	5	V_{IN} = V_{SS} or V_{DD}	–	1.0	–	0.005	1.0	–	30	µAdc
		10	All valid input	–	2.0	–	0.01	2.0	–	60	
		15	combinations	–	4.0	–	0.02	4.0	–	120	
MINIMUM INPUT HIGH VOLTAGE SCL4009UB	V_{IH}	5	V_{OL} = 0.5V	–	4.0	–	2.75	4.0	–	4.0	Vdc
		10	V_{OL} = 1.0V	–	8.0	–	5.5	8.0	–	8.0	
		15	V_{OL} = 1.5V	–	12.0	–	8.25	12.0	–	12.0	
			I_O < 1µA								
MAXIMUM INPUT LOW VOLTAGE SCL4009UB	V_{IL}	5	V_{OH} = 3.6V	1.0	–	1.0	2.25	–	1.0	–	Vdc
		10	V_{OH} = 7.2V	2.0	–	2.0	4.5	–	2.0	–	
		15	V_{OH} = 10.8V	3.0	–	3.0	6.75	–	3.0	–	
			I_O < 1µA								
OUTPUT LOW (SINK) CURRENT C, D, F, H device	I_{OL}	5	V_{OL} = 0.4V	3.8	–	3.0	4.0	–	2.2	–	mAdc
		10	V_{OL} = 0.5V	10.0	–	8.0	10	–	5.6	–	
		15	V_{OL} = 1.5V	30	–	24	36	–	16	–	
			V_{IN} = V_{SS} or V_{DD}								
E device		5	V_{OL} = 0.4V	3.6	–	3.0	4.0	–	2.4	–	mAdc
		10	V_{OL} = 0.5V	9.6	–	8.0	10	–	6.4	–	
		15	V_{OL} = 1.5V	28	–	24	36	–	20	–	
			V_{IN} = V_{SS} or V_{DD}								

NOTES: [1] Remaining Static Electrical Characteristics are listed under "SCL4000B Series Family Specifications".
[2] T_{LOW} = -55°C for C, D, F, H device
= -40°C for E device.
T_{HIGH} = +125°C for C, D, F, H device
= + 85°C for E device.
[3] V_{CC} = V_{DD}

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V_{DD} (Vdc)	V_{CC} (Vdc)	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME Driving CMOS	t_{PLH}	5	5	–	60	120	ns
		10	10	–	35	70	
		15	15	–	28	56	
Driving TTL/DTL		5	5	–	45	90	ns
		10	5	–	20	40	
		15	5	–	15	30	
Driving CMOS	t_{PHL}	5	5	–	30	60	ns
		10	10	–	18	36	
		15	15	–	12	24	
Driving TTL/DTL		5	5	–	35	70	ns
		10	5	–	15	30	
		15	5	–	10	20	
OUTPUT TRANSITION TIME	t_{TLH}	5	5	–	150	300	ns
		10	10	–	75	150	
		15	15	–	60	120	
	t_{THL}	5	5	–	30	60	ns
		10	10	–	20	40	
		15	15	–	12	24	
INPUT CAPACITANCE SCL4009UB	C_{IN}	–	–	–	10	15	pF
SCL4010B		–		–	5	7.5	

SCL4011UB

CMOS NAND GATE (Unbuffered)

FEATURES

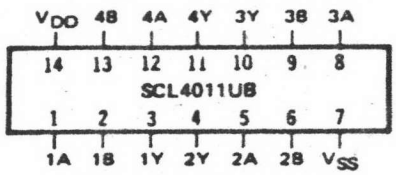
- Unbuffered Outputs for Quasi-Linear Applications
- Quad 2-Input NAND Configuration
- Diode Protection on all Inputs
- Output Drive Current Compatible with "B" Series
- Pin Compatible with Buffered SCL4011B
- Balanced Output Drive Current Specifications

DESCRIPTION

The SCL4011UB consists of four positive-logic NAND gates. The outputs are unbuffered, making the device suitable for quasi-linear applications, such as gated oscillators, multivibrators, and pulse shaping circuits.

For digital applications, the buffered SCL4011B is recommended for its higher gain and input pattern insensitivity.

CONNECTION DIAGRAM
(all packages)



Add suffix for package:

--- C 14-pin Cerdip
D 14-pin Ceramic
E 14-pin Epoxy
F 14-pin Flat
H Chip

TRUTH TABLE

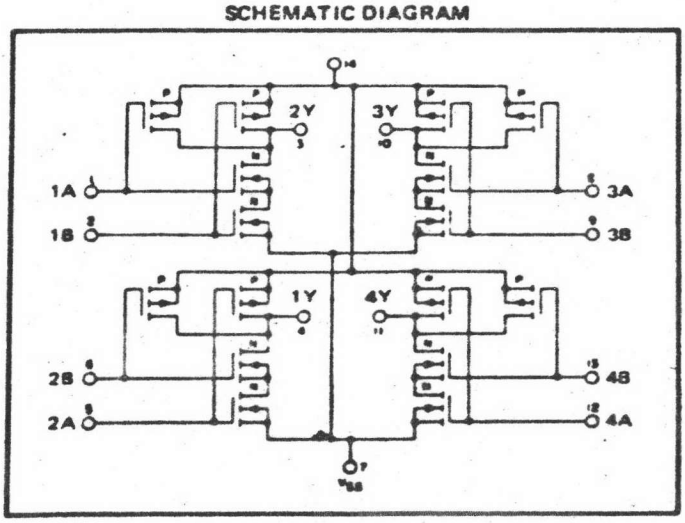
Inputs	Output
1 1	0
All other combinations	1

RECOMMENDED OPERATING CONDITIONS

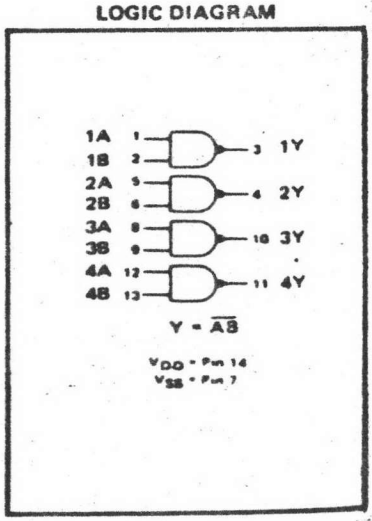
For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

SCHEMATIC DIAGRAM



LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS

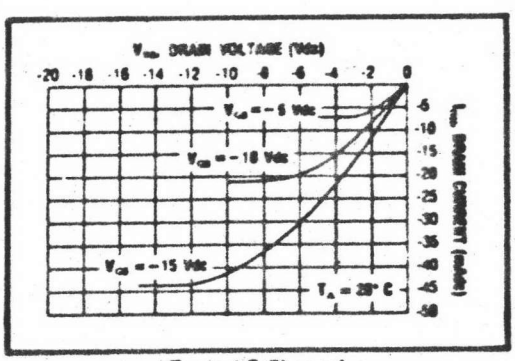
STATIC CHARACTERISTICS [1, 3]

PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW} [2]		+25°C			T_{HIGH} [2]		Units
				Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I_{DD}	5	$V_{IN} = V_{SS}$ or V_{DD}	–	0.05	–	0.0005	0.05	–	1.5	μAdc
		10	All valid input	–	0.10	–	0.001	0.10	–	3.0	
		15	combinations	–	0.20	–	0.002	0.20	–	6.0	

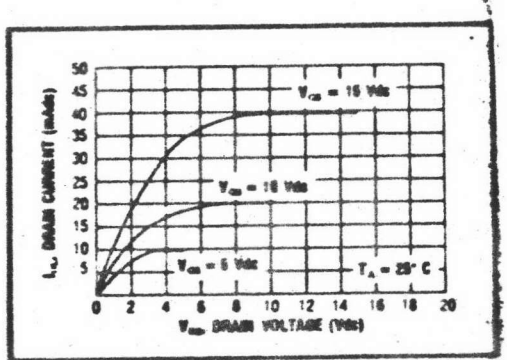
NOTES: [1] Remaining Static Electrical Characteristics are listed under "SCL4000B Series Family Specifications".
[2] T_{LOW} = -55°C for C, D, F, H device.
= -40°C for E device.
T_{HIGH} = +125°C for C, D, F, H device.
= + 85°C for E device.
[3] This device has been designed for balanced output drive current specifications. Consult Family Specifications.

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V_{DD} (Vdc)	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME	t_{PLH}, t_{PHL}	5	–	75	150	ns
		10	–	35	70	
		15	–	25	50	
OUTPUT TRANSITION TIME	t_{TLH}, t_{THL}	5	–	100	200	ns
		10	–	50	100	
		15	–	40	80	



Typical P-Channel
Source Current Characteristics



Typical N-Channel
Sink Current Characteristics

SCL4016AB

CMOS QUAD ANALOG SWITCH

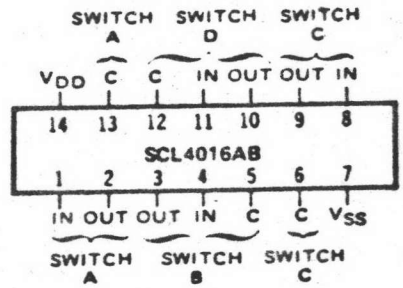
FEATURES

- Wide Range of Digital and Analog Signal Levels-Digital or Analog Signals to 18 Volts peak
- Low ON Resistance — 200 Ω typ. over 15Vp-p Signal Input Range, @ 15Vdc
- Matched Switch Characteristics - 10Ω typ. Difference between R_{ON} Values at a Fixed Bias Point over 15Vp-p Signal Input Range @ 15Vdc
- High On/Off Output Voltage Ratio – 65 dB typ. @ f_{is} = 10kHz, R_L = 10KΩ
- High degree of Linearity - ≤ 0.4% Distortion typ. @ f_{is} = 1kHz, V_{is} = $5V_{p-p}$, V_{DD}-V_{SS}≥10V, R_L = 10kΩ
- Extremely Low OFF Switch Leakage Resulting in Very Low Offset Current and High Effective OFF resistance - 10pA typ. @ V_{DD}-V_{SS} = 10V, T_A = 25°C
- Extremely High Control Input Impedance (Control Circuit Isolated from Signal Circuit) - 10^{12}Ω typ.
- Low Crosstalk between Switches - -50dB typ. @ f_{is} = 0.9MHz, R_L = 1kΩ
- Matched Control-Input to Signal-Output Capacitances - Reduces Output Signal Transients
- Transmits Frequencies up to 40MHz

DESCRIPTION

The SCL4016AB is a single-chip monolithic silicon integrated circuit containing eight N-channel and eight P-channel enhancement-mode MOS transistors connected to form four independent bilateral signal switches. Each switch consists of both P- and N-channel devices with common source and drain connections. A single control signal is required per switch. Both P and N devices in a given switch are biased ON or OFF by the control signal. The CMOS switch permits peak input-signal voltage swings equal to the full supply voltage, a considerable advantage over single-channel types.

CONNECTION DIAGRAM
(all packages)



Add suffix for package:

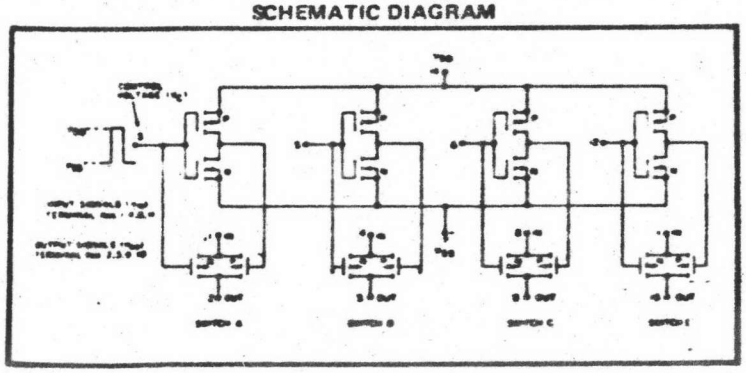
C	14-pin Cerdip
D	14-pin Ceramic
E	14-pin Epoxy
F	14-pin Flat
H	Chip

RECOMMENDED OPERATING CONDITIONS

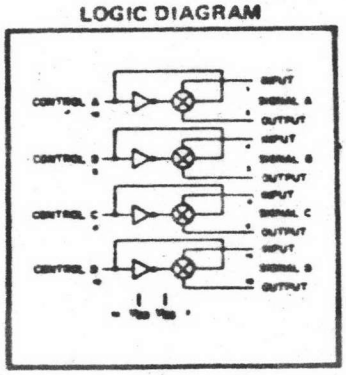
For maximum reliability:

DC Supply Voltage	V_{DD} - V_{SS}	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

SCHEMATIC DIAGRAM



LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS[1,2]

PARAMETER		CONDITIONS	V_{SS} (Vdc)	V_{DD} (Vdc)	T_{LOW}[3] Min.	T_{LOW}[3] Max.	25°C Min.	25°C Typ.	25°C Max.	T_{HIGH}[3] Min.	T_{HIGH}[3] Max.	Units
QUIESCENT DEVICE CURRENT	I_{DD}	V_{IN} = V_{SS} or V_{DD} All valid input combinations	0 0 0	5 10 15	–	0.05 0.1 0.2	–	0.0005 0.001 0.002	0.05 0.1 0.2	–	15 30 60	µAdc
MINIMUM INPUT HIGH VOLTAGE (Control Input)	V_{IH}	V_{IS} = V_{SS} V_{OS} = V_{DD} I_{OS} = 10µA	0 0 0	5 10 15	– – –	2.9 2.9 2.9	– – –	1.5 1.5 1.5	2.9 2.7 2.7	– – –	2.4 2.4 2.4	Vdc
MAXIMUM INPUT LOW VOLTAGE (Control Input)	V_{IL}	V_{IS} = V_{SS} V_{OS} = V_{DD} I_{OS} = 10µA	0 0 0	5 10 15	0.9 0.9 0.9	– – –	0.7 0.7 0.7	1.5 1.5 1.5	– – –	0.4 0.4 0.4	– – –	Vdc
SWITCH INPUT/OUTPUT LEAKAGE (Switch off)	I_{OFF}	V_C = V_{SS}	V_{IS} (Vdc)									
			±7.5	7.5	+7.5	–	±250	–	±0.1	±250	–	±2500	nAdc
			±5	5	+5	–	±125	–	±0.01	±125	–	±1250	
ON RESISTANCE C, D, F, H device	R_{ON}	V_C = V_{DD} R_L = 10kΩ	V_{IS} (Vdc)									
			+7.5	-7.5	+7.5	–	380	–	200	400	–	600	Ω
			-7.5			–	380	–	200	400	–	600	
			±0.25			–	775	–	280	850	–	1230	
			+5	-5	+5	–	600	–	250	660	–	980	Ω
			-5			–	600	–	250	660	–	980	
			±0.25			–	1870	–	580	2000	–	2600	
			+15	0	+15	–	380	–	200	400	–	600	Ω
			+0.25			–	380	–	200	400	–	600	
			+9.3			–	775	–	300	850	–	1230	
			+10	0	+10	–	600	–	250	660	–	980	Ω
			+0.25			–	600	–	250	660	–	980	
			+5.6			–	1870	–	580	2000	–	2600	
E device	R_{ON}	V_C = V_{DD} R_L = 10kΩ	V_{IS} (Vdc)									
			+7.5	-7.5	+7.5	–	370	–	200	400	–	520	Ω
			-7.5			–	370	–	200	400	–	520	
			±0.25			–	790	–	280	850	–	1080	
			+5	-5	+5	–	610	–	250	660	–	840	Ω
			-5			–	610	–	250	660	–	840	
			±0.25			–	1900	–	580	2000	–	2380	
			+15	0	+15	–	370	–	200	400	–	520	Ω
			+0.25			–	370	–	200	400	–	520	
			+9.3			–	790	–	300	850	–	1080	
			+10	0	+10	–	610	–	250	660	–	840	Ω
			+0.25			–	610	–	250	660	–	840	
			+5.6			–	1900	–	580	2000	–	2380	
ON RESISTANCE MATCH (Same package)	ΔR_{ON}	V_C = V_{DD} R_L = 10kΩ	V_{IS} (Vdc)									
			±7.5	7.5	+7.5	–	–	–	10	–	–	–	Ω
			±5	5	+5	–	–	–	15	–	–	–	

NOTES: [1] Remaining Static Electrical Characteristics are listed under "SCL4000B Series Family Specifications".
[2] T_{LOW} = -55°C for C, D, F, H device.
= -40°C for E device
T_{HIGH} = +125°C for C, D, F, H device.
= + 85°C for E device.
[3] This device has been designed for balanced output drive current specifications. Consult Family Specifications.

DYNAMIC CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

PARAMETER		CONDITIONS		V_{SS} (Vdc)	V_{DD} (Vdc)	Min.	Typ.	Max.	UNIT
SIGNAL INPUTS (V_{IS}) AND OUTPUTS (V_{OS})									
PROPAGATION DELAY TIME Signal input to signal output	t_{PLH}, t_{PHL}	V_C = V_{DD} V_{IS} = square wave R_L = 10kΩ		0 0 0	5 10 15	– – –	20 10 7.5	40 20 15	ns
BANDWIDTH (-3dB) (Sine Wave)	BW	V_C = V_{DD} V_{IS} = $5V_{p-p}$ centered @0.0Vdc	R_L 1kΩ 10kΩ 100kΩ 1MΩ	5	+5	– – – –	54 40 38 37	– – – –	MHz

SCL4022AB

CMOS OCTAL COUNTER/DIVIDER

FEATURES

- Eight Decoded Outputs
- Direct Reset
- Trigger from either Edge of Clock Input
- Carry Output for Cascading Stages
- Fully Static Operation - DC to 5MHz @ 10Vdc

DESCRIPTION

The SCL4022AB consists of a 4-stage Johnson Divide-by-8 Counter and an Output Decoder. Inputs include Clock, Reset, and Clock Enable signals.

The counter has interchangeable Clock and Clock Enable lines for incrementing on either a positive-going or negative-going transition, respectively. A high Reset signal clears the counter to its zero count.

Use of the Johnson divide-by-eight counter configuration permits high-speed operation, 2-input decode gating, and spike-free decoded outputs. Anti-lock gating is provided, thus assuring proper counting sequence. The 8 decoded outputs are normally low and go high only at their respective decoded time slot. Each decoded output remains high for one full clock cycle. A Carry-out (C_{OUT}) signal completes one cycle every 8 clock input cycles and is used to directly clock the succeeding counter in multi-stage applications.

This part can be used in frequency division circuits as well as octal counter or octal decode display applications.

FUNCTIONAL TRUTH TABLE

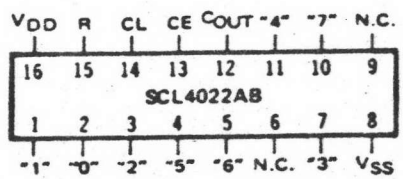
(Positive Logic)

Clock	Clock Enable	Reset	Output = n
0	X	0	n
X	1	0	n
⌐	0	0	n + 1
⌐	X	0	n
1	⌐	0	n + 1
X	⌐	0	n
X	X	1	"0"

X Don't Care If n < 4 Carry = 1, otherwise = 0

CONNECTION DIAGRAM

(all packages)



Add suffix for package:

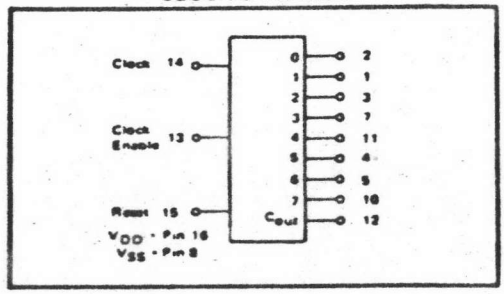
- C 16-pin Cerdip
- D 16-pin Ceramic
- E 16-pin Epoxy
- F 16-pin Flat
- H Chip

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS [1]

PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW} [2] Min.	T_{LOW} [2] Max.	+25°C Min.	+25°C Typ.	+25°C Max.	T_{HIGH} [2] Min.	T_{HIGH} [2] Max.	Units
QUIESCENT DEVICE CURRENT	I_{DD}	5	$V_{IN} = V_{SS}$ or V_{DD}	–	5	–	0.05	5	–	150	μAdc
		10	All valid input	–	10	–	0.1	10	–	300	
		15	combinations	–	20	–	0.2	20	–	600	
OUTPUT HIGH (SOURCE) CURRENT C, D, F, H device: Decoded Outputs	I_{OH}	5	$V_{OH} = 4.6V$	-0.05	–	-0.04	-0.3	–	-0.028	–	mAdc
		10	$V_{OH} = 9.5V$	-0.125	–	-0.1	-0.75	–	-0.07	–	
		15	$V_{OH} = 13.5V$ $V_{IN} = V_{SS}$ or V_{DD}	-0.375	–	-0.3	-2.5	–	-0.21	–	
Carry Output		5	$V_{OH} = 4.6V$	-0.25	–	-0.2	-0.75	–	-0.14	–	mAdc
		10	$V_{OH} = 9.5V$	-0.62	–	-0.5	-1.1	–	-0.35	–	
		15	$V_{OH} = 13.5V$ $V_{IN} = V_{SS}$ or V_{DD}	-1.9	–	-1.5	-3.5	–	-1.1	–	
E device: Decoded Outputs	I_{OH}	5	$V_{OH} = 4.6V$	-0.048	–	-0.04	-0.3	–	-0.032	–	mAdc
		10	$V_{OH} = 9.5V$	-0.12	–	-0.1	-0.75	–	-0.08	–	
		15	$V_{OH} = 13.5V$ $V_{IN} = V_{SS}$ or V_{DD}	-0.36	–	-0.3	-2.5	–	-0.24	–	
Carry Output		5	$V_{OH} = 4.6V$	-0.24	–	-0.2	-0.75	–	-0.16	–	mAdc
		10	$V_{OH} = 9.5V$	-0.6	–	-0.5	-1.1	–	-0.4	–	
		15	$V_{OH} = 13.5V$ $V_{IN} = V_{SS}$ or V_{DD}	-1.8	–	-1.5	-3.5	–	-1.2	–	
OUTPUT LOW (SINK) CURRENT C, D, F, H device: Decoded Outputs	I_{OL}	5	$V_{OL} = 0.4V$	0.05	–	0.04	0.4	–	0.028	–	mAdc
		10	$V_{OL} = 0.5V$	0.125	–	0.1	1.0	–	0.07	–	
		15	$V_{OL} = 1.5V$ $V_{IN} = V_{SS}$ or V_{DD}	0.375	–	0.3	3.0	–	0.21	–	
Carry Output		5	$V_{OL} = 0.4V$	0.25	–	0.2	0.75	–	0.14	–	mAdc
		10	$V_{OL} = 0.5V$	0.62	–	0.5	1.3	–	0.35	–	
		15	$V_{OL} = 1.5V$ $V_{IN} = V_{SS}$ or V_{DD}	1.9	–	1.5	4.0	–	1.1	–	
E device: Decoded Outputs	I_{OL}	5	$V_{OL} = 0.4V$	0.048	–	0.04	0.4	–	0.032	–	mAdc
		10	$V_{OL} = 0.5V$	0.12	–	0.1	1.0	–	0.08	–	
		15	$V_{OL} = 1.5V$ $V_{IN} = V_{SS}$ or V_{DD}	0.36	–	0.3	3.0	–	0.24	–	
Carry Output		5	$V_{OL} = 0.4V$	0.24	–	0.2	0.75	–	0.16	–	mAdc
		10	$V_{OL} = 0.5V$	0.6	–	0.5	1.3	–	0.4	–	
		15	$V_{OL} = 1.5V$ $V_{IN} = V_{SS}$ or V_{DD}	1.8	–	1.5	4.0	–	1.2	–	

NOTES: [1] Remaining Static Electrical Characteristics are listed under "SCL4000B Series Family Specifications".

[2] T_{LOW} = -55°C for C, D, F, H device.
= -40°C for E device.
T_{HIGH} = +125°C for C, D, F, H device.
= + 85°C for E device.

SCL4024B

CMOS 7-STAGE BINARY COUNTER

FEATURES

- 7 Fully Static Stages
- Buffered Outputs Available from All Stages
- Common Reset Line
- 8 MHz Counting Rate @ 10Vdc
- All Inputs Buffered

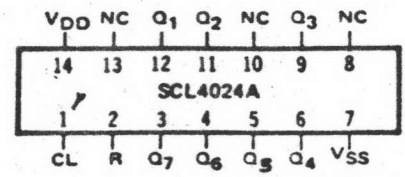
DESCRIPTION

The SCL4024B is a single chip monolithic medium scale integrated circuit containing N-Channel and P-Channel enhancement-mode MOS transistors. Seven single-phase clocked counting stages are provided with the Q output of each stage accessible. The Counter is reset to "zero" by a high level on the Reset input. Each counter stage is a static master-slave flip-flop. The counter state is advanced one count on the negative-going transition of each input pulse.

TRUTH TABLE

Clock	Reset	State
0	0	No Change
0	1	All Outputs Low
1	0	No Change
1	1	All Outputs Low
⌐⌐	0	No Change
⌐⌐	1	All Outputs Low
⌐⌐	0	Advance One Count
⌐⌐	1	All Outputs Low

CONNECTION DIAGRAM
(all packages)



Add suffix for package:

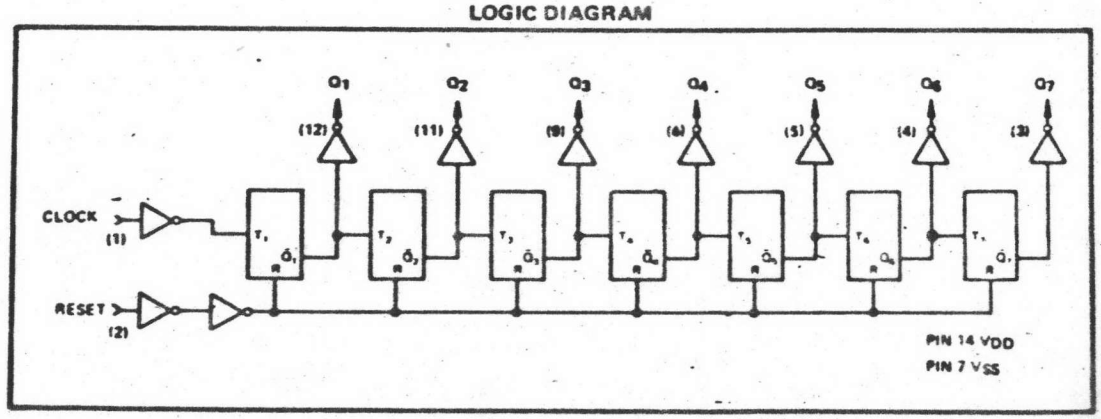
- C 14-pin Cerdip
- D 14-pin Ceramic
- E 14-pin Epoxy
- F 14-pin Flat
- H Chip

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS [1]

PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW} [2] Min.	T_{LOW} [2] Max.	+25°C Min.	+25°C Typ.	+25°C Max.	T_{HIGH} [3] Min.	T_{HIGH} [3] Max.	Units
QUIESCENT DEVICE CURRENT	I_{DD}	5	V_{IN} = V_{SS} or V_{DD}	–	5	–	0.05	5	–	150	µAdc
		10	All valid input	–	10	–	0.1	10	–	300	
		15	combinations	–	20	–	0.2	20	–	600	

NOTES: [1] Remaining Static Electrical Characteristics are listed under "SCL40008 Series Family Specifications".
[2] T_{LOW} = -55°C for C, D, F, H device.
= -40°C for E device.
T_{HIGH} = +125°C for C, D, F, H device.
= + 85°C for E device.

DYNAMIC CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

PARAMETER		V_{DD} (Vdc)	Min.	Typ.	Max.	Units
CLOCKED OPERATION						
PROPAGATION DELAY TIME Clock to Q_1	t_{PLH}, t_{PHL}	5	–	200	400	ns
		10	–	100	200	
		15	–	80	160	
Q_1 to Q_{1+1}	t_{PLH}, t_{PHL}	5	–	125	250	ns
		10	–	60	120	
		15	–	45	90	
OUTPUT TRANSITION TIME	t_{TLH}, t_{THL}	5	–	130	260	ns
		10	–	65	130	
		15	–	50	100	
MINIMUM CLOCK PULSE WIDTH	PW_{CL}	5	–	165	330	ns
		10	–	60	120	
		15	–	45	90	
MAXIMUM CLOCK FREQUENCY	f_{CL}	5	1.5	3.0	—	MHz
		10	4.0	8.0	—	
		15	5.5	11	—	
MAXIMUM CLOCK RISE AND FALL TIME	t_{rCL}, t_{fCL}	5	15	–	—	µs
		10	10	–	—	
		15	5	–	—	
RESET OPERATION						
PROPAGATION DELAY TIME	t_{PHL}	5	–	350	700	ns
		10	–	175	350	
		15	–	130	260	
MINIMUM RESET PULSE WIDTH	PW_R	5	–	250	500	ns
		10	–	125	250	
		15	–	100	200	
RESET REMOVAL TIME	t_{rem}	5	–	250	500	ns
		10	–	75	150	
		15	–	60	120	

SCL4027B

CMOS DUAL J-K FLIP-FLOP

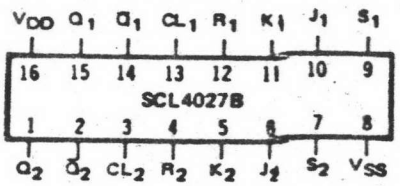
FEATURES

- Individual Set and Reset Controls
- Fully Static Operation
- Logic Edge-Clocked Design
- 8MHz Toggle Rate @ 10Vdc
- Balanced Output Drive Current Specifications

DESCRIPTION

The SCL4027B consists of two identical independent CMOS J-K master-slave Flip-Flops. The SCL4027B is useful in performing control, register, and toggle functions. Logic levels present at the J and K inputs along with internal self-steering control the state of each flip-flop; changes in the flip-flop state are synchronous with the positive-going transition of the Clock pulse. Set and Reset functions are independent of the Clock and are initiated when a high level signal is present at either the Set or Reset input.

CONNECTION DIAGRAM
(all packages)



Add suffix for package:

C	16-pin Cerdip	F	16-pin Flat
D	16-pin Ceramic	H	Chip
E	16-pin Epoxy		

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

TRUTH TABLE

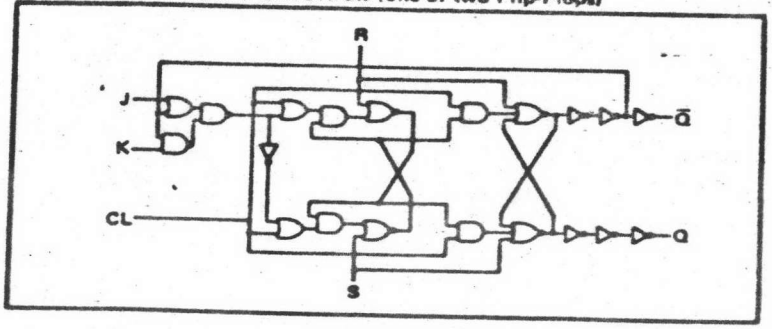
●t_{n-1} INPUTS						†t_n OUTPUTS		
CL▲	J	K	S	R	Q	Q	Q̄	
▲	1	X	0	0	0	1	0	
▲	X	0	0	0	1	1	0	
▲	0	X	0	0	0	0	1	
▲	X	1	0	0	1	0	1	
▼	X	X	0	0	X	(No Change)		
X	X	X	1	0	X	1	0	
X	X	X	0	1	X	0	1	
X	X	X	1	1	X	1	1	

WHERE 1 = HIGH LEVEL
0 = LOW LEVEL
▲ = LEVEL CHANGE
X = DON'T CARE

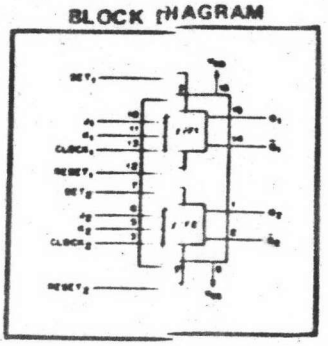
● t_{n-1} REFERS TO THE INTERVAL PRIOR TO THE POSITIVE CLOCK PULSE TRANSITION

† t_n REFERS TO THE TIME INTERVAL AFTER THE POSITIVE CLOCK PULSE TRANSITION

LOGIC DIAGRAM (one of two Flip-Flops)



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS [1]

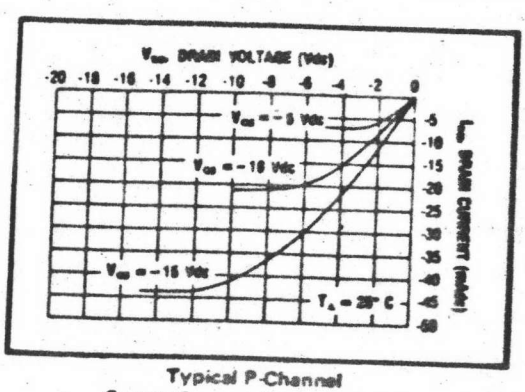
PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW} [2] Min.	T_{LOW} [2] Max.	+25°C Min.	+25°C Typ.	+25°C Max.	T_{HIGH} [2] Min.	T_{HIGH} [2] Max.	Units
QUIESCENT DEVICE CURRENT	I_{DD}	5 10 15	$V_{IN}=V_{SS}$ or V_{DD} All valid input combinations	– – –	1.0 2.0 4.0	– – –	0.005 0.01 0.02	1.0 2.0 4.0	– – –	30 60 120	μAdc

NOTES: [1] Remaining Static Electrical Characteristics are listed under "SCL4000B Series Family Specifications".
[2] T_{LOW} = -55°C for C, D, F, H device.
= -40°C for E device.
T_{HIGH} = +125°C for C, D, F, H device.
= + 85°C for E device.
[3] This device has been designed for balanced output drive current specifications. Consult Family Specifications.

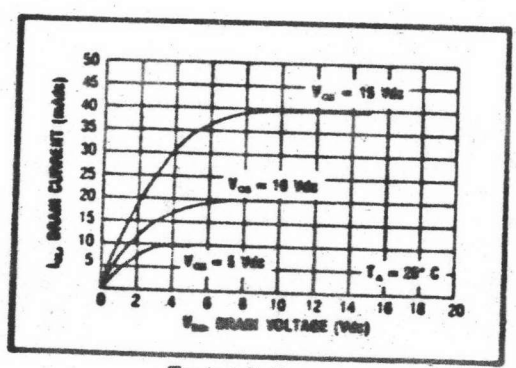
DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V_{DD} (Vdc)	Min.	Typ.	Max.	Units
CLOCKED OPERATION						
PROPAGATION DELAY TIME	t_{PLH}, t_{PHL}	5 10 15	– – –	175 80 60	350 160 120	ns
OUTPUT TRANSITION TIME	t_{TLH}, t_{THL}	5 10 15	– – –	100 50 40	200 100 80	ns
MINIMUM CLOCK PULSE WIDTH	t_{WCL}	5 10 15	– – –	165 80 50	330 120 100	ns
MAXIMUM CLOCK FREQUENCY	f_{CL}	5 10 15	1.5 4.0 5.0	3.0 8.0 10	– –	MHz
MAXIMUM CLOCK RISE AND FALL TIME [1]	t_{rCL}, t_{fCL}	5 10 15	15 5 3	– – –	– – –	μs
MINIMUM SETUP TIME	t_{su}	5 10 15	– – –	100 50 40	200 100 80	ns
MINIMUM HOLD TIME	t_{hold}	5 10 15	– – –	-25 -10 -5	0 0 0	ns
SET AND RESET OPERATION						
PROPAGATION DELAY TIME S to Q, R to Q	t_{PLH}	5 10 15	– – –	150 70 55	300 140 110	ns
MINIMUM SET AND RESET PULSE WIDTH	t_{WS}, t_{WR}	5 10 15	– – –	100 50 40	200 100 80	ns
SET AND RESET REMOVAL TIME	t_{rem}	5 10 15	– – –	0 0 0	25 10 5	ns

[1] When units are cascaded, the maximum rise and fall times of the clock input should be equal to or less than the transition times of the data outputs driving data inputs, plus the propagation delay of the output driving stage for the output capacitive load.



Typical P-Channel
Source Current Characteristics



Typical N-Channel
Sink Current Characteristics

SCL4040AB

CMOS 12-STAGE BINARY COUNTER

FEATURES

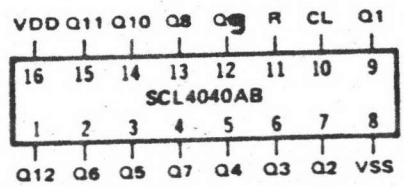
- 12 Fully Static Stages
- All 12 Buffered Outputs Available
- Common Reset Line
- 8MHz Counting Rate @ 10Vdc
- All Inputs Buffered

DESCRIPTION

The SCL4040AB consists of 12-ripple-carry binary counter stages with appropriate input buffers and reset circuitry. The counter is reset to its "all 0's" state by a high level on the Reset input. The counter is advanced one count on the negative-going transition of each input pulse. Isolation from external noise and the effects of loads is provided by output buffering.

Applications include time delay circuits, counter controls, and frequency dividers.

CONNECTION DIAGRAM
(all packages)



Add suffix for package:

C	16-pin Cerdip
D	16-pin Ceramic
E	16-pin Epoxy
F	16-pin Flat
H	Chip

TRUTH TABLE

Clock	Reset	Output State
↓	0	No Change
↓	0	Advance to next state
x	1	All Outputs are low

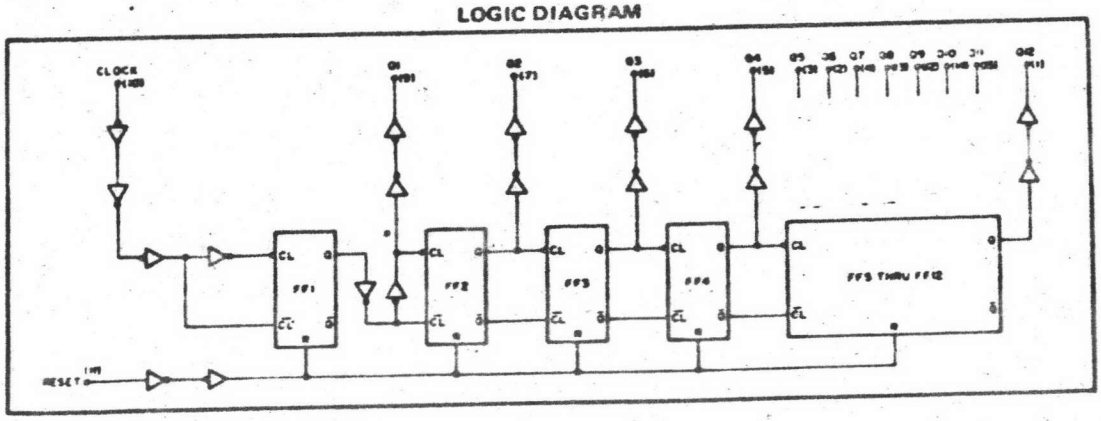
X = Don't Care

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS

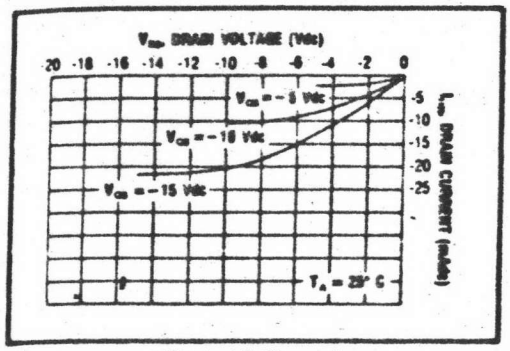
STATIC CHARACTERISTICS [1]

PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW} [2] Min.	T_{LOW} [2] Max.	+25°C Min.	+25°C Typ.	+25°C Max.	T_{HIGH} [2] Min.	T_{HIGH} [2] Max.	Units
QUIESCENT DEVICE CURRENT	I_{DD}	5 10 15	$V_{IN}=V_{SS}$ or V_{DD} All valid input combinations	– – –	5 10 15	– – –	0.05 0.1 0.2	5 10 20	– – –	150 300 600	µAdc
OUTPUT HIGH (SOURCE) CURRENT C, D, F, H device	I_{OH}	5 10 15	V_{OH}=4.6V V_{OH}=9.5V V_{OH}=13.5V $V_{IN}=V_{SS}$ or V_{DD}	-0.15 -0.37 -1.25	– – –	-0.12 -0.3 -1.0	-0.5 -1.15 -4.5	– – –	-0.08 -0.21 -0.69	– – –	mAdc
E device		5 10 15	V_{OH}=4.6V V_{OH}=9.5V V_{OH}=13.5V $V_{IN}=V_{SS}$ or V_{DD}	-0.14 -0.36 -1.2	– – –	-0.12 -0.3 -1.0	-0.5 -1.15 -4.5	– – –	-0.10 -0.25 -0.85	– – –	mAdc
OUTPUT LOW (SINK) CURRENT C, D, F, H device	I_{OL}	5 10 15	V_{OL}=0.4V V_{OL}=0.5V V_{OL}=1.5V $V_{IN}=V_{SS}$ or V_{DD}	0.16 0.37 1.25	– – –	0.12 0.3 1.0	0.5 1.0 5.8	– – –	0.08 0.21 0.69	– – –	mAdc
E device		5 10 15	V_{OL}=0.4V V_{OL}=0.5V V_{OL}=1.5V $V_{IN}=V_{SS}$ or V_{DD}	0.14 0.36 1.2	– – –	0.12 0.3 1.0	0.5 1.0 5.8	– – –	0.10 0.25 0.85	– – –	mAdc

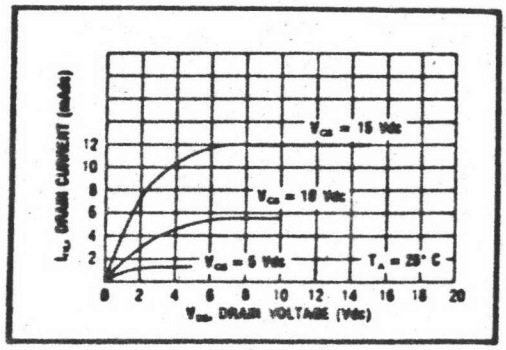
NOTES: [1] Remaining Static Electrical Characteristics are listed under "SCL4000B Series Family Specifications".
[2] T_{LOW} = -55°C for C, D, F, H device.
= -40°C for E device.
T_{HIGH} = +125°C for C, D, F, H device.
= + 85°C for E device.

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V_{DD} (Vdc)	Min.	Typ.	Max.	Units
CLOCKED OPERATION						
PROPAGATION DELAY TIME Clock to Q1	t_{PLH}, t_{PHL}	5 10 15	– – –	200 100 80	400 200 160	ns
Q_i to Q_{i+1}	t_{PLH}, t_{PHL}	5 10 15	– – –	150 75 60	300 150 120	ns
OUTPUT TRANSITION TIME	t_{TLH}, t_{THL}	5 10 15	– – –	180 90 65	360 180 130	ns
MINIMUM CLOCK PULSE WIDTH	PW_{CL}	5 10 15	– – –	100 50 40	200 100 80	ns
MAXIMUM CLOCK FREQUENCY	f_{CL}	5 10 15	2.0 4.0 5.0	4.0 8.0 10.0	– – –	MHz
MAXIMUM CLOCK RISE AND FALL TIME	t_{rCL}, t_{fCL}	5 10 15	15 15 5	– – –	– – –	µs
RESET OPERATION						
PROPAGATION DELAY TIME	t_{PHL}	5 10 15	– – –	300 150 120	600 300 240	ns
MINIMUM RESET PULSE WIDTH	PW_R	5 10 15	– – –	150 75 60	300 150 120	ns
RESET REMOVAL TIME	t_{rem}	5 10 15	– – –	250 125 100	500 250 200	ns

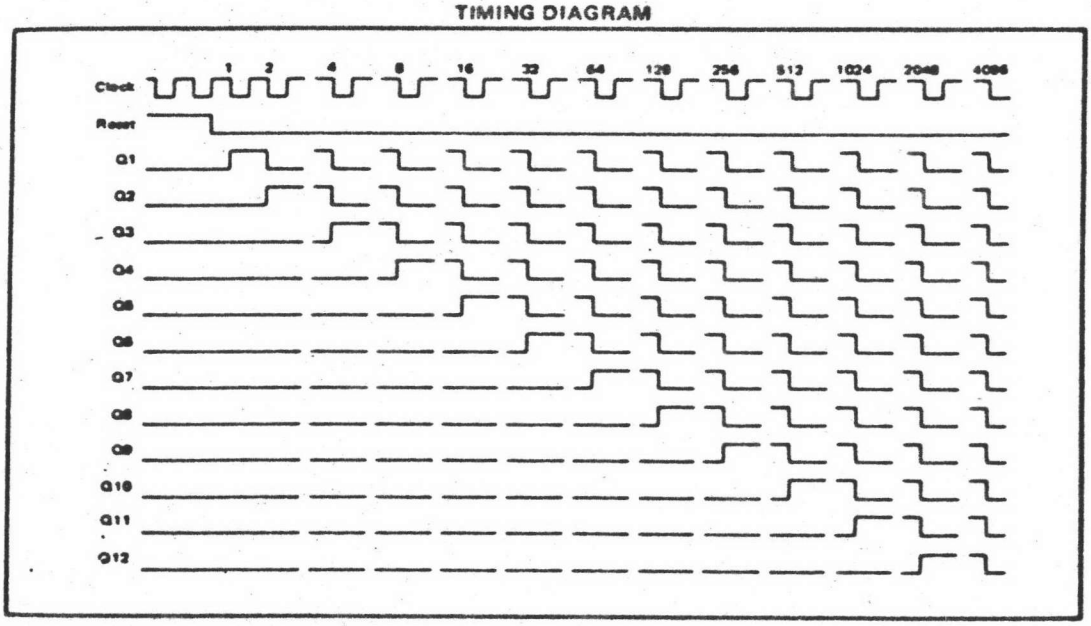


Typical P-Channel
Source Current Characteristics

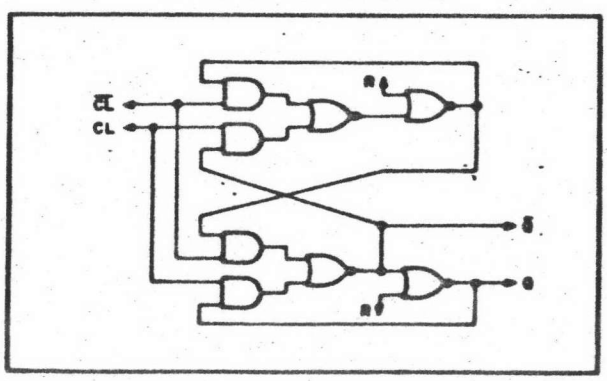


Typical N-Channel
Sink Current Characteristics

TIMING DIAGRAM



TYPICAL COUNTER STAGE



SCL4069UB

CMOS HEX INVERTER

FEATURES

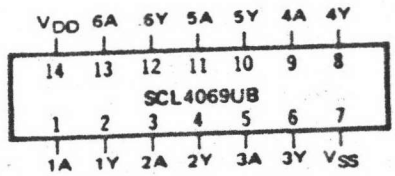
- Fully "B"-Series Compatible
- Diode Protection on all Inputs
- Balanced Output Drive Current Specifications
- Pin Compatible with 74C04

DESCRIPTION

The SCL4069UB consists of six CMOS inverter circuits. The device is intended for general-purpose inverter applications where the higher output drive and level-shifting feature of the SCL4009UB and SCL4049UB are not required.* The SCL4069UB is particularly useful for quasi-linear circuits such as oscillators (See Applications Information).

*For pin-to-pin compatibility with the SCL4009UB and SCL4049UB, the SCL4449UB is available.

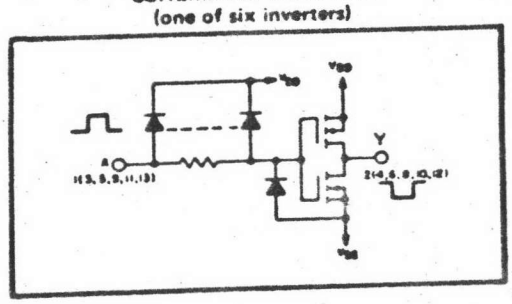
CONNECTION DIAGRAM
(all packages)



Add suffix for package:

C	14-pin Cerdip
D	14-pin Ceramic
E	14-pin Epoxy
F	14-pin Flat
H	Chip

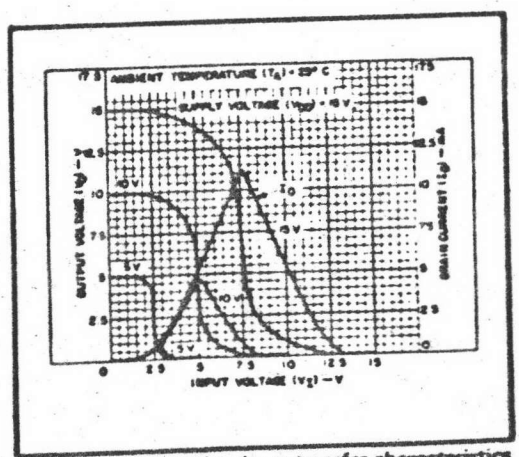
SCHEMATIC DIAGRAM
(one of six inverters)



RECOMMENDED OPERATING CONDITIONS

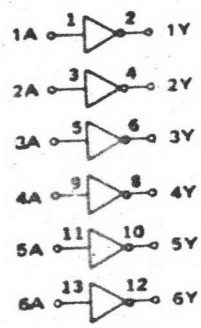
For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C



Typical current and voltage transfer characteristics

LOGIC DIAGRAM



V_{SS} = 7
V_{DD} = 14

ELECTRICAL CHARACTERISTICS

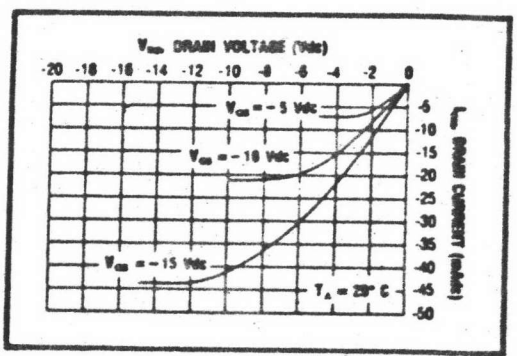
STATIC CHARACTERISTICS[1,3]

PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW}[2]		+25°C			T_{HIGH}[2]		Units
				Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I_{DD}	5	$V_{IN}=V_{SS}$ or V_{DD}	–	0.05	–	0.0005	0.05	–	1.5	μAdc
		10	All valid input	–	0.10	–	0.001	0.10	–	3.0	
		15	combinations	–	0.20	–	0.002	0.20	–	6.0	

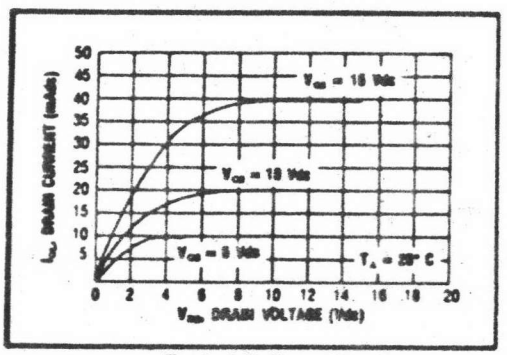
NOTES: [1] Remaining Static Electrical Characteristics are listed under "SCL40008 Series Family Specifications".
[2] T_{LOW} = -55°C for C, D, F, H device.
= -40°C for E device.
T_{HIGH} = +125°C for C, D, F, H device.
= + 85°C for E device.
[3] This device has been designed for balanced output drive current specifications. Consult Family Specifications.

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V_{DD} (Vdc)	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME	t_{PLH}, t_{PHL}	5	–	80	120	ns
		10	–	30	60	
		15	–	25	50	
OUTPUT TRANSITION TIME	t_{TLH}, t_{THL}	5	–	100	200	ns
		10	–	50	100	
		15	–	40	80	

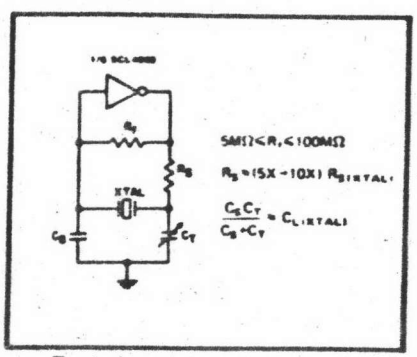


Typical P-Channel
Source Current Characteristics

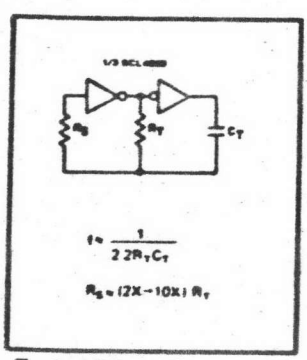


Typical N-Channel
Sink Current Characteristics

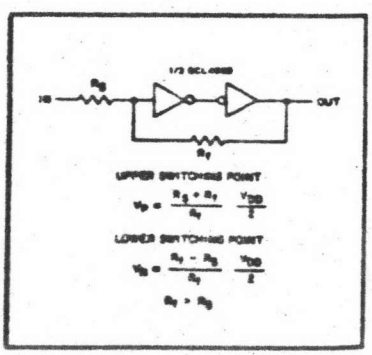
APPLICATIONS INFORMATION



Typical crystal oscillator circuit



Typical RC oscillator circuit



Input pluse shaping circuit (Schmitt Trigger)

SCL4511B

CMOS BCD-TO-SEVEN SEGMENT LATCH/DECODER/DRIVER

FEATURES

- High-Current Sourcing Bipolar Outputs (Up to 25 mA)
- Latched Storage of Input Code
- Blanking Input for Display Intensity Modulation
- Lamp Test Provision
- Readout Blanking for Illegal Input Combinations

DESCRIPTION

The SCL4511B provides the functions of a 4-bit storage latch, an 8421 BCD-to-seven segment decoder, and an output drive capability to source up to 25 mA of current. Lamp Test, Blanking, and Latch Enable inputs are used to test the display, turn off the display, and store a BCD code, respectively. It can be used with LED, incandescent, fluorescent, gas discharge, or liquid crystal readouts either directly or indirectly.

Applications include counter display drivers, seven-segment decimal display, and various clock, watch, and timer uses.

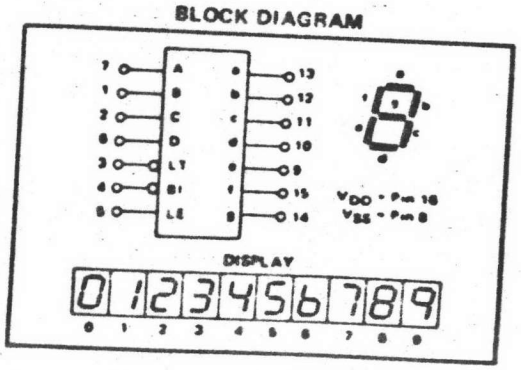
TRUTH TABLE

LE	BI	LT	D	C	B	A	a	b	c	d	e	f	g	DISPLAY
X	X	0	X	X	X	X	1	1	1	1	1	1	1	.8
X	0	1	X	X	X	X	0	0	0	0	0	0	0	Blank
0	1	1	0	0	0	0	1	1	1	1	1	1	0	0
0	1	1	0	0	0	1	0	1	1	0	0	0	0	1
0	1	1	0	0	1	0	1	1	0	1	1	0	1	2
0	1	1	0	0	1	1	1	1	1	1	0	0	1	3
0	1	1	0	1	0	0	0	1	1	0	0	1	1	4
0	1	1	0	1	0	1	1	0	1	1	0	1	1	5
0	1	1	0	1	1	0	0	0	1	1	1	1	1	6
0	1	1	0	1	1	1	1	1	1	0	0	0	0	7
0	1	1	1	0	0	0	1	1	1	1	1	1	1	8
0	1	1	1	0	0	1	1	1	1	0	0	1	1	9
0	1	1	1	0	1	0	0	0	0	0	0	0	0	Blank
0	1	1	1	0	1	1	0	0	0	0	0	0	0	Blank
0	1	1	1	1	0	0	0	0	0	0	0	0	0	Blank
0	1	1	1	1	0	1	0	0	0	0	0	0	0	Blank
0	1	1	1	1	1	0	0	0	0	0	0	0	0	Blank
0	1	1	1	1	1	1	0	0	0	0	0	0	0	Blank
1	1	1	X	X	X	X	*							*

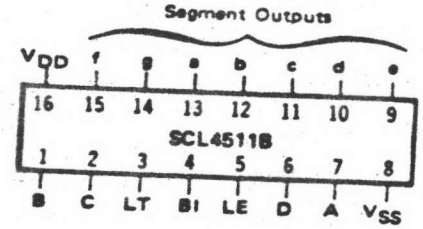
X = Don't care

* Depends upon the BCD code applied during the 0 to 1 transition of LE.

BLOCK DIAGRAM



CONNECTION DIAGRAM
(all packages)



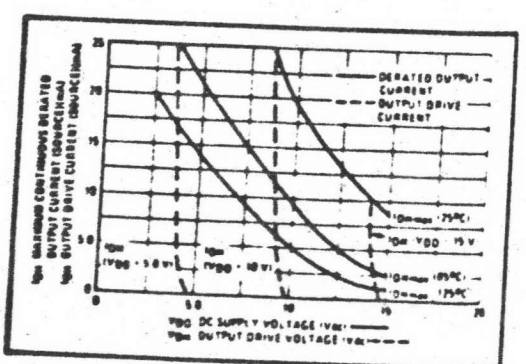
Add suffix for package:

C	16-pin Cerdip
D	16-pin Ceramic
E	16-pin Epoxy
F	16-pin Flat
H	Chip

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C



Typical P-Channel
Source Current Characteristics

The maximum continuous (worst case) derated output drive current applies to a single output with all other outputs sourcing an equal amount of current. Operation above the derating curve at a given temperature is not recommended.

ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS [1]

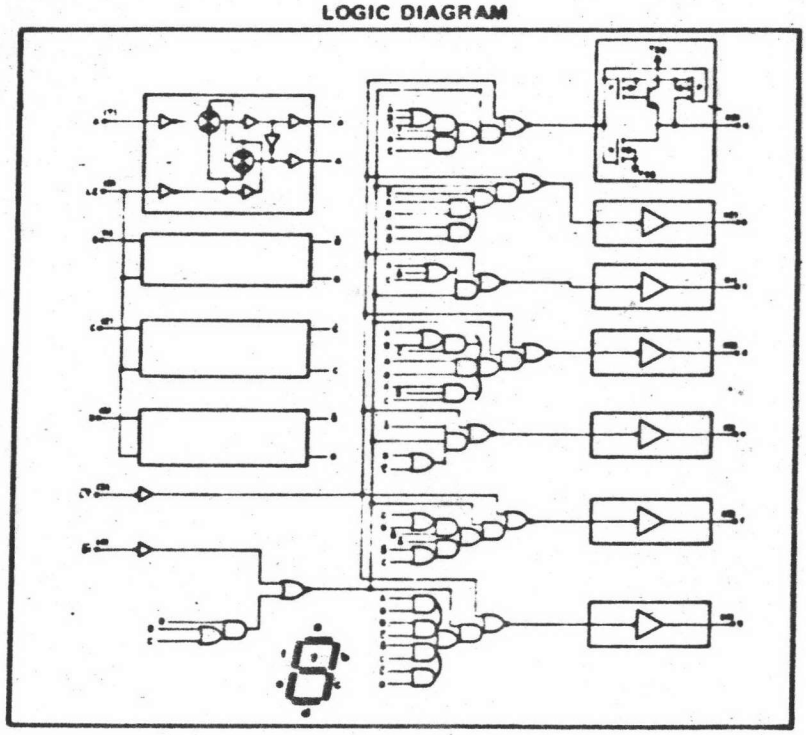
PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{Low} [2] Min.	T_{Low} [2] Max.	-55°C Min.	-55°C Typ	-55°C Max.	T_{High} [2] Min.	T_{High} [2] Max.	Units
QUIESCENT DEVICE CURRENT	I_{DD}	5	$V_{in} = V_{SS}$ or V_{DD}	–	5	–	0.05	5	–	150	μAdc
		10	All valid input	–	10	–	0.1	10	–	300	
		15	combinations	–	20	–	0.2	20	–	600	
OUTPUT DRIVE VOLTAGE	V_{OH}	5	I_{OH} = 0 mAdc	4.99	–	4.99	5.0	–	4.95	–	Vdc
			-.5	–	–	–	4.75	–	–	–	
			-10	–	–	3.8	4.13	–	–	–	
			-15	–	–	–	3.98	–	–	–	
			-20	–	–	3.4	3.75	–	–	–	
			-25	–	–	–	3.5	–	–	–	
		10	I_{OH} = 0mAdc	9.99	–	9.99	10	–	9.95	–	Vdc
			-.5	–	–	–	9.75	–	–	–	
			-10	–	–	9.0	9.15	–	–	–	
			-15	–	–	–	9.03	–	–	–	
			-20	–	–	8.6	8.90	–	–	–	
			-25	–	–	–	8.75	–	–	–	
		15	I_{OH} = 0mAdc	14.99	–	14.99	15	–	14.95	–	Vdc
			-.5	–	–	–	14.75	–	–	–	
			-10	–	–	14.0	14.18	–	–	–	
			-15	–	–	–	14.08	–	–	–	
			-20	–	–	13.6	13.95	–	–	–	
			-25	–	–	–	13.80	–	–	–	
OUTPUT LOW (SINK) CURRENT C, D, F, H device	I_{OL}	5	V_{OL} = 0.4V	1.9	–	1.5	3.4	–	1.1	–	mAdc
		10	V_{OL} = 0.5V	5.0	–	4.0	6.5	–	2.8	–	
		15	V_{OL} = 1.5V	13.8	–	11.0	24	–	7.7	–	
			$V_{in} = V_{SS}$ or V_{DD}								
E device		5	V_{OL} = 0.4V	1.8	–	1.5	3.4	–	1.2	–	mAdc
		10	V_{OL} = 0.5V	4.8	–	4.0	6.5	–	3.2	–	
		15	V_{OL} = 1.5V	13.2	–	11.0	24	–	8.8	–	
			$V_{in} = V_{SS}$ or V_{DD}								

NOTES: [1] Remaining Static Electrical Characteristics are listed under "SCL40008 Series Family Specifications".
[2] T_{Low} = -55°C for C, D, F, H devices.
= -40°C for E devices.
T_{High} = +125°C for C, D, F, H devices.
= +85°C for E devices.

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

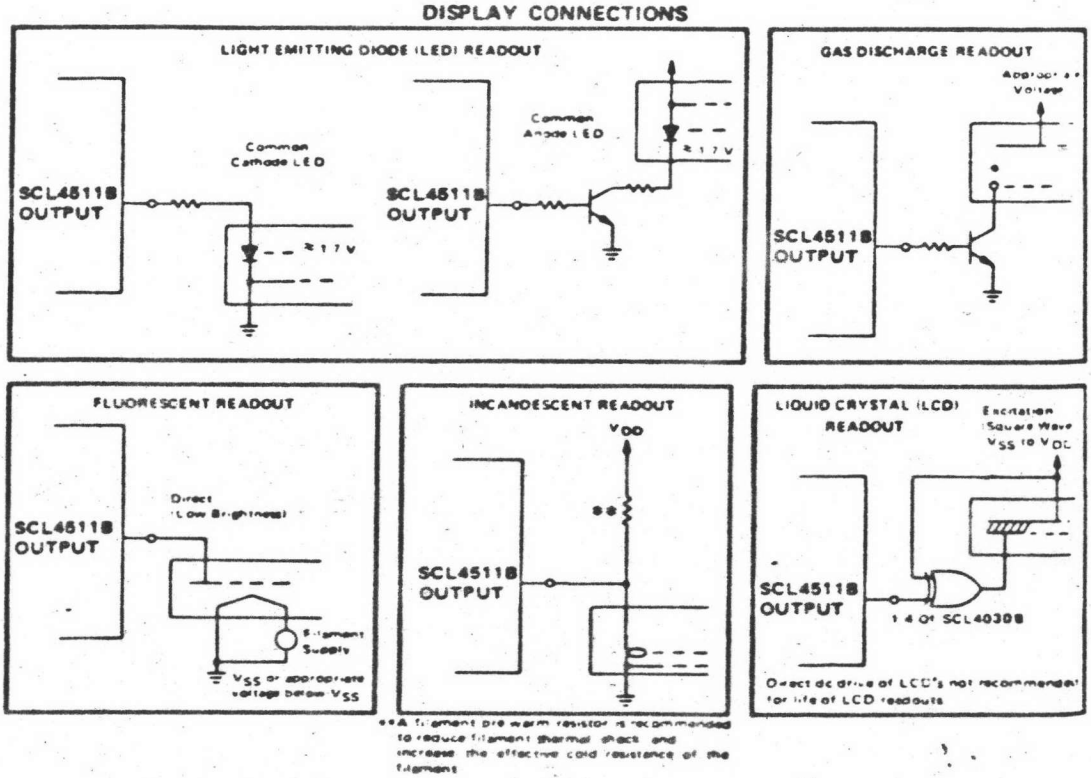
PARAMETER		V_{DD} (Vdc)	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME From Data Inputs	t_{PLH}	5	–	650	1300	ns
		10	–	250	500	
		15	–	200	400	
	t_{PHL}	5	–	750	1500	ns
		10	–	300	600	
		15	–	200	400	
From Blanking Input	t_{PLH}	5	–	300	600	ns
		10	–	125	250	
		15	–	100	200	
	t_{PHL}	5	–	500	1000	ns
		10	–	200	400	
		15	–	160	320	
From Lamp Test Input	t_{PLH}	5	–	300	600	ns
		10	–	120	240	
		15	–	80	160	
	t_{PHL}	5	–	325	650	ns
		10	–	130	260	
		15	–	95	190	
OUTPUT TRANSITION TIME	t_{TLH}	5	–	90	180	ns
		10	–	40	80	
		15	–	35	70	
	t_{THL}	5	–	1000	2000	ns
		10	–	1000	2000	
		15	–	1000	2000	
MINIMUM DATA INPUT SETUP TIME	t_{su}	5	–	80	160	ns
		10	–	40	80	
		15	–	30	60	
MINIMUM DATA INPUT HOLD TIME	t_{su}	5	–	60	0	ns
		10	–	40	0	
		15	–	20	0	
MINIMUM LATCH ENABLE PULSE WIDTH	PW_{LE}	5	–	260	520	ns
		10	–	110	220	
		15	–	65	130	

LOGIC DIAGRAM



APPLICATIONS INFORMATION

DISPLAY CONNECTIONS



**A filament pre-warm resistor is recommended to reduce filament thermal shock and increase the effective cold resistance of the filament.

National Semiconductor

MOS RAMs

MM2102, MM2102-1, MM2102-2
1024-bit fully decoded static random access memories

general description

The MM2102 family of 1024 word by one bit static random access read write memories are manufactured using N-channel enhancement mode silicon gate technology. Static storage cells eliminate the need for clocks and refresh. Data in and data out have the same polarity and the read operation is nondestructive.

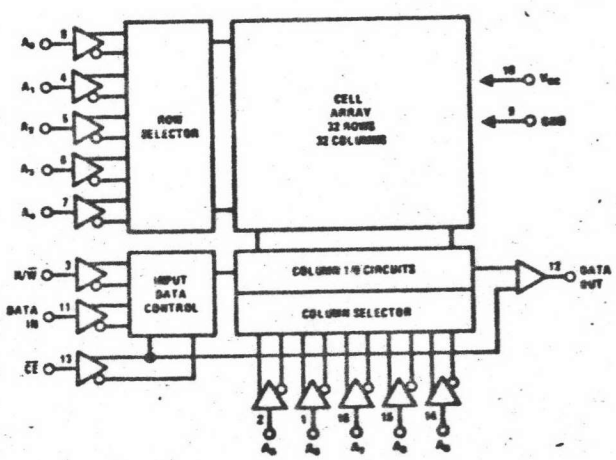
Low threshold silicon gate N-channel technology allows complete DTL/TTL compatibility of all inputs and outputs as well as a single +5V supply. The separate chip enable input ($\overline{CE}$) controlling the TRI-STATE® output allows easy memory expansion by OR-tying individual devices to a data bus.

The simple interface and high performance make the MM2102 family ideally suited for those applications, for large and small storage capacity, where cost is an important design consideration.

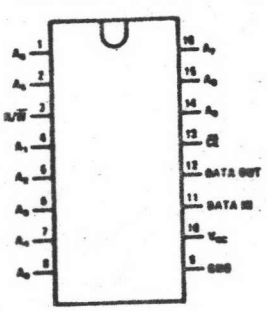
features

- Single +5V supply
- All inputs and output directly DTL/TTL compatible
- Static operation—no clocks or refreshing required
- Low power — 150 mW typ
- Fast access
  - MM2102 — 1 µs
  - MM2102-1 — 500 ns
  - MM2102-2 — 650 ns
- TRI-STATE output for bus interface
- Chip enable allows simple memory expansion
- On chip address decode
- All inputs protected against static discharge
- Low cost 16-pin Epoxy B package

block and connection diagrams



Dual-In-Line Package



Order Number MM2102D, MM2102-1D or MM2102-2D
See Package 3
Order Number MM2102N, MM2102-1N or MM2102-2N
See Package 15

absolute maximum ratings (Note 1)

Voltage at Any Pin	−0.5V to +7.0V
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Power Dissipation	1W
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics

(T_A within operating temperature range, V_{CC} = 5V ±5%, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage (V_{IH})		2.2		V_{CC}	V
Logical "0" Input Voltage (V_{IL})		−0.5		0.65	V
Logical "1" Output Voltage (V_{OH})	I_{OH} = −100μA	2.2			V
Logical "0" Output Voltage (V_{OL})	I_{OL} = 1.9 mA			0.45	V
Input Load Current (I_{LI})	V_{IN} = 0 to 5.25V			10	μA
Output Leakage Current (I_{LOH})	$\overline{CE}$ = 2.2V, V_{OUT} = 4.0V			10	μA
Output Leakage Current (I_{LOL})	$\overline{CE}$ = 2.2V, V_{OUT} = 0.45V			−100	μA
Power Supply Current (I_{CC1})	All Inputs = 5.25V, Data Out Open, T_A = 25°C		30	60	mA
Power Supply Current (I_{CC2})	All Inputs = 5.25V, Data Out Open, T_A = 0°C			70	mA

ac electrical characteristics

(T_A within operating temperature range, V_{CC} = 5V ±5%, unless otherwise specified.)
See ac test circuit and switching time waveforms.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
READ CYCLE					
Read Cycle (t_{RC})					
MM2102	R/$\overline{W}$ = V_{IH}	1000			ns
MM2102-1	R/$\overline{W}$ = V_{IH}	500			ns
MM2102-2	R/$\overline{W}$ = V_{IH}	650			ns
Access Time (t_A)					
MM2102				1000	ns
MM2102-1				500	ns
MM2102-2				650	ns
Chip Enable to Output Time (t_{CO})					
MM2102				500	ns
MM2102-1				350	ns
MM2102-2				400	ns
Previous Read Data Valid with Respect to Address (t_{OH1})		50			ns
Previous Read Data Valid with Respect to Chip Enable (t_{OH2})		0			ns

ac electrical characteristics (con't)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
WRITE CYCLE					
Write Cycle (t_{WC})					
MM2102		1000			ns
MM2102-1		500			ns
MM2102-2		650			ns
Address to Write Set-up Time (t_{AW})					
MM2102		200			ns
MM2102-1		150			ns
MM2102-2		200			ns
Write Pulse Width (t_{WP})					
MM2102		750			ns
MM2102-1		300			ns
MM2102-2		400			ns
Write Recovery Time (t_{WR})		50			ns
Data Set-up Time (t_{DW})					
MM2102		800			ns
MM2102-1		330			ns
MM2102-2		450			ns
Data Hold Time (t_{DH})		100			ns
Chip Enable to Write Set-up Time (t_{CW})					
MM2102		900			ns
MM2102-1		400			ns
MM2102-2		550			ns
CAPACITANCE					
Input Capacitance (All Inputs) (C_{IN}) (Note 4)	V_{IN} = 0V, T_A = 25°C, f = 1.0 MHz (Note 2)		3.0	5.0	pF
Output Capacitance (C_{OUT}) (Note 4)	V_{OUT} = 0V, T_A = 25°C, f = 1.0 MHz (Note 2)		7.0	10.0	pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

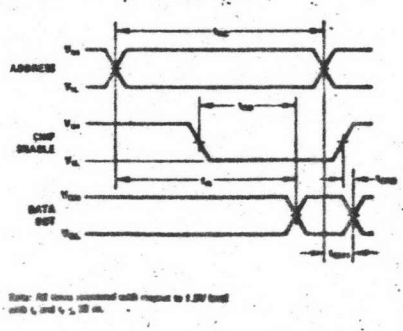
Note 2: Capacitance is guaranteed by periodic testing.

Note 3: Positive true logic notation is used: Logical "1" = most positive voltage level, Logical "0" = most negative voltage level.

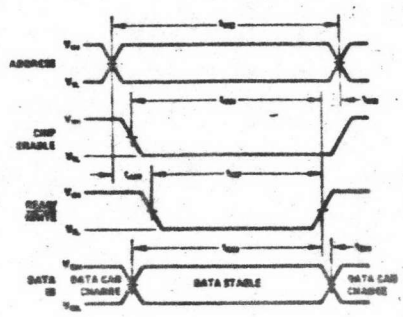
Note 4: Typical values are for T_A = 25°C and nominal supply voltage.

switching time waveforms

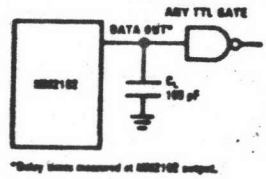
Read Cycle



Write Cycle



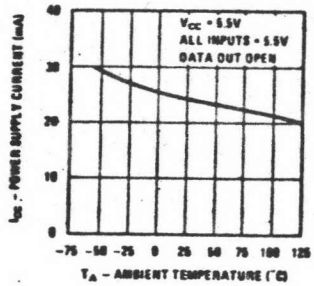
ac test circuit



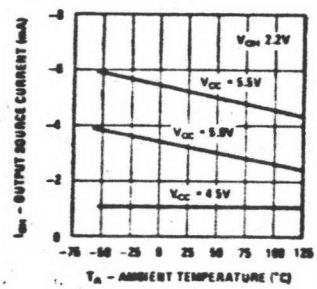
*Delay times measured at MM2102 output.

typical performance characteristics

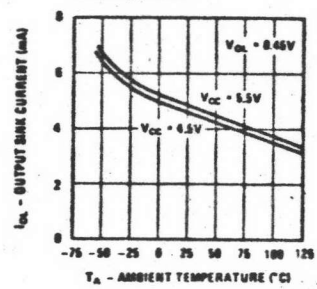
Power Supply Current vs Temperature



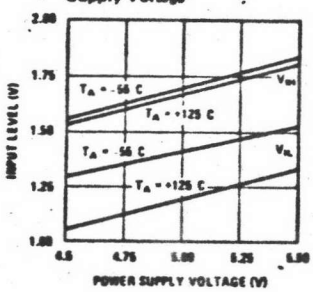
Output Source Current vs Temperature



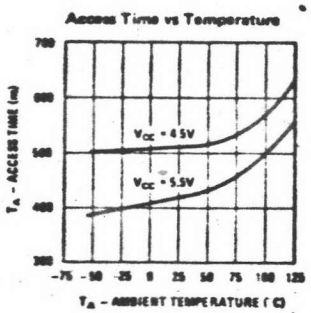
Output Sink Current vs Temperature



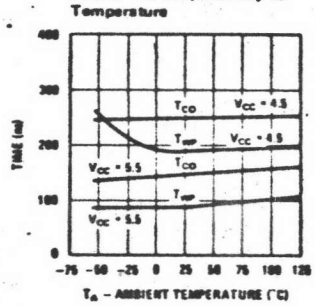
Input Levels vs Power Supply Voltage



Access Time vs Temperature



Write Pulse Width and Chip Enable—To Output Delay vs Temperature



DECADE COUNTER 54/74

SPEED/PACKAGE AVAILABILITY

54	F,W	74	A,F
54LS	F,W	74LS	A,F

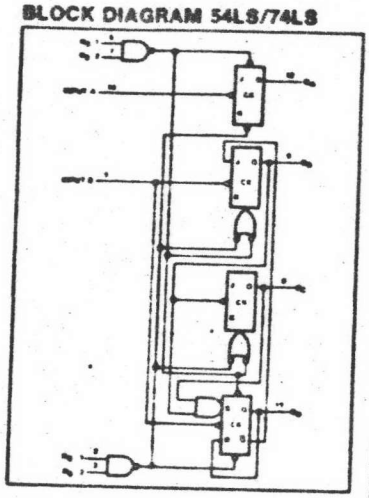
DESCRIPTION

This monolithic counter contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five.

The 54/74LS90 also has a gated zero reset and gated set-to-nine inputs for use in BCD nine's complement applications.

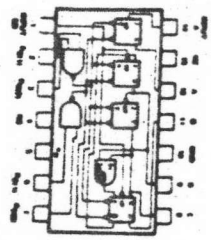
To use its maximum count length of this counter, the B input is connected to the Q_A output. The input count pulses are applied to input A and the outputs are as described in the function table. A symmetrical divide-by-ten count can be obtained by connecting the Q_D output to the A input and applying the input count to the B input which gives a divide-by-ten square wave at output Q_A.

BLOCK DIAGRAM 54LS/74LS

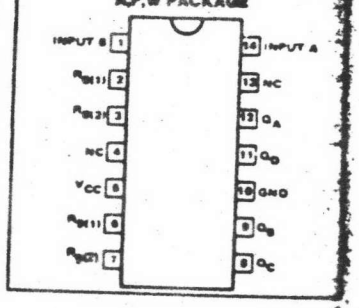


PIN CONFIGURATION

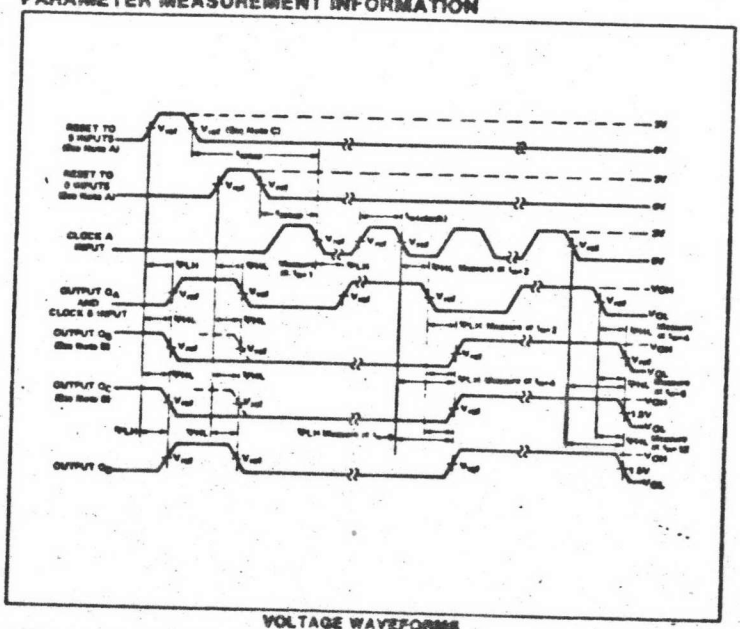
54/74
A,F,W PACKAGE



54LS/74LS
A,F,W PACKAGE



PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

A. Each reset input is tested separately with the other reset at 4.5 V
B. Reference waveforms are shown with dashed lines.
C. V_{ref} = 1.3 V
Load circuit is shown at front of section (for totem pole outputs)

DECADE COUNTER 54/7490

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS				54/74 C_L = 15pF, R_L = 400Ω			54/74LS C_L = 15pF, R_L = 2kΩ			
PARAMETER		FROM INPUT	TO OUTPUT	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
f_{count}	Count frequency			10	18					MHz
		A	Q_A				32	42		
		B	Q_B				16			
$t_{w(Clock)}$	Width of clock pulse			50						ns
		A	Q				16			
		B	Q				30			
		Reset	Q				15			
$t_{w(Reset)}$	Width of reset pulse			50			25			ns
Propagation delay time										
t_{PLH}	Low-to-high	Input Count Pulse	Q_C		60	100				ns
t_{PHL}	High-to-low				60	100				
t_{PLH}	Low-to-high	A	Q_A					10	16	
t_{PHL}	High-to-low							12	18	
t_{PLH}	Low-to-high	A	Q_D					32	48	
t_{PHL}	High-to-low							34	50	
t_{PLH}	Low-to-high	B	Q_B					10	16	
t_{PHL}	High-to-low							14	21	
t_{PLH}	Low-to-high	B	Q_C					21	32	
t_{PHL}	High-to-low							23	35	
t_{PLH}	Low-to-high	B	Q_D					21	32	
t_{PHL}	High-to-low							23	35	
t_{PHL}	High-to-low	Set-to-0	Any					26	40	
t_{PLH}	Low-to-high	Set-to-9	Q_A.Q_D					20	30	
t_{PHL}	High-to-low	Set-to-9	Q_B.Q_C					26	40	

ear circuit and typical waveforms shown at front of section.

BCD COUNT SEQUENCE (See Note A)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

BI-QUINARY (5-2) (See Note B)

COUNT	OUTPUT			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

RESET/COUNT FUNCTION TABLE

RESET INPUTS				OUTPUT			
$R_{0(1)}$	$R_{0(2)}$	$R_{9(1)}$	$R_{9(2)}$	Q_D	Q_C	Q_B	Q_A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	COUNT			
L	X	L	X	COUNT			
L	X	X	L	COUNT			
X	L	L	X	COUNT			

NOTES:
A. Output Q_A is connected to input B for BCD count.
B. Output Q_D is connected to input A for bi-quinary count.
C. Output Q_A is connected to input B.
D. H = high level, L = low level, X = irrelevant

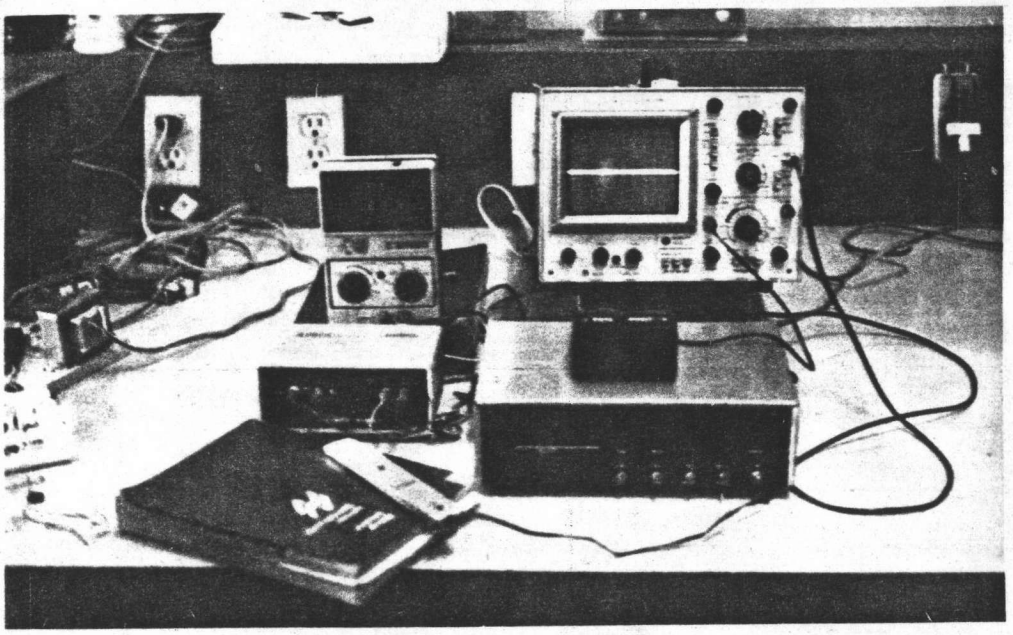
ภาคผนวก ค.

แผนภาพแสดงวงจรของเครื่องวัดการรับรังสีของดวงอาทิตย์

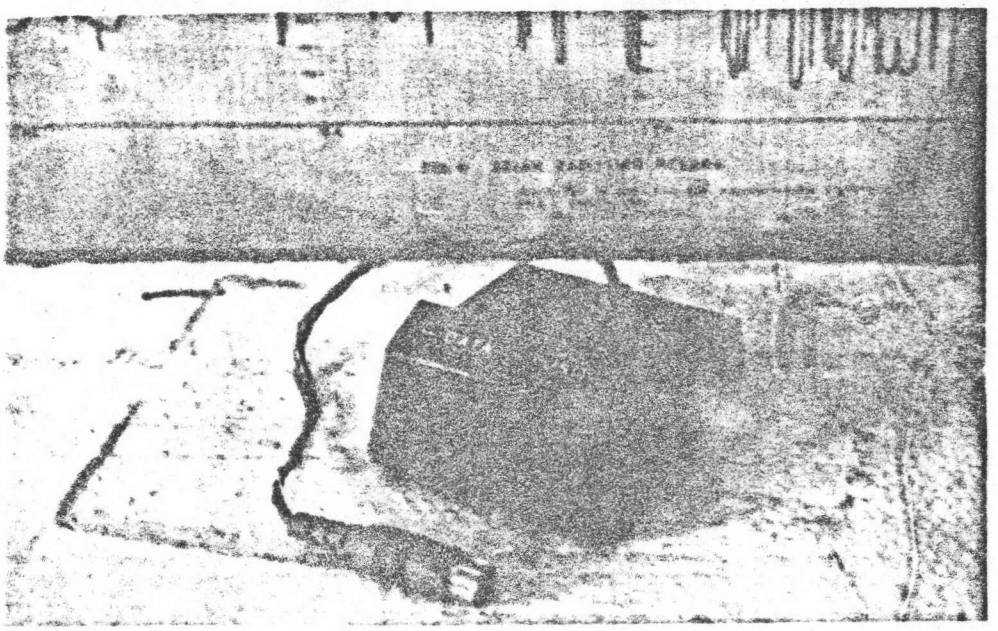
SOLAR IRRADIANCE METER.

ภาคผนวก ง.

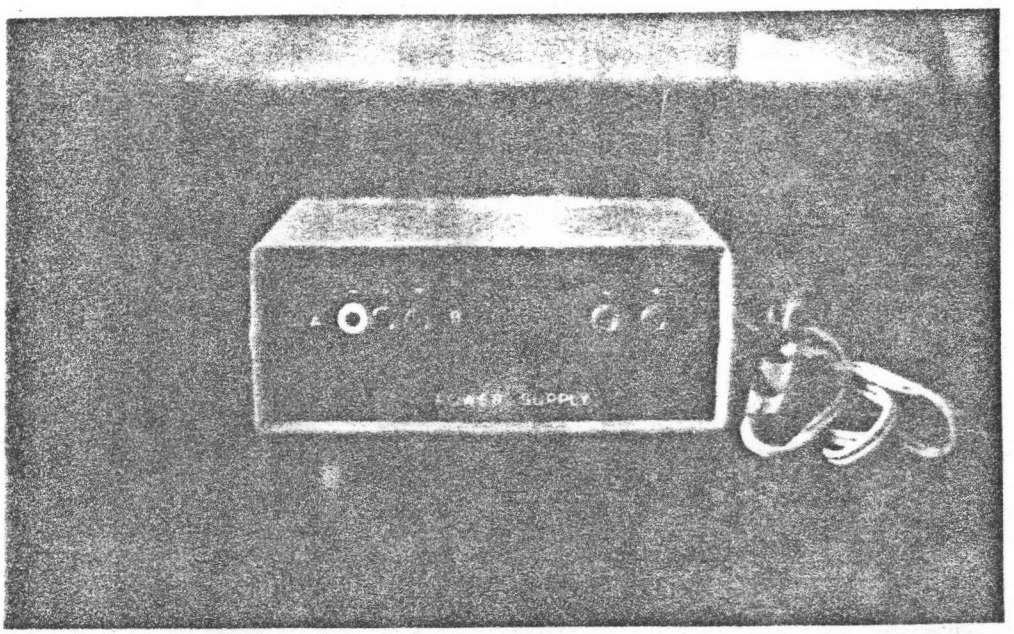
รูปภาพแสดงลักษณะของเครื่องวัดการรับรังสีของดวงอาทิตย์



รูปที่ 1. เครื่องวัดการรับรังสีของดวงอาทิตย์ เครื่องบอกตำแหน่งและแหล่งจ่ายไฟ



รูปที่ 2 เครื่องควบคุม 2



รูปที่ 3 เครื่องจ่ายไฟ

ภาคผนวก จ.

ลักษณะของเซลล์แสงอาทิตย์อ้างอิงที่ใช้สำหรับเครื่องวัดการรับรังสีของดวงอาทิตย์

Solarex®
SOLAREX CORPORATION
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ROCKVILLE, MD 20850
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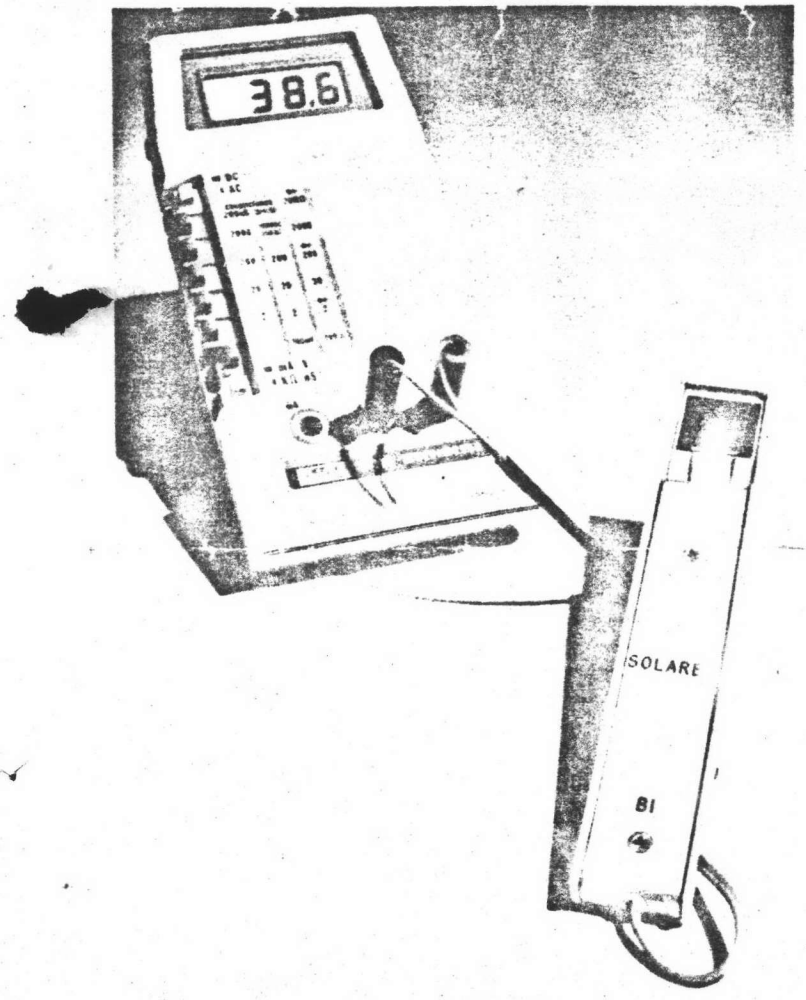
TWX: 710 828 9709
CABLE ADDRESS: SOLAREX

THE REFERENCE SOLAR CELL



Meter not included

The Solarex Reference Cell comprises a premium-quality silicon solar cell and a precision resistor heat-sinked and encapsulated in a rugged, compact (1-1/2" X 6" X 1/4") anodized aluminum case. Used in conjunction with an accurate millivoltmeter, the Reference Cell enables precise solar measurements including:

- sunlight intensity measurements;
- design measurements for photovoltaic and solar thermal systems;
- determination of photovoltaic cell and module efficiency;
- calibration of sun simulators and measuring instruments.

The Reference Cell utilizes a broad-response Solarex silicon cell of International Space Standard size (2 cm X 2 cm) and quality, encapsulated in specially formulated UV-stable clear silicone rubber. The cell's high-technology features include:

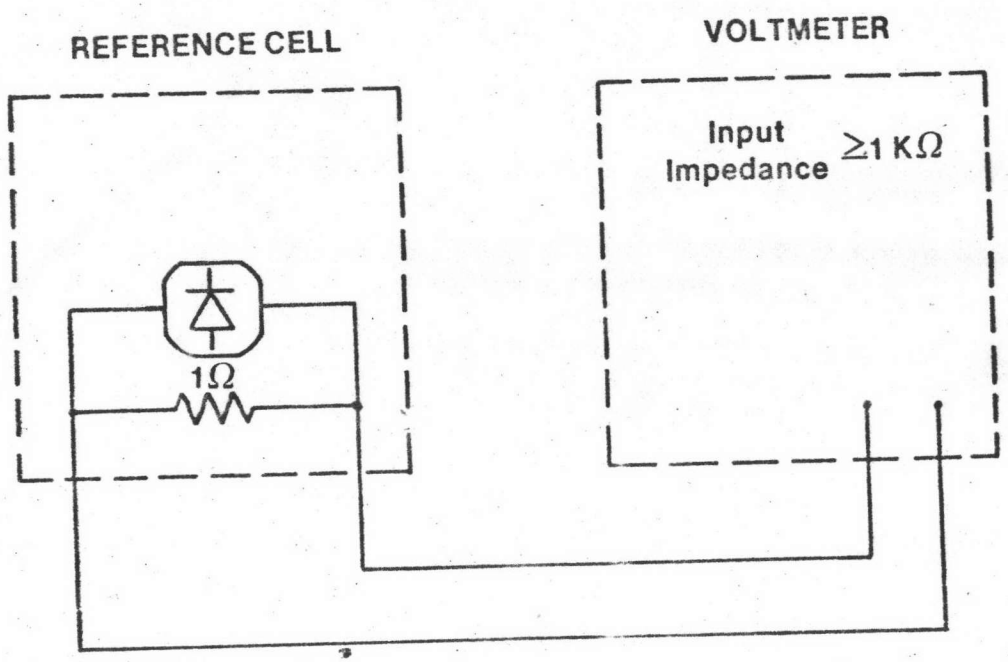
- photolithographically applied Trimet™ current-collecting metallization;[1]
- precision quarter-wavelength tantalum oxide antireflective coating;
- P^+ back surface field for wide spectral response.

Reference Cells are individually calibrated for Air Mass One (AM1) full-sun intensity (1 kW/m²) at 25°C. The output voltage produced across the integral 1-ohm shunt resistor under these conditions is stamped on the unit's nameplate. This low shunt resistance maintains the cell voltage near short-circuit conditions (where current precisely tracks illumination) and provides very low output impedance, assuring precise measurement regardless of voltmeter impedance. Consequently, the Reference Cell's output voltage provides a precise measure of sunlight intensity.

[1]"Trimet" is Solarex's trademark for its non-corroding titanium/palladium/silver cell metallization.

As an example of Reference Cell use, assume the object is to determine a site's insolation with reference to AM1 standards. Also assume the Cell in use produces 148 mV under calibration conditions. At the appointed measurement time, the Cell produces 94 mV; sunlight intensity at that time, therefore, is:

$$\frac{94\text{mV}}{148\text{ mV}} = 0.635 \text{ suns or } 635 \text{ W/m}^2$$



SCHEMATIC

CALIBRATION

Reference Cells are calibrated against a Solarex Standard Cell, which is standardized using an Eppley pyranometer (Model 8-48). Calibration reference for this pyranometer is the Eppley primary standard group of Angstrom Pyrheliometers, which are in close agreement (better than 0.5%) with the primary standards maintained at the National Physical Laboratory in London and the National Research Council in Ottawa. In addition, Solarex Standard Cells are checked against balloon-flown cells of similar spectral response, providing calibration verification for the broader extraterrestrial radiation spectrum.

All Reference Cell components are of the highest quality, and will not degrade or change value for many years. Readings may be affected, however, by marring or contamination (fingerprints, etc.) of the encapsulant surface. This surface should be cleaned periodically with alcohol or soap and a damp cloth.

Solarex recommends periodic recalibration for heavily used units and applications requiring extreme precision over extended time periods. Both recalibration and resurfacing service (for units displaying encapsulant abrasion) are available from Solarex.

Printed in U.S.A.

ประวัติผู้เขียน

นายไพสิฐ คัณฑุลพงษ์ เกิดเมื่อวันที่ 30 มกราคม พ.ศ.2522 ที่กรุงเทพฯ สำเร็จการศึกษาปริญญาวิศวกรรมศาสตรบัณฑิต สาขาวิศวกรรมไฟฟ้าสื่อสารและไฟฟ้ากำลัง จากมหาวิทยาลัยขอนแก่น เมื่อปี พ.ศ. 2522