CHAPTER 3

MATHEMATICAL ANALYSIS OF SWITCHING REGULATOR

3.1 Introduction

An analysis of a switching regulator system is introduced in this chapter. A ¶-type filter circuit is used as a RF Noise Filter in the regulator system. The mathematical analysis of the switching regulator system will be performed for easy referred in the following chapters. In addition, the switching losses due to all conductions, switching in power transistors, driver circuits and transformer losses are also presented.

3.2 RF Noise Filter

In the high speed switching operation, the interference voltage at the line input voltage due to noise is the major problem. Using Fouries analysis,the harmonics at higher frequencies will be reduced,but in the switching system the harmonics do not obey this rule. Tunnbull[13] observed that the anomolous magnitudes of these harmonics occur during the frequency ranges of 1 MHz to 10 MHz. Recently, John Turnbull has discussed this phenomena and also suggested some techniques to reduce these anomolous voltages. Consequently, this difficulty may be overcome by using a RF Noise Filter which will be designed and used in this research.

In practice, low pass filters are considered to attenuate any particular interference frequency and their transmission losses can be determined. A ¶-type filter circuit is used here and shown in Fig 3.1.

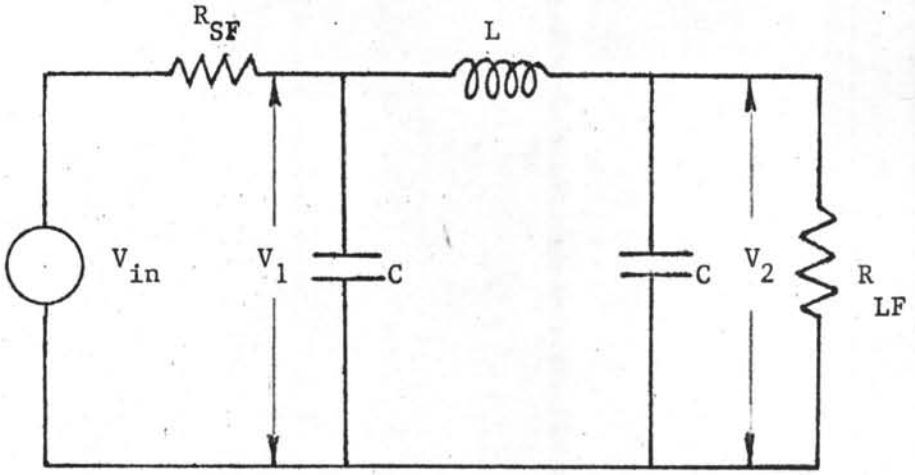


Fig 3.1 A ¶-type filter circuit

For maximum power transfer condition, the load impedance R_{LF} must be equal to the source impedance R_{SF}, therefore the output voltage, V_2, can be expressed as

$$V_2 = \frac{V_{in}}{2-2\omega^2 LC+j\left[\frac{\omega L}{R_{LF}}+ 2R_{LF}\omega C-\omega^3 R_{LF}C^2L\right]} \qquad (3.1)$$

From Fig. 3.1, the ¶-type filter circuit may be considered as a no loss filter, then the input voltage, V_{in} becomes

$$V_{in} = 2V_1 \qquad (3.2)$$

Consequently, the ratio of the square of the absolute magnitude voltage between V_1 and V_2 is written as

$$\left|\frac{V_1}{V_2}\right|^2 = 1+\omega^2\left(\frac{L^2}{4R_{LF}^2} + C^2R_{LF}^2 - LC\right)+\omega^4\left(\frac{L^2C^2}{2} - LR_{LF}^2C^3\right)$$

$$+\frac{\omega^6 R_{LF}^2 L^2 C}{4} \qquad (3.3)$$

and the power loss in dB may be obtained as

$$P_f = 10 \log_{10}\left|\frac{V_1}{V_2}\right|^2 \qquad (3.4)$$

It can be seen that this power loss will be zero when the output voltage V_2 is equal to V_1

Since the ratio of $\frac{V_1}{V_2}$ at the cut-off frequency, f_o is $\sqrt{2}$, then the ratio of the square of the absolute magnitude voltages in eqn.(3.3) becomes.

$$1 + \omega_o^2\left(\frac{L^2}{4R_{LF}^2} + C^2R_{LF}^2 - LC\right) + \omega_o^4\left(\frac{L^2C^2}{2} - LR_{LF}^2C^3\right) + \frac{\omega_o^6R_{LF}^2L^2C^4}{4}$$

$$= 2 \qquad (3.5)$$

From the above equation, it is seen that the term $\frac{\omega_o^6R_{LF}^2L^2C^4}{4}$ is very greater than $\omega_o^2\left(\frac{L^2}{4R_{LF}^2} + C^2R_{LF}^2 - LC\right)$ and $\omega_o^4\left(\frac{L^2C^2}{2} - LR_{LF}^2C^3\right)$. Hence the value of the frequency ω_o can be approximately calculated by

$$\omega_o = \left\{\frac{2}{R_{LF}LC^2}\right\}^{1/3} \qquad (3.6)$$

From the equation (3.4), the power loss P_f can be expressed in terms of the damping ratio, d and the frequency as

$$P_f = 10 \log_{10}\left\{1 + \frac{\omega^2}{\omega_o^2}\left(\frac{1}{d^{1/3}} - d^{2/3}\right)^2 - \frac{2\omega^4}{\omega_o^4}\left(\frac{1}{d^{1/3}} - d^{2/3}\right) + \frac{\omega^6}{\omega_o^6}\right\} \qquad (3.7)$$

Where d is the damping ratio, and

$$d = \frac{L}{2CR_{LF}^2} \qquad (3.8)$$

In general, the design engineers will first choose the cut-off frequency f_o and the value of the damping ratio d then the appropriate values of L, C can be determined from eqns.(3.6) and(3.7). A typical example for determining these values of L, C in the π -type filter will be given in chapter 5.

3.3 Mathematical analysis

The mathematical analysis of the switching regulator system shown in Fig 3.2 is based on the following assumptions.

(a) During each operation cycle, T,the voltage across the choke L is assumed to be constant.

(b) The saturation voltage of transistors, T_1 and T_2 and the conduction voltage of the diodes, D_1 and D_2 are assumed to be zero for the analysis.

(c) The rise time, fall time and delay time of the voltage waveform in the system are neglected.

(d) The choke L is assumed to be lossless.

(e) The transformer loss is also neglected.

Consider a switching system shown in Fig. 3.2

Let V_i be the input voltage

V_o be the output voltage

I_i be the input current

I_L be the output current

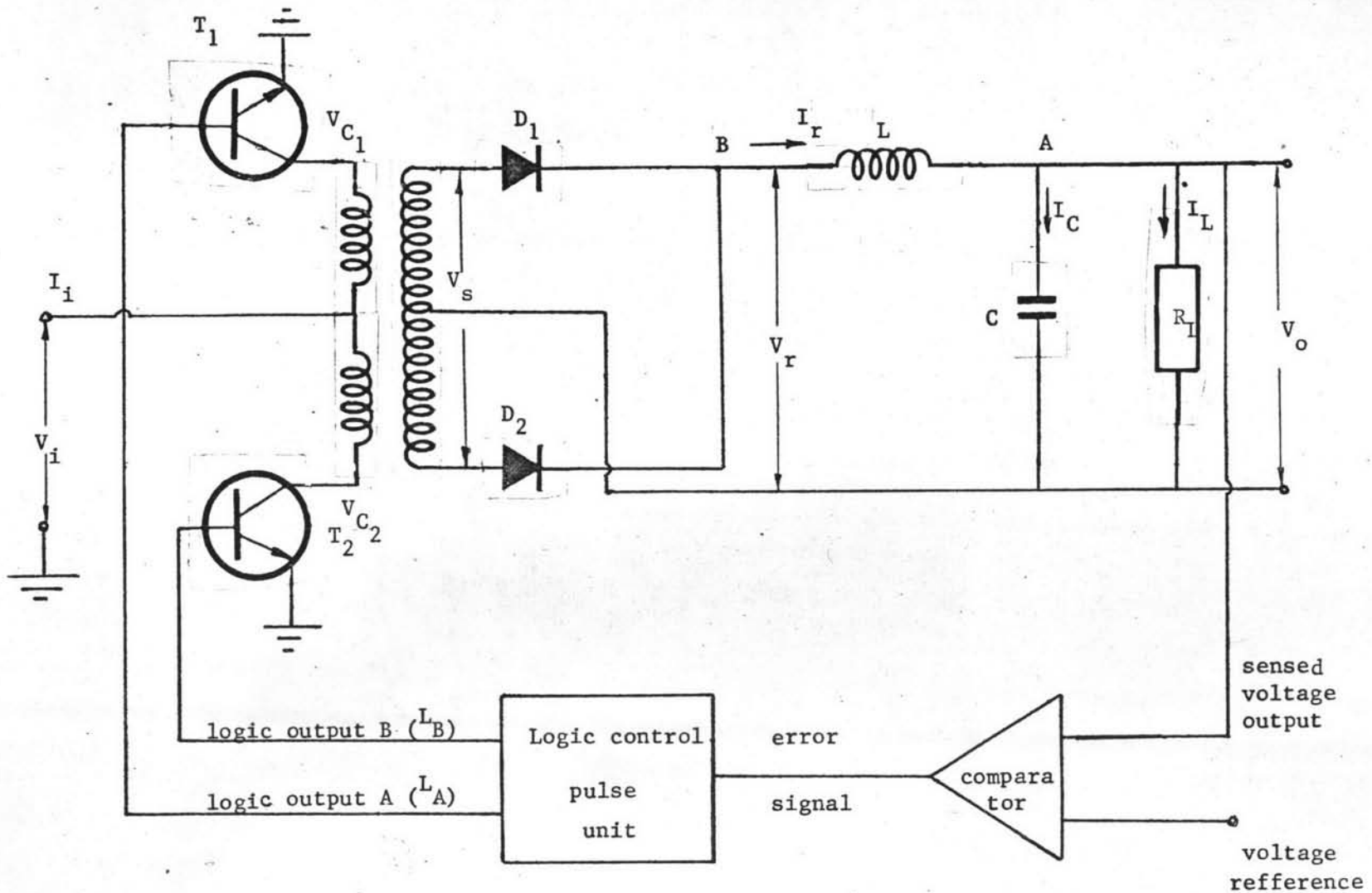


Fig. 3.2 A switching regulator system

V_{pp} be the output ripple voltage

I_{CT1} be the average collector current of transistor T_1

I_{CT2} be the average collector current of transistor T_2

V_r be the secondary voltage at point B

n be the number of turn ratio n:1 of transformer

I_r be the choke current

f be the operating frequency of a switching power transistor

E_o be the output voltage at which transistor turn on

I_C be the capacitor current

V_C be the voltage on capacitor(at $t = 0, V_C = E_o$)

From Fig.3.2,after comparing the voltage output and the refference voltage,the duration of the logic pulse will be controled by the error signal.The dc input voltage V_i is chopped by transistors T_1 and T_2 controlled by the logic control pulse unit. The waveform of the voltages at L_A,L_B and collector voltage of transistors can be illustrated in Fig.3.3

At steady state condition,let the output voltage be V_o and the pulse width produced by the logic control pulse unit be t_1 as indicated in Fig.3.3

Hence, the average input current, I_{av} may be determined by integration the current waveform.

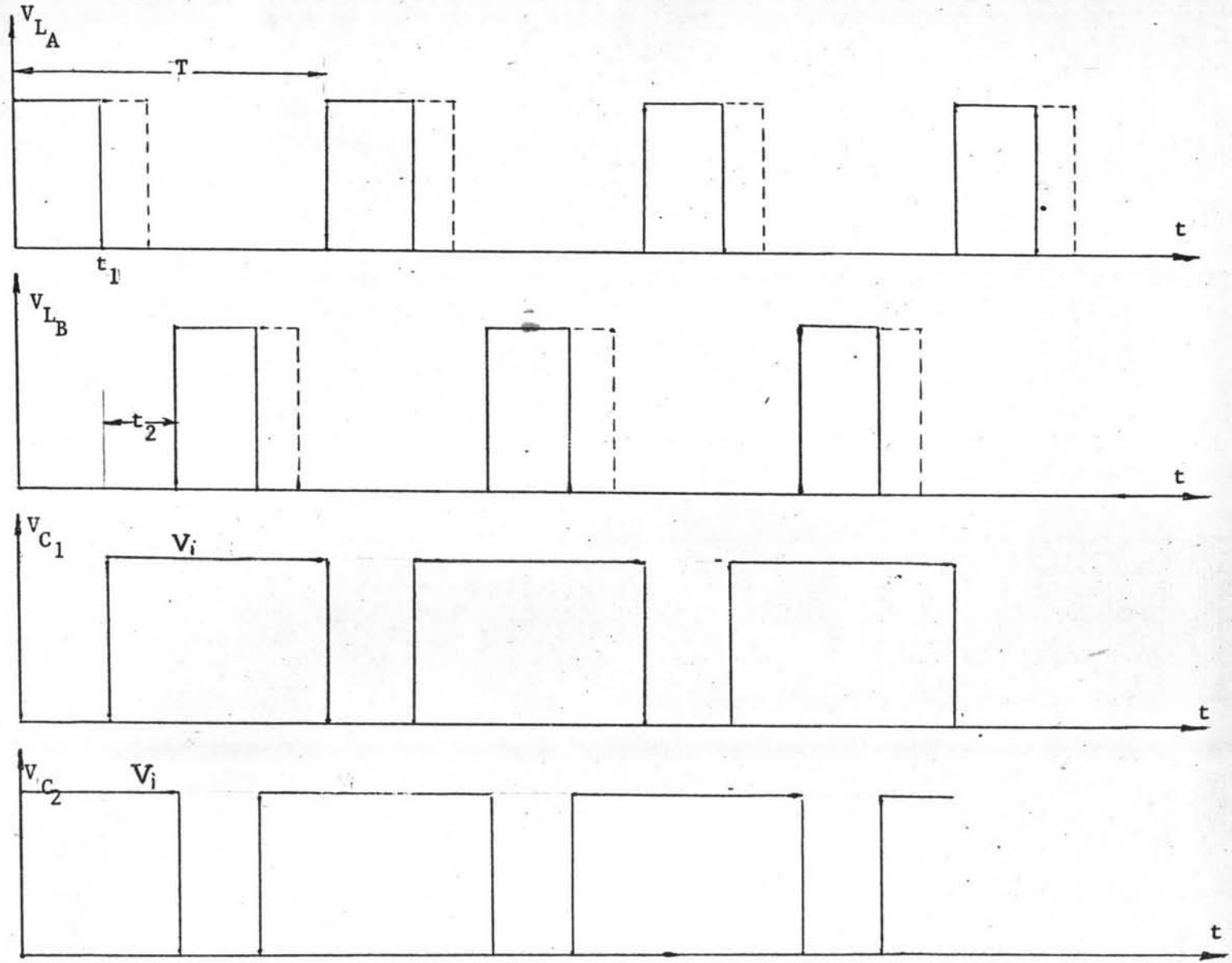


Fig. 3.3 The voltage waveforms at the output of the control pulse unit, L_A, L_B and the collector voltage , V_{C_1}, V_{C_2}

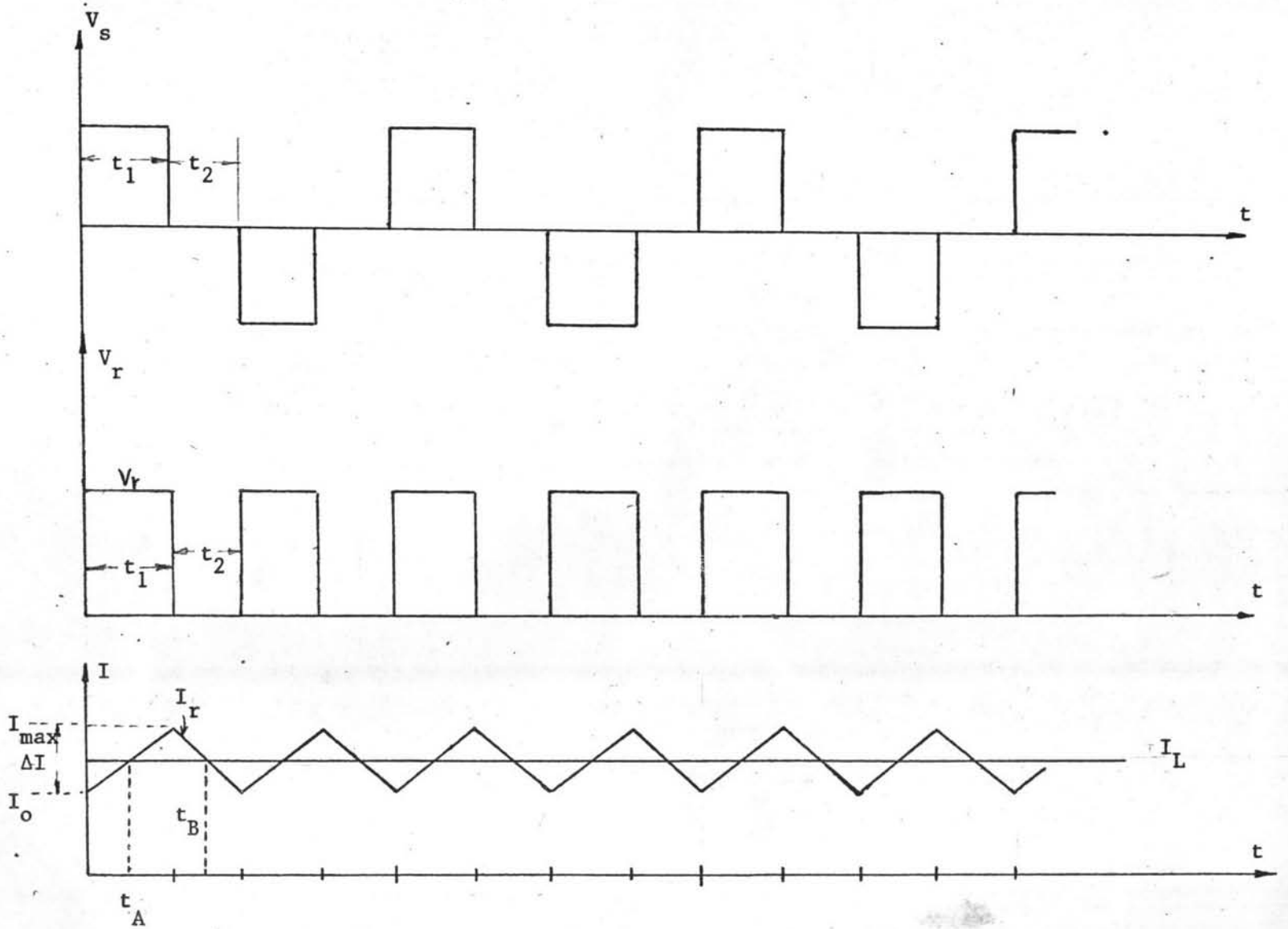
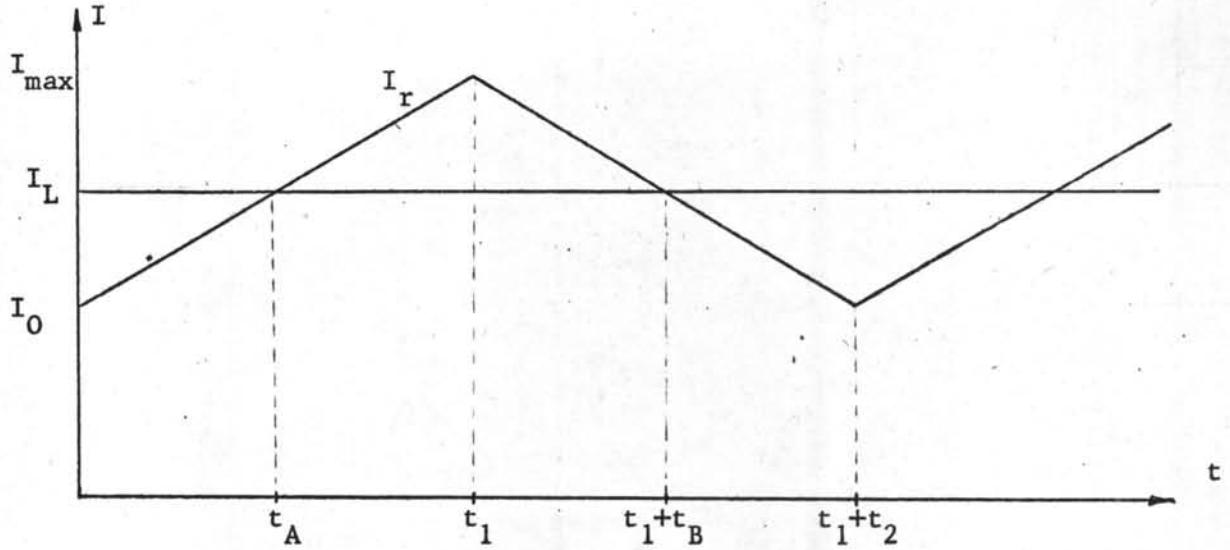
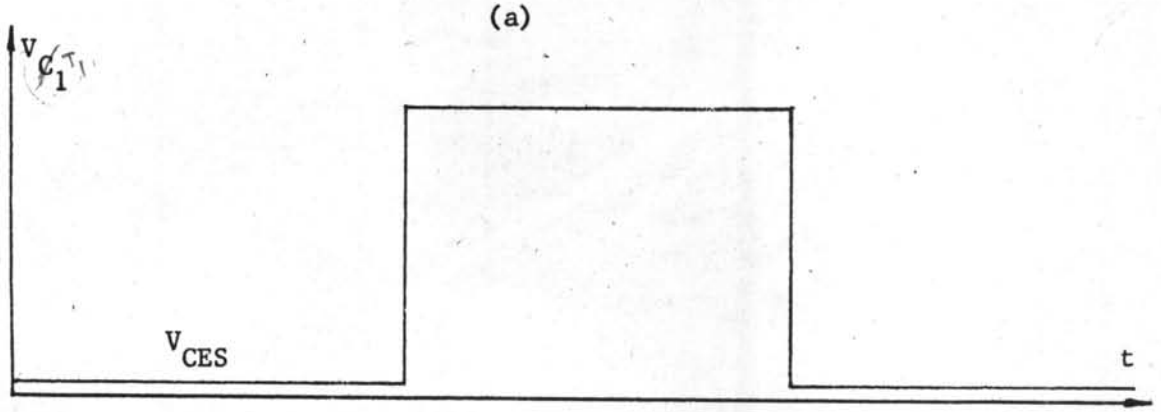


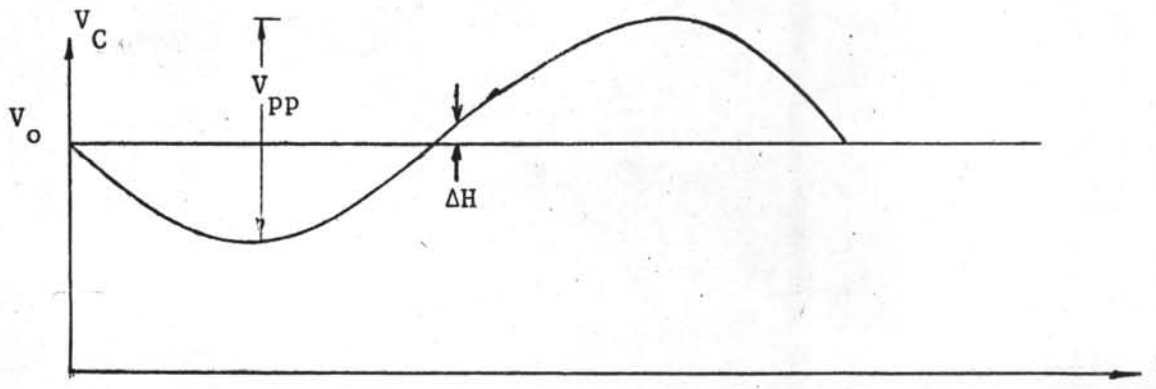
Fig. 3.4 The waveform of voltage and current at various points of the system shown in Fig. 3.2



(a)



(b)



(c)

Fig.3.5 (a) The waveform of the current delivered to load

(b) The collector voltage of the transistor T_1

(c) The output ripple voltage waveform

$$I_{av} = \frac{1}{T}\int_0^T I_i dt$$

$$= \frac{1}{T}\int_0^{t_1} \frac{E_i}{n^2 R_L} dt + \frac{1}{T}\int_{t_1+t_2}^{2t_1+t_2} \frac{E_i}{n^2 R_L} dt$$

$$= \frac{2E_i t_1}{Tn^2 R_L} \qquad (3.9)$$

Where t_1 be the time corresponding to the pulse width produced by the logic control pulse unit.

t_2 be the time corresponding to the off duty produced by the logic control pulse unit.

Similarly, the average collector currents of the transistors T_1 and T_2 are

$$I_{CT_1} = \frac{1}{T}\int_0^T I_{CT_1} dt$$

$$= \frac{V_i t_1}{Tn^2 R_L} \qquad (3.10)$$

$$I_{CT_2} = \frac{1}{T}\int_0^T I_{CT_2} dt$$

$$= \frac{V_i t_1}{Tn^2 R_L} \qquad (3.11)$$

It can be seen that the average collector current in both eqns. (3.10)and(3.11) are the same.

In the secondary side of the transformer shown in the Fig. 3.2 , the current I_r during the time $0 < t < t_1$ can be expressed as

$$I_r = \frac{(V_r - V_o)}{L} t + I_o \qquad (3.12)$$

Hence, the energy per cycle at the secondary transformer is determined by

$$P_C = 2 \int_o^{t_1} V_r I_r dt$$

$$= \frac{V_r (V_r - V_o) t_1^2}{L} + 2 V_r I_o t_1 \qquad (3.13)$$

According to the previous assumptions(b)and(d), the energy per cycle P_C divided by T will be the average power output of the system.

From Fig3.2 and eqn(3.12), the maximum current in diodes can be expressed as

$$I_{max} = \frac{(V_r - V_o)}{L} t_1 + I_o \qquad (3.14)$$

From eqns.(3.13)and(3.14), the energy per cycle becomes

$$P_C = \frac{V_r L (I_{max}^2 - I_o^2)}{V_r - V_o}$$

From Fig. 3.3 , the current I_r along the choke during the time $t_1 < t < t_1 + t_2$ can be expressed as

$$I_r = I_{max} - \frac{V_o (t - t_1)}{L} \qquad (3.16)$$

When the time $t = t_1 + t_2$, the current I_r is then equal to I_o . Therefore, the time t_2 will be

$$t_2 = \frac{L (I_{max} - I_o)}{V_o} \qquad (3.17)$$

From Fig. 3.3 the operating frequency of power transistors is

$$f = \frac{1}{2(t_1 + t_2)} \qquad (3.18)$$

From eqns.(3.14),(3.17)and(3.18), the value of the choke,L,can be expressed as

$$L = \frac{V_o (V_r - V_o)}{2 V_r f (I_{max} - I_o)} \qquad (3.19)$$

From Fig. 3.4, it can be seen that the time t_A is the time when the value of I_r reaches I_L, for $0 < t_A < t_1$, and the time t_B is the time when the value of I_r decays to I_L, for $t_1 < t_B < t_1 + t_2$

Hence, from eqns. (3.12) and (3.16) the value of t_A, t_B can be expressed as

$$t_A = \frac{(I_L - I_o)\, L}{V_r - V_o} \tag{3.20}$$

$$t_B = \frac{I_{max} - I_L\, L}{V_o} \tag{3.21}$$

respectively,

The ripple peak to peak voltage may be expressed as

$$V_{pp} = V_{Cmax} - V_{Cmin} \tag{3.22}$$

where

V_{pp} is the peak to peak ripple voltage

V_{Cmax} is the upper ripple voltage

V_{Cmin} is the lower ripple voltage

From Fig. 3.5 let

E_o be the output voltage at which transistor turns on.

$E_o + \Delta H$ be the output voltage at which transistor turns off.

From Fig 3.2, and applying Kirchoff's current law at node A, the current I_C along the capacitor during the time $0 < t < t_1$ is

$$I_C = -I_L + \frac{(V_r - V_o)}{L}\, t + I_o \tag{3.23}$$

Therefore, the value of voltage across the capacitor during the time $0 < t < t_1$ is

$$V_C(t) = E_o - \frac{(I_L - I_o)t}{C} + \frac{(V_r - V_o)t^2}{2LC} \tag{3.24}$$

From Fig. 3.5, the minimum value of $V_C(t)$ occurs when $t = t_A$ thus, we obtain

$$V_{Cmin}(t_A) = E_o - \frac{(I_L - I_o)^2 L}{2C\,(V_r - V_o)} \tag{3.25}$$

When $t = t_1$, the capacitor voltage becomes

$$V_C(t_1) = E_o - \frac{(I_L - I_o)}{C} t_1 + \frac{(V_r - V_o)}{2LC} t_1^2 \qquad (3.26)$$

From eqns. (3.12) and (3.16), the different current ΔI in these equations can be expressed as

$$\Delta I = \frac{(V_r - V_o)}{L} t_1 = \frac{V_o t_2}{L} \qquad (3.27)$$

From eqns (3.18) and (3.27) the time t_1 becomes

$$t_1 = \frac{V_o}{2fV_r} \qquad (3.28)$$

From Fig.3.5, substituting the value of t_1 into eqn.(3.26), then the different voltage between $V_C(t_1)$ and E_o, ΔH will be

$$\Delta H = (V_r - V_o)\left[\frac{V_o}{2fV_r}\right]^2 \frac{1}{2LC} - \frac{(I_L - I_o)}{2fCV_r} V_o \qquad (3.29)$$

Similarly, from Fig.3.2 and applying Kirchoff's current law at node A, the current I_C along the capacitor during the time $t_1 < t < t_1 + t_2$ is

$$I_C = -I_L + I_{max} - \frac{V_o(t - t_1)}{L} \qquad (3.30)$$

Therefore, the voltage across the capacity during the time $t_1 < t < t_1 + t_2$ is

$$V_C(t) = E_o + \Delta H + \frac{(I_{max} - I_L)(t - t_1)}{C} - \frac{V_o(t - t_1)^2}{2LC} \qquad (3.31)$$

Thus, we obtain

$$V_{Cmax}(t + t_B) = E_o + \Delta H + \frac{(I_{max} - I_L)^2 L}{2CV_o} \qquad (3.32)$$

The peak to peak ripple voltage V_{pp} can be determined by

$$V_{pp} = V_{Cmax}(t_1 + t_B) - V_{Cmin}(t_A)$$

$$= \Delta H + \frac{LV_r(I_{max} - I_L)^2}{2CV_o(V_r - V_o)} \qquad (3.33)$$

Substituting the value of ΔH into eqn (3.33) then the peak to peak ripple voltage V_{pp} will be

$$V_{pp} = \frac{V_r - V_o}{2LC}\left[\frac{V_o}{2fV_r}\right]^2 - \frac{(I_L - I_o)\,V_o}{2fCV_r} + \frac{LV_r(I_{max} - I_L)^2}{2CV_o(V_r - V_o)} \qquad (3.34)$$

Therefore the ripple factor is

$$r = \frac{V_{pp}}{E_o} \times 100 \qquad (3.35)$$

It can be seen that this ripple factor varies with L, V_r, V_o, f, I_{max}, I_L and C

3.4 Switching regulator loss

In a switching regulator system, most designers have their attention on four main types of losses.

These losses are summarized as .

(a) Conduction loss

(b) Switching loss

(c) Driver loss & control circuit loss

(d) Transformer loss

3.4.1 Conduction loss

This type of losses can be divided into three parts.

First part

Normally, the saturation voltage of a silicon type transistor is in the value of 0.5 to 1 Volt. Therefore, the loss occurs in the transistor will be

$$P_{TL} = V_{CES} I_C \frac{t_1}{T} \quad \text{Watts} \qquad (3.36)$$

Where V_{CES} be a saturation voltage drop between collector and emitter. (Volt)

I_C be the collector current of the transistor. (Amp.)

Second part

This loss occurs during the forward. The voltage drop in a silicon diode is about 0.6 to 1 Volt. Therefore the power loss can be obtained by

$$P_{DL} = V_d I_d \frac{t_1}{T} \text{ Watts} \tag{3.37}$$

Where V_d be the forward voltage drop across the diode.

I_d be the forward current in diode.

Third part

This loss occurs due to the resistance of the winding and normally is expressed in term of a factor of merit Q. In this case, the power loss can be determined by

$$P_{LL} = \frac{Q}{P_{re}} \tag{3.38}$$

Where P_{re} be the reactive loss and is obtained from

$$P_{re} = I_{Ch}^2 \times X_L \tag{3.39}$$

3.4.2 Switching loss

This type of loss occurs during the switching operation when transistors and diodes are used. In practice, the power loss due to this situration can be expressed in the form.

$$P_{ST} = fE_C I_C t_{off} \tag{3.40}$$

$$P_{SD} = fE_r I_D t_{off} \tag{3.41}$$

Where P_{ST} is the switching loss for transistor.

E_C is a collector voltage during the transistor off.

I_C is the collector current for transistor during the transistor on.

P_{SD} is the switching loss for diode.

I_d is the forward current of diode.

t_{off} is the turn off time.

3.4.3 Driver loss and control unit loss

The switching transistors must be driven with a substantial amount of base current to keep the saturation voltage down. The amount of the base current varies from device to device, and a reasonable guess is to choose industrial silicon type transistors having the value of $h_{FEmin} = 10$

In this case, the approximate power loss due to the driver can be expressed as.

$$P_{DR} = \frac{I_C}{h_{FE}} \times V_{CC} \qquad (3.42)$$

For the control unit, loss the IC's which consume low current are used. Therefore this loss is very small when compared to the driver loss.

3.4.4 High frequency transformer loss

This loss may be reduced when the high grade ferrite material is used. The efficiency of this kind of transformer can be greatly improved if the proper design has been made. A typical design of a high frequency transformer including numerical results will be presented in chapter 4.