CHAPTER IV

DESIGN OF REGULATOR CIRCUIT

A step by step calulation of circuits elements of an automatic voltage regulator for alternator will be described in the following sections in this chapter. The design is started at the power controller stage and worked backward to the comparison and sensing stages. The required specification of the regulator to be designed are as follows:

Voltage Regulation : Within $\pm 2.5\%$ from no load to full load and over a range of power factor from 1.0 to 0.8 lagging.

Regulator Output : 25 to 85 VDC at 10 amperes maximum continuous.

Voltage Adjust Range at No Load : $\pm$ 10 %

4.1 Power Controller Stage

Refer to Figure 3.6, A 110 VAC which is taken from the alternator terminals was chosen as the input voltage to the power controller stage. It is most practical to select the values of resistor R_{11} and capacitor C_5 in the suppression circuit by trial method via an examination of the waveform on an oscilloscope, and practically the value of R_{11} is in the order of a few hundred ohms and a capacitor C_5 in the order of 0.1 to 0.22 microfarads.

Selection of a 270 Ω for R_{11} and 0.1 microfarad for C_5 in this circuit provide a proper suppression. Other components value in the circuit can, however, determined by a straight forward manner.

The rating of components in this circuit are listed below:

SCR_1 and SCR_2	:	15 A (rms)	400 V (S4015L)
$D_8 - D_{12}$	:	10 A (avg)	200 V
C_5	:	0.1 μF	400 V
R_{11}	:	270 Ω	1 W.

4.2 Firing Circuit

In designing the firing circuit the triggering pulse period must be determined first. The period of the free running frequency of UJT is long when the alternator is at no load and becomes shorter when the load on the alternator is increased. The triggering pulse period at these conditions (no load and full load) can be determined as follows.

a) For Alternator at Noload. (Minimum Regulator Output)

Since the specified minimum output voltage of the regulator is 25 VDC, but it is a common practice to design a regulator with a slightly lower output value than that of the specified value, ie. a 20 VDC for this design, in order to ensure satisfactory operation of the circuit.

The average voltage from a full wave rectifier circuit is

$$V_{av} = \frac{1}{\pi} \int_{\theta}^{\pi} V_m \sin \omega t \, d\, \omega t \quad \ldots\ldots\ldots\ldots \quad (4.1)$$

Where V_{av} : average voltage

V_m : peak or crest voltage of the sine wave

ω : angular velocity

θ : firing angle

The output voltage of the regulator at this no load condition is

$$V_{av} = 20$$

$$= \frac{1}{\pi} \int_{\theta}^{\pi} V_m \sin \omega t \, d\, \omega t$$

$$= \frac{1}{\pi} \int_{\theta}^{\pi} 110\sqrt{2} \sin \omega t \, d\, \omega t$$

$$= \frac{110\sqrt{2}}{\pi} \left(- \cos \omega t \right)_{\theta}^{\pi}$$

or $\theta = 126.6^{\circ}$

The frequency of the generated voltage is 50 Hz , that is each half cycle (180°) of the sine wave will correspond to a period of time of 10 ms. Then at the firing angle of 126.6° will correspond to a period of time of $\frac{10}{180} \times 126.6 = 7.0$ ms.

It is therefore, at minium regulator output voltage, the timing period of the triggering pulse is 7.0 ms.

b) For Alternator at Full-load (Maximum Regulator Output)

At the maximum regulator output voltage, a slightly higher output value than that of the specified value, ie. a 90 VDC was selected for the design in order to ensure satisfactory operation of the circuit. The triggering pulse period of this condition can be determined in the same way as at the noload condition and this value of time is 1.9 ms.

A 27 VDC was selected for the DC supphy voltage of the circuit. A 2N2646 unijunction transistor was chosen for the firing circuit for it has low peak-point current, low emitter reverse current and easily obtained in local market with a resonable price. The data sheet for the 2N2646 (Appendix A) gives the following specifications.

$V_{EB1\,(sat)}$ = 3.5 V typical I_p = 5.0 μA maximum

η = 0.56 - 0.75 I_v = 4.0 mA minimum

r_{BB} = 4.7 - 9.1 KΩ (Typical 7.0 KΩ)

The average value of the intrinsic standoff ratio is

$$\eta_{av} = \frac{0.56 + 0.75}{2} = 0.655$$

From eq. 3.3 ; the peak-point voltage is

$$V_p = V_D + \eta V_{EE}$$
$$= 0.6 + (0.655 \times 27)$$
$$= 18.285 \text{ V}$$

And the valley voltage

$$V_v \doteq V_{EB1}(sat)$$

$$= 3.5 \text{ V}$$

From eq. 3.2

$$R_E(max) \leq \frac{V_{EE} - V_p}{I_p}$$

$$= \frac{27 - 18.285}{5\ \mu A}$$

$$= 1.743 \text{ M}\Omega$$

From eq. 3.4

$$R_E(min) \leq \frac{V_{EE} - V_v}{I_v}$$

$$= \frac{27 - 3.5}{4 \text{ mA}}$$

$$= 5.875 \text{ K}\Omega$$

It is seen from Figure 3.4 that the output pulse or the oscillation period of the UJT Q_3 is controlled by varying the emitter resistance (R_{CE} of Q_2), the value of the emitter capacitor C_6 must be determined at the minimum time of pulse period (maximum regulator output voltage) that is at the pulse period of 1.9 mS.

From eq. 3.1

$$C_6 \leq \frac{t\,(\min)}{R_{E_{min}} \ln\left(\frac{V_{EE} - V_o}{V_{EE} - V_c}\right)}$$

$$= \frac{1.9 \times 10^{-3}}{5.875 \times 10^{3} \ln\left(\frac{27 - 3.5}{27 - 18.285}\right)}$$

$$= 0.326 \ \mu F$$

A standard value of 0.22 μF 400 V for C_6 was used.

The base 1 resistor R_{18} can be directly determined from equation 3.5 as follow,

$$R_{18} \doteq \frac{0.2\, r_{BB}\,(\min)}{V_{EE}}$$

$$= \frac{0.2 \times 4.7 \times 10^{3}}{27}$$

$$= 34.82 \ \Omega$$

A standard value of 33 Ω $\frac{1}{2}$ W for R_{18} was used.

The temperature compensation resistor R_{17} can be approximately determined by using equation 3.6 as follow,

$$R_{17} \doteq \frac{0.7\, r_{BB}}{\eta\, V_{EE}} + \frac{(1 - \eta)\ R_{18}}{\eta}$$

$$= \frac{0.7 \times 7.0 \times 10^{3}}{0.655 \times 27} + \frac{(1 - 0.655) \times 33}{0.655}$$

$$= 294.45 \ \Omega$$

A typical standard value of 330 Ω $\frac{1}{2}$ W for R_{17} was used.

The resistors R_{19} and R_{20} presented in the circuit of Figure 3.4 are used to limit the gate current of the thyristors, and their values can be determined as follow.

From the specifications of the SCR1 and SCR2 (S 4015L)

I_{GT} (max) = 20 mA at T_C 25° C

V_{GT} (max) = 1.5 V at T_C 25° C

P_G (av) = 0.6 W

Since $P_G = I_G * V_G$

$$I_G = \frac{P_G}{V_G}$$

$$= \frac{0.6}{1.5} = 0.40 \text{ A}$$

The peak voltage of the output pulse from base 1 of the UJT (Q_3) is

$$V_{oB1} = V_p - V_v$$

$$= 18.285 - 3.5 = 14.79 \text{ V}$$

Then $R_{19} = R_{20} = \frac{V_{oB1} - V_G}{I_G}$

$$= \frac{14.79 - 1.5}{0.40}$$

$$= 33.29 \ \Omega$$

A typical standard resistor of 33 Ω $\frac{1}{2}$ W was used for R_{19} and R_{20}. A 2N4037 silicon PNP transistors of which specification given hereunder was selected for the transistors Q_1 and Q_2 of Fig 3.4.

P_D = 1.0 W

T_J = 200° C

V_{CEO} = 40 V

h_{FE} (min) = 50

h_{FE} (max) = 250 at I_C 0.15 A

V_{CBO} = 60 V

f_T = 60 MHz

Since, the charge in any capacitor can be written as

$$\Delta Q = C \Delta V$$

In term of charging current, it well be

$$I \Delta t = C \Delta V$$

or $$I = \frac{C \Delta V}{\Delta t}$$

Where I = charging current of the capacitor (amp.)

C = capacitance (farad)

ΔV = change in voltage across capacitor during time Δt (volt)

Δt = duration of time (sec.)

Since the capacitance of the capacitor C_6 is 0.22 μF

Then $\Delta V = V_p - V_{EB1}(sat)$

$= 18.285 - 3.5$

$= 14.785$ V

At maximum regulator output

Since, at maximum output voltage from the regulator the time of oscillation period is 1.9 ms (see Fig. 4.1) and this corresponds to a maximum average collector current of the transistor Q_2

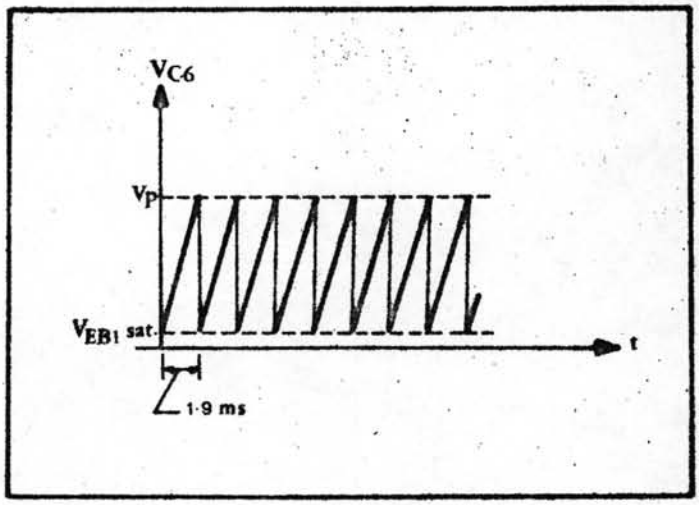

Figure 4.1 : Voltage Across Emitter Capacitor at Maximum Regulator Output.

Therefore, $I_{cQ2_{max}} = \frac{C_6 \Delta V}{\Delta t_{min}}$

$= \frac{0.22 \times 10^{-6} \times 14.785}{1.9 \times 10^{-3}}$

$= 1.712$ mA

$$I_{bQ2_{max}} = \frac{I_{cQ2_{max}}}{h_{FE_{min}}}$$

$$= \frac{1.712 \text{ mA}}{50}$$

$$= 0.034 \text{ mA}$$

Given the collector voltage of transistor Q_1 ($V_{c_{Q1}}$) to be a half of the dc supply voltage.

That is $V_{c_{Q1}} = \frac{27}{2}$

$= 13.5$ V

Then $V_{R14} = 13.5$ V

In DC amplifier the quiescent voltage must be compensated for in some way in order that the following stage is not saturated and for the circuit of Figure 3.4 the voltage across R_{13} should be approximately equal to V_{CB} of transistor Q_1 (7)

Since $V_{CB_{Q1}} = V_{CE_{Q1}} - V_{BE_{Q1}}$

and $V_{CE_{Q1}} = V_{EE} - V_{R14} - V_{z1}$

Select V_{z1} to be 6.2 volts.

$$V_{CB_{Q1}} = V_{EE} - V_{R14} - V_{z1} - V_{BE_{Q1}}$$

$$= 27 - 13.5 - 6.2 - 0.6$$

$$= 6.7 \text{ V}$$

Then $V_{R13} = 6.7\ V$

$V_{R12} = V_{EE} - V_{R14} - V_{R13}$

$= 27 - 13.5 - 6.7$

$= 6.8\ V$

It is most practical to design the current through resistors R_{12} and R_{13} to such a level that current Ib_{Q2} will not loaded the divider network.

For this design, a current of 0.6 mA will be chosen for I_{R12} which is much more than the current Ib_{Q2} (0.034 mA)

$$R_{12} = \frac{V_{R12}}{I_{R12}}$$

$$= \frac{6.8}{0.6\ mA}$$

$$= 11.33\ K\Omega$$

A typical standard value of 12 KΩ $\frac{1}{2}$ W was used for R_{12}

$$R_{13} = \frac{V_{R13}}{I_{R13}} \doteq \frac{V_{R13}}{I_{R12}}$$

$$= \frac{6.7}{0.6\ mA}$$

$$= 11.17\ K\Omega$$

A 12 KΩ $\frac{1}{2}$ W standard resistor for R_{13} was used.

It can be seen from the characteristics curves of 2N 4037 that the maximum DC forward current gain (h_{FE}) occurs at its collector of about

8 - 12 mA, but high I_C will consequence in high losses, therefore operating collector current of Q_1 must be chosen at a suitable value near to the current at which maximum h_{FE} occurs but with a resonable losses.

In this design, therefore, a minimum collector current of 3 mA is chosen.

Therefore, at maximum regulator output;

$$I_{c_{Q1}} = I_{c_{Q1\ min}} = 3 \text{ mA}$$

$$I_{R14} = I_{c_{Q1\ min}} + I_{R13}$$

$$= 3 + 0.6$$

$$= 3.6 \text{ mA}$$

$$R_{14} = \frac{V_{R14}}{I_{R14}}$$

$$= \frac{13.5}{3.6 \text{ mA}}$$

$$= 3.75 \text{ K}\Omega$$

A 3.9 KΩ $\frac{1}{2}$ W typical standard resistor for R_{14} was used

$$V_{R16} = V_{EE} - V_{R12} - V_{CB_{Q2}} - V_p$$

$$= V_{EE} - V_{R12} - (V_{CE_{Q2}} - V_{BE_{Q2}}) - V_p$$

The minimum collector to emitter voltage of the transistor Q_2 should be more than 1 volt in order to assure that this transistor will never saturated.

$V_{CE_{Q2\ min}} = 1\ V$

Then $V_{R16} = 27 - 6.8 - (1 - 0.6) - 18.285$

$= 1.52\ V$

$$R_{16} = \frac{V_{R16}}{I_{C_{Q2\ max}}}$$

$$= \frac{1.52}{1.712\ mA}$$

$= 0.89\ K\Omega$

A typical standard resistor of 1 KΩ $\frac{1}{2}$ W for R_{16} was used.

<u>At minimum regulator output</u>

At the output from the regulator is minimum, the time of oscillation period is 7.0 ms (see Fig. 4.2) and this corresponds to a minimum average current of transistor Q_2

Therefore, $$I_{C_{Q2\ min}} = \frac{C_6\ \Delta V}{\Delta t\ max}$$

$$= \frac{0.22 \times 10^{-6} \times 14.785}{7.0 \times 10^{-3}}$$

$= 0.465\ mA$

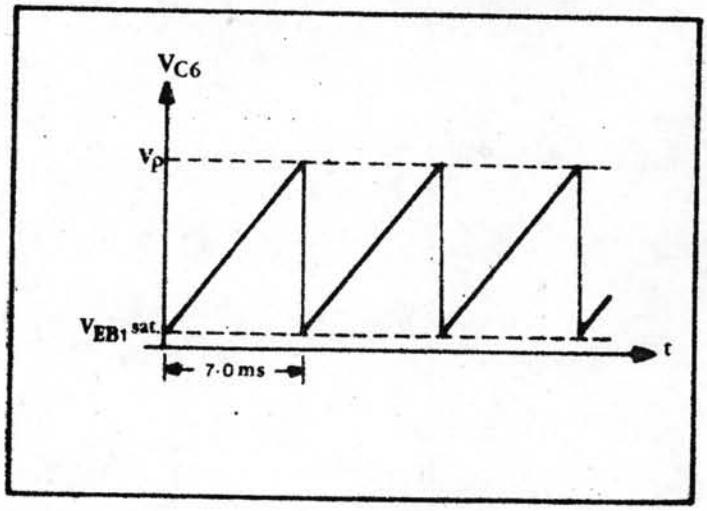

Figure 4.2 : Voltage Across Emitter Capacitor at Minimum Regulator Output.

$$Ib_{Q2\ min} = \frac{I_{c_{Q2\ min}}}{h_{FE\ min}}$$

$$= \frac{0.465}{50}$$

$$= 0.009 \text{ mA}$$

$$I_{E_{Q2\ min}} = Ib_{Q2\ min} + I_{cQ2\ min}$$

$$= 0.009 + 0.465$$

$$= 0.474 \text{ mA}$$

$$V_{R15} = V_{EE} - V_{R14} - V_{R13} - V_{BE_{Q2}}$$

$$= V_{EE} - (V_{EE} - V_{z1} - V_{CE_{Q1\ sat.}}) - V_{R13} - V_{BE\ Q2}$$

$$= V_{z1} + V_{CE_{Q1\ sat.}} - V_{R13} - V_{BE_{Q2}}$$

Since $I_{R13} = \frac{V_{R12} + V_{R13}}{R_{12} + R_{13}}$

$$I_{R13} = \frac{V_{z1} + V_{CE_{Q1\ sat.}}}{R_{12} + R_{13}}$$

$$= \frac{6.2 + 0.3}{12\ K\Omega + 12\ K\Omega}$$

$$= 0.271\ mA$$

Then $V_{R15} = 6.2 + 0.3 - (0.271 \times 12) - 0.6$

$$= 2.64\ V$$

$$R_{15} \leq \frac{V_{R15}}{I_{E_{Q2\ min.}}} = \frac{2.64}{0.474\ mA}$$

$$= 5.57\ K\Omega$$

A 4.7 KΩ $\frac{1}{2}$ W standard resistor value for R_{15} was used.

4.3 Comparison and Error Amplifier.

A 27 VDC was also selected for the supply voltage (V_1) of the comparison and error amplifier circuit of Fig. 3.3.

The value of the current through the divider network R_1, R_2, R_3 and R_4 must be much more than the base current of the transistor Q_1 in order that the transistor Q_1 will not loaded the network.

$$\therefore I_{R1} >> Ib_{Q1}$$

$$\therefore \text{Since } I_{c_{Q1\ max}} = \frac{V_{EE} - V_{z1} - V_{CE_{Q1\ (sat)}}}{R_{14}}$$

$$I_{c_{Q1\ max}} = \frac{27 - 6.2 - 0.3}{3.9\ K\Omega}$$

$$= 5.26\ mA$$

$$Ib_{Q1} = \frac{I_{c_{Q1\ max}}}{h_{FE}}$$

$$= \frac{5.26\ mA}{50}$$

$$= 0.11\ mA$$

In this design, $I_{R1} = 15\ mA$ was selected.

Since, the specification of the regulator to be designed specified an allowable voltage adjust range of the alternator terminal voltage to be ± 10 % of the nominal voltage, then the variable resister R_2 must be designed to fulfill this requirement.

Therefore $$R_2 = \frac{V_{R2\ max}}{I_{R_2}}$$

$$= \frac{0.1\ V_1}{I_{R2}} \doteq \frac{0.1\ V_1}{I_{R1}}$$

$$= \frac{0.1 \times 27}{15\ mA}$$

$$= 180\ \Omega$$

A standard variable wire-wound resitor of 200 Ω for R_2 was used.

The variable resistor R_3 was included for providing an additional fine adjustment of the alternator voltage, therefore a 100 Ω variable wire-wound resistor was selected for R_3

$$V_{R1} + \tfrac{1}{2} V_{R2\ max} \doteq V_{z1} + V_{BE_{Q1}}$$

$$V_{R1} = V_{z1} + V_{BE_{Q1}} - \tfrac{1}{2} V_{R2\ max}$$

$$= 6.2 + 0.6 - \tfrac{1}{2} (0.1 \times 27)$$

$$= 5.45 \text{ V}$$

$$R1 = \frac{V_{R1}}{I_{R1}}$$

$$= \frac{5.45}{15 \text{ mA}}$$

$$= 363.3\ \Omega \text{ , Used } 330\ \Omega \text{ std. value.}$$

The power dissipated in R_1 is :

$$P_{R_1} = I_{R_1}^2 \times R_1$$

$$= (15 \times 10^{-3})^2 \times 330$$

$$= 0.074 \text{ W}$$

A $330\ \Omega$ $\frac{1}{2}$ W standard resistor for R_1 was used.

$$V_{R_4} = V_1 - V_{R_1} - \tfrac{1}{2} V_{R_{2\ max}}$$

$$= 27 - 5.45 - \tfrac{1}{2} (0.1 \times 27)$$

$$= 20.20 \text{ V}$$

$$R_4 = \frac{V_{R4}}{I_{R4}} \doteq \frac{V_{R4}}{I_{R1}}$$

$$= \frac{20.20}{15 \text{ mA}}$$

$$= 1.35\ \text{K}\Omega \text{ , used } 1.5\ \text{K}\Omega \text{ std. value.}$$

Power dissipated in R_4 is :

$$P_{R4} = I_{R4}^2 \times R_4$$

$$= (15 \times 10^{-3})^2 \times 1.5 \times 10^3$$

$$= 0.34 \text{ W}$$

A 1.5 KΩ 1 W standard resistor for R_4 was used.

The current through resistor R_5 must be much more than the emitter current of Q_1 in order to keep the voltage across zener diode z_1 to a nearly constant value.

Select $I_{R5} = 15 \text{ mA}$

$$V_{R5} = V_1 - V_{z1}$$

$$= 27 - 6.2$$

$$= 20.80 \text{ V}$$

$$R_5 = \frac{V_{R5}}{I_{R5}}$$

$$= \frac{20.80}{15 \text{ mA}}$$

$$= 1.39 \text{ KΩ}, \text{ used } 1.5 \text{ KΩ std. value.}$$

The power dissipated in R_5 is :

$$P_{R5} = I_{R5}^2 \times R_5$$

$$= (15 \times 10^{-3})^2 \times 1.5 \times 10^3$$

$$= 0.34 \text{ W}$$

A 1.5 KΩ 1 W standard resistor was chosen for R_5.

Power dissipated in the zener diode z_1 is :

$$P_{z1} = I_{z1} \times V_{z1} \doteq I_{R1} \times V_{z1}$$

$$= (15 \times 10^{-3}) \times 6.2$$

$$= 0.093 \text{ W}$$

Therefore a BZX 83 C 6V2 zener diode which has a zener voltage of 6.2 volts and rating of 400 mW was chosen for Z1.

4.4 Sensing Circuit

A Simple full wave rectifier and L-section LC filter as illustrated in Figure 3.2 was used for the sensing circuit.

Since, the load current of the sensing circuit is $(I_{R1} + I_{R5})$

$$I_{R1} + I_{R5} = 15 + 15$$

$$= 30 \text{ mA}$$

Then, the load resistance of this circuit is

$$R_L = \frac{V_1}{I_{R1} + I_{R5}}$$

$$= \frac{27}{30 \text{ mA}}$$

$$= 900 \ \Omega$$

From L-section LC filter, the value of inductance of the filter choke can be determined by[8]:

$$L \geq \frac{R_L}{3\omega}$$

Where L : inductance of the filter choke (Henry)

ω : angular velocity = $2\pi f$ (Radian)

R_L : load resistance (Ohm)

f : supply frequency (Hz)

Then $L_1 \geq \frac{900}{3(2\pi \times 50)}$

$= 0.96$ Henry

In practical designs, two or three times higher inductance than that calculated value is chosen in order to avoid the saturation of the filter choke.[9]

Therefore, a 3 Henry 100 mA was chosen for L_1

Given the ripple of the output voltage from the filter to be 2 %, then the value of filter capacitor C_1 can be easily determined as follow.[8]

From L-section LC filter, $r = \frac{\sqrt{2}}{3} \times \frac{1}{2\omega C} \times \frac{1}{2\omega L}$

Where r : ripple factor

ω : angular velocity = $2\pi f$ (radian)

f : supply frequency (Hz)

C : capacitance of the filter capacitor (farad)

L : inductance of the filter choke (henry)

$$\text{Then} \quad 0.02 = \frac{\sqrt{2}}{3} \quad \frac{\uparrow}{2\,(2\pi \times 50)C_1} \times \frac{\uparrow}{2\,(2\pi \times 50) \times 3}$$

$$C_1 = 19.9\ \mu F$$

Therefore, a standard capacitor of 22 μF/50 WV was chosen for C_1

All other remaining components in the sensing circuit can be determined by a straight forward manner. The rating of the components composite in the sensing circuit is listed below

Potential transformer T_1;

Primary : 0 - 380 V and tapped at 110, 190, 220 volts

Secondary : 30 V 100 mA

Diode $D_1 - D_4$: 1N4004

Choke L_1 : 3 H 100 mA

Capacitor C_1 : 22 μF 50 WV

4.6 Stabilizing Network

Consider the stabilizing network of Figure 3.7, if V_i denotes the input voltage to the network and V_o is the output voltage from the network.

Then the transfer function can be written as equation 4.2

$$\frac{V_o(s)}{V_i(s)} = \frac{1 + aTS}{1 + TS} \quad \ldots\ldots\ldots\ldots\ldots (4.2)$$

Where T : time constant = $(R_9 + R_{10})\, C_4$

$$a : \frac{R_9}{R_9 + R_{10}}$$

The technique of improving the response of the system is to choose values of C_4 and $(R_9 + R_{10})$ so that the time constant T is equal to the time constant of the field winding of the alternator[6]. For the conventional alternators of rating in the range considered in this work, ie. 10 - 25 KW, the time constant of the field winding is in the order of 0.2 second.

In this case ; $(R_9 + R_{10})\, C_4 = 0.2$

If a capacitor of 8 μF 100 V is chosen for C_4.

Then $$R_9 + R_{10} = \frac{0.2}{8 \times 10^{-6}}$$

$$= 25 \text{ K}\Omega$$

The fraction $a = \frac{R_9}{R_9 + R_{10}}$ is less than unity and if "a" is set to be 0.1

Then $$\frac{R_9}{R_9 + R_{10}} = 0.1$$

$$R_9 = 0.1\,(R_9 + R_{10})$$

$$= 0.1 \times 25$$

$$= 2.5 \text{ K}\Omega$$

A standard resistor of 2.2 KΩ $\frac{1}{2}$ W for R_9 was used.

Substituting R_9 we get ; $\frac{2.2}{2.2 + R_{10}} = 0.1$

$$R_{10} = 19.8 \text{ K}\Omega$$

A standard value of 22 KΩ $\frac{1}{2}$ W for R_{10} was used.

A resistor of 47 KΩ $\frac{1}{2}$W and a capacitor of 5 μF 160 V were also chosen for R_8 and C_3 respectively in order to provide a feedback path from the stability network to the error amplifier stage.

The variable resistor R_6 of 2.2 KΩ was added for providing a further adjust of the feedback current from the R-C stabilizing network to the error amplifier stage input.

The completed circuit diagram of the voltage regulator for alternator that had just designed is shown in Figure 4.3. The capacitor C_7 of 50 V was provided as a smoothing component to ensure a good DC supply for the error amplifier stage and the diode D_7 prevent the discharge current from C_7 to flow into the firing circuit.

Zener diode Z_2 used to stabilize the supply bias voltage for the transistor circuits to a nearly constant level. The zener current of the zener diode Z_2 must be chosen at such a level that has a comparatively larger than its load current.

Since, $I_{D7} \doteq I_{EQ1} + I_{R12} + I_{EQ2}$

$$= \left(3 + \frac{3}{50}\right) + 0.6 + (1.712 + 0.034)$$

$$= 5.41 \text{ mA}$$

Then, choose $I_{Z2\ max} = 15$ mA

The maximum power disipation of the zener diode Z_2 is :

$$P_{Z2} = I_{Z2} \times V_{Z2}$$
$$= 15 \text{ mA} \times 27 \text{ V}$$
$$= 0.41 \text{ W}$$

A 27 V 1 W zener diode for Z_2 was used.

The resistor R_{21} used to reduce the supply voltage to a suitable level for supplying the transistor circuits, and this resistance value can be calculated as follow.

$$R_{21} = \frac{V_{R21}}{I_{R21}}$$
$$= \frac{(110/1.11) - V_{Z2}}{I_{Z2 \text{ max}}}$$
$$= \frac{(110/1.11) - 27}{15 \text{ mA}}$$
$$= 4.81 \text{ K}\Omega \text{ , used } 4.7 \text{ K}\Omega \text{ std. value.}$$

The power dissipated in R_{21} is

$$P_{R21} = I_{R21}^2 \times R_{21}$$
$$= (15 \times 10^{-3})^2 \times 4.7 \times 10^3$$
$$= 1.06 \text{ W}$$

A 4.7 KΩ 5 W resistor for R_{21} was used.

The resistor R_7 of 1.5 KΩ and the capacitor C_2 of 6 μF/25V had been added in the circuit of Fig. 4.3 to prevent high-frequency instability.

The waveform at various parts on the completed circuit of Fig. 4.3 traced on an oscilloscope, by supply a 50 Hz sinusoidal voltage to the power input terminals of the regulator, are illustrated in Figure 4.4 and 4.5.

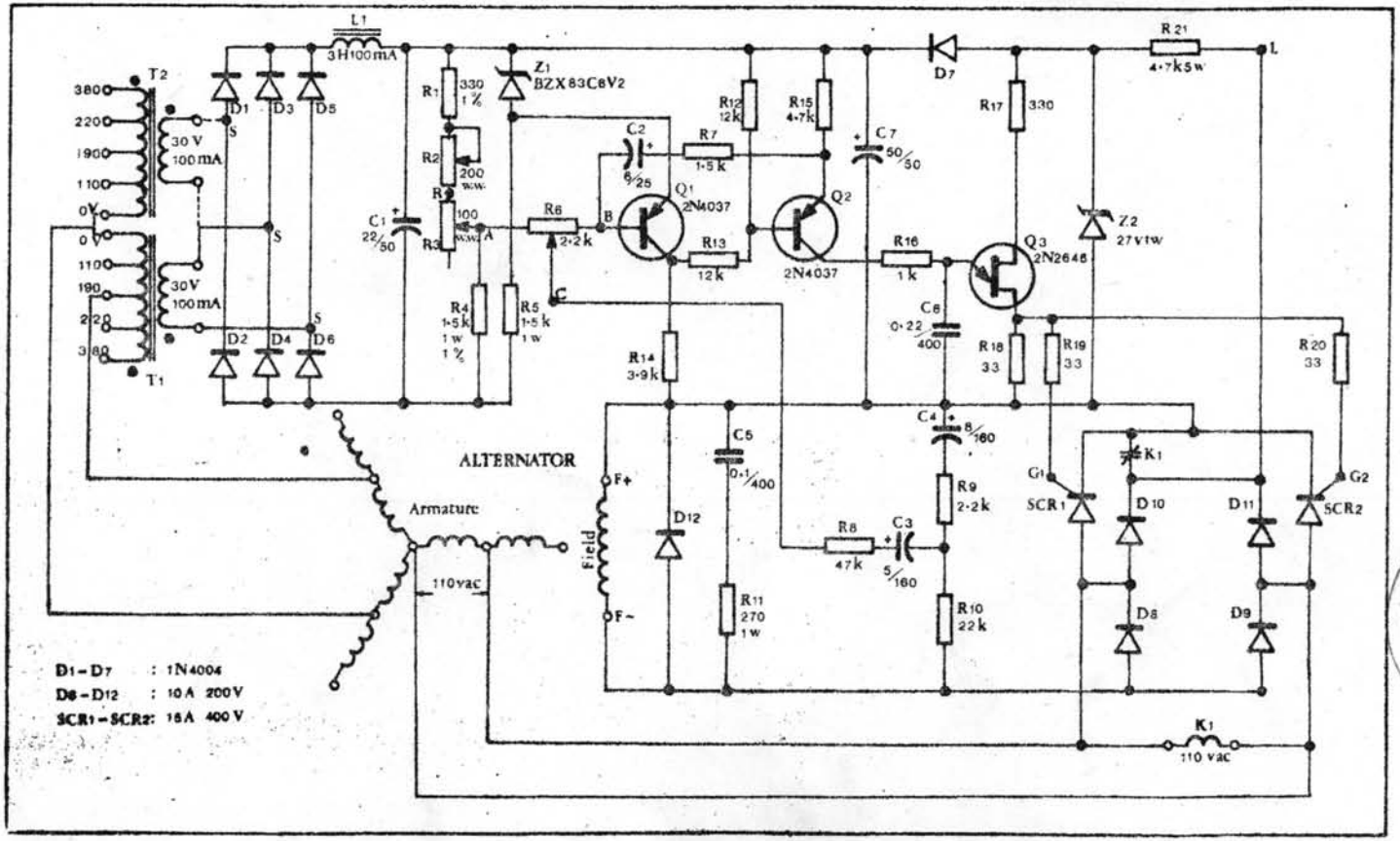

Figure 4.3 : Complete Circuit Diagram of the Voltage Regulator for Alternator.

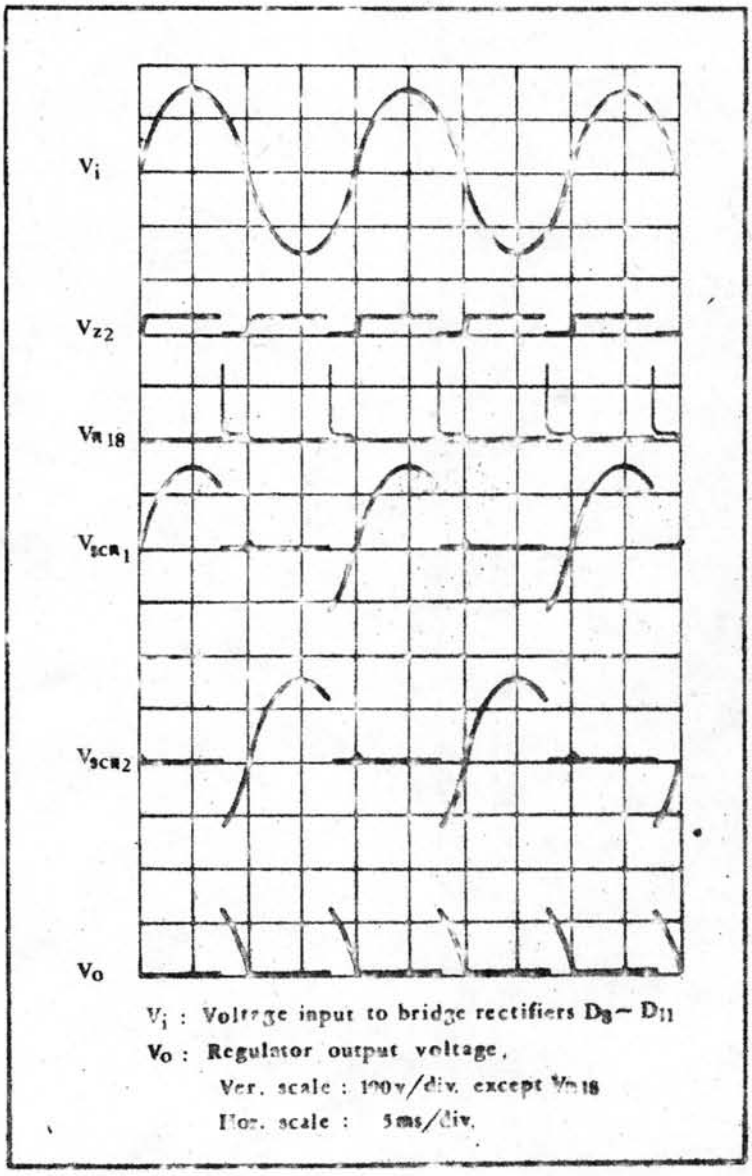

Figure 4.4 : Voltage Waveforms at Minimum Specified Regulator Output Voltage.

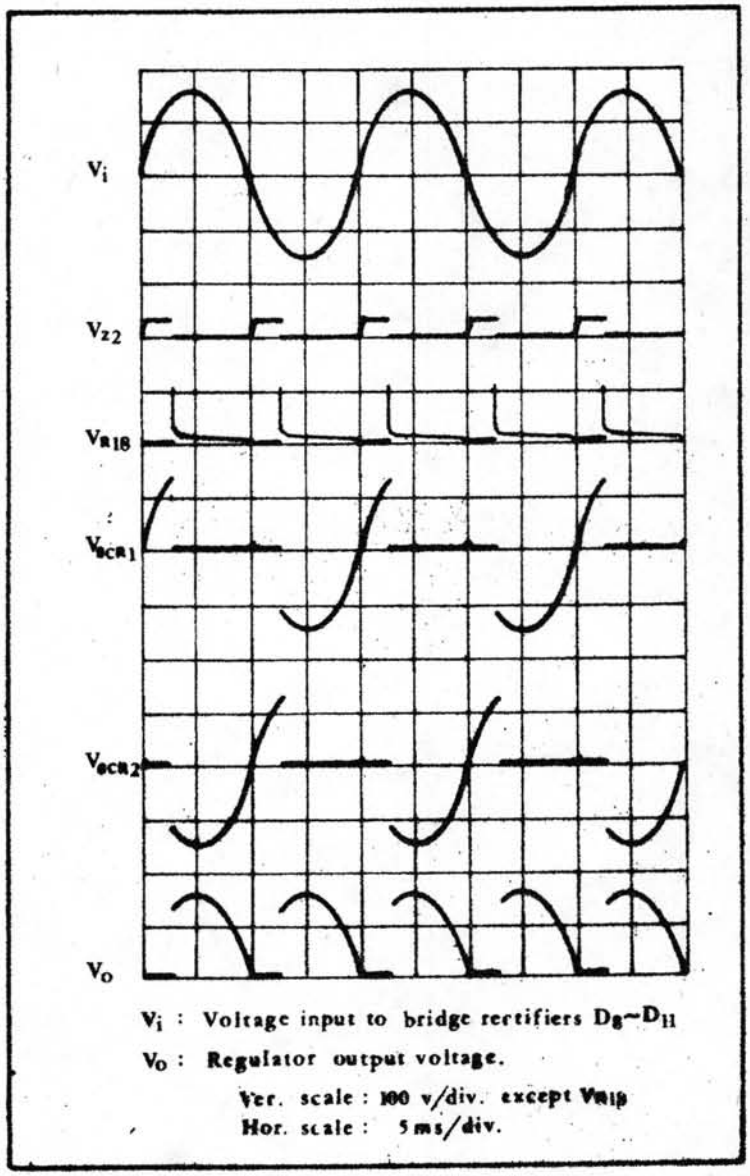

Figure 4.5 : Voltage Waveforms at Maximum Specified Regulator Output Voltage.