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ภาคผนวก

ภาคผนวก ก

รายการอุปกรณ์ที่ใช้ออกแบบแหล่งจ่ายศักดาไฟฟ้าสูงและแหล่งจ่ายศักดาไฟฟ้าต่ำจุดไส้หลอด

IC1 LM 3525 A 1 ตัว	C12 0.01 μF 35 V 1 ตัว
IC2 TL 081 1 ตัว	C15,C16,C21,C22, 3300 μF 4 ตัว 100 V
IC3 LM 350 1 ตัว	
IC4 MC 7812 1 ตัว	R1 11 k Ω 1/2 W 1 ตัว
IC5 MC 7815 1 ตัว	R2,R21 10 k Ω 2 ตัว
IC6 MC 7915 1 ตัว	R23 100 kΩ 1 ตัว
ZD1 1N 4148 1 ตัว	R24 1 kΩ 1 ตัว
ZD2 1N 4742 1 ตัว	R4,R5, 100 kΩ 1/2 W 2 ตัว
SCR MCR 106 1 ตัว	R8,R9,R10,R11 75 MΩ 1/2 W 4 ตัว
D1,D2 MBR 1035 2 ตัว	R12,R13, 0.2 Ω 5 W 2 ตัว
D3,D4 GD 3000 28 ตัว	R14,R15 120 kΩ 1/2 W 2 ตัว
C1 10 μF 35 V 1 ตัว	R16 60 kΩ 1/2 W 1 ตัว
C2,C14 0.1 μF 35 V 2 ตัว	R17,R18 1 MΩ 1/2 W 2 ตัว
C3,C4 0.18 μF 50 V 2 ตัว	R19 40 kΩ 1/2 W 1 ตัว
C5,C6,C7,C8 0.01 μF 10 kV 4 ตัว	R20 300 Ω 1/2 W 1 ตัว
C9,C10 0.22 μF 50 V 2 ตัว	R22,R23 4.7 Ω 1 W 2 ตัว
C11,C17,C18,C19,C20 1000 μF 6 ตัว 35 V	R25 120 Ω 1/2 W 1 ตัว

ภาคผนวก ข

รายละเอียดข้อมูลของหัวกำเนิดรังสีที่เกี่ยวข้องกับการออกแบบ

Philips ORALX 65S

TECHNICAL DATA

Mains: 220,240 V, 5 A (momentary load) 50/60 Hz or 100, 120 V, 7,5 A (momentary load) 50/60 Hz.
Max. mains deviation: ± 10%.
Mains resistance: 0,5 Ohm nominal.

Tube: 65 kV ± 5%, 7,5 mA ± 10% at normal mains conditions.

Permissible current: 360 mAs/h.

Switching time/cooling ratio: 1:75.

Inherent filtration: 2 mm. Al. eq.

Cone radiated field at tip of cone: 6 cm ø.

Focus to skin distance: 8 in. or 20 cm.

Focus: 0,7 nom. according to IEC 336.

Leakage radiation: Less than 5 mR/h (0,044 mGy/h) at 1 m. distance from focus.

CLEANING AND DISINFECTION

The procedure listed below should be followed carefully in order to ensure safe and efficient operation.

Cleaning

Always disconnect the equipment from the mains supply before cleaning.
Do not allow water or other liquids to enter the equipment, as they may cause circuits and corrosion.
Enamelled parts must only be cleaned by wiping with a damp cloth and mild detergent, followed by rubbing down with a dry woollen cloth.
Do not use abrasive polishes.
Wax car polish is recommended for preservation of the finish.

Disinfection

Always disconnect the equipment from the mains supply before disinfection.
The energized equipment, accessories and connecting cables can be disinfected by wiping with a cloth dampened with a disinfectant solution.
Do not use solvent or corrosive disinfectants.
The equipment must not be exposed to gaseous disinfectants.
Spray disinfectants are not recommended, as the disinfectant may enter the equipment causing short circuits or corrosion.

If sprays are unavoidable the following precautious shall be taken:

- If the room in which the equipment is installed is to be disinfected by means of an atomizer: the equipment should be carefully covered with plastic sheet.
- The equipment should be switched off and allowed to cool down well in advance in order to prevent convection currents drawing the disinfectant mist into the equipment.
- After dispersal of disinfectant mist the plastic sheeting can be removed. and the equipment can be disinfected by wiping.
- The equipment may not be used in the presence of disinfectants which vaporize to form explosive mixtures, and the vapour must be allowed to diperse before the equipment is returned to use.

The method of disinfection used should comply with current regulations and recommendations. including those concerning the prevention of explosion hazards.

ภาคผนวก ค

รายละเอียดข้อมูลเทคนิคของหัววัดรังสี

Photon Detectors

HPGe LEPS (Low Energy Photon Spectrometers) GLP Series

The EG&G ORTEC GLP Series Low Energy Photon Spectrometer (LEPS) is a planar high-purity germanium photon detector for use in applications over the approximate energy range of 3 keV to 1 MeV. Because of our advanced crystal-growing technology we are able to produce our own high-purity germanium crystals to use in the manufacture of these detectors. This capability, coupled with our exclusive ion-implanted front contact, results in the most rugged and reliable detector of this type available.

The ion-implanted front contact eliminates the x-ray spectral interference that is inherent with a less reliable metal contact. The interference from characteristic x rays that is generated when the radiation to be measured passes through a heavy metal contact is not generated with the implanted contact. This means a cleaner spectrum over the entire useful energy range of the detector. The contact is much more rugged since it is actually buried in, not evaporated on, the face of the detector. Also, the resulting dead layer is as thin as, or thinner than, a metallic front contact.

The use of high-purity germanium and state-of-the-art cryostat designs allows these systems to be cycled repeatedly to room temperature without performance degradation.

GLP detectors may be repeatedly temperature cycled and stored warm for extended periods. The systems are shipped without liquid nitrogen, eliminating the problems and expenses associated with handling similar detector systems in the past.

The EG&G ORTEC GLP Series HPGe LEPS provides excellent energy resolution performance due to an exclusive high gain, low-noise, hybridized preamplifier, located inside the streamline cryostat package. With the standard feedback resistor normally supplied, the GLP Series preamplifier is capable of impressive energy rate performance (Fig. 1). By selection of an optional feedback resistor, the GLP Series detectors can be modified to provide state-of-the-art resolution performance at higher counting rates.

Figure 1 shows the energy resolution and peak shift vs count rate performance of a 16-mm diameter, 200-mm² area, 10-mm deep GLP Series detector supplied with the standard feedback resistor. Note the excellent resolution at low and medium counting rates.

- **Ion-implanted front contact eliminates x-ray spectral interference**
- **Exclusive streamline cryostat configuration with hybridized preamplifier**
- **EG&G ORTEC's own high-purity germanium crystals**
- **Automatic high-voltage shutdown protects FET**
- **Unparalleled reliability**
- **Fully cyclable to room temperature**
- **Portable systems available**
- **High-rate indicator**
- **Spectroscopy from 3 keV to 1 MeV**
- **Room temperature shipment**

Figure 2 shows the same data, obtained with the same detector, modified with the optional feedback resistor selected for higher counting rates. Note that there is a trade-off in energy resolution to achieve higher counting rates, yet good spectroscopy is possible at count rates in excess of 500,000 cps. If your application involves higher counting rates, ensure that these rates are specified at order placement.

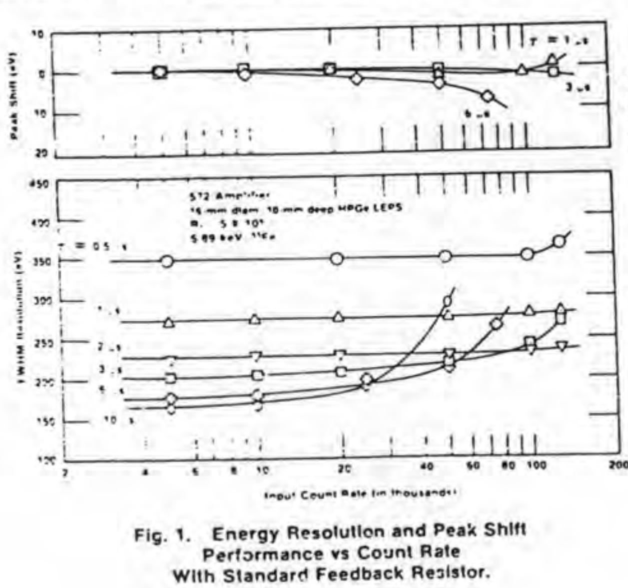


Fig. 1. Energy Resolution and Peak Shift Performance vs Count Rate With Standard Feedback Resistor.

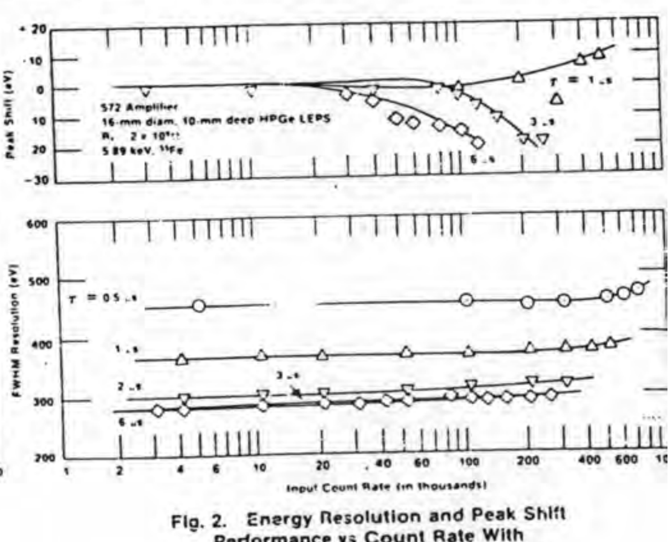
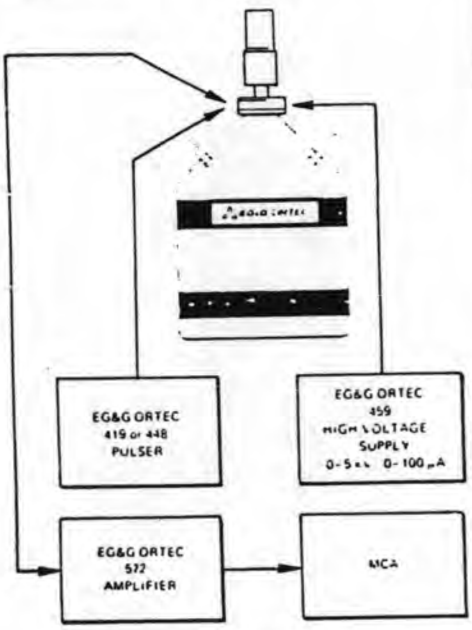


Fig. 2. Energy Resolution and Peak Shift Performance vs Count Rate With Optional Selected Feedback Resistor for Higher Count Rates.

GLP Series (Continued)

The GLP Series detectors have an exclusive high-rate indicator and high-voltage shutdown protection feature. If the LN_2 supply is exhausted and the detector begins to warm while high-voltage bias is applied (when using EG&G ORTEC Model 459 Bias Supply), the high voltage will automatically shut off, thus protecting the FET from damage. (An interface box is available on request to provide this feature when using a bias supply other than the EG&G ORTEC 459).



Typical GLP
LEPS Detector Spectroscopy System.

GLP Series HPGe LEPS Detector Performance Matrix

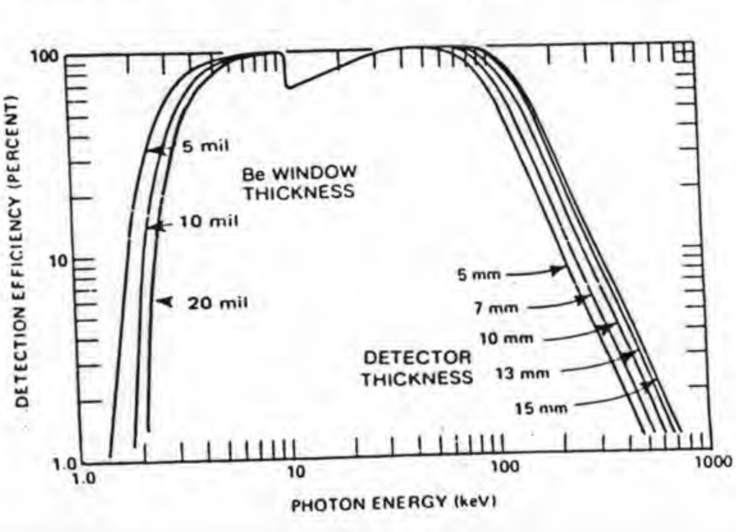
Unless otherwise specified each HPGe LEPS is supplied with streamline vertical configuration (CFG-SV), 30-liter dewar (DWR-30), and 5-, 10-, or 20-mil Be window as noted. See later pages for other standard configurations. Entries in boldface are recommended best value in price/performance.

	Detector Dimensions			Resolution (FWHM)	
Model No.	Diameter (mm)	Area (mm^2)	Depth* (mm)	at 5.9 keV (eV)	at 122 keV (eV)
GLP-06165/05	**≥6†**	**≥28**	**≥5**	**≤165**	**≤480**
GLP-10210/05	10†	80	5	210	495
GLP-10180/07	**10†**	**80**	**7**	**180**	**485**
GLP-16270/05	16†	200	5	270	520
GLP-16230/07	16†	200	7	230	515
GLP-16195/10	**16†**	**200**	**10**	**195**	**495**
GLP-25385/05	25‡	500	5	385	600
GLP-25355/07	25‡	500	7	355	585
GLP-25325/10	**25‡**	**500**	**10**	**325**	**550**
GLP-25300/13	**25‡**	**500**	**13**	**300**	**545**
GLP-32490/05	32‡	800	5	490	660
GLP-32440/07	32‡	800	7	440	630
GLP-32355/10	**32‡**	**800**	**10**	**355**	**580**
GLP-32340/13	**32‡**	**800**	**13**	**340**	**570**
GLP-36490/05	36‡	1000	5	490	660
GLP-36440/07	36‡	1000	7	440	630
GLP-36385/10	**36‡**	**1000**	**10**	**385**	**595**
GLP-36360/13	**36‡**	**1000**	**13**	**360**	**585**
Special Order	44§	1500	5	Special Order	
Special Order	44§	1500	7	Special Order	
GLP-44560/10	44§	1500	10	560	730
GLP-44525/13	44§	1500	13	525	710
GLP-44510/15	44§	1500	15	510	700
Special Order	51§	2000	5	Special Order	
Special Order	51§	2000	7	Special Order	
GLP-51615/10	51§	2000	10	615	770
GLP-51565/13	51§	2000	13	565	740
GLP-51545/15	51§	2000	15	545	725

*Depletion depths are minimums. If a specific maximu depth is required, please specify.
†Supplied with 5-mil Be window.
‡Supplied with 10-mil Be window.
§Supplied with 20-mil Be window.
‖Resolution performance specifications shown are a plicable to standard feedback resistor systems. N discussion regarding resolution performance trade for high-count rates when selected optional feedb resistor is specified.

IMPORTANT NOTES

1. **Entries in boldface type are best value in price/performance.**
2. **Depletion depths are minimums. If a specific maximum depth is required, please specify.**



Efficiency vs Energy Curve as a Function of Be Window Thickness and Detector Thickness.

ภาคผนวก ง

รายละเอียดของข้อมูลไอซีที่ใช้กำเนิดความถี่

National Semiconductor

LM1525A/LM3525A/LM1527A/LM3527A Pulse Width Modulator

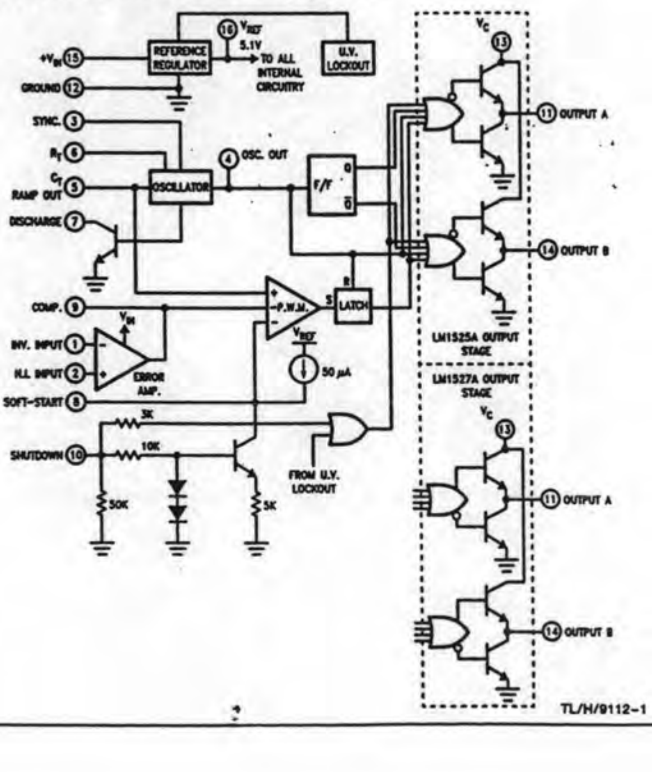
General Description

The LM1525A/1527A series of pulse-width-modulator integrated circuits are designed to offer improved performance and lowered external parts count when used to implement all types of switching power supplies. The on-chip +5.1V reference is trimmed to ±1% initial accuracy, and the input common mode range of the error amplifier includes the reference voltage, eliminating external potentiometers and dividers. A Sync input to the oscillator permits multiple devices to be slaved together, or a single device to be synchronized to an external system clock. A single resistor between the C_T pin and the Discharge pin provides a wide range of deadtime adjustment. These devices also feature built-in soft-start circuitry with only a timing capacitor required externally. A Shutdown pin controls both the soft-start circuitry and the output stages, providing instantaneous turn-off with soft-start recycle for slow turn-on. These functions are also controlled by an undervoltage lockout which keeps the outputs off and the soft-start capacitor discharged for input voltages less than that required for normal operation. The undervoltage lockout circuitry features approximately 200 mV of hysteresis to prevent threshold oscillations. Another unique feature of these improved PWM integrated circuits is the latch following the comparator (thus preventing double-pulsing). Once a PWM pulse has been terminated for any reason, the outputs will remain OFF for the duration of that period. The latch is reset with each clock pulse. The output stages are totem-pole designs capable of sourcing or sinking more than 200 mA. The LM1525A output stage features NOR logic, resulting in LOW outputs for an OFF stage. The LM1527A uses OR logic which results in HIGH outputs when OFF.

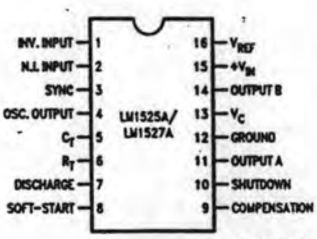
Features

- 8 to 35V operation
- 5.1V reference trimmed to ±1%
- 100 Hz to 500 kHz oscillator range
- Separate oscillator sync terminal
- Adjustable deadtime control
- Internal soft-start
- Input undervoltage lockout with hysteresis
- Latching P.W.M. to prevent multiple pulses
- Dual source/sink output drivers

Block & Connection Diagrams



TL/H/9112-1



TL/H/9112-2

Top View

Order Number LM1525AJ, LM3525AJ, LM1527AJ, LM3527AJ, LM3525AN or LM3527AN
See NS Package Number J16A or N16A

Absolute Maximum Ratings (Note 7)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Input Voltage (Pins 13, and 15)	−0.3V to +40V
Reference Output Current (Pin 16)	50 mA DC
Reference Output Short Circuit	5 Seconds
Output Current (Pins 11, 14)	±200 mA
Oscillator Current (Pins 5, 6, 7) (Note 8)	5 mA DC
Op Amp Inputs: V_{CM}	−0.3V to $+V_{in}$
(Pins 1, 2) V_{DIFF}	±6V
Logic Inputs	−0.3V to +5.5V
Storage Temperature	−65°C to +150°C
Operating Temperature Range ($T_{min} \le T_j \le T_{max}$)	
LM1525A, LM1527A	−55°C to +150°C
LM3525A, LM3527A	0°C to +150°C
Lead Temperature (Soldering, 4 Seconds)	
J Package	+300°C
N Package	+260°C
Power Dissipation (Note 9)	1 Watt
ESD Tolerance	
Czap = 100 pF, Rzap = 1.5k	2000V

Electrical Characteristics

V_{in} = 20 V_{dc}, **Boldface** limits apply from T_{MIN} to T_{MAX} (Note 1), all other limits T_j = 25°C unless otherwise noted

Parameter	Conditions	LM1525A LM1527A			LM3525A LM3527A			Units
		Typical	Tested Limit (Note 2)	Design Limit (Note 3)	Typical	Tested Limit (Note 2)	Design Limit (Note 3)	
REFERENCE SECTION								
Reference Voltage Output	T_j = 25°C	5.10	5.05 5.15		5.10	5.00 5.20		V_{min} V_{max}
Line Regulation	+8.0V ≤ V_{in} ≤ + 35V	10	**20**		10	15	**20**	mV_{max}
Load Regulation	0 mA ≤ I_L ≤ 20 mA	20	**50**		20	20	**50**	mV_{max}
Temperature Stability		20		**50**	20		**50**	mV_{max}
Reference Voltage Output	+8.0V ≤ V_{in} ≤ +35V 0 mA ≤ I_L ≤ 20 mA And Over Operating Temp.	5.08	**5.20** **5.00**		5.08		**5.25** **4.95**	V_{max} V_{min}
Short Circuit Current	T_j = 25°C V_{ref} = 0V	70	100		70	100		mA_{max}
Output Noise Voltage	10 Hz ≤ f ≤ 10 kHz T_j = 25°C	40		200	40		200	μV_{rms} max
Long Term Stability	T_j = 125°C	20		50	20		50	mV/KHour
OSCILLATOR SECTION (Note 4) Unless otherwise specified								
Initial Accuracy	T_j = 25°C	±2	±6		±2	±6		%
Accuracy of Freq. vs. Temp.		±3	**±8**		±3		**±10**	%
Voltage Stability	8.0V ≤ V_{in} ≤ 35V	±0.3	**±1**		±0.3	±2	**±2**	%
Temperature Stability	$\Delta F_{osc}/F_{osc}$	±3		**±6**	±3		**±6**	%
Minimum Frequency	R_T = 300 kΩ, C_T = 0.1 μF, R_D = 0 (Note 5)	70	**100**		70	90	**100**	Hz max
Maximum Frequency	R_T = 2.0 kΩ, C_T = 1 nF, R_D = 0	450	**400**		450	430	**400**	kHz min
Current Mirror $I_{pin\ 5}$	I_{RT} = 2.0 mA	2.0	**1.7** **2.2**		2.0	1.8 2.1	**1.7** **2.2**	mA_{min} mA_{max}
Clock Amplitude	At pin 4	3.5		**3.0**	3.5		**3.0**	V_{min}
Clock Width	T_j = 25°C	0.5		1.0 0.3	0.5		1.0 0.3	μs max μs min
Sync Threshold	(Note 6)	1.8	**1.2** **2.8**		1.8	1.25 2.8	**1.2** **2.8**	V min V max
Sync Input Current	Sync Voltage = 3.5V	1.0	**2.5**		1.0	2.30	**2.5**	mA_{max}

Electrical Characteristics

V_{in} = 20 V_{dc}, **Boldface** limits apply from T_{MIN} to T_{MAX} (Note 1), all other limits T_j = 25°C unless otherwise noted (Continued)

Parameter	Conditions	LM1525A LM1527A			LM3525A LM3527A			Units
		Typical	Tested Limit (Note 2)	Design Limit (Note 3)	Typical	Tested Limit (Note 2)	Design Limit (Note 3)	
ERROR AMPLIFIER SECTION V_{CM} = 5.1V, Unless otherwise noted								
Input Offset Voltage		0.5	**5**		2	7	**10**	mV_{max}
Input Bias Current		1	**10**		1	2	**10**	μA_{max}
Input Offset Current		0.1	**1**		0.1	0.8	**1**	μA_{max}
DC Open Loop Gain	$R_L \geq 10$ MΩ	80	**66**		80	66	**60**	dB min
Gain Bandwidth Product	$A_V = 0$, T_j = 25°C $C_L \leq 30$ pF	2		1	2		1	MHz_{min}
Output Low Level		0.2	**0.5**		0.2	0.4	**0.5**	V_{max}
Output High Level		5.6	**3.8**		5.6	4.1	**3.8**	V_{min}
Common Mode Rejection	V_{CM} = 1.5V to 5.2V	80	**66**		80	70	**66**	dB min
Supply Voltage Rejection	V_{IN} = 8V to 35V	90	**60**		90	64	**60**	dB min
P.W.M. COMPARATOR								
Minimum Duty Cycle			**0**			0	**0**	% max
Maximum Duty Cycle		49	**45**		49	46	**45**	% min
Input Threshold	Zero Duty Cycle	0.9	**0.6**		0.9	0.70	**0.6**	V_{min}
Input Threshold	Max. Duty Cycle	3.3	**3.6**		3.3	3.6	**3.6**	V_{max}
Input Bias Current		0.05		**1.0**	0.05		**1.0**	μA_{max}
SOFT-START SECTION								
Soft Start Current	$V_{SHUTDOWN}$ = 0V	50	**80** **25**		50	74 36	**80** **25**	μA_{max} μA_{min}
Soft Start Voltage	$V_{SHUTDOWN}$ = 2.0V	0.35	**0.6**		0.35	0.5	**0.6**	V_{max}
Shutdown Input Current	$V_{SHUTDOWN}$ = 2.5V	0.4	**1.0**		0.4	0.85	**1.0**	mA_{max}
OUTPUT DRIVERS (Each Output) V_C = 20V, Unless otherwise noted								
Undervoltage Lockout Hysteresis		0.2			0.2			V
Output Low Level	I_{SINK} = 20 mA	0.2	**0.4**		0.2	0.35	**0.4**	V_{max}
	I_{SINK} = 100 mA	1.0	**2.0**		1.0	1.9	**2.0**	V_{max}
Output High Level	I_{SOURCE} = 20 mA	19	**18**		19	18.2	**18**	V_{min}
	I_{SOURCE} = 100 mA	18	**17**		18	17.4	**17**	V_{min}
Undervoltage Lockout	V_{COMP} and V_{SS} = High	7	**8** **6**		7	7.7 6.3	**8** **6**	V_{max} V_{min}
Collector Leakage	LM1525A and LM3525A Only V_C = 35V		**200**			120	**200**	μA_{max}
Rise Time	C_L = 1 nf, T_j = 25°C	100		600	100		600	ns max
Fall Time	C_L = 1 nf, T_j = 25°C	50		300	50		300	ns max

Electrical Characteristics

V_{in} = 20 V_{dc}, **Boldface** limits apply from T_{MIN} to T_{MAX} (Note 1), all other limits T_j = 25°C unless otherwise noted (Continued)

Parameter	Conditions	LM1525A LM1527A			LM3525A LM3527A			Units
		Typical	Tested Limit (Note 2)	Design Limit (Note 3)	Typical	Tested Limit (Note 2)	Design Limit (Note 3)	
Shutdown Delay	V_{SD} = 3V, C_L = 0, T_j = 25°C	200		500	200		500	ns max
TOTAL STANDBY CURRENT								
Supply Current	V_{IN} = 35V	13	**18**		13	14.5	**20**	mA

Note 1: Unless otherwise noted these specifications apply: −55°C < T_j < +125°C for LM1525A and LM1527A, 0°C < T_j < +125°C for LM3525A and LM3527A.

Note 2: Tested limits are guaranteed and 100% tested in production.

Note 3: Design limits are guaranteed (but not 100% production tested) over the indicated temperature and supply ranges.

Note 4: Tested at F_{osc} = 40 kHz (Rt = 3.6k, Ct = 0.01 μF, Rd = 0).

Note 5: These specifications are also guaranteed with Rt = 150k, Ct = 0.2 μF, Rd = 0.

Note 6: Tested with a pulse of width 500 ns and amplitudes of 1.2 and 2.8V at 50 kHz.

Note 7: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions. See Note 1 and conditions.

Note 8: Do not ground pin 6.

Note 9: For operation at elevated temperatures, devices in the J package must be derated based on thermal resistance of 90°C/W (junction to ambient), or 65°C/W in the N package.

SHUTDOWN OPTIONS (See Block Diagram)

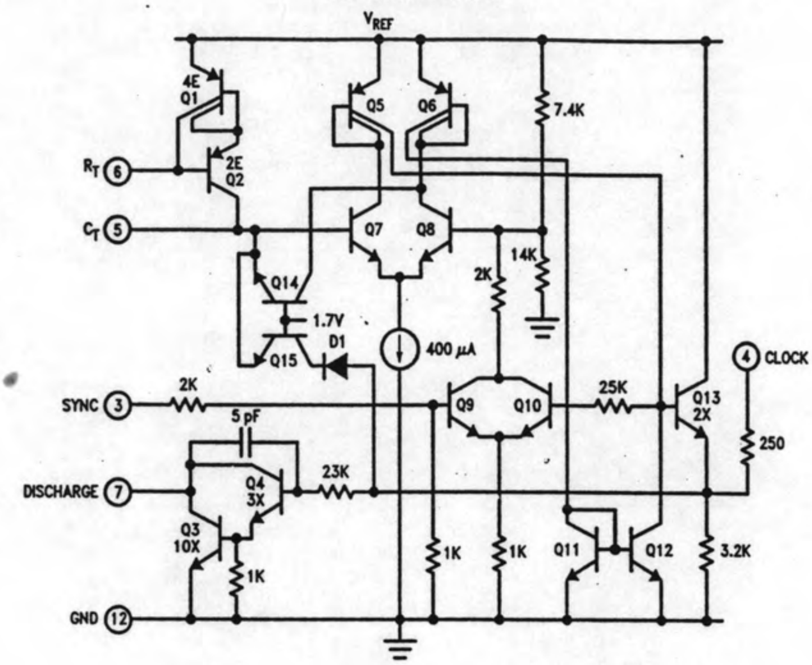
1. Since both the compensation and soft-start terminals (pins 9 and 8) have current source pull-ups, either can readily accept a pull-down signal which only has to sink a maximum of 100 μA to turn off the outputs. This is subject to the added requirement of discharging whatever external capacitance may be attached to these pins.
2. An alternative approach is the use of the shutdown circuitry of pin 10. Activating this circuit by applying a positive-going pulse at pin 10 will result in the output of the comparator going high, and thus turning off the outputs. The pulse will start the fast discharge of the soft-start capacitor. If the shutdown command is short, the PWM signal is terminated without significant discharge of the soft-start capacitor, thus allowing, for example, a convenient implementation of pulse-by-pulse current limiting. Holding pin 10 high for a long time will ultimately discharge the soft-start capacitor, thus recycling slow turn on upon release. This method of shutdown is the fastest shutdown possible.

SYNCHRONIZATION PROCEDURE

The device may be synchronized to an external clock; however the following points have to be observed: a) The frequency of the free-running oscillator of the device must be set at least 10% less than the frequency of the external clock. b) The external clock pulse must be at least 300 ns wide but must not exceed the free-running pulse width (pin 4) by more than 200 ns. c) The amplitude of the external pulse must be between 2 and 5V.

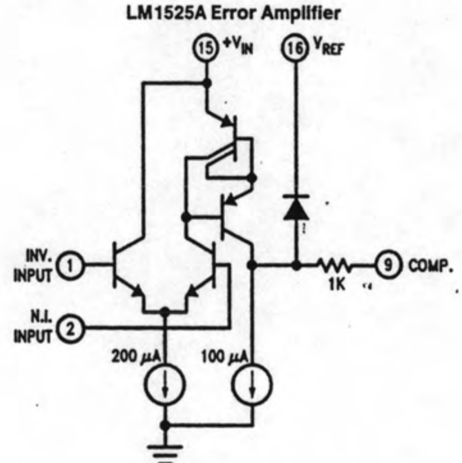
Multiple devices may be synchronized together by connecting all pin 4's together and all pin 5's together; pins 6 and 7 of slave oscillator must be left open.

LM1525A Oscillator



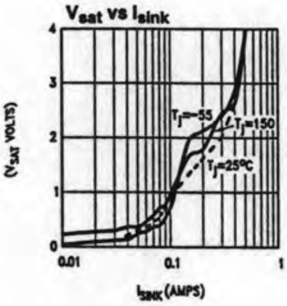
TL/H/9112-5

LM1525A Error Amplifier

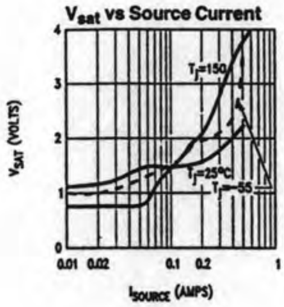


TL/H/9112-4

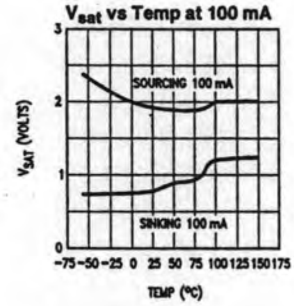
V_{sat} vs I_{sink}



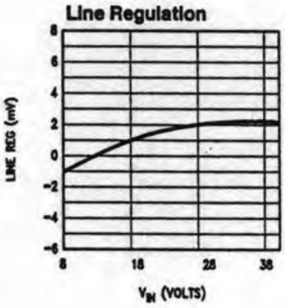
V_{sat} vs Source Current



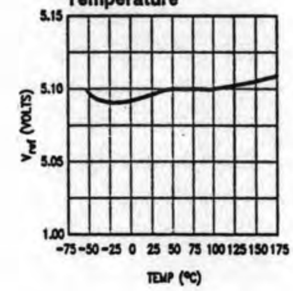
V_{sat} vs Temp at 100 mA



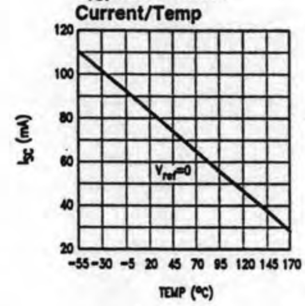
Line Regulation



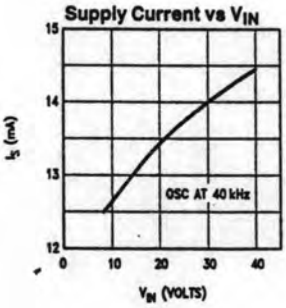
Typical V_{ref} vs Temperature



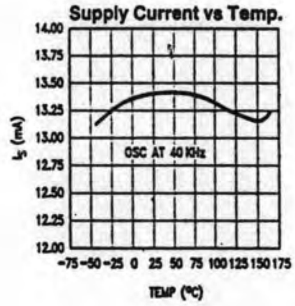
V_{ref} Short-Circuit Current/Temp



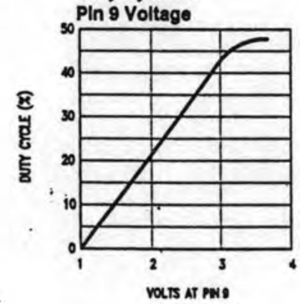
Supply Current vs V_{IN}



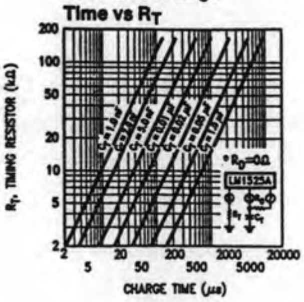
Supply Current vs Temp.



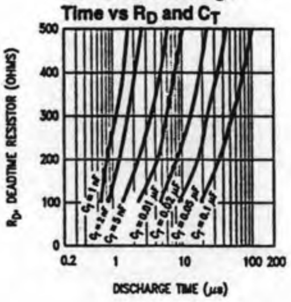
Duty Cycle vs Pin 9 Voltage



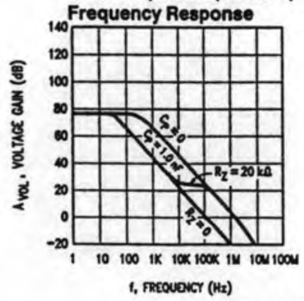
Oscillator Charge Time vs R_T



Oscillator Discharge Time vs R_D and C_T

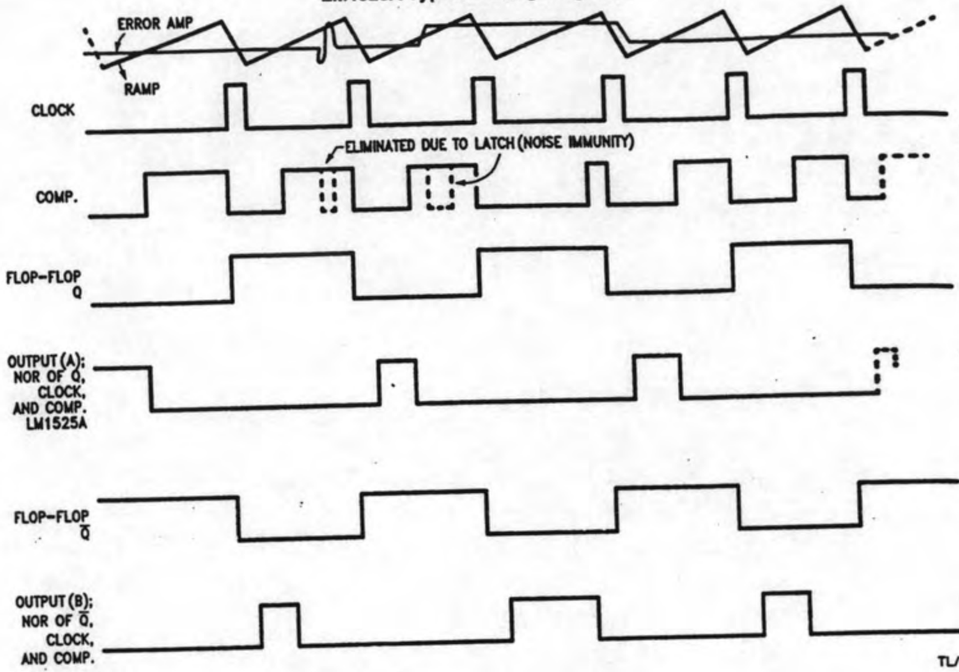


Error Amplifier Open-Loop Frequency Response



TL/H/9112–14

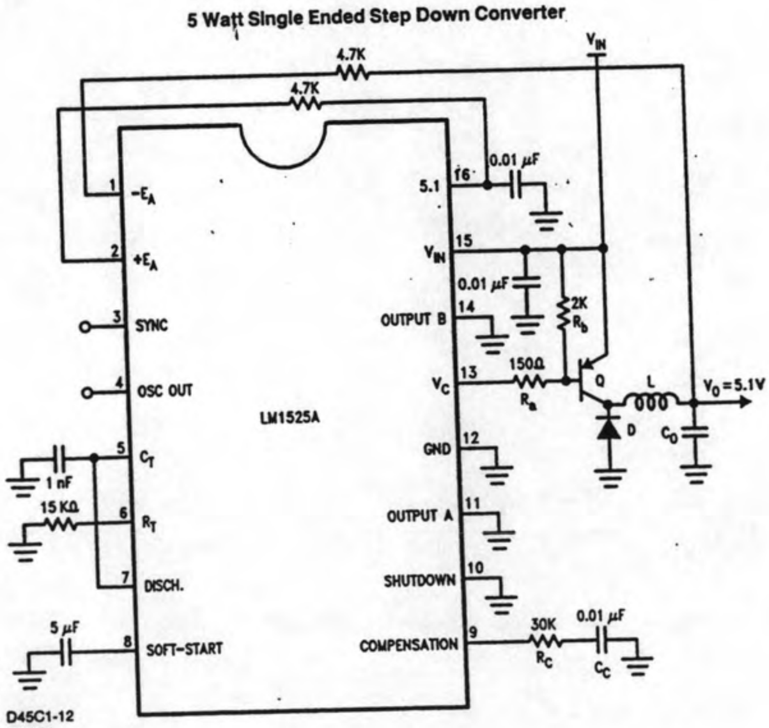
LM1525A Typical Timing Diagram



TL/H/9112-7

Typical Applications

5 Watt Single Ended Step Down Converter

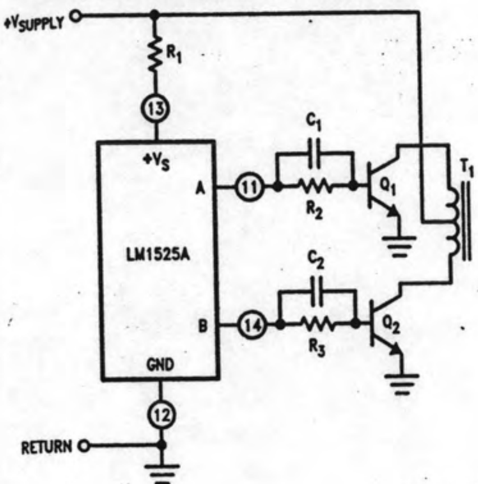


TL/H/9112-8

V_{IN} = 28V Q = D45C1-12
V_{OUT} = 5.1V D = IN5821
L = 150 µH
C_O = 500 µF

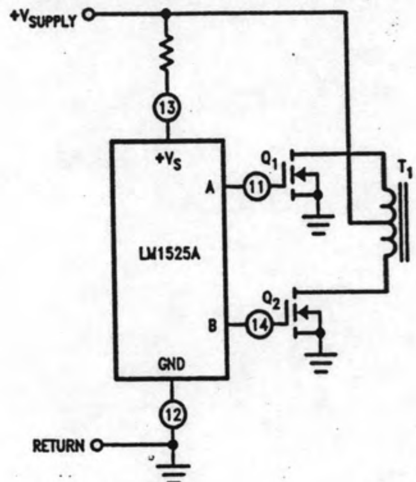
Typical Applications (Continued)

Bipolar Drive for Push-Pull Converters



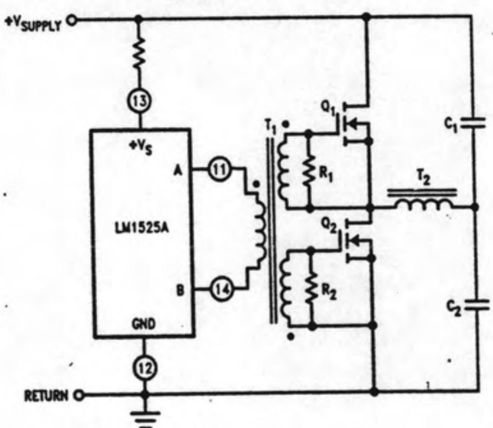
TL/H/9112-9

3 MOSFET Drive for Push-Pull Converters



TL/H/9112-10

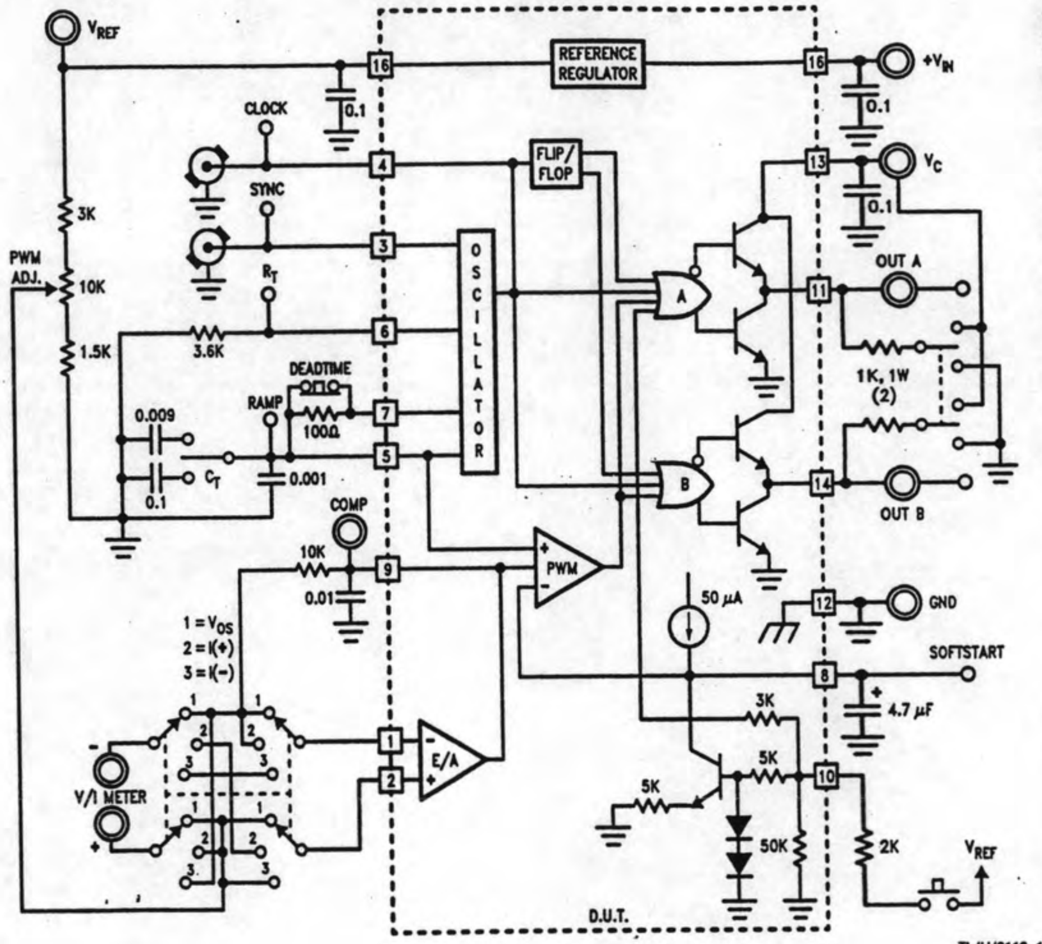
Direct Drive for Transformer



TL/H/9112-11

Typical Applications (Continued)

LM1525A/1527A Lab Test Fixture



TL/H/9112-12

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

IRF150
IRF151
IRF152

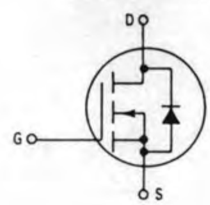
Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS

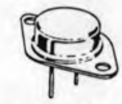
These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds
- Low $r_{DS(on)}$ to Minimize On-Losses. Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

TMOS™



TMOS POWER FETs
33 and 40 AMPERES
$r_{DS(on)}$ = 0.055 OHM
60 and 100 VOLTS
$r_{DS(on)}$ = 0.08 OHMS
100 VOLTS



CASE 197A-02
TO-204AE

MAXIMUM RATINGS

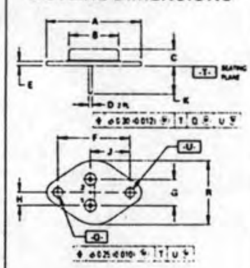
Rating	Symbol	IRF 150	IRF 151	IRF 152	Unit
Drain-Source Voltage	V_{DSS}	100	60	100	Vdc
Drain-Gate Voltage (R_{GS} = 20 kΩ)	V_{DGR}	100	60	100	Vdc
Gate-Source Voltage	V_{GS}	±20			Vdc
Drain Current Continuous, T_C = 25°C T_C = 100°C Peak, T_C = 25°C	I_D	 40 25 160		 33 20 132	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	150 1.2			Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to 150			°C

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	0.83 30	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from Case for 5 Seconds	T_L	300	°C

See the MTM55N08 Designer's Data Sheet for a complete set of design curves for the product on this data sheet. Design curves of the MTM55N10 are applicable for this series of product.

OUTLINE DIMENSIONS



STYLE 3:
PIN 1. GATE
2. SOURCE
CASE. DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	38.36	39.37	1.510	1.550
B	19.31	21.08	0.760	0.830
C	6.35	8.25	0.250	0.325
D	1.45	1.60	0.057	0.063
E	1.53	1.77	0.060	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.84	4.19	0.151	0.165
R	25.15	26.67	0.990	1.050
U	3.84	4.19	0.151	0.165

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)	IRF150, IRF152 IRF151	$V_{(BR)DSS}$	100 60	— —	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)		I_{DSS}	— —	0.2 1	mAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 0.25 mA)		$V_{GS(th)}$	2	4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 20 Adc)	IRF150, IRF151 IRF152	$r_{DS(on)}$	— —	0.055 0.080	Ohm
On-State Drain Current (V_{GS} = 10 V) (V_{DS} ≥ 2.2 Vdc) (V_{DS} ≥ 2.6 Vdc)	IRF150, IRF151 IRF152	$I_{D(on)}$	40 33	— —	Adc
Forward Transconductance (V_{DS} ≥ 2.2 V, I_D = 20 A) (V_{DS} ≥ 2.6 V, I_D = 20 A)	IRF150, IRF151 IRF152	g_{FS}	9 9	— —	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz)	C_{iss}	—	3000	pF
Output Capacitance		C_{oss}	—	1500	
Reverse Transfer Capacitance		C_{rss}	—	500	
SWITCHING CHARACTERISTICS*					
Turn-On Delay Time	(V_{DD} ≈ 24 V, I_D = 20 Apk, R_{gen} = 4.7 Ohms)	$t_{d(on)}$	—	35	ns
Rise Time		t_r	—	100	
Turn-Off Delay Time		$t_{d(off)}$	—	125	
Fall Time		t_f	—	100	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 10 Vdc, I_D = Rated I_D)	Q_g	60 (Typ)	120	nC
Gate-Source Charge		Q_{gs}	25 (Typ)	—	
Gate-Drain Charge		Q_{gd}	35 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = Rated I_D, V_{GS} = 0)	V_{SD}	1.5 (Typ)	2.3(1)	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	450 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE					
Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die)		L_d	5 (Typ)	—	nH
Internal Source Inductance (Measured from the source pin, 0.25" from the package to the source bond pad)		L_s	12.5 (Typ)	—	nH

*Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2%.
(1) Add 0.2 V for IRF150 and IRF151.

ประวัติผู้เขียน

นางสาวสาหร่าย เล็กชะอุ่ม เกิดวันที่ 31 ตุลาคม พ.ศ. 2510 ที่อำเภอเมืองฉะเชิงเทรา จังหวัดฉะเชิงเทรา สำเร็จการศึกษาปริญญาวิทยาศาสตรบัณฑิต สาขาฟิสิกส์ ภาควิชาฟิสิกส์ คณะวิทยาศาสตร์ มหาวิทยาลัยบูรพา ในปีการศึกษา 2533 และเข้าศึกษาต่อในหลักสูตรวิศวกรรมศาสตรมหาบัณฑิต สาขานิวเคลียร์เทคโนโลยี คณะวิศวกรรมศาสตร์ จุฬาลงกรณ์มหาวิทยาลัย เมื่อ พ.ศ.2535