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ภาคผนวก

ภาคผนวก ก.

```
                                    'PROGRAM MCA via USB
 Option Explicit
Dim adcip As Integer
Dim chnel(4095) As Long      'long max 2,147,438,647  approx 6day on
Dim serialmon  As Long       'input count from serial port for monitor
Dim integral As Long
Dim dispint As Long
Dim reset1 As Integer        'for rest all chnel(adcip) to 0

 '"for serial input
Dim vin As String            'for value input of serial
Dim stemp1 As String         'stemp 1,2,3 for temporary string exchange
Dim stemp2 As String
Dim stemp3 As String

 '"for timer

Dim timeset As Integer       ' input sting value for time count down in text6
Dim timebox As String
Dim compare1 As Integer      ' compare for countdown control
Dim comsel As Integer
Dim spare  As Integer        '0 to 4095 for disp work
Dim spare2 As Integer
Dim spare3 As Integer
Dim spare4 As Integer
Dim disp(4095) As Long       'move chnel(adcip) to disp
Dim ymax As Long
Dim ydiv As Single


Private Sub Command10_Click()
      CommonDialog1.InitDir = "C:\UsbMcaLog"
   CommonDialog1.FileName = "*.*"
   CommonDialog1.Filter = "All Files(*.*) "
   'txtFile1 = CommonDialog1.File1

   CommonDialog1.ShowOpen
End Sub

Private Sub Command5_Click()
    Unload Form1
End Sub

Private Sub Command7_Click()
```

```
    For spare3 = 1 To 4095
      MSFlexGrid1.TextMatrix(spare3, 1) = disp(spare3)
      Next spare3

End Sub

Private Sub Command9_Click()
 Dim strdata As String                    'strData = txtData1.Text
 Dim strname As String

   'strname = "c:\UsbMcaLog"              'Open Path for mode as Number File
à»ç¹¡ÒÃÊÃéÒ§ä¿Åì µÒÁpath
    strname = Text10.Text
  If Dir(strname, vbDirectory) = "" Then     ' check diretory if have before no need
create
    MkDir (strname)
  End If

    strdata = Text10.Text + Text11.Text & Day(Date) & Month(Date) & Year(Date)
& Hour(Time) & Minute(Time) & Second(Time) & ".text"
    Open strdata For Append As #1
    Print #1, "THIS IS OUTPUT FILE FROM USB EMBLEDED MCA "
    Print #1, strdata; vbTab; Now
  For spare4 = 1 To 4095
     Print #1, spare4; vbTab; disp(spare4)
     Next spare4
Close #1
  MsgBox "   save file ok"

End Sub

Private Sub Timer1_Timer()        ' current time on label1
    Label1.Caption = Format(Now)
End Sub


                  """""""""start form"""""""""""

Private Sub Form_Load()

    Timer1.Enabled = True              'timer1 for display day time
    Timer1.Interval = 1000

    'Timer2.Enabled = False            'timer2 for countdown
    'Timer2.Interval = 1000            'BAD PRECISTIMER

    RSTimer3.Enabled = True              'timer3 for display
    RSTimer3.Interval = 1000

    RSTimer2.Enabled = False
    RSTimer2.Interval = 1000
```

```
        """""""""""THIS IS DEDICATE PRECISTIMER TO EASY CODER.ORG"""""
                    ' RS Timer 2.1
' This control is a high precision 32-bit (apartment threaded) timer that can be used for
 applications which require to perform certain tasks in a period of time.
'For any doubt or technical support please contact to one of the e-mail addresses
indicated
 below. Thank you.

 'elprogramari@ easycoder.org
 'asm@ easycoder.org
 'rsala@ easycoder.org
 'http://www.easycoder.org

'Copyright © 2000-2005 Ramon Sala
'This control has been developed with Microsoft Visual C/C++ 6.0
     """""""""MOST THANK  FOR OCX FILE' JATURAPUT DANGNIAM"""""


     vin = ""       ' vin as blank
     adcip = 0
     Picture1.AutoRedraw = True
     Picture1.BackColor = vbBlack
     Picture1.ForeColor = vbWhite
     Picture1.Cls

     Text1.Text = 0
     Text2.Text = 0
     Text3.Text = 0
     Text4.Text = 0
     Text5.Text = 0
     Text6.Text = 0
     Label1.Caption = 0
     DoEvents                    'Doevents for CPU can tasking another program

    """""""for cell output columm
    MSFlexGrid1.TextMatrix(0, 0) = "CHANNEL"
    MSFlexGrid1.TextMatrix(0, 1) = "COUNT"
    For spare2 = 1 To 4095
      MSFlexGrid1.TextMatrix(spare2, 0) = (spare2)
      Next spare2


End Sub

Private Sub Form_Unload(Cancel As Integer)
    ' MSComm1.PortOpen = False    ' Close the comm port
End Sub

Private Sub Command2_Click()          'Command Button to open or close the
port(toggle)
     If Option1.Value = True Then     ' If for select comport
```

```
        comsel = 3
    ElseIf Option2.Value = True Then
        comsel = 4
    ElseIf Option3.Value = True Then
        comsel = 5
    ElseIf Option4.Value = True Then
        comsel = 6
    ElseIf Option5.Value = True Then
        comsel = 7
    ElseIf Option6.Value = True Then
        comsel = 8
        End If
    If MSComm1.PortOpen = False Then          ' If for comm port is not open
      MSComm1.CommPort = comsel
      MSComm1.InBufferSize = 16384
      MSComm1.Settings = "921600,n,8,1"
      MSComm1.RThreshold = 1
      MSComm1.DTREnable = False
      MSComm1.RTSEnable = False
      MSComm1.InputLen = 1
      MSComm1.PortOpen = True          ' Open  it
      Command2.Caption = "Close Port"   'Modify the caption of the button
   Else
      MSComm1.PortOpen = False          'If the port is open then close it
      Command2.Caption = "Open Port"    'Again modify the caption.
   End If

 ' End If


End Sub

 Private Sub MSComm1_OnComm()            ' oncomm activate after command2
open port on

                 ' DoEvents
                vin = MSComm1.Input
              stemp3 = CDec(Asc(vin))           'chr32=space
                vin = ""
                  adcip = (stemp3 - 128) * 64

        '''''''''''''''''''''''''''''''''''''''''''


 ' If adcip > 0 Then
      chnel(adcip) = chnel(adcip) + 1        'major count

  '    serialmon = serialmon + 1           'integral counting system from 0 to 4095
  '    Text5.Text = serialmon             'xxserial count output at text5
      integral = integral + 1            'xxintegral count output at text7

 ' End If
```

```
  End Sub

Private Sub Text6_Change()
     Label6.Caption = Text6     'for control timer
End Sub

 Private Sub Command1_Click()      'start count

 For reset1 = 0 To 4095
          chnel(reset1) = 0          ' all adc chnel clear to zero
          ' you can add some reset comand from chnel 0-4095 here IE text1-5 cls

  Next reset1
          integral = 0               '  integral counting=0
          Picture1.Cls               '  spectram in piture1 clr
     ' Text7.Text = integral            'display 0


     ' Text1.Text = chnel(1)           'display 0
     ' Text2.Text = chnel(1234)         'xx
      'Text3.Text = chnel(2955)        'xx
     ' Text4.Text = chnel(4095)        'xx

       """""""""""next is count down timer process""""
            timebox = Text6.Text

          compare1 = IsNumeric(timebox) + 1  'compre int or not string=1 , int=0
      'Print compare1                'print compare1 for check Int or Str
  If compare1 = 1 Then
          Text6.Text = 0
            timebox = 0
  End If

        If timebox = 0 Then      ' incase of label6 shown 0 (after run 1 time)
           Label6.Caption = Text6.Text
           timebox = Label6.Caption
        End If

          timeset = timebox
           'Print timeset
        If timeset > 0 Then              '>zero next you can open
          Label3.Caption = 10
          RSTimer2.Enabled = True          ' Open  it
        End If

     """""""""""""end count down""""""""
End Sub
 Private Sub Command4_Click()             ' stop count
     RSTimer2.Enabled = False
End Sub
```

```
Private Sub Command3_Click()            'reset count function (comport still open)
    RSTimer2.Enabled = False

For reset1 = 0 To 4095
        chnel(reset1) = 0          ' all adc chnel clear to zero
        ' you can add some reset comand from chnel 0-4095 here IE text1-5 cls

Next reset1
        integral = 0               ' integral counting=0
        Picture1.Cls               ' spectram in piture1 clr
    Text7.Text = dispint
    'Picture1.PSet (((adcip * 3.3) + 200), (-chnel(adcip) + 5500)), RGB(155, 155,
155)

    Text1.Text = disp(1)           'xx  =0 for test input corection or not
    Text2.Text = disp(1234)        'xx  =0
    Text3.Text = disp(2955)        'xx  =0
    Text4.Text = disp(4095)        'xx  =0


      """""""""timer function""""""""

    timeset = 0

    Label6.Caption = 0


      """""""""end timer funtion"""""""
End Sub



Private Sub RSTimer2_Timer()

   If timeset > 0 Then
        timeset = timeset - 1
        Label6.Caption = timeset
    End If
        ydiv = (Label3.Caption / 500)
    For spare = 1 To 4095                  'REDRAW GRAPH
      disp(spare) = chnel(spare)
            If disp(spare) > disp(spare - 1) Then
               ymax = disp(spare)
            End If
            If ymax > (0.75 * (Label3.Caption)) Then
              Label3.Caption = ymax
              ydiv = (Label3.Caption) / 6400

            End If
          Next spare
```

```
For spare = 1 To 4095                    'REDRAW GRAPH
    disp(spare) = chnel(spare)
Picture1.Line (((spare * 3.41) + 1), (5799))-(((spare * 3.41) + 1), ((-disp(spare) / 0.5)
+ 5799)), RGB(155, 155, 155)
    'PICTURE1.LINE(X1,Y1)-(X2,Y2),COLOR
    '(spare * 3.41) + 1)  =X1   ADC CHANEL NUMBER
    ', (5799))            =Y1   MEAN X AXIS=0  ORIGIN
    '(spare * 3.41) + 1)  =X2   ADC CHANEL NUMBER
    '(-disp(spare) + 5799)=Y2   MEAN Y AMPLITDE(COUNT MAX)
<<SCALE CAN REDUCE HERE


Next spare

    dispint = integral                   'disp_intEGRAL for export file


''''''''''''''''''''''''''''''''''''''''

Text7.Text = integral
'Picture1.PSet
' Picture1.Line (((adcip * 3.3) + 300), (5500))-(((adcip * 3.3) + 300), (-
chnel(adcip) + 5500)), RGB(155, 155, 155)

Text1.Text = disp(1)          'xxtest input corection or not
Text2.Text = disp(1234)         'xx
Text3.Text = disp(2955)         'xx
Text4.Text = disp(4095)         'xx

''''''''''''''''''''''''''''''''''''''''

If timeset = 0 Then
    Label6.Caption = "0"           ' do not use reset1 here because it use only
command click cannot in timer module
    RSTimer2.Enabled = False          ' if you want reset some thing use new
reset2

End If

End Sub
```

ภาคผนวก ข.

ANALOG DEVICES

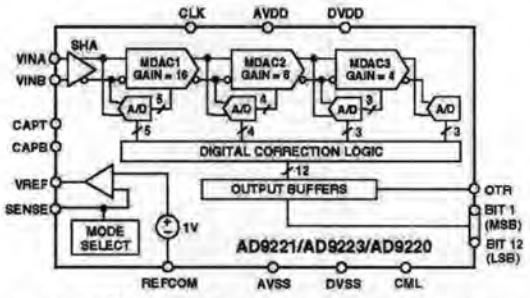
Complete 12-Bit 1.5/3.0/10.0 MSPS Monolithic A/D Converters

AD9221/AD9223/AD9220

FEATURES

Monolithic 12-Bit A/D Converter Product Family
Family Members Are: AD9221, AD9223, and AD9220
Flexible Sampling Rates: 1.5 MSPS, 3.0 MSPS, and 10.0 MSPS
Low Power Dissipation: 59 mW, 100 mW, and 250 mW
Single 5 V Supply
Integral Nonlinearity Error: 0.5 LSB
Differential Nonlinearity Error: 0.3 LSB
Input Referred Noise: 0.09 LSB
Complete On-Chip Sample-and-Hold Amplifier and Voltage Reference
Signal-to-Noise and Distortion Ratio: 70 dB
Spurious-Free Dynamic Range: 86 dB
Out-of-Range Indicator
Straight Binary Output Data
28-Lead SOIC and 28-Lead SSOP

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD9221, AD9223, and AD9220 are a generation of high performance, single supply 12-bit analog-to-digital converters. Each device exhibits true 12-bit linearity and temperature drift performance[1] as well as 11.5-bit or better ac performance.[2] The AD9221/AD9223/AD9220 share the same interface options, package, and pinout. Thus, the product family provides an upward or downward component selection path based on performance, sample rate and power. The devices differ with respect to their specified sampling rate, and power consumption, which is reflected in their dynamic performance over frequency.

The AD9221/AD9223/AD9220 combine a low cost, high speed CMOS process and a novel architecture to achieve the resolution and speed of existing hybrid and monolithic implementations at a fraction of the power consumption and cost. Each device is a complete, monolithic ADC with an on-chip, high performance, low noise sample-and-hold amplifier and programmable voltage reference. An external reference can also be chosen to suit the dc accuracy and temperature drift requirements of the application. The devices use a multistage differential pipelined architecture with digital output error correction logic to provide 12-bit accuracy at the specified data rates and to guarantee no missing codes over the full operating temperature range.

The input of the AD9221/AD9223/AD9220 is highly flexible, allowing for easy interfacing to imaging, communications, medical, and data-acquisition systems. A truly differential input structure allows for both single-ended and differential input interfaces of varying input spans. The sample-and-hold amplifier (SHA) is equally suited for both multiplexed systems that switch full-scale voltage levels in successive channels as well as sampling single-channel inputs at frequencies up to and beyond the Nyquist rate. Also, the AD9221/AD9223/AD9220 is well suited for communication systems employing Direct-IF down conversion since the SHA in the differential input mode can achieve excellent dynamic performance *far beyond* its specified Nyquist frequency.[2]

A single clock input is used to control all internal conversion cycles. The digital output data is presented in straight binary output format. An out-of-range (OTR) signal indicates an overflow condition that can be used with the most significant bit to determine low or high overflow.

PRODUCT HIGHLIGHTS

The AD9221/AD9223/AD9220 family offers a complete single-chip sampling 12-bit, analog-to-digital conversion function in pin compatible 28-lead SOIC and SSOP packages.

Flexible Sampling Rates—The AD9221, AD9223, and AD9220 offer sampling rates of 1.5 MSPS, 3.0 MSPS, and 10.0 MSPS, respectively.

Low Power and Single Supply—The AD9221, AD9223, and AD9220 consume only 59 mW, 100 mW, and 250 mW, respectively, on a single 5 V power supply.

Excellent DC Performance Over Temperature—The AD9221/AD9223/AD9220 provide 12-bit linearity and temperature drift performance.[1]

Excellent AC Performance and Low Noise—The AD9221/AD9223/AD9220 provide better than 11.3 ENOB performance and have an input referred noise of 0.09 LSB rms.[2]

Flexible Analog Input Range—The versatile on-board sample-and-hold (SHA) can be configured for either single-ended or differential inputs of varying input spans.

NOTES
[1]Excluding internal voltage reference.
[2]Depends on the analog input configuration.

REV. E

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Tel: 781/329-4700 www.analog.com
Fax: 781/326-8703

AD9221/AD9223/AD9220–SPECIFICATIONS

DC SPECIFICATIONS

(AVDD = 5 V, DVDD = 5 V, f_{SAMPLE} = Max Conversion Rate, V_{REF} = 2.5 V, VINB = 2.5 V, T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	AD9221	AD9223	AD9220	Unit
RESOLUTION	12	12	12	Bits min
MAX CONVERSION RATE	1.5	3	10	MHz min
INPUT REFERRED NOISE (TYP)				
V_{REF} = 1 V	0.23	0.23	0.23	LSB rms typ
V_{REF} = 2.5 V	0.09	0.09	0.09	LSB rms typ
ACCURACY				
Integral Nonlinearity (INL)	±0.4	±0.5	±0.5	LSB typ
	±1.25	±1.25	±1.25	LSB max
Differential Nonlinearity (DNL)	±0.3	±0.3	±0.3	LSB typ
	±0.75	±0.75	±0.75	LSB max
INL[1]	±0.6	±0.6	±0.7	LSB typ
DNL[1]	±0.3	±0.3	±0.35	LSB typ
No Missing Codes	12	12	12	Bits Guaranteed
Zero Error (@ 25°C)	±0.3	±0.3	±0.3	% FSR max
Gain Error (@ 25°C)[2]	±1.5	±1.5	±1.5	% FSR max
Gain Error (@ 25°C)[3]	±0.75	±0.75	±0.75	% FSR max
TEMPERATURE DRIFT				
Zero Error	±2	±2	±2	ppm/°C typ
Gain Error[2]	±26	±26	±26	ppm/°C typ
Gain Error[3]	±0.4	±0.4	±0.4	ppm/°C typ
POWER SUPPLY REJECTION				
AVDD, DVDD (+5 V ± 0.25 V)	±0.06	±0.06	±0.06	% FSR max
ANALOG INPUT				
Input Span (with V_{REF} = 1.0 V)	2	2	2	V p-p min
Input Span (with V_{REF} = 2.5 V)	5	5	5	V p-p max
Input (VINA or VINB) Range	0	0	0	V min
	AVDD	AVDD	AVDD	V max
Input Capacitance	16	16	16	pF typ
INTERNAL VOLTAGE REFERENCE				
Output Voltage (1 V Mode)	1	1	1	V typ
Output Voltage Tolerance (1 V Mode)	±14	±14	±14	mV max
Output Voltage (2.5 V Mode)	2.5	2.5	2.5	V typ
Output Voltage Tolerance (2.5 V Mode)	±35	±35	±35	mV max
Load Regulation[4]	2.0	2.0	2.0	mV max
REFERENCE INPUT RESISTANCE	5	5	5	kΩ typ
POWER SUPPLIES				
Supply Voltages				
AVDD	5	5	5	V (±5% AVDD Operating)
DVDD	2.7 to 5.25	2.7 to 5.25	2.7 to 5.25	V
Supply Current				
IAVDD	14.0	26	58	mA max
	11.8	20	51	mA typ
IDVDD	0.5	0.5	4.0	mA max
	0.02	0.02	<1.0	mA typ
POWER CONSUMPTION	59.0	100	254	mW typ
	70.0	130	310	mW max

NOTES
[1]V_{REF} = 1 V.
[2]Including internal reference.
[3]Excluding internal reference.
[4]Load regulation with 1 mA load current (in addition to that required by the AD9221/AD9223/AD9220).
Specification subject to change without notice.

AC SPECIFICATIONS (AVDD = 5 V, DVDD= 5 V, f_{SAMPLE} = Max Conversion Rate, V_{REF} = 1.0 V, VINB = 2.5 V, DC Coupled/Single-Ended Input T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	AD9221	AD9223	AD9220	Unit
MAX CONVERSION RATE	1.5	3.0	10.0	MHz min
DYNAMIC PERFORMANCE				
Input Test Frequency 1 (VINA = –0.5 dBFS)	100	500	1000	kHz
Signal-to-Noise and Distortion (SINAD)	70.0	70.0	70	dB typ
	69.0	68.5	68.5	dB min
Effective Number of Bits (ENOBs)	11.3	11.3	11.3	dB typ
	11.2	11.1	11.1	dB min
Signal-to-Noise Ratio (SNR)	70.2	70.0	70.2	dB typ
	69.0	68.5	69.0	dB min
Total Harmonic Distortion (THD)	–83.4	–83.4	–83.7	dB typ
	–77.5	–76.0	–76.0	dB max
Spurious Free Dynamic Range (SFDR)	86.0	87.5	88.0	dB typ
	79.0	77.5	77.5	dB max
Input Test Frequency 2 (VINA = –0.5 dBFS)	0.50	1.50	5.0	MHz
Signal-to-Noise and Distortion (SINAD)	69.9	69.4	67.0	dB typ
	69.0	68.0	65.0	dB min
Effective Number of Bits (ENOBs)	11.3	11.2	10.8	dB typ
	11.2	11.1	10.5	dB min
Signal-to-Noise Ratio (SNR)	70.1	69.7	68.8	dB typ
	69.0	68.5	67.5	dB min
Total Harmonic Distortion (THD)	–83.4	–82.9	–72.0	dB typ
	–77.5	–75.0	–68.0	dB max
Spurious Free Dynamic Range (SFDR)	86.0	85.7	75.0	dB typ
	79.0	76.0	69.0	dB max
Full Power Bandwidth	25	40	60	MHz typ
Small Signal Bandwidth	25	40	60	MHz typ
Aperture Delay	1	1	1	ns typ
Aperture Jitter	4	4	4	ps rms typ
Acquisition to Full-Scale Step	125	43	30	ns typ

Specifications subject to change without notice.

DIGITAL SPECIFICATIONS (AVDD = 5 V, DVDD = 5 V, T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	Symbol		Unit
CLOCK INPUT			
High Level Input Voltage	V_{IH}	3.5	V min
Low Level Input Voltage	V_{IL}	1.0	V max
High Level Input Current (V_{IN} = DVDD)	I_{IH}	±10	μA max
Low Level Input Current (V_{IN} = 0 V)	I_{IL}	±10	μA max
Input Capacitance	C_{IN}	5	pF typ
LOGIC OUTPUTS			
DVDD = 5 V			
High Level Output Voltage (I_{OH} = 50 μA)	V_{OH}	4.5	V min
High Level Output Voltage (I_{OH} = 0.5 mA)	V_{OH}	2.4	V min
Low Level Output Voltage (I_{OL} = 1.6 mA)	V_{OL}	0.4	V max
Low Level Output Voltage (I_{OL} = 50 μA)	V_{OL}	0.1	V max
DVDD = 3 V			
High Level Output Voltage (I_{OH} = 50 μA)	V_{OH}	2.95	V min
High Level Output Voltage (I_{OH} = 0.5 mA)	V_{OH}	2.80	V min
Low Level Output Voltage (I_{OL} = 1.6 mA)	V_{OL}	0.4	V max
Low Level Output Voltage (I_{OL} = 50 μA)	V_{OL}	0.05	V max
Output Capacitance	C_{OUT}	5	pF typ

Specifications subject to change without notice.

AD9221/AD9223/AD9220

SWITCHING SPECIFICATIONS (T_{MIN} to T_{MAX} with AVDD = 5 V, DVDD = 5 V, C_L = 20 pF)

Parameter	Symbol	AD9221	AD9223	AD9220	Unit
Clock Period*	t_C	667	333	100	ns min
CLOCK Pulsewidth High	t_{CH}	300	150	45	ns min
CLOCK Pulsewidth Low	t_{CL}	300	150	45	ns min
Output Delay	t_{OD}	8	8	8	ns min
		13	13	13	ns typ
		19	19	19	ns max
Pipeline Delay (Latency)		3	3	3	Clock Cycles

*The clock period may be extended to 1 ms without degradation in specified performance @ 25 °C.

Specifications subject to change without notice.

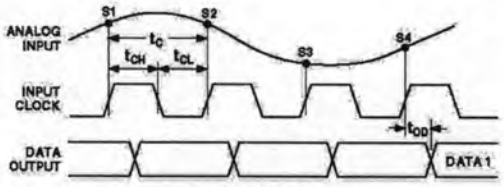


Figure 1. Timing Diagram

ABSOLUTE MAXIMUM RATINGS*

Parameter	With Respect to	Min	Max	Unit
AVDD	AVSS	–0.3	+6.5	V
DVDD	DVSS	–0.3	+6.5	V
AVSS	DVSS	–0.3	+0.3	V
AVDD	DVDD	–6.5	+6.5	V
REFCOM	AVSS	–0.3	+0.3	V
CLK	AVSS	–0.3	AVDD + 0.3	V
Digital Outputs	DVSS	–0.3	DVDD + 0.3	V
VINA, VINB	AVSS	–0.3	AVDD + 0.3	V
VREF	AVSS	–0.3	AVDD + 0.3	V
SENSE	AVSS	–0.3	AVDD + 0.3	V
CAPB, CAPT	AVSS	–0.3	AVDD + 0.3	V
Junction Temperature			150	°C
Storage Temperature		–65	+150	°C
Lead Temperature (10 sec)			300	°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may effect device reliability.

THERMAL CHARACTERISTICS

Thermal Resistance

28-Lead SOIC

θ_{JA} = 71.4°C/W

θ_{JC} = 23°C/W

28-Lead SSOP

θ_{JA} = 63.3°C/W

θ_{JC} = 23°C/W

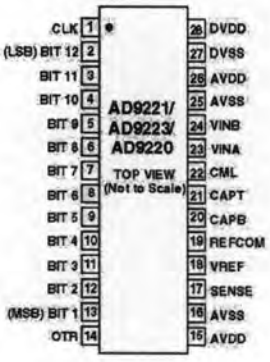
ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9221AR	–40°C to +85°C	28-Lead SOIC	R-28
AD9223AR	–40°C to +85°C	28-Lead SOIC	R-28
AD9220AR	–40°C to +85°C	28-Lead SOIC	R-28
AD9221ARS	–40°C to +85°C	28-Lead SSOP	RS-28
AD9223ARS	–40°C to +85°C	28-Lead SSOP	RS-28
AD9220ARS	–40°C to +85°C	28-Lead SSOP	RS-28
AD9221-EB		Evaluation Board	
AD9223-EB		Evaluation Board	
AD9220-EB		Evaluation Board	

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9221/AD9223/AD9220 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION



PIN FUNCTION DESCRIPTIONS

Pin Number	Mnemonic	Description
1	CLK	Clock Input Pin
2	BIT 12	Least Significant Data Bit (LSB)
3–12	BITS 11–2	Data Output Bit
13	BIT 1	Most Significant Data Bit (MSB)
14	OTR	Out of Range
15, 26	AVDD	5 V Analog Supply
16, 25	AVSS	Analog Ground
17	SENSE	Reference Select
18	VREF	Reference I/O
19	REFCOM	Reference Common
20	CAPB	Noise Reduction Pin
21	CAPT	Noise Reduction Pin
22	CML	Common-Mode Level (Midsupply)
23	VINA	Analog Input Pin (+)
24	VINB	Analog Input Pin (–)
27	DVSS	Digital Ground
28	DVDD	3 V to 5 V Digital Supply

DEFINITIONS OF SPECIFICATIONS

Integral Nonlinearity (INL)
INL refers to the deviation of each individual code from a line drawn from "negative full scale" through "positive full scale." The point used as negative full scale occurs 1/2 LSB before the first code transition. Positive full scale is defined as a level 1 1/2 LSB beyond the last code transition. The deviation is measured from the middle of each particular code to the true straight line.

Differential Nonlinearity (DNL, No Missing Codes)
An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. Guaranteed no missing codes to 12-bit resolution indicates that all 4096 codes, respectively, must be present over all operating ranges.

Zero Error
The major carry transition should occur for an analog value 1/2 LSB below VINA = VINB. Zero error is defined as the deviation of the actual transition from that point.

Gain Error
The first code transition should occur at an analog value 1/2 LSB above negative full scale. The last transition should occur at an analog value 1 1/2 LSB below the nominal full scale. Gain error is the deviation of the actual difference between first and last code transitions and the ideal difference between first and last code transitions.

Temperature Drift
The temperature drift for zero error and gain error specifies the maximum change from the initial (25°C) value to the value at T_{MIN} or T_{MAX}.

Power Supply Rejection
The specification shows the maximum change in full scale from the value with the supply at the minimum limit to the value with the supply at its maximum limit.

Aperture Jitter
Aperture jitter is the variation in aperture delay for successive samples and is manifested as noise on the input to the A/D.

Aperture Delay
Aperture delay is a measure of the sample-and-hold amplifier (SHA) performance and is measured from the rising edge of the clock input to when the input signal is held for conversion.

Signal-to-Noise and Distortion (S/N+D, SINAD) Ratio
S/N+D is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for S/N+D is expressed in decibels.

Effective Number of Bits (ENOB)
For a sine wave, SINAD can be expressed in terms of the number of bits. Using the following formula,

$$N = (SINAD - 1.76)/6.02$$

it is possible to get a measure of performance expressed as N, the effective number of bits.

Thus, effective number of bits for a device for sine wave inputs at a given input frequency can be calculated directly from its measured SINAD.

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of the first six harmonic components to the rms value of the measured input signal and is expressed as a percentage or in decibels.

Signal-to-Noise Ratio (SNR)
SNR is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding the first six harmonics and dc. The value for SNR is expressed in decibels.

Spurious Free Dynamic Range (SFDR)
SFDR is the difference in dB between the rms amplitude of the input signal and the peak spurious signal.

Low Cost, High Performance Voltage Feedback, 325 MHz Amplifiers

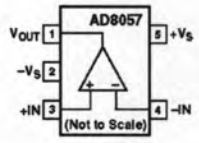
AD8057/AD8058

FEATURES
Low Cost Single (AD8057) and Dual (AD8058)
High Speed
325 MHz –3 dB Bandwidth (G = +1)
1000 V/μs Slew Rate
Gain Flatness 0.1 dB to 28 MHz
Low Noise
7 nV/√Hz
Low Power
5.4 mA/Amplifier Typical Supply Current @ 5 V
Low Distortion
–85 dBc @ 5 MHz, R_L = 1 kΩ
Wide Supply Range from 3 V to 12 V
Small Packaging
AD8057 Available in SOIC-8 and SOT-23-5
AD8058 Available in SOIC-8 and MSOP

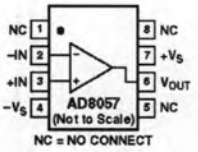
APPLICATIONS
Imaging
DVD/CD
Photodiode Preamp
A-to-D Driver
Professional Cameras
Filters

CONNECTION DIAGRAMS (TOP VIEW)

RT-5 (SOT-23-5)

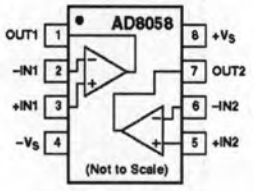


R-8 (SOIC)



NC = NO CONNECT

RM-8 (MSOP)
R-8 (SOIC)



GENERAL DESCRIPTION

The AD8057 (single) and AD8058 (dual) are very high performance amplifiers with a very low cost. The balance between cost and performance make them ideal for many applications. The AD8057 and AD8058 will reduce the need to qualify a variety of specialty amplifiers.

The AD8057 and AD8058 are voltage feedback amplifiers with the bandwidth and slew rate normally found in current feedback amplifiers. The AD8057 and AD8058 are low power amplifiers having low quiescent current and a wide supply range from 3 V to 12 V. They have noise and distortion performance required for high end video systems as well as dc performance parameters rarely found in high speed amplifiers.

The AD8057 and AD8058 are available in standard SOIC packaging as well as tiny SOT-23-5 (AD8057) and MSOP (AD8058) packages. These amplifiers are available in the industrial temperature range of –40°C to +85°C.

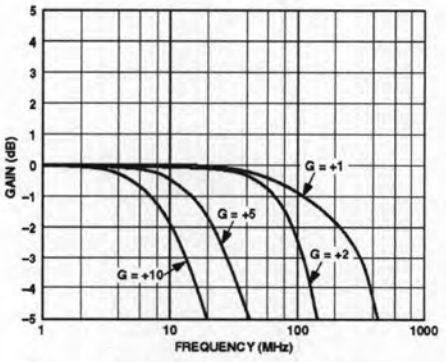


Figure 1. Small Signal Frequency Response

REV. B

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 www.analog.com
Fax: 781/326-8703

AD8057/AD8058–SPECIFICATIONS (@ T_A = 25°C, V_S = ±5 V, R_L = 100 Ω, R_F = 0 Ω, Gain = +1, unless otherwise noted.)

Parameter	Conditions	AD8057/AD8058 Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
–3 dB Bandwidth	G = +1, V_O = 0.2 V p-p		325		MHz
	G = –1, V_O = 0.2 V p-p		95		MHz
	G = +1, V_O = 2 V p-p		175		MHz
Bandwidth for 0.1 dB Flatness	G = +1, V_O = 0.2 V p-p		30		MHz
Slew Rate	G = +1, V_O = 2 V Step, R_L = 2 kΩ		850		V/µs
	G = +1, V_O = 4 V Step, R_L = 2 kΩ		1150		V/µs
Settling Time to 0.1%	G = +2, V_O = 2 V Step		30		ns
NOISE/HARMONIC PERFORMANCE					
Total Harmonic Distortion	f_C = 5 MHz, V_O = 2 V p-p, R_L = 1 kΩ		–85		dBc
	f_C = 20 MHz, V_O = 2 V p-p, R_L = 1 kΩ		–62		dBc
SFDR	f = 5 MHz, V_O = 2 V p-p, R_L = 150 Ω		–68		dB
Third Order Intercept	f = 5 MHz, V_O = 2 V p-p		–35		dBm
Crosstalk, Output to Output	f = 5 MHz, G = +2		–60		dB
Input Voltage Noise	f = 100 kHz		7		$nV/\sqrt{Hz}$
Input Current Noise	f = 100 kHz		0.7		$pA/\sqrt{Hz}$
Differential Gain Error	NTSC, G = +2, R_L = 150 Ω		0.01		%
	NTSC, G = +2, R_L = 1 kΩ		0.02		%
Differential Phase Error	NTSC, G = +2, R_L = 150 Ω		0.15		Degree
	NTSC, G = +2, R_L = 1 kΩ		0.01		Degree
Overload Recovery	V_{IN} = 200 mV p-p, G = +1		30		ns
DC PERFORMANCE					
Input Offset Voltage			1	5	mV
	T_{MIN} to T_{MAX}		2.5		mV
Input Offset Voltage Drift			3		µV/°C
Input Bias Current			0.5	2.5	µA
	T_{MIN} to T_{MAX}		3.0		µA
Input Offset Current				±0.75	µA
Open-Loop Gain	V_O = ±2.5 V, R_L = 2 kΩ	50	55		dB
	V_O = ±2.5 V, R_L = 150 Ω	50	52		dB
INPUT CHARACTERISTICS					
Input Resistance			10		MΩ
Input Capacitance	+Input		2		pF
Input Common-Mode Voltage Range	R_L = 1 kΩ	–4.0		+4.0	V
Common-Mode Rejection Ratio	VCM = ±2.5 V	48	60		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing	RL = 2 kΩ	–4.0		+4.0	V
	R_L = 150 Ω		±3.9		V
Capacitive Load Drive	30% Overshoot		30		pF
POWER SUPPLY					
Operating Range			±5.0		V
Quiescent Current for AD8057			6.0	7.5	mA
Quiescent Current for AD8058			14.0	15	mA
Power Supply Rejection Ratio	V_S = ±5 V to ±1.5 V	54	59		dB

Specifications subject to change without notice.

SPECIFICATIONS (@ T_A = 25°C, V_S = 5 V, R_L = 100 Ω, R_F = 0 Ω, Gain = +1, unless otherwise noted.)

Parameter	Conditions	AD8057/AD8058 Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
–3 dB Bandwidth	G = +1, V_O = 0.2 V p-p		300		MHz
	G = +1, V_O = 2 V p-p		155		MHz
Bandwidth for 0.1 dB Flatness	V_O = 0.2 V p-p		28		MHz
Slew Rate	G = +1, V_O = 2 V Step, R_L = 2 kΩ		700		V/µs
Settling Time to 0.1%	G = +2, V_O = 2 V Step		35		ns
NOISE/HARMONIC PERFORMANCE					
Total Harmonic Distortion	f_C = 5 MHz, V_O = 2 V p-p, R_L = 1 kΩ		–75		dBc
	f_C = 20 MHz, V_O = 2 V p-p, R_L = 1 kΩ		–54		dBc
Crosstalk, Output to Output	f = 5 MHz, G = +2		–60		dB
Input Voltage Noise	f = 100 kHz		7		nV/√Hz
Input Current Noise	f = 100 kHz		0.7		pA/√Hz
Differential Gain Error	NTSC, G = +2, R_L = 150 Ω		0.05		%
	NTSC, G = +2, R_L = 1 kΩ		0.05		%
Differential Phase Error	NTSC, G = +2, R_L = 150 Ω		0.10		Degree
	NTSC, G = +2, R_L = 1 kΩ		0.02		Degree
DC PERFORMANCE					
Input Offset Voltage			1	5	mV
	T_{MIN} to T_{MAX}		2.5		mV
Input Offset Voltage Drift			3		µV/°C
Input Bias Current			0.5	2.5	µA
	T_{MIN} to T_{MAX}		3.0		µA
Input Offset Current				0.75	µA
Open-Loop Gain	V_O = ±1.25 V, R_L = 2 kΩ to Midsupply	50	55		dB
	V_O = ±1.25 V, R_L = 150 Ω to Midsupply	45	52		dB
INPUT CHARACTERISTICS					
Input Resistance			10		MΩ
Input Capacitance	+Input		2		pF
Input Common-Mode Voltage Range	R_L = 1 kΩ		±0.9 to ±3.4		V
Common-Mode Rejection Ratio	V_{CM} = ±2.5 V	48	60		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing	R_L = 2 kΩ		0.9 to 4.1		V
	R_L = 150 Ω		1.2 to 3.8		V
Capacitive Load Drive	30% Overshoot		30		pF
POWER SUPPLY					
Operating Range			5.0		V
Quiescent Current for AD8057			5.4	7.0	mA
Quiescent Current for AD8058			13.5	14	mA
Power Supply Rejection Ratio		54	58		dB

Specifications subject to change without notice.

FT245BM USB FIFO (USB - Parallel) I.C.

The FT245BM is the 2nd generation of FTDI's popular USB FIFO i.c. This device not only adds extra functionality to it's FT8U245AM predecessor and reduces external component count, but also maintains a high degree of pin compatibility with the original, making it easy to upgrade or cost reduce existing designs as well as increasing the potential for using the device in new application areas.

1.0 Features

HARDWARE FEATURES

- Single Chip USB ⇔ Parallel FIFO bi-directional Data Transfer
- Transfer Data rate to 1M Byte / Sec - D2XX Drivers
- Transfer Data rate to 300 Kilobyte / Sec - VCP Drivers
- Simple to interface to MCU/ PLD / FPGA logic with a 4 wire handshake interface
- Entire USB protocol handled on-chip ... no USB-specific firmware programming required
- FTDI's royalty-free VCP and D2XX drivers eliminate the requirement for USB driver development in most cases.
- 384 Byte FIFO Tx buffer / 128 Byte FIFO Rx Buffer for high data throughput.
- New Send Immediate support via SI Pin for optimised data throughput.
- Support for USB Suspend / Resume through PWREN# and WAKEUP pins.
- Support for high power USB Bus powered devices through PWREN# pin
- Adjustable RX buffer timeout
- In-built support for event characters
- Integrated level converter on FIFO and control signals for interfacing to 5V and 3.3V logic
- Integrated 3.3V regulator for USB IO
- Integrated Power-On-Reset circuit
- Integrated 6MHz – 48Mhz clock multiplier PLL
- USB Bulk or Isochronous data transfer modes
- New Bit-Bang Mode allows the data bus to be used as an 8 bit general purpose IO Port without the need for MCU or other support logic.
- 4.35V to 5.25V single supply operation
- UHCI / OHCI / EHCI host controller compatible
- USB 1.1 and USB 2.0 compatible
- USB VID, PID , Serial Number and Product Description strings in external EEPROM
- EEPROM programmable on-board via USB
- Compact 32LD LQFP package

VIRTUAL COM PORT (VCP) DRIVERS for

- Windows 98 and Windows 98 SE
- Windows 2000 / ME / XP
- Windows CE **
- MAC OS-8 and OS-9
- MAC OS-X
- Linux 2.40 and greater

D2XX (USB Direct Drivers + DLL S/W Interface)

- Windows 98 and Windows 98 SE
- Windows 2000 / ME / XP

APPLICATION AREAS

- Easy MCU / PLD / FPGA interface to USB
- Upgrading Legacy Peripheral Designs to USB
- USB Instrumentation
- USB Industrial Control
- USB Audio and Low Bandwidth Video data transfer
- PDA ⇔ USB data transfer
- USB MP3 Player Interface
- USB FLASH Card Reader / Writers
- Set Top Box (S.T.B.) PC - USB interface
- USB Digital Camera Interface
- USB Hardware Modems
- USB Wireless Modems

[** = In planning or under development]

1.1 General Description

The FT245BM provides an easy cost-effective method of transferring data to / from a peripheral and a host P.C. at up to 8 Million bits (1 Megabyte) per second. Its simple, FIFO-like design makes it easy to interface to any microcontroller or microprocessor via IO ports.

To send data from the peripheral to the host computer, simply write the byte-wide data into the module when TXE# is low. If the (384-byte) transmit buffer fills up or is busy storing the previously written byte, the device keeps TXE# high in order to stop further data from being written until some of the FIFO data has been transferred over USB to the host. TXE# goes high after every byte written.

When the host sends data to the peripheral over USB, the device will take RXF# low to let the peripheral know that at least one byte of data is available. The peripheral can read a data byte every time RXF# goes low. RXF# goes high after every byte read.

By using FTDI's virtual COM port drivers, the peripheral looks like a standard COM port to the application software. Commands to set the baud rate are ignored - the device always transfers data at its fastest rate regardless of the application's baud-rate setting. Alternatively, FTDI's D2XX drivers allow application software to access the device "directly" through a published DLL based API. Details of the current VCP and D2XX driver can be found on FTDI's web site (http://www.ftdichip.com)

2.0 Enhancements

This section summarises the enhancements of the 2nd generation device compared to it's FT8U245AM predecessor. For further details, consult the device pin-out description and functional descriptions.

- **Integrated Power-On-Reset (POR) Circuit**
  The device now incorporates an internal POR function. The existing RESET# pin is maintained in order to allow external logic to reset the device where required, however for many applications this pin can now be either left N/C or hard wired to VCC. In addition, a new reset output pin (RSTOUT#) is provided in order to allow the new POR circuit to provide a stable reset to external MCU and other devices. RSTOUT# was the TEST pin on the previous generation of devices.
- **Integrated RCCLK Circuit**
  In the previous devices, an external RC circuit was required to ensure that the oscillator and clock multiplier PLL frequency was stable prior to enabling the clock internal to the device. This circuit is now embedded on-chip – the pin assigned to this function is now designated as the TEST pin and should be tied to GND for normal operation.
- **Integrated Level Converter on FIFO interface and control signals**
  The previous devices would drive the FIFO and control signals at 5V CMOS logic levels. The new device has a separate VCCIO pin allowing the device to directly interface to 3.3V and other logic families without the need for external level converter i.c.'s
- **Power Management control for USB Bus Powered, high current devices**
  A new PWREN# signal is provided which can be used to directly drive a transistor or P-Channel MOSFET in applications where power switching of external circuitry is required. A new EEPROM based option makes the device pull gently down it's FIFO interface lines when the power is shut off (PWREN# is High). In this mode, any residual voltage on external circuitry is bled to GND when power is removed thus ensuring that external

circuitry controlled by PWREN# resets reliably when power is restored. PWREN# can also be used by external circuitry to determine when USB is in suspend mode (PWREN# goes high).

- **Send Immediate / WakeUp (SI / WU) signal**
  The new Send Immediate / WakeUp signal combines two functions on a single pin. If USB is in suspend mode (and remote wakeup is enabled in the EEPROM), strobing this pin low will cause the device to request a resume from suspend (WakeUp) on the USB Bus. Normally, this can be used to wake up the Host PC. During normal operation, if this pin is strobed low any data in the device RX buffer will be sent out over USB on the next Bulk-IN request from the drivers regardless of the packet size. This can be used to optimise USB transfer speed for some applications.
- **Lower Suspend Current**
  Integration of RCCLK within the device and internal design improvements reduce the suspend current of the FT245BM to under 100uA typical (excluding the 1.5k pull-up on USB DP) in USB suspend mode. This allows greater margin for peripherals to meet the USB Suspend current limit of 500uA.
- **Support for USB Isochronous Transfers**
  Whilst USB Bulk transfer is usually the best choice for data transfer, the scheduling time of the data is not guaranteed. For applications where scheduling latency takes priority over data integrity such as transferring audio and low bandwidth video data, the new device now offers an option of USB Isochronous transfer via an option bit in the EEPROM.
- **Programmable FIFO TX Buffer Timeout**
  In the previous device, the TX buffer timeout used to flush remaining data from the TX buffer was fixed at 16ms timeout. This timeout is now programmable over USB in 1ms increments from 1ms to 255ms, thus allowing the device to be better optimised for protocols requiring faster response times from short data packets.
- **Relaxed VCC Decoupling**
  The 2nd generation devices now incorporate a level of on-chip VCC decoupling. Though this does not eliminate the need for external decoupling capacitors, it significantly improves the ease of PCB design requirements to meet FCC, CE and other EMI related specifications.
- **Bit Bang Mode**
  The 2nd generation device has a new option referred to as "Bit Bang" mode. In Bit Bang mode, the eight FIFO data lines can be switched between FIFO interface mode and an 8-bit Parallel IO port. Data packets can be sent to the device and they will be sequentially sent to the interface at a rate controlled by an internal timer (equivalent to the prescaler of the FT232BM device). As well as allowing the device to be used stand-alone as a general purpose IO controller for example controlling lights, relays and switches, some other interesting possibilities exist. For instance, it may be possible to connect the device to an SRAM configurable FPGA as supplied by vendors such as Altera and Xilinx. The FPGA device would normally be un-configured (i.e. have no defined function) at power-up. Application software on the PC could use Bit Bang Mode to download configuration data to the FPGA which would define it's hardware function, then after the FPGA device is configured the FT245BM can switch back into FIFO interface mode to allow the programmed FPGA device to communicate with the PC over USB. This approach allows a customer to create a "generic" USB peripheral who's hardware function can be defined under control of the application software. The FPGA based hardware can be easily upgraded or totally changed simply by changing the FPGA configuration data file. Application notes, software and development modules for this application area will be available from FTDI and other 3rd party developers.

- **Less External Support Components**

  As well as eliminating the RCCLK RC network, and for most applications the need for an external reset circuit, we have also eliminated the requirement for a 100k pull-up on EECS to select 6MHz operation. When the FT245BM is being used without the configuration EEPROM, EECS, EESK and EEDATA can now be left n/c. For circuits requiring a long reset time (where the device is reset externally using a reset generator i.c., or reset is controlled by the IO port of a MCU, FPGA or ASIC device) an external transistor circuit is no longer required as the 1k5 pull-up resistor on USBDP can be wired to the RSTOUT# pin instead of to 3.3V. Note : RSTOUT# drives out at 3.3V level, not at 5V VCC level. This is the preferred configuration for new designs.

- **Extended EEPROM Support**

  The previous generation of devices only supported EEPROM of type 93C46 (64 x 16 bit). The new devices will also work with EEPROM type 93C56 (128 x 16 bit) and 93C66 (256 x 16 bit). The extra space is not used by the device, however it is available for use by other external MCU / logic whilst the FT245BM is being held in reset.

- **USB 2.0 (full speed option)**

  A new EEPROM based option allows the FT245BM to return a USB 2.0 device descriptor as opposed to USB 1.1. Note : The device would be a USB 2.0 Full Speed device (12Mb/s) as opposed to a USB 2.0 High Speed device (480Mb/s).

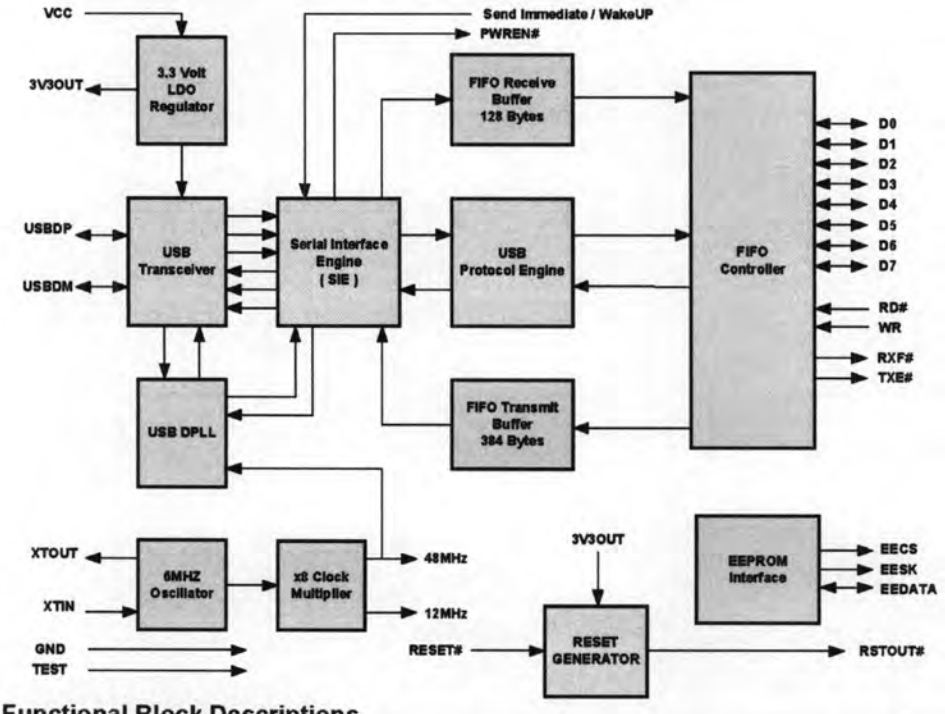
- **Multiple Device Support without EEPROM**

  When no EEPROM (or a blank or invalid EEPROM) is attached to the device, the FT245BM no longer gives a serial number as part of it's USB descriptor. This allows multiple devices to be simultaneously connected to the same PC. However, we still highly recommend that EEPROM is used, as without serial numbers a device can only be identified by which hub port in the USB tree it is connected to which can change if the end user re-plugs the device into a different USB port.

- **EEREQ# / EEGNT#**

  These (FT8U245AM) pins are not supported on the FT245BM device. They have been replaced with the new SI / WU and PWREN# signals respectively.

3.0 Block Diagram (simplified)



3.1 Functional Block Descriptions

- **3.3V LDO Regulator**
  The 3.3V LDO Regulator generates the 3.3 volt reference voltage for driving the USB transceiver cell output buffers. It requires an external decoupling capacitor to be attached to the 3V3OUT regulator output pin. It also provides 3.3V power to the RSTOUT# pin. The main function of this block is to power the USB Transceiver and the Reset Generator Cells rather than to power external logic. However, external circuitry requiring 3.3V nominal at a current of not greater than 5mA could also draw it's power from the 3V3OUT pin if required.
- **USB Transceiver**
  The USB Transceiver Cell provides the USB 1.1 / USB 2.0 full-speed physical interface to the USB cable. The output drivers provide 3.3 volt level slew rate control signalling, whilst a differential receiver and two single ended receivers provide USB data in, SEO and USB Reset condition detection.
- **USB DPLL**
  The USB DPLL cell locks on to the incoming NRZI USB data and provides separate recovered clock and data signals to the SIE block.
- **6MHz Oscillator**
  The 6MHz Oscillator cell generates a 6MHz reference clock input to the x8 Clock multiplier from an external 6MHz crystal or ceramic resonator.
- **x8 Clock Multiplier**
  The x8 Clock Multiplier takes the 6MHz input from the Oscillator cell and generates a 12MHz reference clock for the SIE, USB Protocol Engine and FIFO controller blocks. It also generates a 48MHz reference clock for the USB DPLL.
- **Serial Interface Engine (SIE)**
  The Serial Interface Engine (SIE) block performs the Parallel to Serial and Serial to Parallel conversion of the USB data. In accordance to the USB 2.0 specification, it performs bit stuffing / un-

stuffing and CRC5 / CRC16 generation / checking on the USB data stream.

- **USB Protocol Engine**
  The USB Protocol Engine manages the data stream from the device USB control endpoint. It handles the low level USB protocol (Chapter 9) requests generated by the USB host controller and the commands for controlling the functional parameters of the FIFO.
- **FIFO Receive Buffer (128 bytes)**
  Data sent from the USB Host to the FIFO via the USB data out endpoint is stored in the FIFO Receive Buffer and is removed from the buffer by reading the FIFO contents using RD#.
- **FIFO Transmit Buffer (384 bytes)**
  Data written into the FIFO using WR# is stored in the FIFO Transmit Buffer. The Host removes Data from the FIFO Transmit Data by sending a USB request for data from the device data in endpoint.
- **FIFO Controller**
  The FIFO Controller handles the transfer of data between the external FIFO interface pins and the FIFO Transmit and Receive buffers.
- **RESET Generator**
  The Reset Generator Cell provides a reliable power-on reset to the device internal circuitry on power up. An additional RESET# input and RSTOUT# output are provided to allow other devices to reset the FT245BM, or the FT245BM to reset other devices respectively. During reset, RSTOUT# is driven low, otherwise it drives out at the 3.3V provided by the onboard regulator. RSTOUT# can be used to control the 1k5 pull-up on USB DP directly where delayed USB enumeration is required. RSTOUT# will be low for approximately 5ms after VCC has risen above 3.5V AND the device oscillator is running AND RESET# is high. RESET# should be tied to VCC unless it is a requirement to reset the device from external logic or an external reset generator i.c.
- **EEPROM Interface**
  Though the FT245BM will work without the optional EEPROM, an external 93C46 (93C56 or 93C66) EEPROM can be used to customise the USB VID, PID, Serial Number, Product Description Strings and Power Descriptor value of the FT245BM for OEM applications. Other parameters controlled by the EEPROM include Remote Wake Up, Isochronous Transfer Mode, Soft Pull Down on Power-Off and USB 2.0 descriptor modes.
  The EEPROM should be a 16 bit wide configuration such as a MicroChip 93LC46B or equivalent capable of a 1Mb/s clock rate at VCC = 4.35V to 5.25V. The EEPROM is programmable-on board over USB using a utility available from FTDI's web site (http://www.ftdichip.com). This allows a blank part to be soldered onto the PCB and programmed as part of the manufacturing and test process.
  If no EEPROM is connected (or the EEPROM is blank), the FT245BM will use it's built-in default VID, PID Product Description and Power Descriptor Value. In this case, the device will not have a serial number as part of the USB descriptor.

4.0 Device Pin-Out

Figure 1
Pin-Out
(LQFP-32 Package)

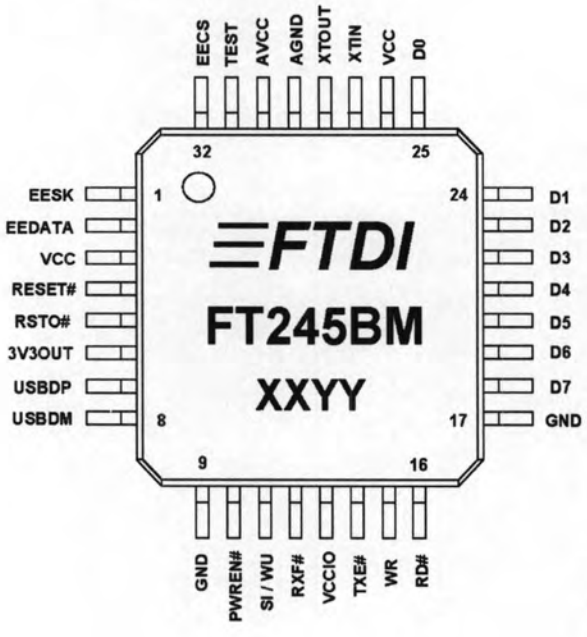
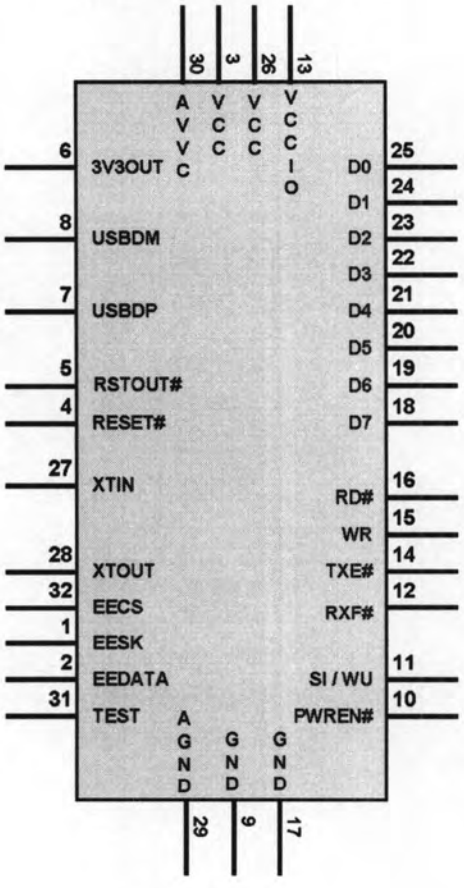


Figure 2
Pin-Out
(Schematic Symbol)



4.1 Signal Descriptions

Table 1 - FT245BM - PINOUT DESCRIPTION

FIFO DATA BUS GROUP (* Note 1)**

Pin#	Signal	Type	Description
25	D0	I/O	FIFO Data Bus Bit 0
24	D1	I/O	FIFO Data Bus Bit 1
23	D2	I/O	FIFO Data Bus Bit 2
22	D3	I/O	FIFO Data Bus Bit 3
21	D4	I/O	FIFO Data Bus Bit 4
20	D5	I/O	FIFO Data Bus Bit 5
19	D6	I/O	FIFO Data Bus Bit 6
18	D7	I/O	FIFO Data Bus Bit 7

FIFO CONTROL INTERFACE GROUP

Pin#	Signal	Type	Description
16	RD#	IN	Enables Current FIFO Data Byte on D0..D7 when low. Fetches the next FIFO Data Byte (if available) from the Receive FIFO Buffer when RD# goes from low to high. (*** Note 1)
15	WR	IN	Writes the Data Byte on the D0..D7 into the Transmit FIFO Buffer when WR goes from high to low. (*** Note 1)
14	TXE#	OUT	When high, do not write data into the FIFO. When low, data can be written into the FIFO by strobing WR high then low. (*** Note 2)
12	RXF#	OUT	When high, do not read data from the FIFO. When low, there is data available in the FIFO which can be read by strobing RD# low then high again (*** Note 2)

USB INTERFACE GROUP

Pin#	Signal	Type	Description
7	USBDP	I/O	USB Data Signal Plus (Requires 1.5k pull-up to 3V3OUT or RSTOUT#)
8	USBDM	I/O	USB Data Signal Minus

EEPROM INTERFACE GROUP

Pin#	Signal	Type	Description
32	EECS	I/O	EEPROM – Chip Select. For 48MHz operation pull EECS to GND using a 10k resistor. For 6MHz operation no resistor is required. (*** Note 3)
1	EESK	OUT	Clock signal to EEPROM. (*** Note 3)
2	EEDATA	I/O	EEPROM – Data I/O Connect directly to Data-In of the EEPROM and to Data-Out of the EEPROM via a 2k2 resistor. Also pull Data-Out of the EEPROM to VCC via a 10k resistor for correct operation. (*** Note 3)

4.1 Signal Descriptions

Table 1 - FT245BM - PINOUT DESCRIPTION

FIFO DATA BUS GROUP (* Note 1)**

Pin#	Signal	Type	Description
25	D0	I/O	FIFO Data Bus Bit 0
24	D1	I/O	FIFO Data Bus Bit 1
23	D2	I/O	FIFO Data Bus Bit 2
22	D3	I/O	FIFO Data Bus Bit 3
21	D4	I/O	FIFO Data Bus Bit 4
20	D5	I/O	FIFO Data Bus Bit 5
19	D6	I/O	FIFO Data Bus Bit 6
18	D7	I/O	FIFO Data Bus Bit 7

FIFO CONTROL INTERFACE GROUP

Pin#	Signal	Type	Description
16	RD#	IN	Enables Current FIFO Data Byte on D0..D7 when low. Fetches the next FIFO Data Byte (if available) from the Receive FIFO Buffer when RD# goes from low to high. (*** Note 1)
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12	RXF#	OUT	When high, do not read data from the FIFO. When low, there is data available in the FIFO which can be read by strobing RD# low then high again (*** Note 2)

USB INTERFACE GROUP

Pin#	Signal	Type	Description
7	USBDP	I/O	USB Data Signal Plus (Requires 1.5k pull-up to 3V3OUT or RSTOUT#)
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EEPROM INTERFACE GROUP

Pin#	Signal	Type	Description
32	EECS	I/O	EEPROM – Chip Select. For 48MHz operation pull EECS to GND using a 10k resistor. For 6MHz operation no resistor is required. (*** Note 3)
1	EESK	OUT	Clock signal to EEPROM. (*** Note 3)
2	EEDATA	I/O	EEPROM – Data I/O Connect directly to Data-In of the EEPROM and to Data-Out of the EEPROM via a 2k2 resistor. Also pull Data-Out of the EEPROM to VCC via a 10k resistor for correct operation. (*** Note 3)

POWER CONTROL GROUP

Pin#	Signal	Type	Description
10	PWREN#	OUT	Goes Low after the device is configured via USB, then high during USB suspend. Can be used to control power to external logic using a P-Channel Logic Level MOSFET switch. Enable the Interface Pull-Down Option in EEPROM when using the PWREN# pin in this way.
11	SI / WU	IN	The Send Immediate / WakeUp signal combines two functions on a single pin. If USB is in suspend mode (PWREN# = 1) and remote wakeup is enabled in the EEPROM , strobing this pin low will cause the device to request a resume on the USB Bus. Normally, this can be used to wake up the Host PC. During normal operation (PWREN# = 0), if this pin is strobed low any data in the device TX buffer will be sent out over USB on the next Bulk-IN request from the drivers regardless of the pending packet size. This can be used to optimise USB transfer speed for some applications. Tie this pin to VCCIO if not used.

MISCELLANEOUS SIGNAL GROUP

Pin#	Signal	Type	Description
4	RESET#	IN	Can be used by an external device to reset the FT245BM. If not required, tie to VCC.
5	RSTOUT#	OUT	Output of the internal Reset Generator. Stays high impedance for ~ 5ms after VCC > 3.5V and the internal clock starts up, then clamps it's output to the 3.3V output of the internal regulator. Taking RESET# low will also force RSTOUT# to drive low. RSTOUT# is NOT affected by a USB Bus Reset.
27	XTIN	IN	Input to 6MHz Crystal Oscillator Cell. This pin can also be driven by an external 6MHz clock if required. Note : Switching threshold of this pin is VCC/2, so if driving from an external source, the source must be driving at 5V CMOS level or a.c. coupled to centre around VCC/2.
28	XTOUT	OUT	Output from 6MHz Crystal Oscillator Cell. XTOUT stops oscillating during USB suspend, so take care if using this signal to clock external logic.
31	TEST	IN	Puts device in i.c. test mode – must be tied to GND for normal operation.

POWER AND GND GROUP

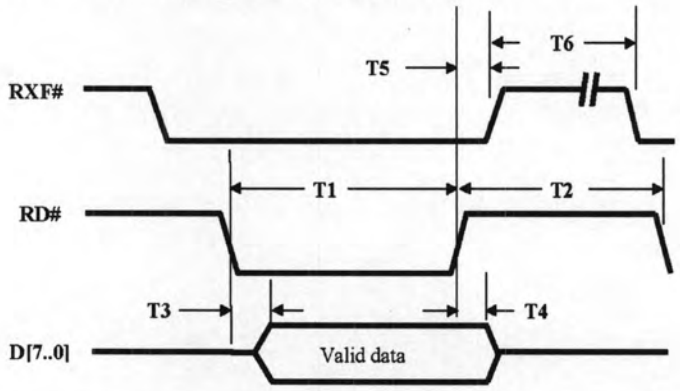
Pin#	Signal	Type	Description
6	3V3OUT	OUT	3.3 volt Output from the integrated L.D.O. regulator This pin should be decoupled to GND using a 33nF ceramic capacitor in close proximity to the device pin. It's prime purpose is to provide the internal 3.3V supply to the USB transceiver cell and the RSTOUT# pin. A small amount of current (<= 5mA) can be drawn from this pin to power external 3.3V logic if required.
3,26	VCC	PWR	+4.35 volt to +5.25 volt VCC to the device core, LDO and none-FIFO interface pins.
13	VCCIO	PWR	+3.0 volt to +5.25 volt VCC to the FIFO interface pins 10..12, 14..16 and 18..25. When interfacing with 3.3V external logic connect VCCIO to the 3.3V supply of the external logic, otherwise connect to VCC to drive out at 5V CMOS level.
9,17	GND	PWR	Device - Ground Supply Pins
30	AVCC	PWR	Device - Analog Power Supply for the internal x8 clock multiplier
29	AGND	PWR	Device - Analog Ground Supply for the internal x8 clock multiplier

Note 1 : In Input Mode, these pins are pulled to VCCIO via internal 200k resistors. These can be programmed to gently pull low during USB suspend (PWREN# = "1") by setting this option in the EEPROM.

Note 2: During device reset, these pins are tri-state but pulled up to VCCIO via internal 200k resistors.

Note 3: During device reset, these pins are tri-state but pulled up to VCC via internal 200k resistors.

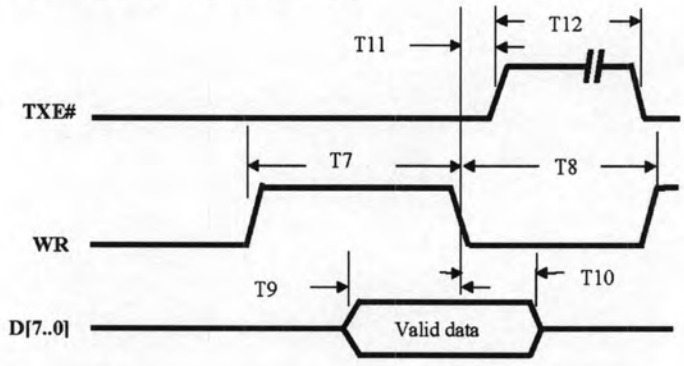
FT245BM TIMING DIAGRAM – FIFO READ CYCLE



Time	Description	Min	Max	Unit
T1	RD Active Pulse Width	50		ns
T2	RD to RD Pre-Charge Time	50 + T6		ns
T3	RD Active to Valid Data ** Note 1	20	50	ns
T4	Valid Data Hold Time from RD Inactive ** Note 1	0		ns
T5	RD Inactive to RXF#	0	25	ns
T6	RXF inactive after RD cycle	80		ns

** Note 1 - Load 30 pF

FT245BM TIMING DIAGRAM – FIFO WRITE CYCLE



Time	Description	Min	Max	Unit
T7	WR Active Pulse Width	50		ns
T8	WR to WR Pre-Charge Time	50 + T12		ns
T9	Data Setup Time before WR inactive	20		ns
T10	Data Hold Time from WR inactive	0		ns
T11	WR Inactive to TXE#	5	25	ns
T12	TXE inactive after RD cycle	80		Ns

ประวัติผู้เขียนวิทยานิพนธ์

นายจตุรภุช แดงเนียม เกิดวันที่ 11 พฤศจิกายน พ.ศ. 2518 ที่จังหวัดสมุทรปราการ สำเร็จการศึกษาระดับปริญญาบัณฑิตจากภาควิชาเทคโนโลยีการวัดคุมทางอุตสาหกรรม คณะวิศวกรรมศาสตร์ สถาบันเทคโนโลยีพระจอมเกล้าเจ้าคุณทหารลาดกระบัง เมื่อปีการศึกษา 2542 และในปีการศึกษา 2546 ได้เข้าศึกษาระดับปริญญามหาบัณฑิตที่ภาควิชานิวเคลียร์เทคโนโลยี คณะวิศวกรรมศาสตร์ จุฬาลงกรณ์มหาวิทยาลัย