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ภาคผนวก ก

คำสั่ง Z-80

Z80 INSTRUCTION CODES

(The literal d is shown as 05 in the object code.)

OBJ CODE	SOURCE STATEMENT	
8E	ADC	A,(HL)
DD8E05	ADC	A,(IX+d)
FD8E05	ADC	A,(IY+d)
8F	ADC	A,A
88	ADC	A,B
89	ADC	A,C
8A	ADC	A,D
8B	ADC	A,E
8C	ADC	A,H
8D	ADC	A,L
CE20	ADC	A,n
ED4A	ADC	HL,BC
ED5A	ADC	HL,DE
ED6A	ADC	HL,HL
ED7A	ADC	HL,SP
86	ADD	A,(HL)
DD8605	ADD	A,(IX+d)
FD8605	ADD	A,(IY+d)
87	ADD	A,A
80	ADD	A,B
81	ADD	A,C
82	ADD	A,D
83	ADD	A,E
84	ADD	A,H
85	ADD	A,L
C620	ADD	A,n
09	ADD	HL,BC
19	ADD	HL,DE
29	ADD	HL,HL
39	ADD	HL,SP
DD09	ADD	IX,BC
DD19	ADD	IX,DE
DD29	ADD	IX,IX
DD39	ADD	IX,SP
FD09	ADD	IY,BC
FD19	ADD	IY,DE
FD29	ADD	IY,IY
FD39	ADD	IY,SP
A6	AND	(HL)
DDA605	AND	(IX+d)
FDA605	AND	(IY+d)
A7	AND	A
A0	AND	B
A1	AND	C
A2	AND	D
A3	AND	E
A4	AND	H
A5	AND	L

OBJ CODE	SOURCE STATEMENT	
E620	AND	n
CB46	BIT	0,(HL)
DDCB0546	BIT	0,(IX+d)
FDCB0546	BIT	0,(IY+d)
CB47	BIT	0,A
CB40	BIT	0,B
CB41	BIT	0,C
CB42	BIT	0,D
CB43	BIT	0,E
CB44	BIT	0,H
CB45	BIT	0,L
CB4E	BIT	1 (HL)
DDCB054E	BIT	1,(IX+d)
FDCB054E	BIT	1,(IY+d)
CB4F	BIT	1,A
CB48	BIT	1,B
CB49	BIT	1,C
CB4A	BIT	1,D
CB4B	BIT	1,E
CB4C	BIT	1,H
CB4D	BIT	1,L
CB56	BIT	2,(HL)
DDCB0556	BIT	2,(IX+d)
FDCB0556	BIT	2,(IY+d)
CB57	BIT	2,A
CB50	BIT	2,B
CB51	BIT	2,C
CB52	BIT	2,D
CB53	BIT	2,E
CB54	BIT	2,H
CB55	BIT	2,L
CB5E	BIT	3,(HL)
DDCB055E	BIT	3,(IX+d)
FDCB055E	BIT	3,(IY+d)
CB5F	BIT	3,A
CB58	BIT	3,B
CB59	BIT	3,C
CB5A	BIT	3,D
CB5B	BIT	3,E
CB5C	BIT	3,H
CB5D	BIT	3,L
CB66	BIT	4,(HL)
DDCB0566	BIT	4,(IX+d)
FDCB0566	BIT	4,(IY+d)
CB67	BIT	4,A
CB60	BIT	4,B
CB61	BIT	4,C
CB62	BIT	4,D

OBJ CODE	SOURCE STATEMENT	
CB63	BIT	4,E
CB64	BIT	4,H
CB65	BIT	4,L
CB6E	BIT	5,(HL)
DDCB056E	BIT	5,(IX+d)
FDCB056E	BIT	5,(IY+d)
CB6F	BIT	5,A
CB68	BIT	5,B
CB69	BIT	5,C
CB6A	BIT	5,D
CB6B	BIT	5,E
CB6C	BIT	5,H
CB6D	BIT	5,L
CB76	BIT	6,(HL)
DDCB0576	BIT	6,(IX+d)
FDCB0576	BIT	6,(IY+d)
CB77	BIT	6,A
CB70	BIT	6,B
CB71	BIT	6,C
CB72	BIT	6,D
CB73	BIT	6,E
CB74	BIT	6,H
CB75	BIT	6,L
CB7E	BIT	7,(HL)
DDCB057E	BIT	7,(IX+d)
FDCB057E	BIT	7,(IY+d)
CB7F	BIT	7,A
CB78	BIT	7,B
CB79	BIT	7,C
CB7A	BIT	7,D
CB7B	BIT	7,E
CB7C	BIT	7,H
CB7D	BIT	7,L
DC8405	CALL	C,nn
FC8405	CALL	M,nn
D48405	CALL	NC,nn
C48405	CALL	NZ,nn
F48405	CALL	P,nn
EC8405	CALL	PE,nn
E48405	CALL	PO,nn
CC8405	CALL	Z,nn
CD8405	CALL	nn
3F	CCF	
BE	CP	(HL)
DDBE05	CP	(IX+d)
FDBE05	CP	(IY+d)
BF	CP	A
B8	CP	B
B9	CP	C
BA	CP	D
BB	CP	E
BC	CP	H
BD	CP	L
FE20	CP	n
EDA9	CPD	
EDB9	CPDR	

OBJ CODE	SOURCE STATEMENT	
EDB1	CPIR	
EDA1	CPI	
2F	CPL	
27	DAA	
35	DEC	(HL)
DD3505	DEC	(IX+d)
FD3505	DEC	(IY+d)
3D	DEC	A
05	DEC	B
0B	DEC	BC
0D	DEC	C
15	DEC	D
1B	DEC	DE
1D	DEC	E
25	DEC	H
2B	DEC	HL
DD2B	DEC	IX
FD2B	DEC	IY
2D	DEC	L
3B	DEC	SP
F3	DI	
102E	DJNZ	e
FB	EI	
E3	EX	(SP),HL
DDE3	EX	(SP),IX
FDE3	EX	(SP),IY
08	EX	AF,AF'
EB	EX	DE,HL
D9	EXX	
76	HALT	
ED46	IM	0
ED56	IM	1
ED5E	IM	2
ED78	IN	A,(C)
ED40	IN	B,(C)
ED48	IN	C,(C)
ED50	IN	D,(C)
ED58	IN	E,(C)
ED60	IN	H,(C)
ED68	IN	L,(C)
34	INC	(HL)
DD3405	INC	(IX+d)
FD3405	INC	(IY+d)
3C	INC	A
04	INC	B
03	INC	BC
0C	INC	C
14	INC	D
13	INC	DE
1C	INC	E
24	INC	H
23	INC	HL
DD23	INC	IX
FD23	INC	IY
2C	INC	L
33	INC	SP
DB20	IN	A,(n)

OBJ CODE	SOURCE STATEMENT	
EDAA	IND	
EDBA	INDR	
EDA2	INI	
EDB2	INIR	
C38405	JP	nn
E9	JP	(HL)
DDE9	JP	(IX)
FDE9	JP	(IY)
DA8405	JP	C,nn
FA8405	JP	M,nn
D28405	JP	NC,nn
C28405	JP	NZ,nn
F28405	JP	P,nn
EA8405	JP	PE,nn
E28405	JP	PO,nn
CA8405	JP	Z,nn
382E	JR	C,e
302E	JR	NC,e
202E	JR	NZ,e
282E	JR	Z,e
182E	JR	e
02	LD	(BC),A
12	LD	(DE),A
77	LD	(HL),A
70	LD	(HL),B
71	LD	(HL),C
72	LD	(HL),D
73	LD	(HL),E
74	LD	(HL),H
75	LD	(HL),L
3620	LD	(HL),n
DD7705	LD	(IX+d),A
DD7005	LD	(IX+d),B
DD7105	LD	(IX+d),C
DD7205	LD	(IX+d),D
DD7305	LD	(IX+d),E
DD7405	LD	(IX+d),H
DD7505	LD	(IX+d),L
DD360520	LD	(IX+d),n
FD7705	LD	(IY+d),A
FD7005	LD	(IY+d),B
FD7105	LD	(IY+d),C
FD7205	LD	(IY+d),D
FD7305	LD	(IY+d),E
FD7405	LD	(IY+d),H
FD7505	LD	(IY+d),L
FD360520	LD	(IY+d),n
328405	LD	(nn),A
ED438405	LD	(nn),BC
ED538405	LD	(nn),DE
228405	LD	(nn),HL
DD228405	LD	(nn),IX
FD228405	LD	(nn),IY
ED738405	LD	(nn),SP
0A	LD	A,(BC)
1A	LD	A,(DE)
7E	LD	A,(HL)

OBJ CODE	SOURCE STATEMENT	
DD7E05	LD	A,(IX+d)
FD7E05	LD	A,(IY+d)
3A8405	LD	A,(nn)
7F	LD	A,A
78	LD	A,B
79	LD	A,C
7A	LD	A,D
7B	LD	A,E
7C	LD	A,H
ED57	LD	A,I
7D	LD	A,L
3E20	LD	A,n
ED5F	LD	A,R
46	LD	B,(HL)
DD4605	LD	B,(IX+d)
FD4605	LD	B,(IY+d)
47	LD	B,A
40	LD	B,B
41	LD	B,C
42	LD	B,D
43	LD	B,E
44	LD	B,H
45	LD	B,L
0620	LD	B,n
ED4B8405	LD	BC,(nn)
018405	LD	BC,nn
4E	LD	C,(HL)
DD4E05	LD	C,(IX+d)
FD4E05	LD	C,(IY+d)
4F	LD	C,A
48	LD	C,B
49	LD	C,C
4A	LD	C,D
4B	LD	C,E
4C	LD	C,H
4D	LD	C,L
0E20	LD	C,n
56	LD	D,(HL)
DD5605	LD	D,(IX+d)
FD5605	LD	D,(IY+d)
57	LD	D,A
50	LD	D,B
51	LD	D,C
52	LD	D,D
53	LD	D,E
54	LD	D,H
55	LD	D,L
1620	LD	D,n
ED5B8405	LD	DE,(nn)
118405	LD	DE,nn
5E	LD	E,(HL)
DD5E05	LD	E,(IX+d)
FD5E05	LD	E,(IY+d)
5F	LD	E,A
58	LD	E,B
59	LD	E,C
5A	LD	E,D

OBJ CODE	SOURCE STATEMENT	
5B	LD	E,E
5C	LD	E,H
5D	LD	E,L
1E20	LD	E,n
66	LD	H,(HL)
DD6605	LD	H,(IX+d)
FD6605	LD	H,(IY+d)
67	LD	H,A
60	LD	H,B
61	LD	H,C
62	LD	H,D
63	LD	H,E
64	LD	H,H
65	LD	H,L
2620	LD	H,n
2A8405	LD	HL,(nn)
218405	LD	HL,nn
ED47	LD	I,A
DD2A8405	LD	IX,(nn)
DD218405	LD	IX,nn
FD2A8405	LD	IY,(nn)
FD218405	LD	IY,nn
6E	LD	L,(HL)
DD6E05	LD	L,(IX+d)
FD6E05	LD	L,(IY+d)
6F	LD	L,A
68	LD	L,B
69	LD	L,C
6A	LD	L,D
6B	LD	L,E
6C	LD	L,H
6D	LD	L,L
2E20	LD	L,n
ED4F	LD	R,A
ED7B8405	LD	SP,(nn)
F9	LD	SP,HL
DDF9	LD	SP,IX
FDF9	LD	SP,IY
318405	LD	SP,nn
EDA8	LDD	
EDB8	LDDR	
EDA0	LDI	
EDB0	LDIR	
ED44	NEG	
00	NOP	
B6	OR	(HL)
DDB605	OR	(IX+d)
FDB605	OR	(IY+d)
B7	OR	A
B0	OR	B
B1	OR	C
B2	OR	D
B3	OR	E
B4	OR	H
B5	OR	L
F620	OR	n
ED8B	OTDR	

OBJ CODE	SOURCE STATEMENT	
EDB3	OTIR	
ED79	OUT	(C),A
ED41	OUT	(C),B
ED49	OUT	(C),C
ED51	OUT	(C),D
ED59	OUT	(C),E
ED61	OUT	(C),H
ED69	OUT	(C),L
D320	OUT	(n),A
EDAB	OUTD	
EDA3	OUTI	
F1	POP	AF
C1	POP	BC
D1	POP	DE
E1	POP	HL
DDE1	POP	IX
FDE1	POP	IY
F5	PUSH	AF
C5	PUSH	BC
D5	PUSH	DE
E5	PUSH	HL
DDE5	PUSH	IX
FDE5	PUSH	IY
CB86	RES	0,(HL)
DDCB0586	RES	0,(IX+d)
FDCB0586	RES	0,(IY+d)
CB87	RES	0,A
CB80	RES	0,B
CB81	RES	0,C
CB82	RES	0,D
CB83	RES	0,E
CB84	RES	0,H
CB85	RES	0,L
CB8E	RES	1,(HL)
DDCB058E	RES	1,(IX+d)
FDCB058E	RES	1,(IY+d)
CB8F	RES	1,A
CB88	RES	1,B
CB89	RES	1,C
CB8A	RES	1,D
CB8B	RES	1,E
CB8C	RES	1,H
CB8D	RES	1,L
CB96	RES	2,(HL)
DDCB0596	RES	2,(IX+d)
FDCB0596	RES	2,(IY+d)
CB97	RES	2,A
CB90	RES	2,B
CB91	RES	2,C
CB92	RES	2,D
CB93	RES	2,E
CB94	RES	2,H
CB95	RES	2,L
CB9E	RES	3,(HL)
DDCB059E	RES	3,(IX+d)
FDCB059E	RES	3,(IY+d)

OBJ CODE	SOURCE STATEMENT	
CB9F	RES	3,A
CB98	RES	3,B
CB99	RES	3,C
CB9A	RES	3,D
CB9B	RES	3,E
CB9C	RES	3,H
CB9D	RES	3,L
CBA6	RES	4,(HL)
DDCB05A6	RES	4,(IX+d)
FDCB05A6	RES	4,(IY+d)
CBA7	RES	4,A
CBA0	RES	4,B
CBA1	RES	4,C
CBA2	RES	4,D
DBA3	RES	4,E
CBA4	RES	4,H
CBA5	RES	4,L
CBAE	RES	5,(HL)
DDCB05AE	RES	5,(IX+d)
FDCB05AE	RES	5,(IY+d)
CBAF	RES	5,A
CBA8	RES	5,B
CBA9	RES	5,C
CBAA	RES	5,D
CBAB	RES	5,E
CBAC	RES	5,H
CBAD	RES	5,L
CBB6	RES	6,(HL)
DDCB05B6	RES	6,(IX+d)
FDCB05B6	RES	6,(IY+d)
CBB7	RES	6,A
CBB0	RES	6,B
CBB1	RES	6,C
CBB2	RES	6,D
CBB3	RES	6,E
CBB4	RES	6,H
CBB5	RES	6,L
CBBE	RES	7,(HL)
DDCB05BE	RES	7,(IX+d)
FDCB05BE	RES	7,(IY+d)
CBBF	RES	7,A
CBB8	RES	7,B
CBB9	RES	7,C
CBBA	RES	7,D
CBBB	RES	7,E
CBBC	RES	7,H
CBBD	RES	7,L
C9	RET	
D8	RET	C
F8	RET	M
D0	RET	NC
C0	RET	NZ
F0	RET	P
E8	RET	PE
E0	RET	PO
C8	RET	Z

OBJ CODE	SOURCE STATEMENT	
ED4D	RETI	
ED45	RETN	
CB16	RL	(HL)
DDCB0516	RL	(IX+d)
FDCB0516	RL	(IY+d)
CB17	RL	A
CB10	RL	B
CB11	RL	C
CB12	RL	D
CB13	RL	E
CB14	RL	H
CB15	RL	L
17	RLA	
CB06	RLC	(HL)
DDCB0506	RLC	(IX+d)
FDCB0506	RLC	(IY+d)
CB07	RLC	A
CB00	RLC	B
CB01	RLC	C
CB02	RLC	D
CB03	RLC	E
CB04	RLC	H
CB05	RLC	L
07	RLCA	
ED6F	RLD	
CB1E	RR	(HL)
DDCB051E	RR	(IX+d)
FDCB051E	RR	(IY+d)
CB1F	RR	A
CB18	RR	B
CB19	RR	C
CB1A	RR	D
CB1B	RR	E
CB1C	RR	H
CB1D	RR	L
1F	RRA	
CB0E	RRC	(HL)
DDCB050E	RRC	(IX+d)
FDCB050E	RRC	(IY+d)
CB0F	RRC	A
CB08	RRC	B
CB09	RRC	C
CB0A	RRC	D
CB0B	RRC	E
CB0C	RRC	H
CB0D	RRC	L
OF	RRCA	
ED67	RRD	
C7	RST	00H
CF	RST	08H
D7	RST	10H
DF	RST	18H
E7	RST	20H
EF	RST	28H
F7	RST	30H
FF	RST	38H
DE20	SBC	A,n

OBJ CODE	SOURCE STATEMENT	
9E	SBC	A,(HL)
DD9E05	SBC	A,(IX+d)
FD9E05	SBC	A,(IY+d)
9F	SBC	A,A
98	SBC	A,B
99	SBC	A,C
9A	SBC	A,D
9B	SBC	A,E
9C	SBC	A,H
9D	SBC	A,L
ED42	SBC	HL,BC
ED52	SBC	HL,DE
ED62	SBC	HL,HL
ED72	SBC	HL,SP
37	SCF	
CBC6	SET	0,(HL)
DDCB05C6	SET	0,(IX+d)
FDCB05C6	SET	0,(IY+d)
CBC7	SET	0,A
CBC0	SET	0,B
CBC1	SET	0,C
CBC2	SET	0,D
CBC3	SET	0,E
CBC4	SET	0,H
CBC5	SET	0,L
CBCE	SET	1,(HL)
DDCB05CE	SET	1,(IX+d)
FDCB05CE	SET	1,(IY+d)
CBCF	SET	1,A
CBC8	SET	1,B
CBC9	SET	1,C
CBCA	SET	1,D
CBCB	SET	1,E
CBCC	SET	1,H
CBCD	SET	1,L
CBD6	SET	2,(HL)
DDCB05D6	SET	2,(IX+d)
FDCB05D6	SET	2,(IY+d)
CBD7	SET	2,A
CBD0	SET	2,B
CBD1	SET	2,C
CBD2	SET	2,D
CBD3	SET	2,E
CBD4	SET	2,H
CBD5	SET	2,L
CBD8	SET	3,B
CBDE	SET	3,(HL)
DDCB05DE	SET	3,(IX+d)
FDCB05DE	SET	3,(IY+d)
CBDF	SET	3,A
CBD9	SET	3,C
CBDA	SET	3,D
CBDB	SET	3,E
CBDC	SET	3,H
CBDD	SET	3,L
CBE6	SET	4,(HL)

OBJ CODE	SOURCE STATEMENT	
DDCB05E6	SET	4,(IX+d)
FDCB05E6	SET	4,(IY+d)
CBE7	SET	4,A
CBE0	SET	4,B
CBE1	SET	4,C
CBE2	SET	4,D
CBE3	SET	4,E
CBE4	SET	4,H
CBE5	SET	4,L
CBEE	SET	5,(HL)
DDCB05EE	SET	5,(IX+d)
FDCB05EE	SET	5,(IY+d)
CBEF	SET	5,A
CBE8	SET	5,B
CBE9	SET	5,C
CBEA	SET	5,D
CBEB	SET	5,E
CBEC	SET	5,H
CBED	SET	5,L
CBF6	SET	6,(HL)
DDCB05F6	SET	6,(IX+d)
FDCB05F6	SET	6,(IY+d)
CBF7	SET	6,A
CBF0	SET	6,B
CBF1	SET	6,C
CBF2	SET	6,D
CBF3	SET	6,E
CBF4	SET	6,H
CBF5	SET	6,L
CBFE	SET	7,(HL)
DDCB05FE	SET	7,(IX+d)
FDCB05FE	SET	7,(IY+d)
CBFF	SET	7,A
CBF8	SET	7,B
CBF9	SET	7,C
CBFA	SET	7,D
CBFB	SET	7,E
CBFC	SET	7,H
CBFD	SET	7,L
CB26	SLA	(HL)
DDCB0526	SLA	(IX+d)
FDCB0526	SLA	(IY+d)
CB27	SLA	A
CB20	SLA	B
CB21	SLA	C
CB22	SLA	D
CB23	SLA	E
CB24	SLA	H
CB25	SLA	L
CB2E	SRA	(HL)
DDCB052E	SRA	(IX+d)
FDCB052E	SRA	(IY+d)
CB2F	SRA	A
CB28	SRA	B
CB29	SRA	C
CB2A	SRA	D

OBJ CODE	SOURCE STATEMENT	
CB2B	SRA	E
CB2C	SRA	H
CB2D	SRA	L
CB3E	SRL	(HL)
DDCB053E	SRL	(IX+d)
FDCB053E	SRL	(IY+d)
CB3F	SRL	A
CB38	SRL	B
CB39	SRL	C
CB3A	SRL	D
CB3B	SRL	E
CB3C	SRL	H
CB3D	SRL	L
96	SUB	(HL)
DD9605	SUB	(IX+d)
FD9605	SUB	(IY+d)
97	SUB	A
90	SUB	B
91	SUB	C
92	SUB	D
93	SUB	E
94	SUB	H
95	SUB	L
D620	SUB	n
AE	XOR	(HL)
DDAE05	XOR	(IX+d)
FDAE05	XOR	(IY+d)
AF	XOR	A
A8	XOR	B
A9	XOR	C
AA	XOR	D
AB	XOR	E
AC	XOR	H
AD	XOR	L
EE20	XOR	n

(Courtesy of Zilog Inc.)

ภาคผนวก ข

การบันทึกโปรแกรมลงอีพรอม

ข.1 ส่วนประกอบ

เมื่อออกแบบโปรแกรมให้ซีพียูทำงานตามขั้นตอนได้แล้ว เราจะต้องทำการแปลงภาษาโปรแกรมจากภาษาแอสเซมบลี้ของ Z-80 ให้เป็นภาษาเครื่อง (Machine Code) โดยใช้ตารางคำสั่งของ Z-80 เมื่อทำการแปลงโปรแกรมเป็นภาษาเครื่องเรียบร้อยแล้ว จะต้องทำการบันทึกลงในอีพรอม ในการบันทึกโปรแกรมจะใช้อุปกรณ์ช่วยดังนี้

ก. เครื่องไมโครคอมพิวเตอร์ แอปเปิ้ล II พร้อมด้วยดิสท์ไดรพท์ (Disk-Drive)

ข. แผ่นวงจรบันทึกอีพรอม (Eprom-writer-card)

ข.2 ขั้นตอนการบันทึก

ขั้นตอนในการบันทึกโปรแกรมมีดังนี้

ก. เปิดเครื่องไมโครคอมพิวเตอร์

ข. ใช้คำสั่ง Call-151 เพื่อให้เครื่องไมโครคอมพิวเตอร์แอปเปิ้ล II เข้าสู่โหมดมอนิเตอร์ (Monitor Mode)

ค. เมื่อเครื่องเข้าสู่โหมามอนิเตอร์แล้ว ให้กำหนดช่วงแอดเดรสของแรมในเครื่องที่จะใช้สำหรับเก็บค่าเลขฐานสิบหกที่จะป้อนเข้าไป สมมติเริ่มต้นที่ 4000 แล้วให้ตามด้วยเครื่องหมาย : (Colon) ดังตัวอย่าง

* 4000 :

ง. ป้อนคำสั่งรหัส ฐานสิบหกครั้งละ 1 ไบท์ รหัส ฐานสิบหก 1 ไบท์ได้จากคำสั่งภาษาเครื่องของ Z-80 เช่น LD A,09H ซึ่งมี รหัสฐานสิบหกดังนี้ 3E 09 ดังตัวอย่าง

* 4000 : 3E 09

จ. เมื่อป้อนโปรแกรมครบแล้ว ให้ทำการรีเซ็ทเพื่อกลับสู่โหมดปกติ เพื่อทำการบันทึกลงอีพรอมหรือบันทึกลงแผ่นดิสท์เกตต์ (Diskette) ก็ได้ ถ้าต้องการเก็บโปรแกรมไว้ในดิสท์เกตต์ ต้องตั้งชื่อโปรแกรม แอดเดรสเริ่มต้น และความยาวของโปรแกรม ดังตัวอย่าง

]BSAVE PHA (4000) , A$ = 4000 , L$ = 1000

ฉ. เมื่อต้องการโหลดโปรแกรมจากแผ่นดิสท์เกตต์ ทำได้โดยคำสั่ง

] BLOAD PHA (4000)

ช. ในการบันทึกโปรแกรม ให้สอดแผ่นวงจรบันทึกอีพรอมลงในสล็อต (Slot) หมายเลข 4 พร้อมอีพรอม ใช้คำสั่ง]PR#4 จะพบข้อความ

MEMORY SIZE ?

1. 2708 or 2508
2. 2716 or 2516
3. 2732 or 2532
4. 2764 or 2564

ซ. ให้เลือกหมายเลข 2 ตามเบอร์ไอซีของอีพรอม จะพบข้อความ

ROM CHECK OK

MODE ?

1. READ
2. WRITE
3. COPY
4. MONITOR

ฌ. ให้เลือกหมายเลข 2 เพราะต้องการบันทึกโปรแกรม จะพบข้อความ

START ADDRESS ?

ให้ป้อนแอดเดรส 4000 จะพบข้อความ

SW ON

ให้ทำการเปิดสวิทซ์ที่แผ่นวงจรบันทึกอีพรอม จากนั้นจะเริ่มทำการบันทึกข้อมูลทันทีเริ่มจาก 0000-07FF

ญ. เมื่อพบข้อความ

VERIFY OK

SW OFF

ให้ปิดสวิทซ์ที่แผ่นวงจรบันทึกโปรแกรม นำอีพรอมออกจากแผ่นวงจรบันทึกโปรแกรมมาใช้งานได้ทันที

ภาคผนวก ค

ตัวอย่างการเขียนโปรแกรม

ค.1 ตัวอย่าง

```
START  LD   HL,2000H  ;  กำหนดบัฟเฟอร์เก็บอักษรที่จะแสดงผล
       LD   (HL),CEH  ;  อักษร P
       INC  HL        ;  แสดงผลที่ดิจิท dg2
       LD   (HL),0AH  ;  อักษร R
       INC  HL        ;  แสดงผลที่ดิจิท dg3
       LD   (HL),3AH  ;  อักษร O
       INC  HL        ;  แสดงผลที่ดิจิท dg4
       LD   (HL),9CH  ;  อักษร C
       INC  HL        ;  แสดงผลที่ดิจิท dg5
       LD   (HL),9EH  ;  อักษร E
       INC  HL        ;  แสกงผลที่ดิจิท dg6
       LD   (HL),B6H  ;  อักษร S
       INC  HL        ;  แสดงผลที่ดิจิท dg7
       LD   (HL),B6H  ;  อักษร S
       INC  HL        ;  แสดงผลที่ดิจิท dg8
       LD   (HL),3AH  ;  อักษร O
       INC  HL        ;  แสดงผลที่ดิจิท dg9
       LD   (HL),0AH  ;  อักษร R
```

ค.2 ตัวอย่าง

```
       CALL KEYDISP   ;  เรียกซับรูทีนสแกนคีย์บอร์ด
       LD   A,(2014H) ;  เก็บ รหัส ของคีย์ที่กด
       LD   B, 18H    ;  รหัสของคีย์ TIME
```

```
        CP    B          ;  ตรวจสอบคีย์ว่าเป็นชนิดเดียวกันหรือไม่
        JR    NZ,SLZ     ;  ถ้าไม่ใช่คีย์ TIME ให้ไปทดสอบหาคีย์อื่นต่อไป
        CALL  TIME       ;  คีย์ที่กดคือคีย์ TIME ให้ไปทำงานที่ซับรูทีน TIME
SL2     ---   ---
        ---   ---
        ---   ---
```

ค.3 ตัวอย่าง

```
        LD    HL,2018H   ;  ค่าตัวเลขจากบัฟเฟอร์
        LD    IX,1400H   ;  แอดเดรสเก็บค่าตัวเลขลำดับสูง
        CALL  TIMEADD    ;  ซับรูทีนบวกค่าเวลา
        DEC   HL         ;  ค่าตัวเลขลำดับต่ำจากบัฟเฟอร์
        LD    IX,1000H   ;  แอดเดรสเก็บค่าตัวเลขลำดับต่ำ
        CALL  TIMEADD    ;  ซับรูทีนบวกค่าเวลา
        CALL  KEYDISP    ;  สแกนหาคีย์ตัวต่อไป
```

ค.4 ตัวอย่าง

```
        LD    (1000H),A  ;  เก็บค่าของรีจิสเตอร์ A ลงในแรม U2-
        LD    (1400H),A  ;  ที่แอดเดรส 1000 และ 1400
```

ค.5 ตัวอย่าง

```
        XOR   A          ;  เคลียร์ค่ารีจิสเตอร์ให้เป็น " Ø "
        OUT   (7),A      ;  ส่งค่าลอจิก " Ø " ออกไปที่พอร์ทหมายเลข 7
```

ค.6 ตัวอย่าง

```
        LD    HL,2000H   ;  กำหนดค่าบัฟเฟอร์
        LD    (HL),CEH   ;  อักษร P
        LD    A,(HL)     ;  เก็บอักษร P เตรียมแสดงผล
        OUT   (1),A      ;  แสดงผล P และ U11 แอคตีฟ
        XOR   A          ;  ต้องการใช้พอร์ทหมายเลข 0
```

```
        OUT   (0),A     ; U12 และ U8 แอคตีฟ Y1 ของ U8 แอคตีฟ
                        ; ให้ไดโอดเปล่งแสงหลักซ้ายมือสุดทำงาน
```

ค.7 ตัวอย่าง

```
KEYDISP LD IY,COLTAB    ; กำหนดค่าสำหรับสแกนคีย์บอร์ดแนวตั้ง
        LD B,Ø5H        ; จะสแกนแนวตั้งของคีย์บอร์ด 5 แนว
KDP2    LD A,(IY +Ø)    ; เริ่มสแกน
        OUT (Ø),A       ; ที่พอร์ทหมายเลข ø
KDP1    IN  A,(3)       ; อ่านค่าที่ได้จากการสแกน
        AND A,ØFH       ; หาค่าที่ได้จากการสแกน
        CP  A,ØFH       ; มีการกดคีย์หรือไม่
        JR  NZ,KDP1     ; ไม่มีการกดคีย์ ให้ตรวจสอบใหม่
        INC IY          ; มีการกดคีย์ ให้สแกนแนวตั้งแนวถัดไป
        DJNZ KDP2       ; เริ่มสแกนใหม่
```

ค.8 ตัวอย่าง

```
CLICK  LD   DE,(2Ø12H) ; กำหนดความยาวเสียง
       INC  D          ;
CYCLE  LD   A,Ø1H      ; ให้เสียงออกลำโพงนานชั่วขณะ
       OUT  (Ø),A      ;
       LD   A,(2Ø1ØH)  ;
       LD   B,A        ;
LENG1  BIT  Ø,(IX)     ;
       DEC  B          ;
       JR   NZ,LENG1   ;
       XOR  A          ; หยุดการให้เสียงออกลำโพงชั่วขณะ
       OUT  (Ø),A      ;
       LD   A,(2Ø1ØH)  ;
       LD   B,A        ;
```

```
LENG2  BIT  Ø,(IX)      ;
       DEC  B           ;
       JR   NZ,LENG2    ;
       DEC  DE          ;  ตรวจสอบหมดความยาวเสียง
       XOR  A           ;
       CP   D           ;
       JR   NZ,CYCLE    ;  ถ้ายังไม่สิ้นสุดให้เริ่มใหม่
       RET              ;  กลับสู่โปรแกรมหลัก
```

ภาคผนวก ง

ตารางแสดง รหัสประจำคีย์และหน้าที่

ง.1 ตารางแสดงรหัส

คีย์	รหัส ฐานสิบหก	คีย์	รหัส ฐานสิบหก	คีย์	รหัส ฐานสิบหก
TIM	18	TAPWR	2A	3	16
RUNADD	28	SCP	3A	4	22
RUNSUB	38	BRK	-	5	24
ADR	48	RST	-	6	26
INC	46	0	42	7	32
DEC	44	1	12	8	34
TAPRD	1A	2	14	9	36

ง.2 หน้าที่ของคีย์ฟังก์ชั่น

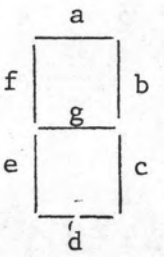
TIM	ตั้งเวลาในการวิเคราะห์
RUNADD	ทำการวิเคราะห์แบบเพิ่มจำนวนนับ
RUNSUB	ทำการวิเคราะห์แบบลดจำนวนนับ
ADR	กำหนดค่าซันแนลแอดเดรส
INC	เพิ่มค่าซันแนลแอดเดรสขึ้นอีกหนึ่งตำแหน่ง
DEC	ลดค่าซันแนลแอดเดรสลงจากเดิมหนึ่งตำแหน่ง
TAPRD	อ่านข้อมูลจากเทปคาสเซทท์
TAPWR	บันทึกข้อมูลลงเทปคาสเซทท์
SCP	แสดงผลบนออสซิลโลสโคป
BRK	หยุดการแสดงผลบนออสซิลโลสโคป
RST	รีเซ็ทระบบ

ภาคผนวก จ

การแสดงผลที่ไดโอดเปล่งแสง 7 ส่วน

จ.1 รูปแบบ

b_0	b_1	b_2	b_3	b_4	b_5	b_6	b_7
a	b	c	d	e	f	g	dp



จ.2 ตารางแสดงรหัส เลขฐานสิบหกที่ใช้แทนตัวอักษรและตัวเลข

ตัวอักษร	รหัส	ตัวอักษร	รหัส	ตัวอักษร	รหัส
A	EE	M	2A	Y	76
B	3E	N	-	Z	-
C	9C	O	3A	0	FC
D	7A	P	CE	1	60
E	9E	Q	-	2	DA
F	8E	R	OA	3	F2
G	E6	S	B6	4	66
H	6E	T	1E	5	D6
I	20	U	C6	6	BE
J	70	V	-	7	EØ
K	-	W	-	8	FØ
L	1C	X	-	9	F6

ภาคผนวก ฉ

รายการอุปกรณ์

รายการอุปกรณ์	จำนวน (ตัว)
Z-80	1
2716	1
6116	2
74LS138	6
74LS04	2
7400	1
74LS373	9
LM324	2
7490	6
7805	1
7905	1
7474	1
X-TAL 2 MHZ	1
IN4148	3
R 1 KΩ 0.5 W	9
R 10 KΩ 0.5 W	14
R 100 Ω 0.5 W	2
R 22 KΩ 0.5 W	1
R 500 Ω 0.5 W	1
R 25 KΩ 0.5 W	2
R 12 KΩ 0.5 W	2
R 6.8 KΩ 0.5 W	2

รายการอุปกรณ์	จำนวน (ตัว)
R 3.3 KΩ 0.5 W	2
R 1.5 KΩ 0.5 W	2
R 820 Ω 0.5 W	2
R 390 Ω 0.5 W	2
R 200 Ω 0.5 W	2
R 8.8 MΩ 0.5 W	11
R 3.3 MΩ 0.5 W	1
R 1.6 MΩ 0.5 W	1
R 820 KΩ 0.5 W	1
R 340 KΩ 0.5 W	1
R 200 KΩ 0.5 W	1
R 100 KΩ 0.5 W	1
R 50 KΩ 0.5 W	1
C 10 µF 16 V อีเล็คโตรไลท์	1
C 0.1 µF แทนทาลัม	25
C 0.05 µF เซอรามิค	2
C 2200 µF 25 V. อีเล็คโตรไลท์	2
หม้อแปลง 220/9-0-9 V 2A	1
คีย์สวิทช์	21
ไดโอดเปล่งแสง 7 ส่วน ชนิดแคโถดร่วม	9
แจ๊คเสียบเทปคาสเซทท์	2
แจ๊ค BNC สำหรับออสซิลโลสโคป	2
แจ๊คเสียบบัสข้อมูล	1
สวิทช์เลือก(Selector Switch)	1
สายไฟ , กระบอกฟิวส์ , ลูกยาง	1

ภาคผนวก ช

ข้อมูล วงจรรวม

Z80®-CPU
Z80A-CPU

Product Specification

MARCH 1978

The Zilog Z80 product line is a complete set of microcomputer components, development systems and support software. The Z80 microcomputer component set includes all of the circuits necessary to build high-performance microcomputer systems with virtually no other logic and a minimum number of low cost standard memory elements.

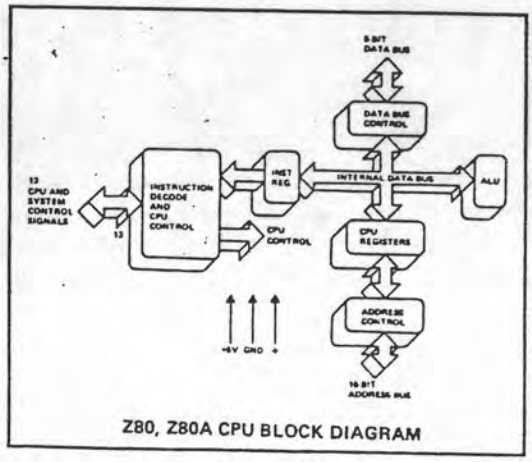
The Z80 and Z80A CPU's are third generation single chip microprocessors with unrivaled computational power. This increased computational power results in higher system through-put and more efficient memory utilization when compared to second generation microprocessors. In addition, the Z80 and Z80A CPU's are very easy to implement into a system because of their single voltage requirement plus all output signals are fully decoded and timed to control standard memory or peripheral circuits. The circuit is implemented using an N-channel, ion implanted, silicon gate MOS process.

Figure 1 is a block diagram of the CPU, Figure 2 details the internal register configuration which contains 208 bits of Read/Write memory that are accessible to the programmer. The registers include two sets of six general purpose registers that may be used individually as 8-bit registers or as 16-bit register pairs. There are also two sets of accumulator and flag registers. The programmer has access to either set of main or alternate registers through a group of exchange instructions. This alternate set allows foreground/background mode of operation or may be reserved for very fast Interrupt response. Each CPU also contains a 16-bit stack pointer which permits simple implementation of multiple level interrupts, unlimited subroutine nesting and simplification of many types of data handling.

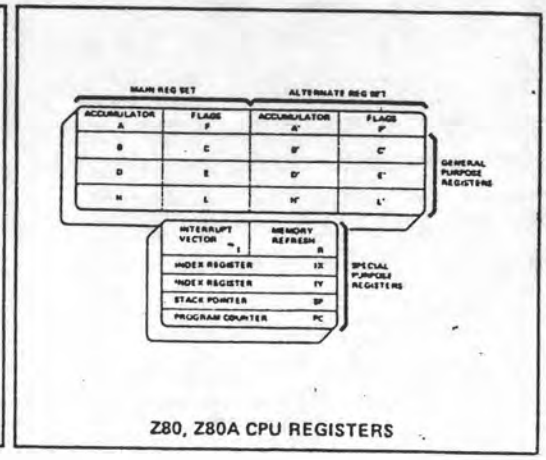
The two 16-bit index registers allow tabular data manipulation and easy implementation of relocatable code. The Refresh register provides for automatic, totally transparent refresh of external dynamic memories. The I register is used in a powerful interrupt response mode to form the upper 8 bits of a pointer to a interrupt service address table, while the interrupting device supplies the lower 8 bits of the pointer. An indirect call is then made to this service address.

FEATURES

- Single chip, N-channel Silicon Gate CPU.
- 158 instructions--includes all 78 of the 8080A instructions with total software compatibility. New instructions include 4-, 8- and 16-bit operations with more useful addressing modes such as indexed, bit and relative.
- 17 internal registers.
- Three modes of fast interrupt response plus a non-maskable interrupt.
- Directly interfaces standard speed static or dynamic memories with virtually no external logic.
- 1.0 μs instruction execution speed.
- Single 5 VDC supply and single-phase 5 volt Clock.
- Out-performs any other single chip microcomputer in 4-, 8-, or 16-bit applications.
- All pins TTL Compatible
- Built-in dynamic RAM refresh circuitry.

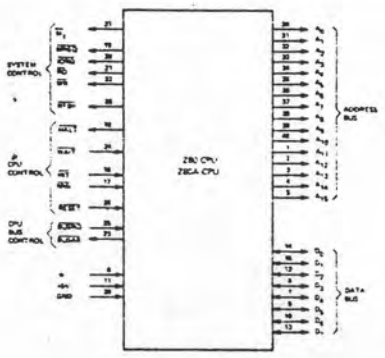


Z80, Z80A CPU BLOCK DIAGRAM



Z80, Z80A CPU REGISTERS

Z80, Z80A-CPU Pin Description



Z80, Z80A CPU PIN CONFIGURATION

A_0-A_{15} (Address Bus) Tri-state output, active high. A_0-A_{15} constitute a 16-bit address bus. The address bus provides the address for memory (up to 64K bytes) data exchanges and for I/O device data exchanges.

D_0-D_7 (Data Bus) Tri-state input/output, active high. D_0-D_7 constitute an 8-bit bidirectional data bus. The data bus is used for data exchanges with memory and I/O devices.

$\overline{M_1}$ (Machine Cycle one) Output, active low. $\overline{M_1}$ indicates that the current machine cycle is the OP code fetch cycle of an instruction execution.

$\overline{MREQ}$ (Memory Request) Tri-state output, active low. The memory request signal indicates that the address bus holds a valid address for a memory read or memory write operation.

$\overline{IORQ}$ (Input/ Output Request) Tri-state output, active low. The $\overline{IORQ}$ signal indicates that the lower half of the address bus holds a valid I/O address for a I/O read or write operation. An $\overline{IORQ}$ signal is also generated when an interrupt is being acknowledged to indicate that an interrupt response vector can be placed on the data bus.

$\overline{RD}$ (Memory Read) Tri-state output, active low. $\overline{RD}$ indicates that the CPU wants to read data from memory or an I/O device. The addressed I/O device or memory should use this signal to gate data onto the CPU data bus.

$\overline{WR}$ (Memory Write) Tri-state output, active low. $\overline{WR}$ indicates that the CPU data bus holds valid data to be stored in the addressed memory or I/O device.

$\overline{RFSH}$ (Refresh) Output, active low. $\overline{RFSH}$ indicates that the lower 7 bits of the address bus contain a refresh address for dynamic memories and the current $\overline{MREQ}$ signal should be used to do a refresh read to all dynamic memories.

$\overline{HALT}$ (Halt state) Output, active low. $\overline{HALT}$ indicates that the CPU has executed a HALT software instruction and is awaiting either a non-maskable or a maskable interrupt (with the mask enabled) before operation can resume. While halted, the CPU executes NOP's to maintain memory refresh activity.

$\overline{WAIT}$ (Wait) Input, active low. $\overline{WAIT}$ indicates to the Z-80 CPU that the addressed memory or I/O devices are not ready for a data transfer. The CPU continues to enter wait states for as long as this signal is active.

$\overline{INT}$ (Interrupt Request) Input, active low. The Interrupt Request signal is generated by I/O devices. A request will be honored at the end of the current instruction if the internal software controlled interrupt enable flip-flop (IFF) is enabled.

$\overline{NMI}$ (Non Maskable Interrupt) Input, active low. The non-maskable nterrupt request line has a higher priority than $\overline{INT}$ and is always recognized at the end of the current instruction, independent of the status of the interrupt enable flip-flop. $\overline{NMI}$ automatically forces the Z-80 CPU to restart to location 0066_H.

$\overline{RESET}$ Input, active low. $\overline{RESET}$ initializes the CPU as follows: reset interrupt enable flip-flop, clear PC and registers I and R and set interrupt to 8080A mode. During reset time, the address and data bus go to a high impedance state and all control output signals go to the inactive state.

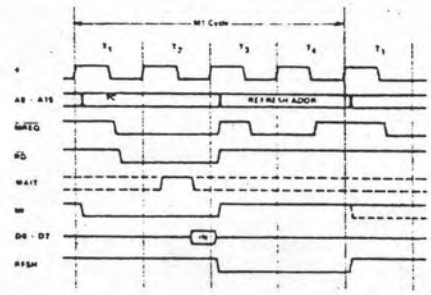
$\overline{BUSRQ}$ (Bus Request) Input, active low. The bus request signal has a higher priority than $\overline{NMI}$ and is always recognized at the end of the current machine cycle and is used to request the CPU address bus, data bus and tri-state output control signals to go to a high impedance state so that other devices can control these busses.

$\overline{BUSAK}$ (Bus Acknowledge) Output, active low. Bus acknowledge is used to indicate to the requesting device that the CPU address bus, data bus and tri-state control bus signals have been set to their high impedance state and the external device can now control these signals.

Timing Waveforms

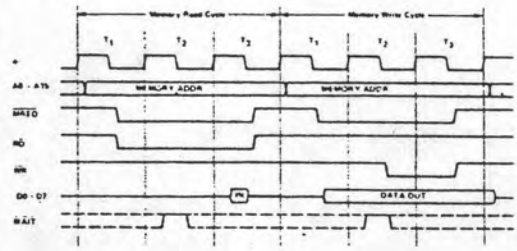
INSTRUCTION OP CODE FETCH

The program counter content (PC) is placed on the address bus immediately at the start of the cycle. One half clock time later $\overline{MREQ}$ goes active. The falling edge of $\overline{MREQ}$ can be used directly as a chip enable to dynamic memories. $\overline{RD}$ when active indicates that the memory data should be enabled onto the CPU data bus. The CPU samples data with the rising edge of the clock state T_3. Clock states T_3 and T_4 of a fetch cycle are used to refresh dynamic memories while the CPU is internally decoding and executing the instruction. The refresh control signal $\overline{RFSH}$ indicates that a refresh read of all dynamic memories should be accomplished.



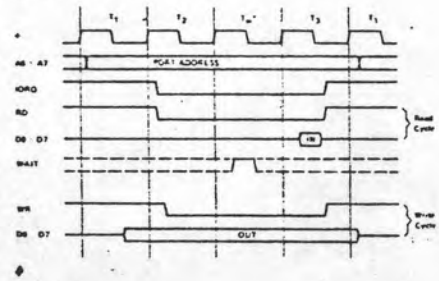
MEMORY READ OR WRITE CYCLES

Illustrated here is the timing of memory read or write cycles other than an OP code fetch (M_1 cycle). The $\overline{MREQ}$ and $\overline{RD}$ signals are used exactly as in the fetch cycle. In the case of a memory write cycle, the $\overline{MREQ}$ also becomes active when the address bus is stable so that it can be used directly as a chip enable for dynamic memories. The $\overline{WR}$ line is active when data on the data bus is stable so that it can be used directly as a R/W pulse to virtually any type of semiconductor memory.



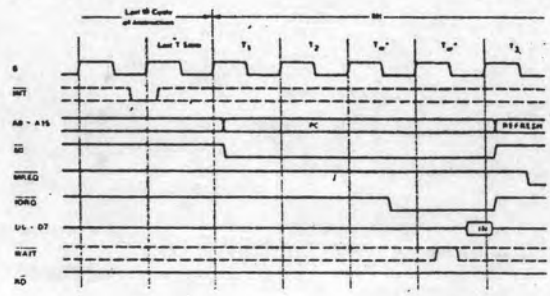
INPUT OR OUTPUT CYCLES

Illustrated here is the timing for an I/O read or I/O write operation. Notice that during I/O operations a single wait state is automatically inserted (Tw*). The reason for this is that during I/O operations this extra state allows sufficient time for an I/O port to decode its address and activate the $\overline{WAIT}$ line if a wait is required.



INTERRUPT REQUEST/ACKNOWLEDGE CYCLE

The interrupt signal is sampled by the CPU with the rising edge of the last clock at the end of any instruction. When an interrupt is accepted, a special M_1 cycle is generated. During this M_1 cycle, the $\overline{IORQ}$ signal becomes active (instead of $\overline{MREQ}$) to indicate that the interrupting device can place an 8-bit vector on the data bus. Two wait states (Tw*) are automatically added to this cycle so that a ripple priority interrupt scheme, such as the one used in the Z80 peripheral controllers, can be easily implemented.



A.C. Characteristics Z80-CPU

T_A = 0°C to 70°C, Vcc = +5V ± 5%, Unless Otherwise Noted.

Signal	Symbol	Parameter	Min	Max	Unit	Test Condition	
Φ	t_c	Clock Period	4	1121	μsec		[12] $t_c = t_{w(\Phi H)} + t_{w(\Phi L)} + t_r + t_f$
	$t_{w(\Phi H)}$	Clock Pulse Width, Clock High	180	[E]	nsec		
	$t_{w(\Phi L)}$	Clock Pulse Width, Clock Low	180	2000	nsec		
	$t_{r,f}$	Clock Rise and Fall Time		30	nsec		
A_{0-15}	$t_{D(AD)}$	Address Output Delay		145	nsec	C_L = 50pF	
	$t_{F(AD)}$	Delay to Float		110	nsec		
	t_{acm}	Address Stable Prior to MREQ (Memory Cycle)	111		nsec		[1] $t_{acm} = t_{w(\Phi H)} + t_f - 75$
	t_{aci}	Address Stable Prior to IORQ, RD or WR (I/O Cycle)	121		nsec		[2] $t_{aci} = t_c - 80$
	t_{ca}	Address Stable from RD, WR, IORQ or MREQ	131		nsec		[3] $t_{ca} = t_{w(\Phi L)} + t_r - 40$
	t_{caf}	Address Stable From RD or WR During Float	141		nsec		[4] $t_{caf} = t_{w(\Phi L)} + t_r - 50$
D_{0-7}	$t_{D(D)}$	Data Output Delay		230	nsec	C_L = 50pF	[5] $t_{dcm} = t_c - 210$
	$t_{F(D)}$	Delay to Float During Write Cycle		90	nsec		[6] $t_{dci} = t_{w(\Phi L)} + t_r - 210$
	$t_{S\Phi(D)}$	Data Setup Time to Rising Edge of Clock During M1 Cycle	50		nsec		[7] $t_{cdf} = t_{w(\Phi L)} + t_r - 80$
	$t_{S\overline{\Phi}(D)}$	Data Setup Time to Falling Edge of Clock During M2 to M5	60		nsec		
	t_{dcm}	Data Stable Prior to WR (Memory Cycle)	151		nsec		
	t_{dci}	Data Stable Prior to WR (I/O Cycle)	161		nsec		
	t_{cdf}	Data Stable From WR	171				
	t_H	Any Hold Time for Setup Time	0		nsec		
MREQ	$t_{DL\overline{\Phi}(MR)}$	MREQ Delay From Falling Edge of Clock, MREQ Low		100	nsec	C_L = 50pF	[8] $t_{w(MRL)} = t_c - 40$
	$t_{DH\Phi(MR)}$	MREQ Delay From Rising Edge of Clock, MREQ High		100	nsec		[9] $t_{w(MRH)} = t_{w(\Phi H)} + t_f - 30$
	$t_{DH\overline{\Phi}(MR)}$	MREQ Delay From Falling Edge of Clock, MREQ High		100	nsec		
	$t_{w(MRL)}$	Pulse Width, MREQ Low	151		nsec		
	$t_{w(MRH)}$	Pulse Width, MREQ High	191		nsec		
IORQ	$t_{DL\Phi(IR)}$	IORQ Delay From Rising Edge of Clock, IORQ Low		90	nsec	C_L = 50pF	
	$t_{DL\overline{\Phi}(IR)}$	IORQ Delay From Falling Edge of Clock, IORQ Low		110	nsec		
	$t_{DH\Phi(IR)}$	IORQ Delay From Rising Edge of Clock, IORQ High		100	nsec		
	$t_{DH\overline{\Phi}(IR)}$	IORQ Delay From Falling Edge of Clock, IORQ High		110	nsec		
RD	$t_{DL\Phi(RD)}$	RD Delay From Rising Edge of Clock, RD Low		100	nsec	C_L = 50pF	
	$t_{DL\overline{\Phi}(RD)}$	RD Delay From Falling Edge of Clock, RD Low		130	nsec		
	$t_{DH\Phi(RD)}$	RD Delay From Rising Edge of Clock, RD High		100	nsec		
	$t_{DH\overline{\Phi}(RD)}$	RD Delay From Falling Edge of Clock, RD High		110	nsec		
WR	$t_{DL\Phi(WR)}$	WR Delay From Rising Edge of Clock, WR Low		80	nsec	C_L = 50pF	
	$t_{DL\overline{\Phi}(WR)}$	WR Delay From Falling Edge of Clock, WR Low		90	nsec		
	$t_{DH\overline{\Phi}(WR)}$	WR Delay From Falling Edge of Clock, WR High		100	nsec		
	$t_{w(WRL)}$	Pulse Width, WR Low	1101		nsec		[10] $t_{w(WRL)} = t_c - 40$
M1	$t_{DL(M1)}$	M1 Delay From Rising Edge of Clock, M1 Low		130	nsec	C_L = 50pF	
	$t_{DH(M1)}$	M1 Delay From Rising Edge of Clock, M1 High		130	nsec		
RFSH	$t_{DL(RF)}$	RFSH Delay From Rising Edge of Clock, RFSH Low		180	nsec	C_L = 50pF	
	$t_{DH(RF)}$	RFSH Delay From Rising Edge of Clock, RFSH High		150	nsec		
WAIT	$t_{s(WT)}$	WAIT Setup Time to Falling Edge of Clock	70		nsec		
HALT	$t_{D(HT)}$	HALT Delay Time From Falling Edge of Clock		300	nsec	C_L = 50pF	
INT	$t_{s(IT)}$	INT Setup Time to Rising Edge of Clock	80		nsec		
NMI	$t_{w(NML)}$	Pulse Width, NMI Low	80		nsec		
BUSRQ	$t_{s(BQ)}$	BUSRQ Setup Time to Rising Edge of Clock	80		nsec		
BUSAK	$t_{DL(BA)}$	BUSAK Delay From Rising Edge of Clock, BUSAK Low		120	nsec	C_L = 50pF	
	$t_{DH(BA)}$	BUSAK Delay From Falling Edge of Clock, BUSAK High		110	nsec		
RESET	$t_{s(RS)}$	RESET Setup Time to Rising Edge of Clock	90		nsec		
	$t_{F(C)}$	Delay to Float (MREQ, IORQ, RD and WR)		100	nsec		
	t_{mr}	M1 Stable Prior to IORQ (Interrupt Ack.)	1111		nsec		[11] $t_{mr} = 2t_c + t_{w(\Phi H)} + t_f - 80$

NOTES

A. Data should be enabled onto the CPU data bus when RD is active. During interrupt acknowledge data should be enabled when M1 and IORQ are both active.

B. All control signals are internally synchronized, so they may be totally asynchronous with respect to the clock.

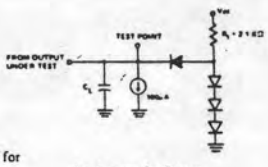
C. The RESET signal must be active for a minimum of 3 clock cycles.

D. Output Delay vs. Loaded Capacitance

TA = 70°C, Vcc = +5V ±5%

Add 10nsec delay for each 50pf increase in load up to a maximum of 200pf for the data bus & 100pf for address & control lines

† Although static by design, testing guarantees $t_{w(\Phi H)}$ of 200 μsec maximum

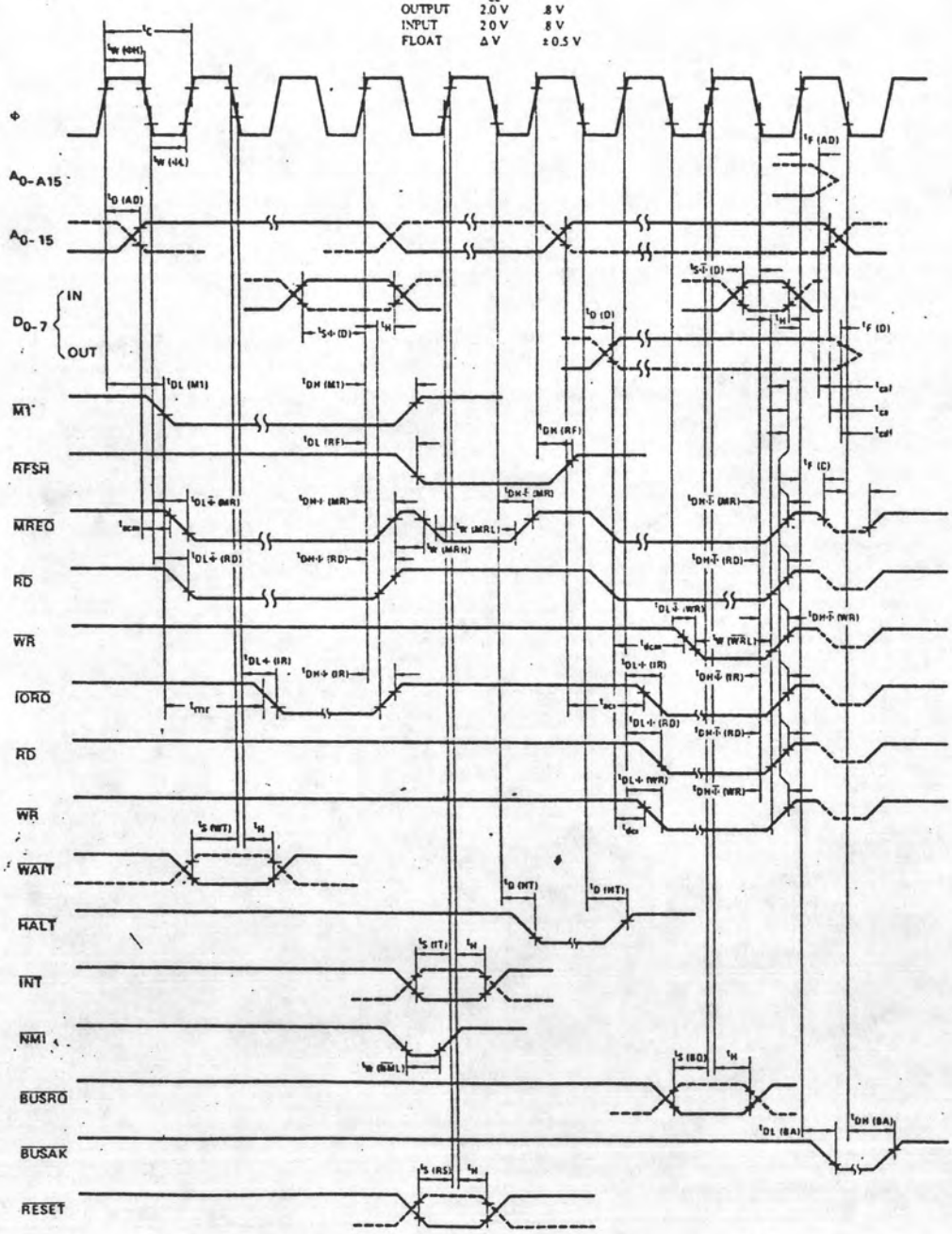


Load circuit for Output

A.C. Timing Diagram

Timing measurements are made at the following voltages, unless otherwise specified:

	"1"	"0"
CLOCK	V_{CC} -.6V	.45V
OUTPUT	2.0 V	.8 V
INPUT	2.0 V	.8 V
FLOAT	Δ V	±0.5 V



Absolute Maximum Ratings

Temperature Under Bias	Specified operating range.
Storage Temperature	-65°C to +150°C
Voltage On Any Pin with Respect to Ground	-0.3V to +7V
Power Dissipation	1.5W

*Comment

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: For Z80-CPU all AC and DC characteristics remain the same for the military grade parts except I_{CC}.

I_{CC} = 200 mA

Z80-CPU D.C. Characteristics

T_A = 0°C to 70°C, V_{CC} = 5V ± 5% unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Condition
V_{ILC}	Clock Input Low Voltage	-0.3		0.45	V	
V_{IHC}	Clock Input High Voltage	V_{CC} -.6		V_{CC}+.3	V	
V_{IL}	Input Low Voltage	-0.3		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC}	V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL}=1.8mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -250μA
I_{CC}	Power Supply Current			150	mA	
I_{LI}	Input Leakage Current			10	μA	V_{IN}=0 to V_{CC}
I_{LOH}	Tri-State Output Leakage Current in Float			10	μA	V_{OUT}=2.4 to V_{CC}
I_{LOL}	Tri-State Output Leakage Current in Float			-10	μA	V_{OUT}=0.4V
I_{LD}	Data Bus Leakage Current in Input Mode			±10	μA	$0 \leq V_{IN} \leq V_{CC}$

Capacitance

T_A = 25°C, f = 1 MHz,
unmeasured pins returned to ground

Symbol	Parameter	Max.	Unit
C_ϕ	Clock Capacitance	35	pF
C_{IN}	Input Capacitance	5	pF
C_{OUT}	Output Capacitance	10	pF

Z80-CPU Ordering Information

C – Ceramic
P – Plastic
S – Standard 5V ±5% 0° to 70°C
E – Extended 5V ±5% -40° to 85°C
M – Military 5V ±10% -55° to 125°C

Z80A-CPU D.C. Characteristics

T_A = 0°C to 70°C, V_{CC} = 5V ± 5% unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Condition
V_{ILC}	Clock Input Low Voltage	-0.3		0.45	V	
V_{IHC}	Clock Input High Voltage	V_{CC} -.6		V_{CC}+.3	V	
V_{IL}	Input Low Voltage	-0.3		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC}	V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL}=1.8mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -250μA
I_{CC}	Power Supply Current		90	200	mA	
I_{LI}	Input Leakage Current			10	μA	V_{IN}=0 to V_{CC}
I_{LOH}	Tri-State Output Leakage Current in Float			10	μA	V_{OUT}=2.4 to V_{CC}
I_{LOL}	Tri-State Output Leakage Current in Float			-10	μA	V_{OUT}=0.4V
I_{LD}	Data Bus Leakage Current in Input Mode			±10	μA	$0 \leq V_{IN} \leq V_{CC}$

Capacitance

T_A = 25°C, f = 1 MHz,
unmeasured pins returned to ground

Symbol	Parameter	Max.	Unit
C_ϕ	Clock Capacitance	35	pF
C_{IN}	Input Capacitance	5	pF
C_{OUT}	Output Capacitance	10	pF

Z80A-CPU Ordering Information

C – Ceramic
P – Plastic
S – Standard 5V ±5% 0° to 70°C

intel

2716*
16K (2K x 8) UV ERASABLE PROM

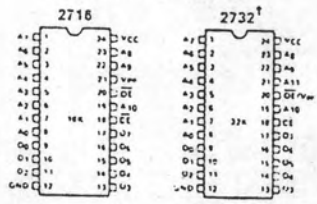
- Fast Access Time
  - 350 ns Max. 2716-1
  - 390 ns Max. 2716-2
  - 450 ns Max. 2716
  - 490 ns Max. 2716-5
  - 650 ns Max. 2716-6
- Single +5V Power Supply
- Low Power Dissipation
  - 525 mW Max. Active Power
  - 132 mW Max. Standby Power
- Pin Compatible to Intel® 2732 EPROM
- Simple Programming Requirements
  - Single Location Programming
  - Programs with One 50 ms Pulse
- Inputs and Outputs TTL Compatible during Read and Program
- Completely Static

The Intel® 2716 is a 16,384-bit ultraviolet erasable and electrically programmable read-only memory (EPROM). The 2716 operates from a single 5-volt power supply, has a static standby mode, and features fast single address location programming. It makes designing with EPROMs faster, easier and more economical.

The 2716, with its single 5-volt supply and with an access time up to 350 ns, is ideal for use with the newer high performance +5V microprocessors such as Intel's 8085 and 8086. A selected 2716-5 and 2716-6 is available for slower speed applications. The 2716 is also the first EPROM with a static standby mode which reduces the power dissipation without increasing access time. The maximum active power dissipation is 525 mW while the maximum standby power dissipation is only 132 mW, a 75% savings.

The 2716 has the simplest and fastest method yet devised for programming EPROMs – single pulse TTL level programming. No need for high voltage pulsing because all programming controls are handled by TTL signals. Program any location at any time—either individually, sequentially or at random, with the 2716's single address location programming. Total programming time for all 16,384 bits is only 100 seconds.

PIN CONFIGURATION



†Refer to 2732 data sheet for specifications

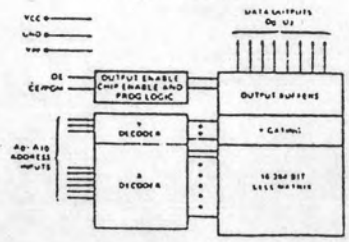
PIN NAMES

A_0 - A_{10}	ADDRESSES
$\overline{CE}/\overline{PGM}$	CHIP ENABLE/PROGRAM
$\overline{OE}$	OUTPUT ENABLE
O_0 - O_7	OUTPUTS

MODE SELECTION

MODE \ PINS	$\overline{CE}/\overline{PGM}$ (18)	$\overline{OE}$ (20)	V_{PP} (21)	V_{CC} (24)	OUTPUTS (9-11, 13-17)
Read	V_{IL}	V_{IL}	+5	+5	D_{OUT}
Standby	V_{IH}	Don't Care	+5	+5	High Z
Program	Pulsed V_{IL} to V_{IH}	V_{IH}	+25	+5	D_{IN}
Program Verify	V_{IL}	V_{IL}	+25	+5	D_{OUT}
Program Inhibit	V_{IL}	V_{IH}	+25	+5	High Z

BLOCK DIAGRAM



PROGRAMMING

The programming specifications are described in the Data Catalog PROM/ROM Programming Instructions Section.

Absolute Maximum Ratings*

Temperature Under Bias	-10°C to +80°C
Storage Temperature	-65°C to +125°C
All Input or Output Voltages with Respect to Ground	+6V to -0.3V
V_{PP} Supply Voltage with Respect to Ground During Program	+26.5V to -0.3V

*COMMENT. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC and AC Operating Conditions During Read

	2716	2716-1	2716-2	2716-5	2716-6
Temperature Range	0°C – 70°C	0°C – 70°C	0°C – 70°C	0°C – 70°C	0°C – 70°C
V_{CC} Power Supply[1,2]	5V ±5%	5V ±10%	5V ±5%	5V ±5%	5V ±5%
V_{PP} Power Supply[2]	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}

READ OPERATION

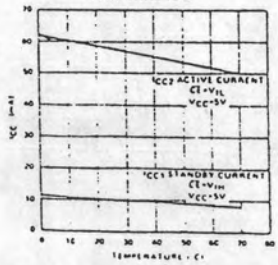
D.C. and Operating Characteristics

Symbol	Parameter	Limits Min	Limits Typ.[3]	Limits Max.	Unit	Conditions
I_{LI}	Input Load Current			10	μA	V_{IN} = 5.25V
I_{LO}	Output Leakage Current			10	μA	V_{OUT} = 5.25V
I_{PP1}[2]	V_{PP} Current			5	mA	V_{PP} = 5.25V
I_{CC1}[2]	V_{CC} Current (Standby)		10	25	mA	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL}
I_{CC2}[2]	V_{CC} Current (Active)		57	100	mA	$\overline{OE}$ = $\overline{CE}$ = V_{IL}
V_{IL}	Input Low Voltage	-0.1		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC}+1	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -400 μA

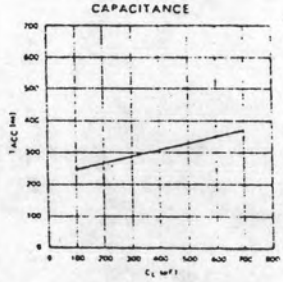
NOTES: 1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. V_{PP} may be connected directly to V_{CC} except during programming. The supply current would then be the sum of I_{CC} and I_{PP1}.
3. Typical values are for T_A = 25°C and nominal supply voltages.
4. This parameter is only sampled and is not 100% tested.

Typical Characteristics

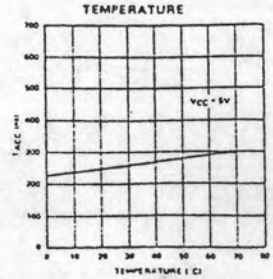
I_{CC} CURRENT vs. TEMPERATURE



ACCESS TIME vs. CAPACITANCE



ACCESS TIME vs. TEMPERATURE



A.C. Characteristics

Symbol	Parameter	Limits (ns)										Test Conditions
		2716		2716-1		2716-2		2716-5		2716-6		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{ACC}	Address to Output Delay		450		350		390		450		450	$\overline{CE} = \overline{OE} = V_{IL}$
t_{CE}	$\overline{CE}$ to Output Delay		450		350		390		490		650	$\overline{OE} = V_{IL}$
t_{OE}	Output Enable to Output Delay		120		120		120		160		200	$\overline{CE} = V_{IL}$
t_{DF}	Output Enable High to Output Float	0	100	0	100	0	100	0	100	0	100	$\overline{CE} = V_{IL}$
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First	0		0		0		0		0		$\overline{CE} = \overline{OE} = V_{IL}$

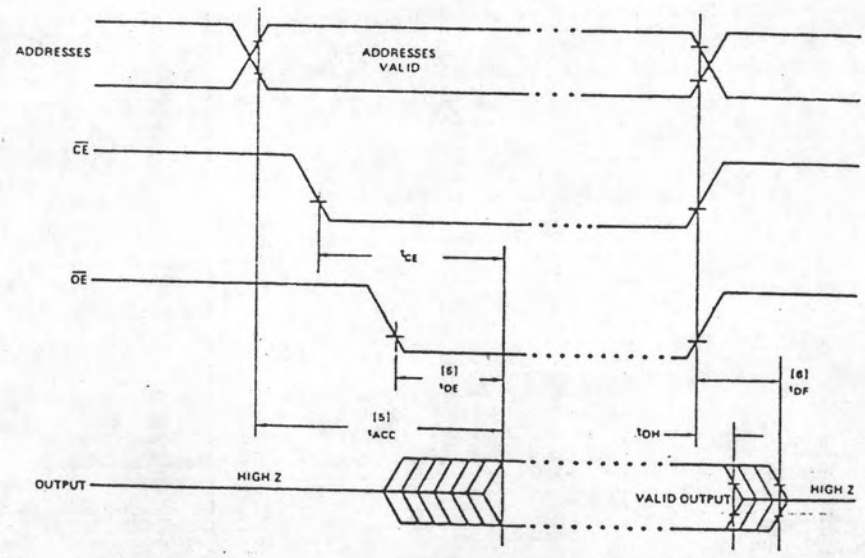
Capacitance [4] $T_A = 25°C$, f = 1 MHz

Symbol	Parameter	Typ.	Max.	Unit	Conditions
C_{IN}	Input Capacitance	4	6	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance	8	12	pF	$V_{OUT} = 0V$

A.C. Test Conditions:

Output Load: 1 TTL gate and $C_L = 100$ pF
Input Rise and Fall Times: ≤20 ns
Input Pulse Levels: 0.8V to 2.2V
Timing Measurement Reference Level:
Inputs 1V and 2V
Outputs 0.8V and 2V

A. C. Waveforms [1]



NOTE:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. V_{PP} may be connected directly to V_{CC} except during programming. The supply current would then be the sum of I_{CC} and I_{PP1}.
3. Typical values are for $T_A = 25°C$ and nominal supply voltages.
4. This parameter is only sampled and is not 100% tested.
5. This parameter is only sampled and is not 100% tested.
6. OE may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of CE without impact on t_{ACC}.
7. t_{DF} is specified from OE or CE, whichever occurs first.

HM6116P-2, HM6116P-3, HM6116P-4

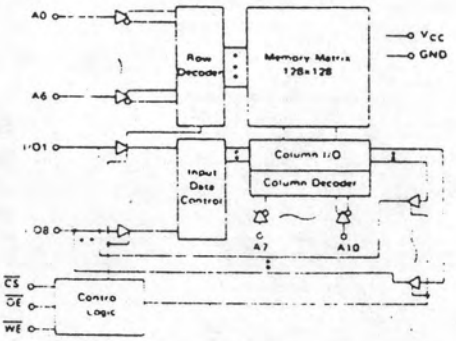
2048-word X 8-bit High Speed Static CMOS RAM

■ FEATURES

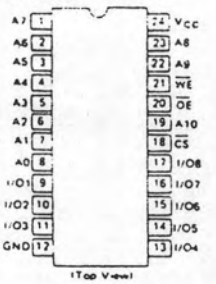
- Single 5V Supply and High Density 24 pin Package
- High Speed Fast Access Time 120ns/150ns/200ns (max.)
- Low Power Standby and Low Power Operation Standby 100μW (typ.)
  Operation 180mW (typ.)
- Completely Static RAM No clock or Timing Strobe Required
- Directly TTL Compatible All Input and Output
- Pin Out Compatible with Standard 16K EPROM/MASK ROM
- Equal Access and Cycle Time

(DP-24)

■ FUNCTIONAL BLOCK DIAGRAM



■ PIN ARRANGEMENT



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to GND	V_{IN}	−0.5 to +7.0	V
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Temperature Under Bias	T_{bias}	−10 to +85	°C
Power Dissipation	P_T	1.0	W

■ TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	X	X	Not Selected	I_{SB}, I_{SB1}	High Z	
L	L	H	Read	I_{CC}	D_{out}	Read Cycle (1) ~ (3)
L	H	L	Write	I_{CC}	D_{in}	Write Cycle (1)
L	L	L	Write	I_{CC}	D_{in}	Write Cycle (2)

Figure 2.19: A data sheet for the 6116—a 2K by 8-bit, common I/O static RAM.

■ RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input Voltage	V_{IH}	2.2	3.5	6.0	V
	V_{IL}	-0.5*		0.8	V

* Pulse Width 50 ns DC V_{IL} min = -0.3V

■ DC AND OPERATING CHARACTERISTICS (V_{CC} = 5V ±10% GND = 0V T_a = 0 to +70°C)

Item	Symbol	Test Conditions	HM6116P-2 min	HM6116P-2 typ*	HM6116P-2 max	HM6116P-3,4 min	HM6116P-3,4 typ*	HM6116P-3,4 max	Unit
Input Leakage Current	I_{LI}	V_{CC} = 5.5V V_{in} = GND to V_{CC}			10			10	μA
Output Leakage Current	I_{LO}	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} $V_{I/O}$ = GND to V_{CC}			10			10	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}$ = V_{IL} $I_{I/O}$ = 0mA		40	80		35	70	mA
	I_{CC1}**	V_{IH} = 3.5V V_{IL} = 0.6V $I_{I/O}$ = 0mA		35			30		mA
Average Operating Current	I_{CC2}	Min cycle duty = 100%		40	80		35	70	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$ = V_{IH}		5	15		5	15	mA
	I_{SB1}	$\overline{CS}$ ≥ V_{CC} -0.2V V_{in} ≥ V_{CC} -0.2V or V_{in} ≤ 0.2V		0.02	2		0.02	2	mA
Output Voltage	V_{OL}	I_{OL} = 4mA			0.4				V
		I_{OL} = 2.1mA						0.4	V
	V_{OH}	I_{OH} = -1.0mA	2.4			2.4			V

* V_{CC} = 5V T_a = 25°C
** Reference Only

■ AC CHARACTERISTICS (V_{CC} = 5V ±10% T_a = 0 to +70°C)

• AC TEST CONDITIONS

Input Pulse Levels 0.8 to 2.4V
Input Rise and Fall Times 10 ns
Input and Output Timing Reference Levels 1.5V
Output Load 1TTL Gate and C_L = 100pF (including scope and jig)

• READ CYCLE

Item	Symbol	HM6116P-2 min	HM6116P-2 max	HM6116P-3 min	HM6116P-3 max	HM6116P-4 min	HM6116P-4 max	Unit
Read Cycle Time	t_{RC}	120		150		200		ns
Address Access Time	t_{AA}		120		150		200	ns
Chip Select Access Time	t_{ACS}		120		150		200	ns
Chip Selection to Output in Low Z	t_{CLZ}	10		15		15		ns
Output Enable to Output Valid	t_{OE}		60		100		120	ns
Output Enable to Output in Low Z	t_{OLZ}	10		15		15		ns
Chip deselection to Output in High Z	t_{CHZ}	0	40	0	50	0	60	ns
Chip Disable to Output in High Z	t_{OHZ}	0	40	0	50	0	60	ns
Output Hold from Address Change	t_{OH}	10		15		15		ns

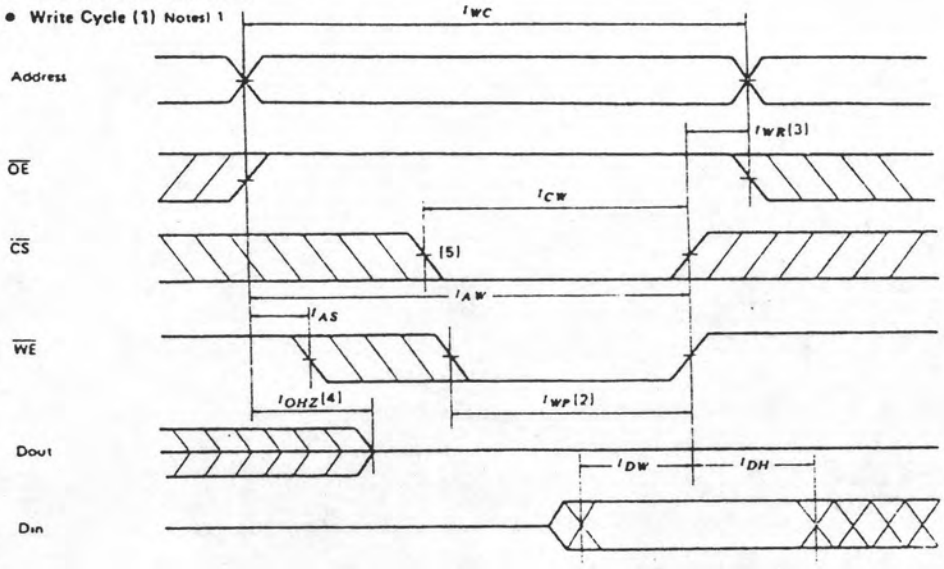
• WRITE CYCLE

Item	Symbol	HM6116P-2 min	HM6116P-2 typ	HM6116P-3 min	HM6116P-3 max	HM6116P-4 min	HM6116P-4 max	Unit
Write Cycle Time	t_{WC}	120		150		200		ns
Chip Selection to End of Write	t_{CW}	70		90		120		ns
Address Valid to End of Write	t_{AW}	105		120		140		ns
Address Set Up Time	t_{AS}	20		20		20		ns
Write Pulse Width	t_{WP}	70		90		120		ns
Write Recovery Time	t_{WR}	5		10		10		ns
Output Disable to Output in High Z	t_{OHZ}	0	40	0	50	0	60	ns
Write to Output in High Z	t_{WHZ}	0	50	0	60	0	60	ns
Data to Write Time Overlap	t_{DW}	35		40		60		ns
Data Hold from Write Time	t_{DH}	5		10		10		ns
Output Active from End of Write	t_{OW}	5		10		10		ns

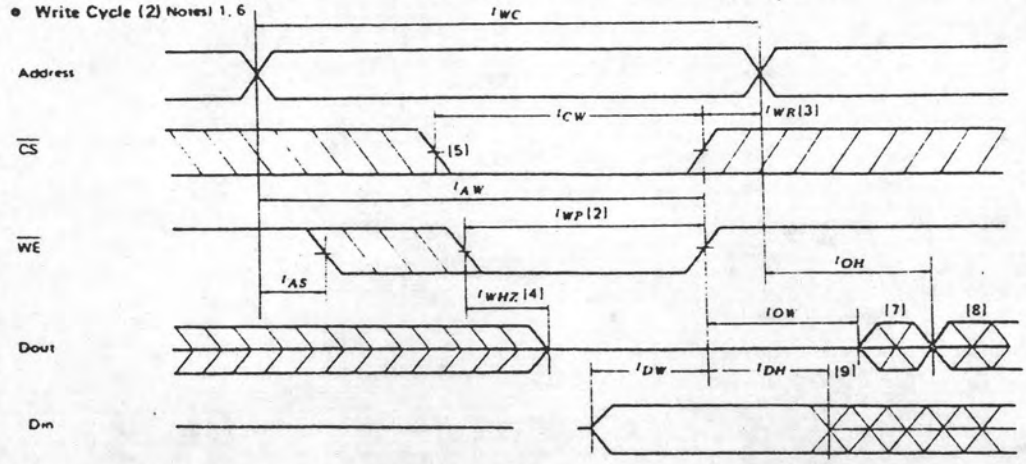
Figure 2.19: Data sheet continued.

■ TIMING WAVEFORM

● Write Cycle (1) Notes) 1



● Write Cycle (2) Notes) 1, 6



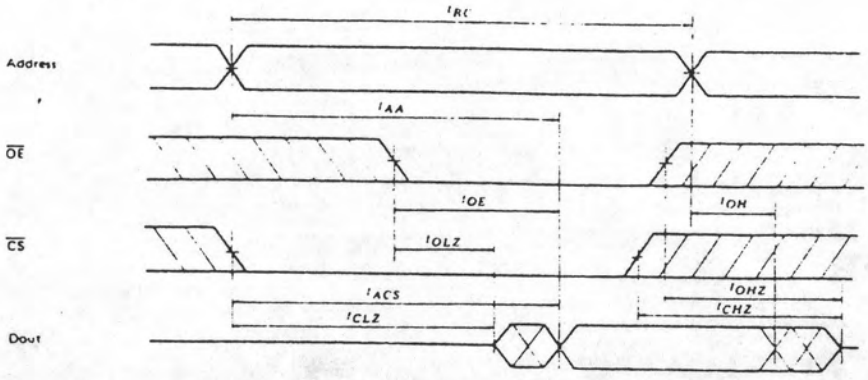
NOTES
1. $\overline{WE}$ must be high during all address transitions
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied
5. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, output remain in a high impedance state
6. $\overline{OE}$ is continuously low ($\overline{OE}$ = V_{IL})
7. D_{out} is the same phase of write data of this write cycle
8. D_{out} is the read data of next address
9. If $\overline{CS}$ is Low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them

Figure 2.19: Data sheet continued.

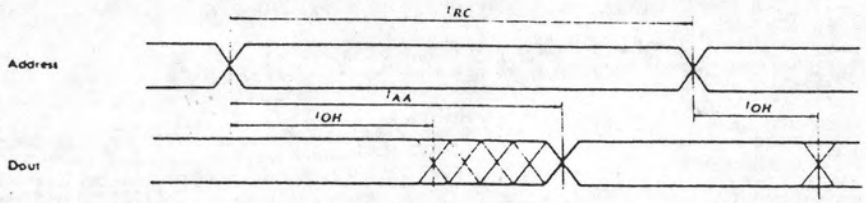
■ CAPACITANCE (f = 1MHz, T_a = 25°C)

Item	Symbol	Test Conditions	typ	max	Unit
Input Capacitance	C_{in}	V_{in} = 0V	3	5	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	5	7	pF

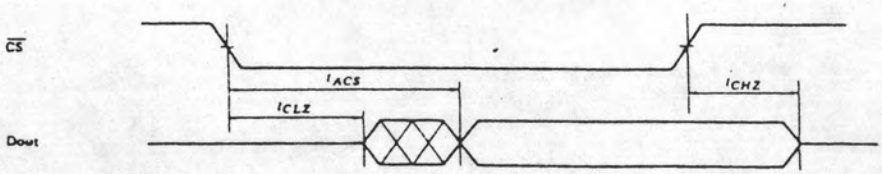
● Read Cycle (1) Notes) 1, 5



● Read Cycle (2) Notes) 1, 2, 4, 5



● Read Cycle (3) Notes) 1, 3, 4, 5



NOTES: 1 $\overline{WE}$ is High for Read Cycle
2 Device is continuously selected, $\overline{CS}$ = V_{IL}
3 Address Valid prior to or coincident with $\overline{CS}$ transition Low
4 $\overline{OE}$ = V_{IL}
5 When $\overline{CS}$ is Low, the address input must not be in the high impedance state

Figure 2.19: Data sheet continued.

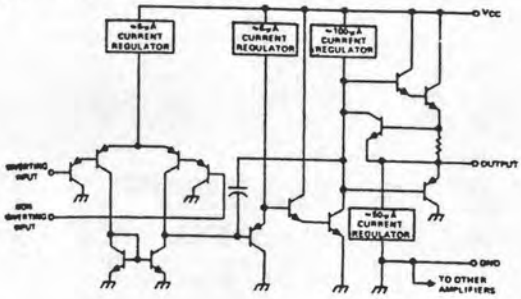
LINEAR INTEGRATED CIRCUITS

TYPES LM124, LM224, LM324
QUADRUPLE OPERATIONAL AMPLIFIERS

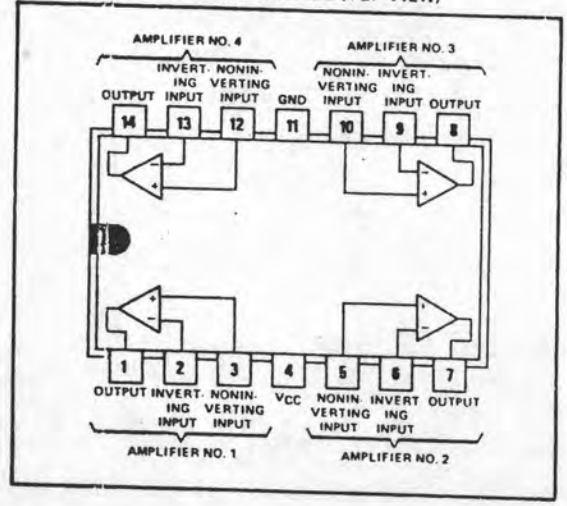
BULLETIN NO. DL-S 12248, SEPTEMBER 1975 – REVISED OCTOBER 1979

- Wide Range of Supply Voltages
  Single Supply . . . 3 V to 30 V
  or Dual Supplies
- Low Supply Current Drain
  Independent of Supply Voltage
  . . . 0.8 mA Typ
- Common-Mode Input Voltage
  Range Includes Ground Allowing
  Direct Sensing near Ground
- Low Input Bias and Offset Parameters
  Input Offset Voltage . . . 2 mV Typ
  Input Offset Current . . . 3 nA Typ (LM124)
  Input Bias Current . . . 45 nA Typ
- Differential Input Voltage Range
  Equal to Maximum-Rated
  Supply Voltage . . . ±32 V
- Open-Loop Differential Voltage
  Amplification . . . 100 V/mV Typ
- Internal Frequency Compensation

schematic (each amplifier)



J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)



description

These devices consist of four independent, high-gain, frequency-compensated operational amplifiers that were designed specifically to operate from a single supply over a wide range of voltages. Operation from split supplies is also possible so long as the difference between the two supplies is 3 volts to 30 volts and Pin 4 is at least 1.5 volts more positive than the input common-mode voltage. The low supply current drain is independent of the magnitude of the supply voltage.

Applications include transducer amplifiers, d-c amplification blocks, and all the conventional operational amplifier circuits that now can be more easily implemented in single-supply-voltage systems. For example, the LM124 can be operated directly off of the standard five-volt supply that is used in digital systems and will easily provide the required interface electronics without requiring additional ± 15-volt supplies.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	32 V
Differential input voltage (see Note 2)	±32 V
Input voltage range (either input)	−0.3 V to 32 V
Duration of output short-circuit (one amplifier) to ground at (or below) 25°C free-air temperature ($V_{CC} \leq 15$ V) (see Note 3)	unlimited
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 4)	900 mW
Operating free-air temperature range: LM124	−55°C to 125°C
LM224	−25°C to 85°C
LM324	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch (1,6 mm) from case for 60 seconds: J or W package	300°C
Lead temperature 1/16 inch (1,6 mm) from case for 10 seconds: N package	260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground terminal.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. Short circuits from outputs to V_{CC} can cause excessive heating and eventual destruction.
4. For operation above 25°C free-air temperature, refer to Dissipation Derating Table. In the J package, LM124 chips are alloy-mounted; LM224 and LM324 chips are glass-mounted.

TYPES LM124, LM224, LM324
QUADRUPLE OPERATIONAL AMPLIFIERS

electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

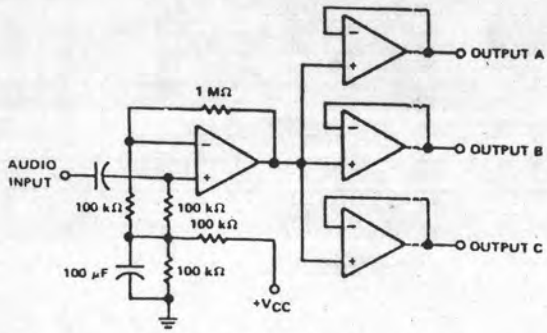
PARAMETER		TEST CONDITIONS†		LM124, LM224			LM324			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1.4 V, V_{CC} = 5 V to 30 V	25°C		2	5		2	7	mV
			Full range			7			9	
I_{IO}	Input offset current	V_O = 1.4 V	25°C		3	30		5	50	nA
			Full range			100			150	
I_{IB}	Input bias current	V_O = 1.4 V, See Note 5	25°C		−45	−150		−45	−250	nA
			Full range			−300			−500	
V_{ICR}	Common-mode input voltage range	V_{CC} = 30 V	25°C	0 to V_{CC}−1.5			0 to V_{CC}−1.5			V
			Full range	0 to V_{CC}−2			0 to V_{CC}−2			
V_{OH}	High-level output voltage	V_{CC} = 30 V, R_L = 2 kΩ	Full range	26			26			V
		V_{CC} = 30 V, R_L ≥ 10 kΩ	Full range	27	28		27	28		
V_{OL}	Low-level output voltage	R_L ≤ 10 kΩ	Full range		5	20		5	20	mV
A_{VD}	Large-signal differential voltage amplification	V_{CC} = 15 V, V_O = 1 V to 11 V, R_L ≥ 2 kΩ	25°C	50	100		25	100		V/mV
			Full range	25			15			
CMRR	Common-mode rejection ratio	R_S ≤ 10 kΩ	25°C	70	85		65	85		dB
k_{SVR}*	Supply voltage rejection ratio	R_S ≤ 10 kΩ	25°C	65	100		65	100		dB
V_{o1} / V_{o2}	Channel separation	f = 1 kHz to 20 kHz	25°C		120			120		dB
I_O	Output current	V_{CC} = 15 V, V_{ID} = 1 V, V_O = 0 V	25°C	−20	−40		−20	−40		mA
			Full range	−10	−20		−10	−20		
		V_{CC} = 15 V, V_{ID} = −1 V, V_O = 5 V	25°C	10	20		10	20		
			Full range	5	8		5	8		
		V_{ID} = −1 V, V_O = 200 mV	25°C	12	50		12	50		μA
I_{CC}	Supply current (four amplifiers)	No load, No signal	25°C		0.8			0.8		mA
			Full range			1.2			1.2	

*$k_{SVR} = \Delta V_{CC}/\Delta V_{IO}$

†All characteristics are specified under open-loop conditions. Full range is −55°C to 125°C for LM124, −25°C to 85°C for LM224, and 0°C to 70°C for LM324.

NOTE 5: The direction of the bias current is out of the device due to the P-N-P input stage. This current is essentially constant, regardless of the state of the output, so no loading change is presented to the input lines.

TYPICAL APPLICATION DATA



AUDIO DISTRIBUTION AMPLIFIER

THERMAL INFORMATION

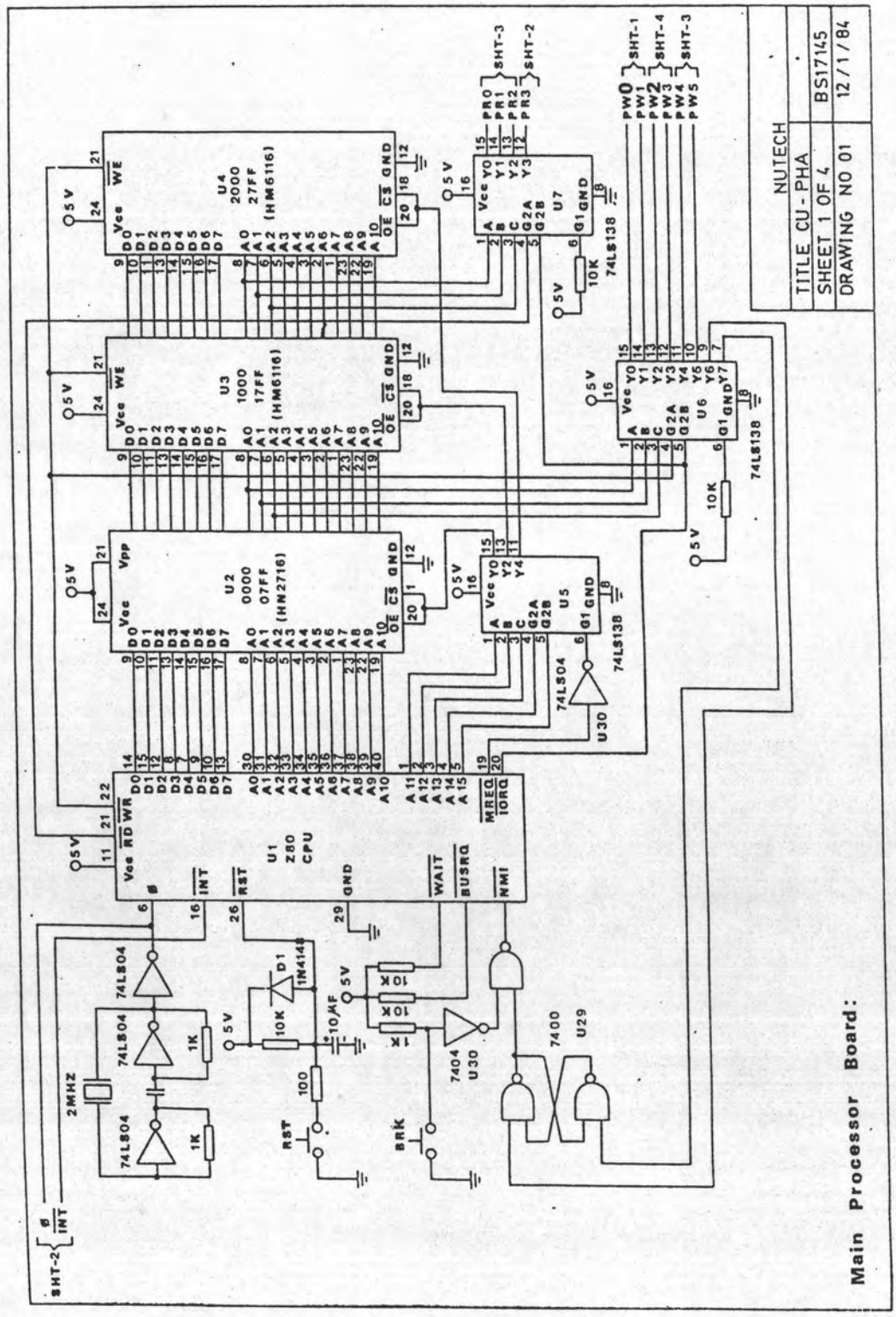
DISSIPATION DERATING TABLE

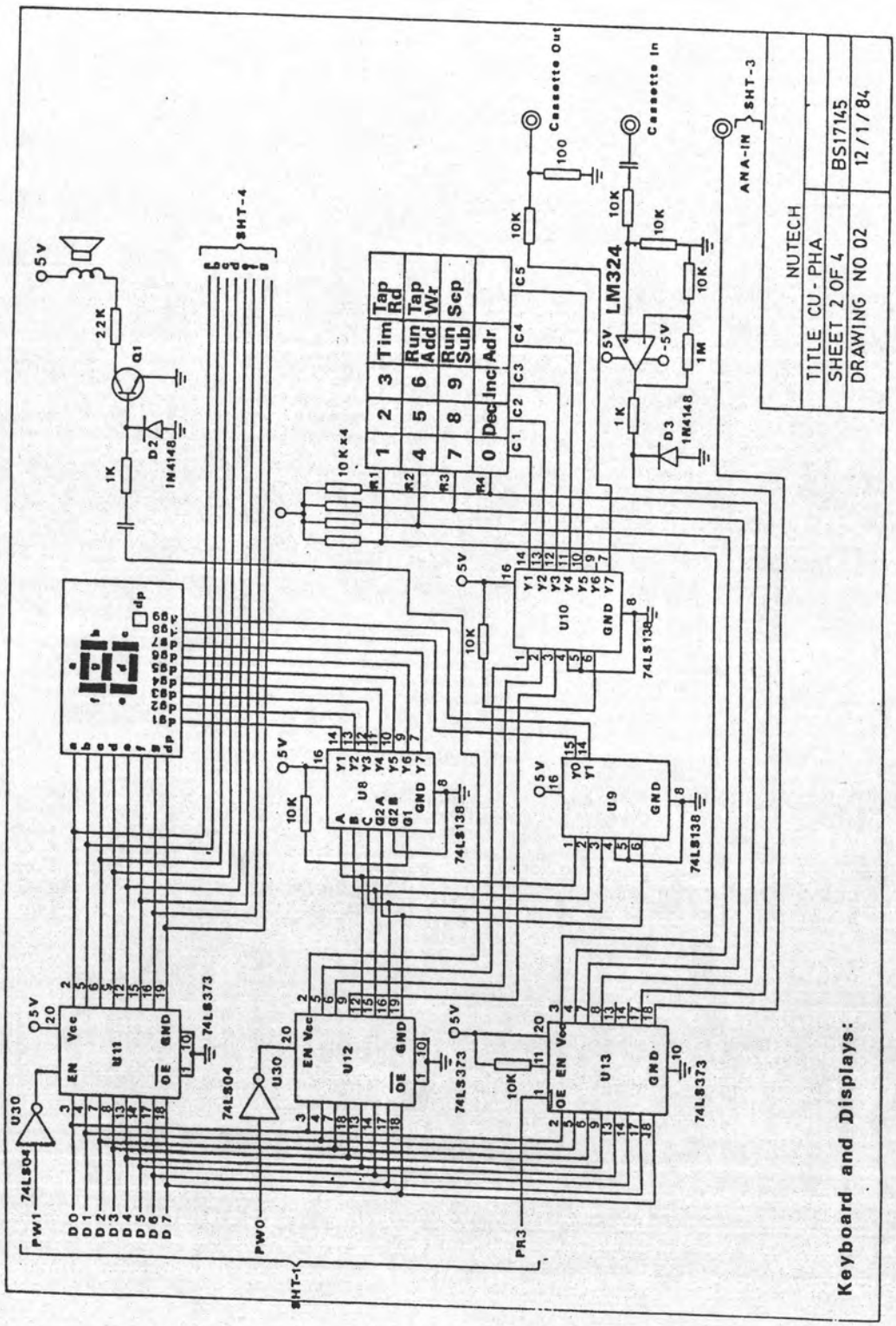
PACKAGE	POWER RATING	DERATING FACTOR	ABOVE T_A
J (Alloy-Mounted Chip)	900 mW	11.0 mW/°C	68°C
J (Glass-Mounted Chip)	900 mW	8.2 mW/°C	40°C
N	900 mW	9.2 mW/°C	52°C
W	900 mW	8.0 mW/°C	37°C

Also see Dissipation Derating Curves, Section 2.

ภาคผนวก ช

วงจรของระบบวิเคราะห์

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SHEET 2 OF 4
DRAWING NO 02
BS17145
12/1/84
Keyboard and Displays:
Cassette Out
Cassette In
ANA-IN
SHT-3
SHT-4
SHT-1
LM324
74LS373
74LS138
74LS04
1N4148
10K x4
22K
1K
10K
1M
100
5V
-5V
PW0
PW1
PR3
D0
D1
D2
D3
D4
D5
D6
D7
U8
U9
U10
U11
U12
U13
U30
Q1
D2
D3
C1
C2
C3
C4
C5
R1
R2
R3
R4
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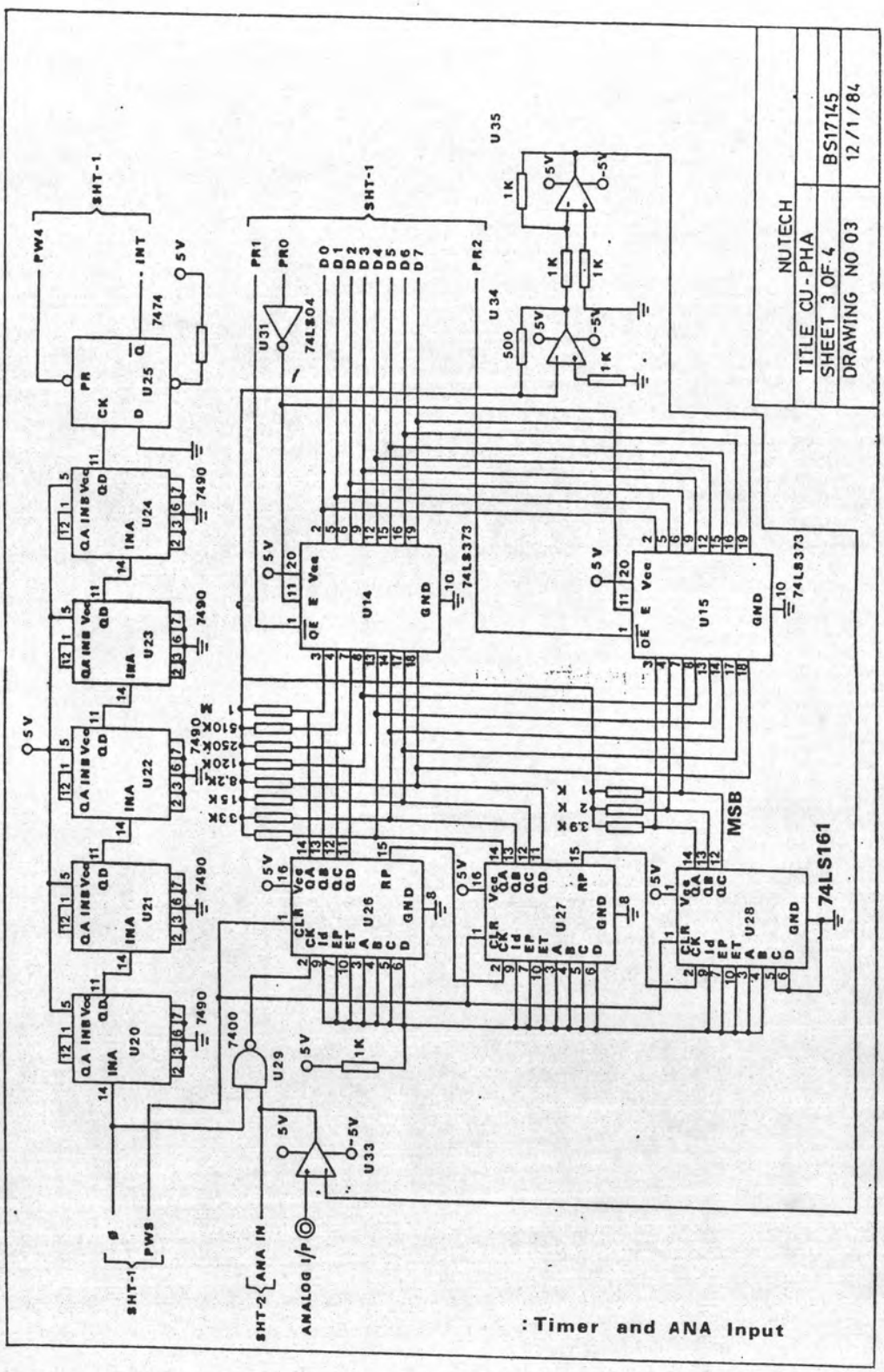
Inc
Adr
Sub
Add
Rd
Wr
Scp
Tim
Tap
Run
GND
Vcc
EN
OE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BS17145
12/1/84
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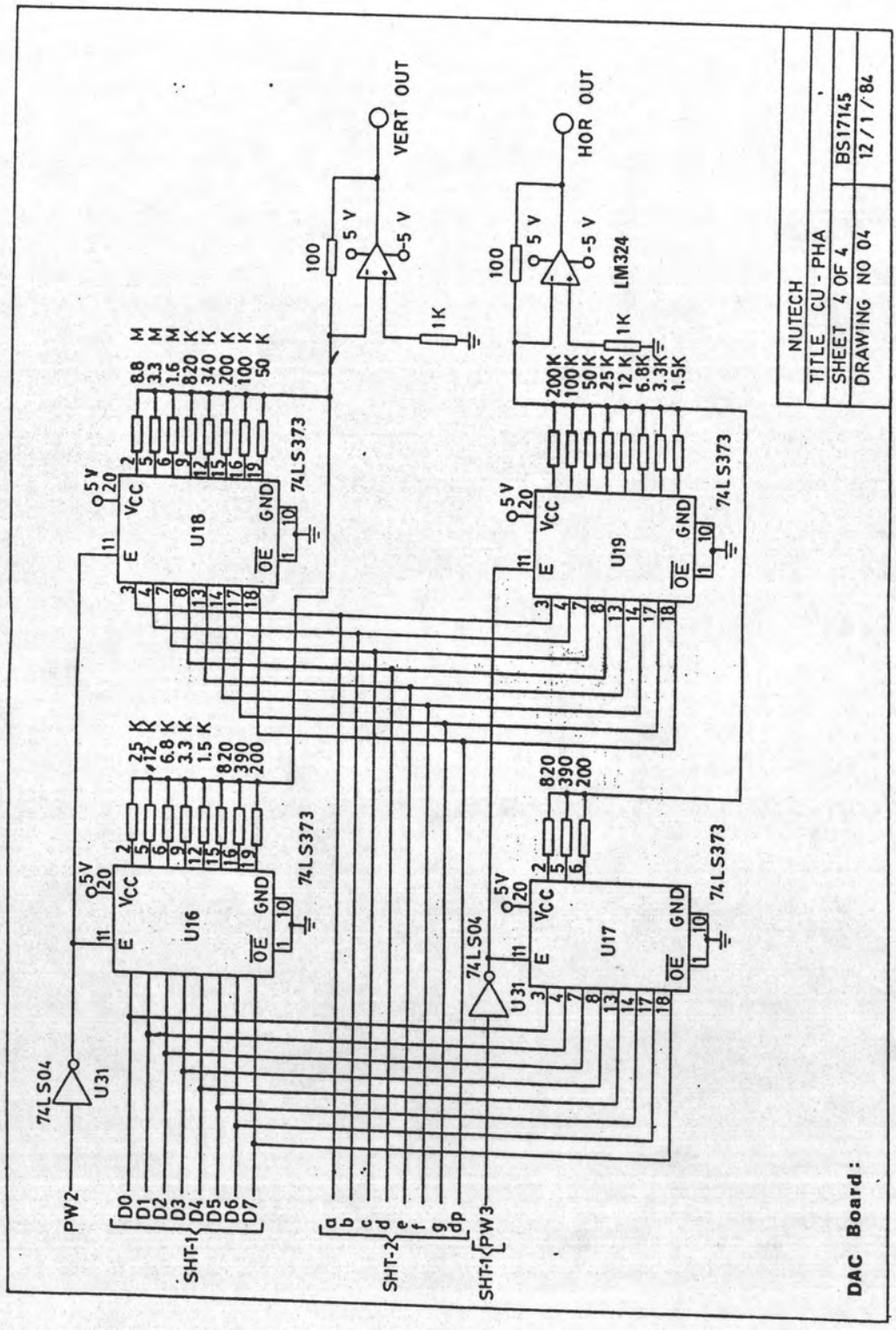
SHT-2
ANALOG I/P
ANA IN
PW4
PWS
INT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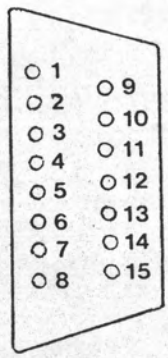
BS17145
DRAWING NO 04
12/1/84
VERT OUT
HOR OUT
LM324
74LS373
74LS04
U16
U17
U18
U19
U31
PW2
PW3
SHT-1
SHT-2
D0
D1
D2
D3
D4
D5
D6
D7
a
b
c
d
e
f
g
dp
5V
-5 V
100
1K
8.8 M
3.3 M
1.6 M
820 K
340 K
200 K
100 K
50 K
200K
100K
50K
25K
12K
6.8K
3.3K
1.5K
25 K
12 K
6.8 K
3.3 K
1.5 K
820
390
200

ภาคผนวก ฌ

ระบบบัสขาเข้า

ฌ.1 ปลักต่อบัสขาเข้า



ฌ.2 รายละเอียดสัญญาณของขา

ขา 1 สัญญาณเข้าบิท MSB

ขา 2 - 9 สัญญาณเข้าบิทลำดับถัดลงมา

ขา 10 สัญญาณเข้าบิท LSB

ขา 11 , 12 ว่าง

ขา 13 สัญญาณสโตรบ (Strobe)

ขา 14 สัญญาณพร้อมรับข้อมูลเข้าระบบ (ready)

ขา 15 กราวนด์ (Ground)

ประวัติผู้เขียน

นาย สุพัฒน์ เอื้องพูลสวัสดิ์ เกิดเมื่อวันที่ 10 มกราคม พ.ศ.2501 ณ.กรุงเทพ-มหานคร สำเร็จการศึกษาระดับปริญญาบัณฑิตจากภาควิชาวิศวกรรมไฟฟ้า คณะวิศวกรรมศาสตร์ สถาบันเทคโนโลยีพระจอมเกล้า พระนครเหนือ เมื่อปี พ.ศ.2524 แล้วเข้าศึกษาต่อในระดับปริญญามหาบัณฑิต สาขานิวเคลียร์เทคโนโลยี คณะวิศวกรรมศาสตร์ จุฬาลงกรณ์มหาวิทยาลัย ในปี พ.ศ.2525