# CHAPTER 5 Results of Improved Process

# 5.1 Introduction

Since new process of monitoring tester performance has been established through using four phases of six sigma in order to use instead of the old method, <u>TSPC</u>, which is perform routinely to control tester performance, there are a lot of advantages that overcome the drawbacks of TSPC process.

In this section, the figures of results are illustrated in the comparisons between the new process of monitoring tester performance and the old process, TSPC. The main issues in comparisons are the effectiveness in identifying tester performance, the saving that new process can provide for the company's gain when the tester can improve yield, errors occurred when using three parts run across testers and when using manufacturing tested data, tester downtime, TSPC part usage, cost of IAT arms, and cost of secondary standard generation process for standard parts using as TSPC parts. There are the other costs spent for performing TSPC but not for the new process such as cost of TTO.

# 5.2 Comparisons of the Results

### **5.2.1 Effectiveness**

Effectiveness can be defined as the ability of the process to inform about the tester performance when problems occur and root causes are from the testing system, including factoring parts, disc or media, and tester issues.

For TSPC, effectiveness is the percent of detection rate when SPC out of control is taken place which root causes are from tester performance. From Pareto diagram in Figure 4.3, it can be seen that as events of SPC out of control occurs and action is taken to find the root causes, just about 30% of detection that the causes are from the testing system. In the other words, the effectiveness of current TSPC is only 30% detection rate.

On the other hand, for new process of monitoring tester performance the new system used in detecting tester performance is established. Effectiveness of the new process is the percent of detection rate when significant difference results are notified, when the interested tester is compared to its own at other time frame, other testers at same time frame, or other testers at different time frame, and root causes can be found they are from the tester performance. Since all of significant difference results events can not be taken actions to find out the root causes at all, some of them that are more severely would be taken first, especially low yield testers mostly caused from low performance of testing system. Therefore, the effectiveness of new process can be determined from the actions taken to find out the root causes that problems are from testing system.

In Table 5.1, testers which provide significant differences with other testers, DS or DD, and impact yield showing by high delta yield are taken the actions. Testers that are taken the actions are totally 32 testers from February 26<sup>th</sup>, 2000 to March 24<sup>th</sup>, 2000. The date of taking actions are illustrated in week that days in a specified week are shown in Table 5.2. The third column "Start" means the week that hypothesis testing gives significance result that notifies the tester problem. The fourth column "Final" means the week that testers are completely fixed and testers are back to the normal conditions. The last column tells about the root causes of tester's problems.

Tester	Parameter	Start	Final	Actions
ECT334Z	LFA	WW35	WW35	Change housing
ECT566Z	LFA	WW35	WW37	Change housing, Calibrate resistance
ECT617Z	LFA	WW35	WW35	Re-calibrate pre-amp board
ECT635Z	LFA	WW35	WW36	Re-calibrate pre-amp board
ECT748Z	LFA	WW35	WW37	Re-calibrate pre-amp board
ECT408Z	LFA	WW36	WW38	Change pogo pin
ECT437Z	LFA	WW36		
ECT446Z	LFA	WW36	WW36	Change housing
ECT482Z	LFA	WW36	WW37	Adjust pogo pin, Change disc
ECT552Z	LFA	WW36	WW37	Adjust air cushion, Adjust phase balance
ECT566Z	LFA	WW36	WW37	Change housing, Calibrate resistance
ECT635Z	LFA	WW36	WW36	Re-calibrate pre-amp board
ECT748Z	LFA	WW36	WW37	Re-calibrate pre-amp board
ECT825Z	LFA	WW36		
ECT431Z	LFA	WW37	WW38	Re-calibrate pre-amp board

Table 5.1: List of testers taken actions

ECT339Z	LFA	WW37		
ECT389Z	LFA	WW37		
ECT408Z	LFA	WW37	WW38	Change pogo pin
ECT437Z	LFA	WW37	WW38	Adjust DC voltage of read/write control board
ECT482Z	LFA	WW37	WW37	Adjust pogo pin, Change disc
ECT552Z	LFA	WW37	WW37	Adjust air cushion, Adjust phase balance
ECT696Z	LFA	WW37		
ECT566Z	LFA	WW37	WW37	Change housing, Calibrate resistance
ECT748Z	LFA	WW37	WW37	Re-calibrate pre-amp board
ECT781Z	LFA	WW37	WW37	Change and calibrate pre-amp board
ECT807Z	LFA	WW37	WW38	Adjust pogo pin
ECTSF8Z	LFA	WW37		
ECT707Z	LFA	WW38		
ECT431Z	LFA	WW38	WW38	Re-calibrate pre-amp board
ECT437Z	LFA	WW38	WW38	Adjust DC voltage of read/write control board
ECT807Z	LFA	WW38	WW38	Adjust pogo pin
ECT408Z	LFA	WW38	WW38	Change pogo pin

Total testers taken actions = 32 No. of testers completed = 25 %Effectiveness = 78.13%



Table 5.2: Days in week35, week36, week37, and week38

	March							
WW	Sat	Sun	Mon	Tue	Wed	Thu	Fri	
35	26	27	28	29	1	2	3	
36	4	5	6	7	8	9	10	
37	11	12	13	14	15	16	17	
38	18	19	20	21	22	23	24	
39	25	26	27	28	29	30	31	

In Table 5.1, 25 of 32 testers can be proved that the significant difference results are from the tester problems. It means that the new process of monitoring tester performance offers 78% effectiveness that is much higher than the current TSPC which offers just about 30% effectiveness. Then, the objective is met that the new process using manufacturing tested data can monitor the tester performance more effectively than the current method that run three parts across group of testers.

In order to compare the detection capability of TSPC and new process using manufacturing tested data, Figure 5.1 shows the results of both methods on LFA of Vail from December 11<sup>th,</sup> 1999 to December 15<sup>th</sup>, 1999. From 102 testers (in horizontal axis) that are performed by TSPC, 39 testers are out of control and only 9 testers of them were coincided as new process comparing to DS. The rest 30 testers or 77% of them were unlikely to take actions for tester investigation.



# Figure 5.1: The comparison of detection capability of TSPC and new process of monitoring tester performance

#### 5.2.2 Saving by Yield Improvement

Since the testers that have significant difference when comparing to other testers and cause low yield will be firstly focused because it tends to be from tester low performance, the costs reduced in the first stage of the implementation are mostly come from the improvement in yield of testers. Yields of the testers are measured before the testers are taken an action and after the testers are completely fixed. Then, savings of higher percent passed parts from improvement can be calculated. As a result, a number of production units that can be saved in a week from the improved yield are obtained. Those are shown in Table 5.3.

Tester	Param.	Final	Actions		Overall yield		Load in 7 days	Saving
				Before	After	Improvement	after fixed	(units)
ECT334Z	LFA	WW35	Change housing	63.90%	73.81%	9.91%	5330	528
ECT617Z	LFA	WW35	Re-calibrate pre-amp board	62.82%	67.07%	4.25%	5705	242
		-						771
ECT635Z	LFA	WW36	Re-calibrate pre-amp board	65.62%	71.64%	6.02%	6743	406
ECT446Z	LFA	WW36	Change housing	60.31%	69.89%	9.58%	7460	715
								1121
ECT748Z	LFA	WW37	Re-calibrate pre-amp board	57.31%	64.33%	7.02%	5356	376
ECT566Z	LFA	WW37	Change hosing, Calibrate resistance	65.01%	72.83%	7.82%	5654	442
ECT482Z	LFA	WW37	Adjust pogo pin, Change disc	66.56%	75.99%	9.43%	10326	974
ECT552Z	LFA	WW37	Adjust air cushion, Adjust phase balance	51.66%	59.74%	8.08%	5498	444
ECT781Z	LFA	WW37	Change and calibrate pre-amp board	58.86%	65.33%	6.47%	10629	688
				1				2924
ECT807Z	LFA	WW38	Adjust pogo pin	57.50%	70.10%	12.60%	4671	589
ECT437Z	LFA	WW38	Adjust DC voltage of read/write control board	65.27%	69.47%	4.20%	10437	438
ECT408Z	LFA	WW38	Change pogo pin	75.87%	79.01%	3.14%	5456	171
ECT431Z	LFA	WW38	Re-calibrate pre-amp board	71.82%	73.99%	2.17%	8297	180
								1378
Total saving						6193		

#### Table 5.3: Saving by yield improvement

It can be seen that when the testers are fixed and the yields are improved, the number of HGAs passing the testing process is more. The company can save 771 HGAs in week35, 1121 in week36, 2924 in week37, and 1378 in week38. The trend of saving is increasing that total saving is 6193 HGAs in a month that costs amount of US\$12,386 saving.

# 5.2.3 Errors from Power of Test

Errors from power of test is Type II error. It is the risk of consumer who might obtains the bad parts since they are classified as good parts. Errors of such a case can be calculated from power of test.

The error of TSPC that run three parts across group of testers is obtained when giving the sample size of three at control limits or detection difference of 3-sigma. Then, the power of test can be calculated from Minitab as shown below.

# Power and Sample Size

1-Sample t Test Testing mean = null (versus not = null) Calculating power for mean = null + 3 Alpha = 0.05 Sigma = 1

Sample Size	Power
3	0.7453
2	0.2608

When three TSPC parts are used to calculated and plotted on the control limits, there are 25.47% error from power of test of 74.53%. It is more severe when only two TSPC parts are used due to outlier. Power of test is only 26.08% causing error high as 73.92%.

On the other hand, the new process of monitoring tester performance that uses manufacturing tested data which is continuous data instead of two or three parts of TSPC. The count of each qualified wafer quad used in comparing to other testers has to meet the power of test at 90% that the sample size requirements are 17 and 23 for LFA and OVW, respectively. Therefore, the errors caused from this process are only 10%. Minitab shows how the sample sizes could be got at detection difference of 0.85-sigma of parametric distribution for LFA and 1-sigma of parametric distribution for OVW.

#### Power and Sample Size of LFA

Testing mean = null (versus not = null) Calculating power for mean = null + 0.85 Alpha = 0.05, Sigma = 1

Sample SizeTarget PowerActual Power170.90000.9079

#### Power and Sample Size of OVW

Testing mean = null (versus not = null) Calculating power for mean = null + 1 Alpha = 0.05, Sigma = 1

Sample SizeTarget PowerActual Power130.90000.9107

It can be concluded that error can be improved from high as 74% of TSPC to minimum as 10% for LFA and OVW of the new process of monitoring tester performance. It can be said that using manufacturing tested data provided more confident level or more accurate classification of good and bad parts than using three parts by TSPC. Thus, Type II error that concerning on consumer's risk could be reduced.

#### **5.2.4 Tester Downtime**

Performing TSPC is the process that provides non value-added to the production. Testers have to be stopped testing the production parts in order to run three standard parts across a group of testers to verify tester performance. Time is also spent on the actions to find out the root causes when out of control happened so that the corrective actions are implemented.

In traditional way, TSPC is performed in routine for all ET once a day. In addition to routine runs, TSPC is also performed when there is a hardware change such as disc and read-write control board. On the other hands, when manufacturing tested data is used instead of routine TSPC, the process of TSPC is performed only when the hardware is changed. Therefore, downtime in running TSPC is reduced since the routine TSPC is eliminated by using manufacturing tested data instead. Table 5.4 shows downtime of TSPC when using TSPC both at routine run and hardware change and new process when using manufacturing tested data instead of routine run and maintain TSPC only for hardware change. The data of tester downtime is collected from February 12<sup>th</sup>, 2000 to March 24<sup>th</sup>, 2000 on LFA and OVW on Vail.

Method	Date	Tester	Downtime (min)	Downtime/tester (min)
	Feb 12 - Feb 18	45	296	6.58
TSPC	Feb 19 - Feb 25	70	1667	23.81
	Feb 26 - Mar 3	195	3812	19.55
	Average downtime / tester =	:	<b>_</b>	16.65
	Mar 4 - Mar 10	150	2983	19.89
New process	Mar 11 - Mar 17	245	2652	10.82
	Mar 18 - Mar 24	255	3250	12.75
	Average downtime / tester =	:	-L	14.49

 Table 5.4: Tester downtime when performing TSPC on traditional process and when

 using manufacturing tested data instead of routine TSPC

Table 5.4 shows that the traditional process provides average weekly downtime 16.65 minutes per tester or 2.78 minutes a day per tester while the new process offered weekly downtime only at 14.49 minutes per tester or 2.42 minutes a day per tester by average. It can be concluded that tester downtime for a week is reduced 2.16 minutes per tester or 12.97% reduction when using manufacturing tested data instead of routine TSPC. Thus, the new process offers the reduction in unnecessary tester unavailability or unnecessary tester downtime which is the weak point of TSPC. However, tester downtime is also depended on tester corrective actions that may take time in some cases. Thus, tester downtime may not be the accurate measurement of the result comparison.

## 5.2.5 TSPC Part Usage and Cost of IAT Arms

TSPC parts are necessary when performing TSPC process. Three parts of TSPC parts which are the standard parts and are from secondary standard generation process are run across a group of testers to monitor and verify tester performance. As mentioned in downtime section, TSPC process is performed in routine and when there is a hardware change. As a result, the traditional way used TSPC parts for routine run and hardware change while the new approach uses TSPC parts only when there is any changes in hardware. TSPC part usage for the traditional method comparing to using for new

Method	Date	Tester	Part usage (part)	Part usage/tester (part)
	Feb 12 - Feb 18	45	53	1.18
TSPC	Feb 19 - Feb 25	70	235	3.36
	Feb 26 - Mar 3	195	110	0.56
:	Average part usage / tester =	1	<b>1</b>	1.70
	Mar 4 - Mar 10	150	87	0.58
New process	Mar 11 - Mar 17	245	319	1.30
	Mar 18 - Mar 24	255	134	0.53
	Average part usage / tester =	I	1	0.80

Table 5.5: TSPC part usage when performing TSPC on traditional process and when using manufacturing tested data instead of routine TSPC

12<sup>th</sup>, 2000 to March 24<sup>th</sup>, 2000 on Vail.

approach is shown in Table 5.5. The data of TSPC part usage is collected from February

From the table, it can be seen that the traditional approach spent about 2 parts per week for a tester but the new approach spent only about 1 part per week for a tester. In summary, the new process can reduce TSPC parts used for 1 part a week comparing to the old way that is about 53% reduction.

In the process of running TSPC parts on a tester, the parts have to be attached on IAT arms which prevent the parts from damages when TTO is catching up them. IAT arms are used for this TSPC process and will be detached before shipping to customers. Then, these arms will be circulated for the other TSPC parts again and again. Unfortunately, IAT arm is much expensive that is about US\$ 65 per arm. Using manufacturing tested data instead of performing routine TSPC can reduce the cost of these IAT arms.

#### 5.2.6 Other Costs

There are a lot of benefits that could be obtained when implementing the new process that is using manufacturing tested data to monitor tester performance. In spite of

saving costs from the advantages mentioned above, the cost of secondary standard generation process (Section 3.5) to generate standard parts, which are TSPC parts, used for performing TSPC process and cost of hiring TTO to perform TSPC process can also be reduced. Since TSPC in routine can be neglected, TSPC parts and TTOs are used only for the hardware changes.

# 5.3 Conclusion

Using manufacturing tested data to monitor tester performance provides a lot of benefits. Some drawbacks of the old process, TSPC, can also be overcome. Effectiveness of tester monitoring process can be increased from 30% to about 78% by using new process. A lot of saving from yield improved is provided. At the same time, cost of standard parts used as TSPC parts, cost of IAT arms, cost of secondary standard generation process, and cost of TTO can also be reduced. In contrast, errors of consumer's risk and tester downtime is improved.