Chapter 3

Discussion of Problem

Background of Business

Founded in 1987, Chartered Semiconductor Manufacturing is one of world leading independent semiconductor foundries. It provides comprehensive wafer fabrication services and technology to semiconductor suppliers and manufacturers in electronics system. CSM is a pure-play foundry, providing advanced technology wafer manufacturing services for the high growth, technology advanced applications, including communication applications. CSM top five customers are Hewlett-Packard, Lucent Technology, Level one Communications, Broadcom and Conexant.

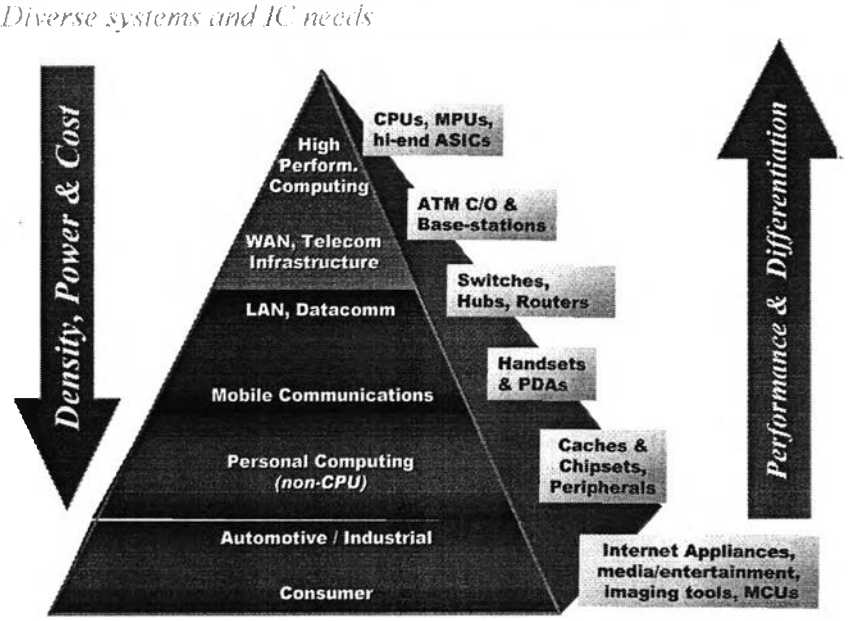

Figure 3.1 : Product Complexity, Performance and Cost Relationship
(Source : CSM Technology Roadmap)

CSM has the most advanced integrated circuit processing facility in South East Asia using a broad range of leading digital and analog technologies, including standard complementary metal oxide or CMOS, Mixed-signal and embedded memory processes.

CSM are also developing additional high performance technologies such as advanced embedded memory technologies and specialized CMOS for wireless application. Its products have more than 1,000 designs for applications as diverse as graphics, memory, communications and networking. In order to enhance its internal development, it has entered into technologies alliance with leading semiconductor companies such as Lucent and Motorola.

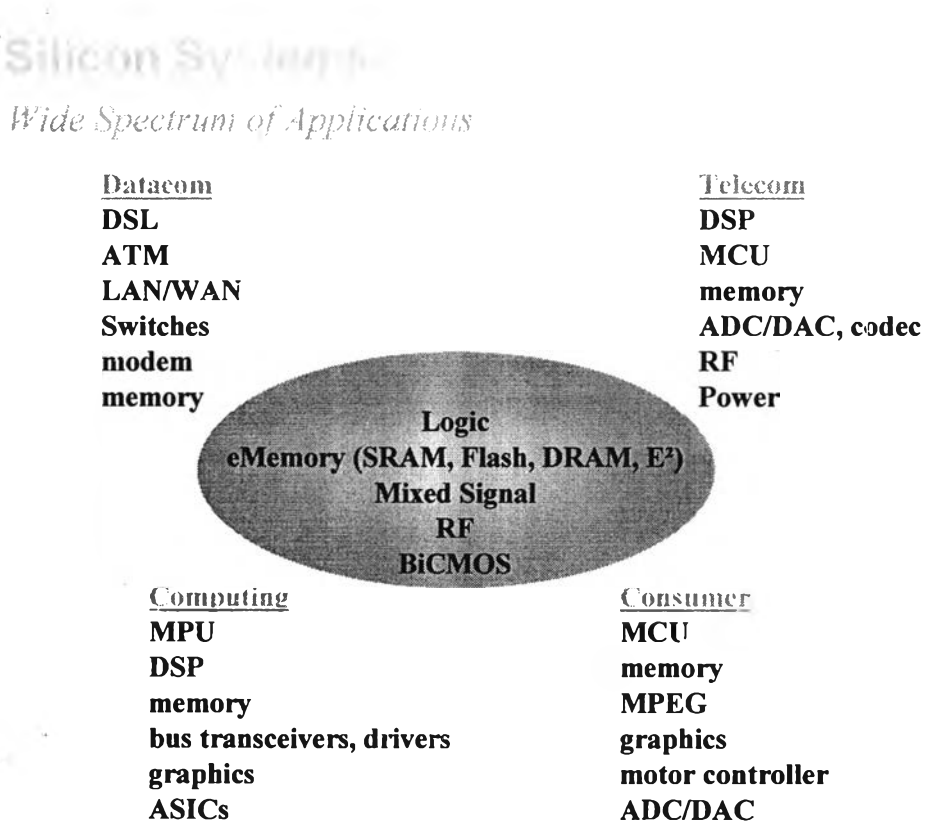

Figure 3.2 : CSM Product Range (Source : CSM Technology Roadmap)

Through strategic partnerships, Chartered is able to facilitate successful silicon implementation of customer designs while providing a full turnkey service ranging from

design to assembly and final test of packaged for customers worldwide. Its partnership and ranges of services enable its customers to integrate an increasing number of functions in their products while accelerate the Time-To-Market and reducing the design and manufacturing risk. CSM partner with leading providers of semiconductor electronics design automation, or EDA, software tools and intellectual property, or IP, and Design Services. Its EDA development and IP partners include Artisan Components, Avant!, Cadence, MIPS, and Synopsis.

Known for quality processes and exceptional customer service, Chartered is a recipient of **Semiconductor International** Magazine's Top Fab award. Headquartered in Singapore, the Company operates sales and service offices worldwide. Chartered Semiconductor Manufacturing is an international company with a diverse population; Chartered employs over 2,800 people at its facilities in the United States, Asia, and Europe.

Organization

Chartered is a member company of Singapore Technologies Semiconductors (STS). The STS companies provide design, integrated circuit wafer fabrication, assembly and test for the global semiconductor industry.

STS is a strategic business area of **Singapore Technologies**, which comprises more than 100 companies whose total 1997 revenues exceed S$5.5 billion (US$3.5 billion). CSM is 89.8% owned by Singapore Technologies Pte Ltd and its affiliate. Singapore Technologies is one of Singapore's largest industrial conglomerates and is indirectly wholly-owned by Government of Singapore.

CSM is currently own five fabrication facilities, which are located in Singapore. Fabs 1, 2 and 3 are wholly-owned by CSM. Fab 5 is operated by Silicon Manufacturing Partners, known as SMP, which is jointly-owned with a subsidiary of Lucent. Fab 6, known as Chartered Silicon Partners, or CSP, is jointly-owned with an affiliate of the Government of Singapore and subsidiary of Hewlett-Packard. CSM plan to increase total production capacity from approximately 60,000 eight-inch equivalent wafers per month in

June 1999 to an estimated 134,000 eight-inch equivalent wafers per month by December 2002.

The Capacity, Product, and Product Market Price are summarized in the table below.

AVERAGE SELLING PRICE PROJECTIONS					
Product mix		**1998**	**1999E**	**2000E**	**2001E**
0.6-3.0 m	%		26	17	13
0.45-0.5m	%		29	19	12
0.3-0.35m	%		35	44	32
0.2-0.25m	%		10	17	32
0.18m	%		0.3	2	8
0.15-0.16m	%			1	4
0.6-3.0 m	US$/wafer		575	500	450
0.45-0.5m	US$/wafer		875	800	750
0.3-0.35m	US$/wafer		1,200	1,200	1,100
0.2-0.25m	US$/wafer		1,650	1,600	1,500
0.18m	US$/wafer		2,400	2,200	1,300
0.15-0.16m	US$/wafer		5,000	4,500	3,000

Table 3.1 : Average Wafer Selling Price Projection [15]

PRODUCTION CAPACITY					
	Fab1	**Fab2**	**Fab3**	**Fab5 (SMP)**	**Fab6 (CSP)**
Clean room size (sq ft)	35,000	70,000	46,000	46,000	85,000
Max capacity 8"eq pm	13,000	40,000	20,000	26,000	35,000
Wafer size	6"	8"	8"	8"	8"
Process technology- m	1.2-0.5	0.6-0.3	0.35-0.22	0.25-0.15	0.25-0.13
Production commenced	1989	1995	1997	1999	2000E
Ownership	100%	100%	100%	49%	51%

Table 3.2 : CSM Production Capacity [15]

CAPACITY AND SHIPMENT						
Shipment	**1996**	**1997**	**1998**	**1999E**	**2000E**	**2001E**
Fab1	140	103	142	200	180	170
Fab2	114	220	265	395	400	420
Fab3		21	32	85	175	250
Fab5 (SMP – 49%)				15	140	226
Fab6 (CSP – 51%)					26	170
Total	253.9	344.1	439.7	695.0	921.0	1236.0
Growth (%)	36.5	35.5	27.8	58.1	32.5	34.2
Available capacity	350.0	440.0	580.0	750.0	936.0	1246.0
Utilisation rate (%)	73	78	76	93	98	98

Note: Capacity and shipment are in 8-inch equivalent wafers in '000 units.

Table 3.3 : CSM Capacity and Shipment

Source : Daiwa Daily, Asia Pacific Daily Notes 13 October 1999

Customer Services

A customer service team is identified for each customer to ensure successful tape-out and mask generation. They track all work in progress and keep a watchful eye on order status to ensure on-time delivery of finished products. At each step of the way, this team provides a seamless interface between wafer fabrication, wafer sort, assembly and test of your products.

To further enhance the quality of services, CSM work closely with their customers and form partnerships with key suppliers. It's one more way that CSM help their customers gain access to the latest process technologies, and gain time-to-market advantage. These services are:

Turnkey Options

For a turnkey solution, Chartered provide comprehensive services from early technology definition and customization through full product qualification. Production burn-in, line monitoring and yield improvement support is available. Customers can select a turnkey option that includes some or all of following

services from design assistance to mask making, wafer fabrication, wafer sort, assembly and test.

Design Assistance

It is said that the number of transistors on a semiconductor product doubles every 18 months, and product life cycles have decreased to 12 months. This frenetic pace places intense pressure on semiconductor companies to create ever more powerful chips at ever faster speeds, and often pushing the limits of technology.

To help customers meet these demands, Chartered works closely with several partners that provide a comprehensive portfolio of design services and products including standard cell and gate array libraries, I/Os, memory compilers, data-paths, and intellectual property cells. This model gives customers maximum flexibility. Customers can choose libraries and services that best fit their product and business strategy, with full vendor support for the complete development life cycle.

eFab™ Initiative— Advance Information Exchange System

Chartered has recently teamed with HP and Lucent to form the eFab™ Alliance, an initiative to create an open standard for secure electronic communications across the semiconductor and foundry industry.

Figure 3.3 : eFab™ Logo

Operating under the nomenclature of the "eFab™ Alliance," the three companies will immediately begin designing a preliminary specification that

outlines the core requirements for implementing secure, standardized electronic communications.

The eFab™ Alliance will also encompass the development of standardized data exchange formats with Chartered Silicon Partners and Silicon Manufacturing Partners, Chartered's joint-ventures with HP and Lucent, respectively.

While standards exist to standardize terminology, there is no open standard for delivery of data. Currently, companies use their own individual formats for information exchanged between customers, suppliers and the foundry. This requires that recipients re-enter or manually re-format the data before they can use it. The eFab™ Alliance seeks to remedy this situation by building a system that will contain standardized terminology and formats for the delivery of information between companies.

The three companies have selected work-in-progress (WIP) as the first segment of tasks to be framed within the new guidelines.

Following its initial work, the eFab™ Alliance will turn its work over to an independent organization that can advance the guidelines into an open industry standard that includes all sectors of semiconductor industry. This includes fabbed and fabless semiconductor companies, foundries, electronic design automation (EDA) and intellectual property (IP) providers, and suppliers.

"The eFab™ Alliance's work will provide the basis for seamless communications between clients and foundries. This will provide virtual organizations with the same real-time supply chain information as physical organizations. The project ownership and support of two industry leaders like HP and Lucent gives the eFab™ Alliance the benefit of experience knowledge, resources and infrastructure to make this a true standard, not just a single-company effort. All companies in the semiconductor industry will be able to participate and benefit from their involvement. This project is the beginning of a new era of global communications.

Current Situation

Chartered has a very big organization structure, in which heavily interrelated together through the worldwide network. This included internal network through worldwide offices and external network to suppliers and customers. To make the matter worse, the new Project eFab™ is another strategic information communication network that Chartered linked to its strategic alliances at core Technology strategic level. CSM cannot effort to fail communication within its' network. In this case, it does not mean just Year 2000 Crisis alone, but also include other disasters as well. This is due to the cost of nonconformance is too great for the organization to take risk. In the fierce competition in this business nature, would not mean just the lost due the products that fail in the production line but include the long-term strategic trust from its customers.

Our Main Competitor is TSMC (Taiwan Semiconductor Manufacturing Company) [See TSMC Company Detail in Appendix D], is the biggest pure-play foundry in the world. The Second is UMC (Taiwan Company United Microelectronics Corp). The Third is Chartered Semiconductor Manufacturing. Chartered has to develop business advantage over its competitors to gain the market share in this industry, in this case Year 2000 Readiness. TSMC start the Year 2000 Project after CSM by 6 months. CSM always benchmark itself against TSMC in term of Technologies, Profit, Production, and in this case Year 2000 Readiness.

In terms of process capacity this year, TSMC will reach 1,870,000 wafers (8-inch equivalent), UMC will touch 1,680,000 while CSM will only churn out 691,000 – a third of TSMC's capacity. In the foundry business, economies of scale play an important role.

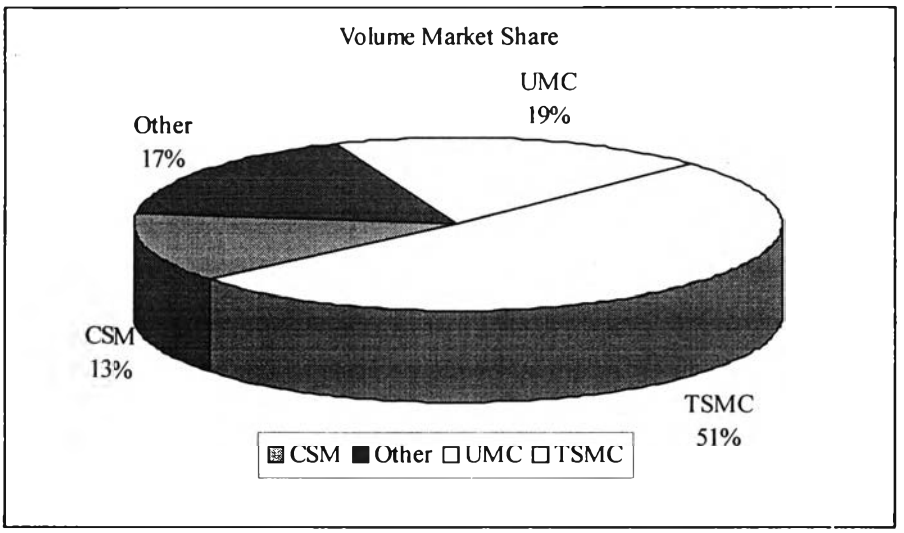

Figure 3.4 : Worldwide Market Share [15]

Since 1987, CSM has incurred significant operating losses and negative cash flows. This is true even in years in which its revenues increased. In 1998, CSM lost $98.1 million on sales of $333 million, due to over-dependence on Memory Chips. CSM changed direction of the target market to product mix with bias toward the data and telecommunications industries. [12] With this niche market, it force CSM to find alliance with technology giant like Hewlett-Packard, Lucent Technologies and Motorola. By doing so, it has introduced tremendous pressure from its alliance to be Year 2000 Compliance through out the system.

Scope of this study is from the beginning of 1998. At that time CSM already started the initial phase of collecting information and formation of Year 2000 Team. The lifecycle of this project will be discussed in following section.

Potential Risks to Business

Nowadays, computer is a common part of the office and operation automation that involve in normal operation environment. The more complexity of the computerization involved is normally mean the more impact it can produce. In most case, there are 3 major areas that computer plays the important role in the operation nature, they are:

- Finance
- Operation
- Legal Liability

These three major areas are heavily integrated into the modern organization that required handling, interpreting and manipulating large database. Chartered is one the companies that implementing the computerize automation in our strategic operation level. The complexity of the communication network is unavoidable.

The lists below are the example of the potential problems that cause by misinterpret and miscalculation of the time format.

Finance

· Distorted financial forecasting,
· Accounts double posting,
· Fiscal year results computation,
· Integrity of figures,
· Invoicing errors,
· Payroll problems,
· Inaccuracy interest payments (due to GPS synchronization of international funds transfer)

Operations

· Errors in corporate investment accounts due to :
· Break down in clearance & settlement transactions,
· Lost electronic stocks & cheque accounts,
· Denied access to customer accounts,
· Deposits trades not credited,
· Customer funds not available,
· Interests not credited correctly,
· Retail transaction fail when credit cards reader encounters Y2K expiry date,
· Other errors in licensing system,
· Failures of process control systems in manufacturing plants,
· Errors in insurance actuarial tables,

- Interest & mortgage rates,
- Age calculations,
- Storage shelf life.

Legal Liabilities

- Class Action Suits
- Professional Malpractice Suits
- Director & Officer Liability Suits

And if any of the problems above happens, it could result in:

- Operational Disruption
- Loss of Market Share
- Loss of Productivity
- Loss of Profitability
- Compromised Safety

However, in IC manufacturing the Potential Hazard in the Operation is different from other industry. As we mention earlier that this study will concentrate on only the production equipment, which is in the operation area. In IC manufacturing industry, can divide roughly the hazard in the operation area into :

1. Production Recipe affected. Since IC Manufacturing process are very complicated, the production recipe and history log may be in jeopardy of loss or misinterpret. Although we may know the quality drift within 15 minutes, but as we know a unit of product is cost from USD 575 to USD5,000. The throughput of the machine is vary from less than hundred wafer per hour to more than 300 wafer per hour per machine. The lost due to the 15 minutes error can be as high as USD375,000 per machine in the worse case.

2. The history log affected. In special product defect case, the history of machine parameters of the processed wafer need to be verify before can send on the wafer. In this case, if cannot retrieve the history, the normal practice is to scrap the wafer. This is due to many nature of this industry.

2.1 Customer paying the wafer price base on the average yield of the Fab, and this process is most of the time done at customer's site. If wafer is in question of the quality is required to scrap beforehand to reduce the profit and reliability loss in long term quality assurance.

2.2 Value added on the product is not as high at the early stages. Some wafer have to go through 200 steps to complete a wafer. If the wafer found a defect at the early stage, dispose the defect wafer will be much cheaper before finding out the end of process.

2.3 On-time Shipment Delivery (OSD). If the product does not deliver within time, the penalty will be introduce, which eventually reduce profit margin of the product. Therefore, if a wafer risk of having failure at the end of process, the shipment will be affected as well. The cost of sending on the wafer may be minimal compare to the penalty. The penalty is depend upon the priority of the wafer.

3. Equipment Failure. This will have direct impact on the processing wafer at that time. It may affect the quality of the wafer in the same batch, which may lead to scrap the batch.

4. Facility failure (Power, DI Water, N_2 , CDA, Silane, Argon). This is the major disaster. All the wafers in the Fab using particular facility are possibly affected by this incident. The Work in Process (WIP) can be as high as 40,000 wafers in Fab 2. The Product price is as high as 1,200 for 0.3 micron, which translate to the casualty of USD 48 millions.

5. Safety. Equipment or facilities failure may cause damage to human, especially person who work around that area.

6. On-time Shipment Delivery (OSD). If disaster happens, the product will not be able to ship on time, hence will affect the penalty and the record of the company. This OSD record will affect the wafer price as well.

CSM Year-2000 Program Objectives

Since mid-1997, Chartered has been taking active steps to ensure that all of its key systems are Year-2000 ready by the third quarter of 1999. Our goal is to ensure that our customers experience no deterioration in quality or disruption in service as a result of Year-2000 issues.

Year-2000 Policy

CSM shall make every effort to work with all our software, equipment, facility, and raw material suppliers to make our manufacturing, sales, distribution, facility and IT systems Year2000 compliant by Q2 1999, so that there shall be no disruption in our service to our customers.

The Scope of Chartered's Year-2000 Audit

The scope of Chartered's Year-2000 preparedness program includes readiness audits for each of the following company wide systems:

- All IT systems including hardware, software, data and communications networks.
- All facility equipment including safety, security, and environmental management systems.
- Production equipment for all manufacturing fabrication facilities including fab utility and support areas.
- Vendor audit and readiness program for all strategic suppliers.

Year2000 STRATEGIES

- Manage as a Critical Project
- Form Year2000 committee, led by IT Department (Team Leader - Director, IT)
- Focus Areas :-
    - IT Systems (Hardware, Software, Networks)
    - Facility Equipment (Safety/Security/Environment)
    - Production Equipment for all Fabs
    - Fab Support Areas
    - Vendors (Materials, Chemical,etc)
- Management to issue Year2000 compliance letters to vendors
- IT VP to represent Management in Year2000 Committee and report status in staff meeting.
- Adopt SEMATECH Year2000 Test Scenarios as CSM Year2000 Test Guidelines
- Fab Operations representatives to actively drive Year2000 compliance testing on Fab production equipment.
- Instill Year2000 awareness company-wide by conducting workshop for management, staff and vendors.
- Establish closer co-operation with vendors to expedite on Year2000 compliance testing.
- Develop contingency plan in the event of Year2000 non-compliance in certain operations areas. Aim to minimize overall business impact.

Year 2000 Team

At Chartered, the Year-2000 Program is a key strategic initiative with considerable resources and a financial investment of nearly $5 million devoted to the effort. The Program enjoys top-level support and direct sponsorship from our president and CEO, Barry Waite and is managed by Justin Lim, vice-president, information technology (IT). Day-to-day implementation is carried out by Teo Kok Sin, deputy director of IT, with the full support of a company-wide cross-functional Year-2000 Program Team.

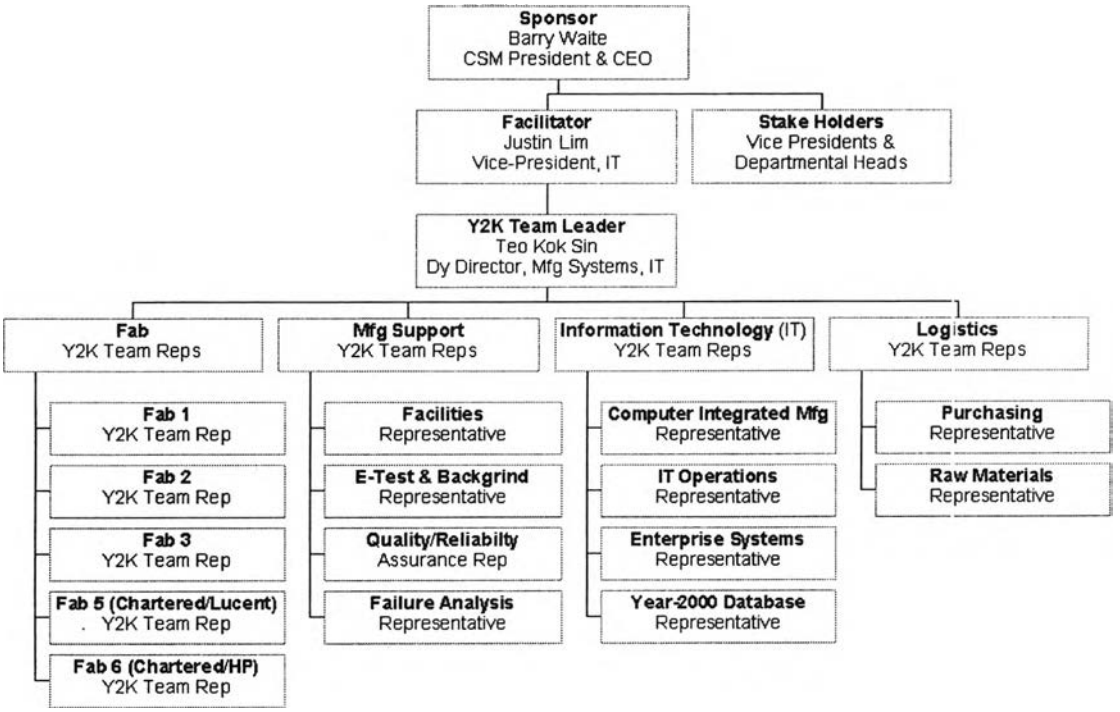

Figure 3.5 : Year 2000 Team Organization Chart

There are committees from each Fab participate and drive the Project to reach the Year 2000 goal. The detail of the Year 2000 team structure for each Fab will contains the Engineering Groups base on functional structure and Production support to represent each of the Fab committee. These Groups are consist of :

1. Clean Tech (Chemical Etch)
2. Diffusion
3. Plasma Etch
4. Ion Implantation
5. Photo Lithography
6. Thin Film
7. Yield Enhancement
8. E-Test (Electrical Test)
9. IT (Production Related, e.g. PROMIS, CIM, etc.)
10. Facility
11. Manufacturing
12. CMP (Chemical Mechanical Polishing)

The year 2000 Team from each Fab will comprise at least one from each module to represent their module cooperation. This team member will act as a coordinator, facilitator, and executor for their area.

Year-2000 Program Activities

At Chartered, we are working proactively with our strategic suppliers of equipment, systems, software, and raw materials to ensure that our manufacturing, sales, distribution, facility and information technology systems are Year-2000 capable company wide. Specific activities include:

- Company wide training programs to instill Year-2000 awareness among employees
- Certifications of Year-2000 readiness are required from all equipment and product vendors
- Chartered tests vendor claims where practical to confirm Year-2000 compliance
- All wafer manufacturing processes are checked and modified if necessary to ensure Year-2000 conformity
- Chartered to develop and execute contingency plans that will minimize the overall business impact in the event of Year-2000 non-compliance in certain operational areas.
- Chartered's executive management team monitors and reviews the status of the Company's Year-2000 Program regularly.
- Chartered participates in SEMATECH (Semiconductor Manufacturing Technology Association) and has adopted its industry standards for Year-2000 testing— SEMI/SEMATECH Year-2000 Readiness Program Guidelines.
- Chartered has also signed the Millennium Accord, an international initiative which provides guidelines for resolving Year-2000 related

disputes through negotiation and mediation as an alternative to potentially lengthy and expensive court actions.

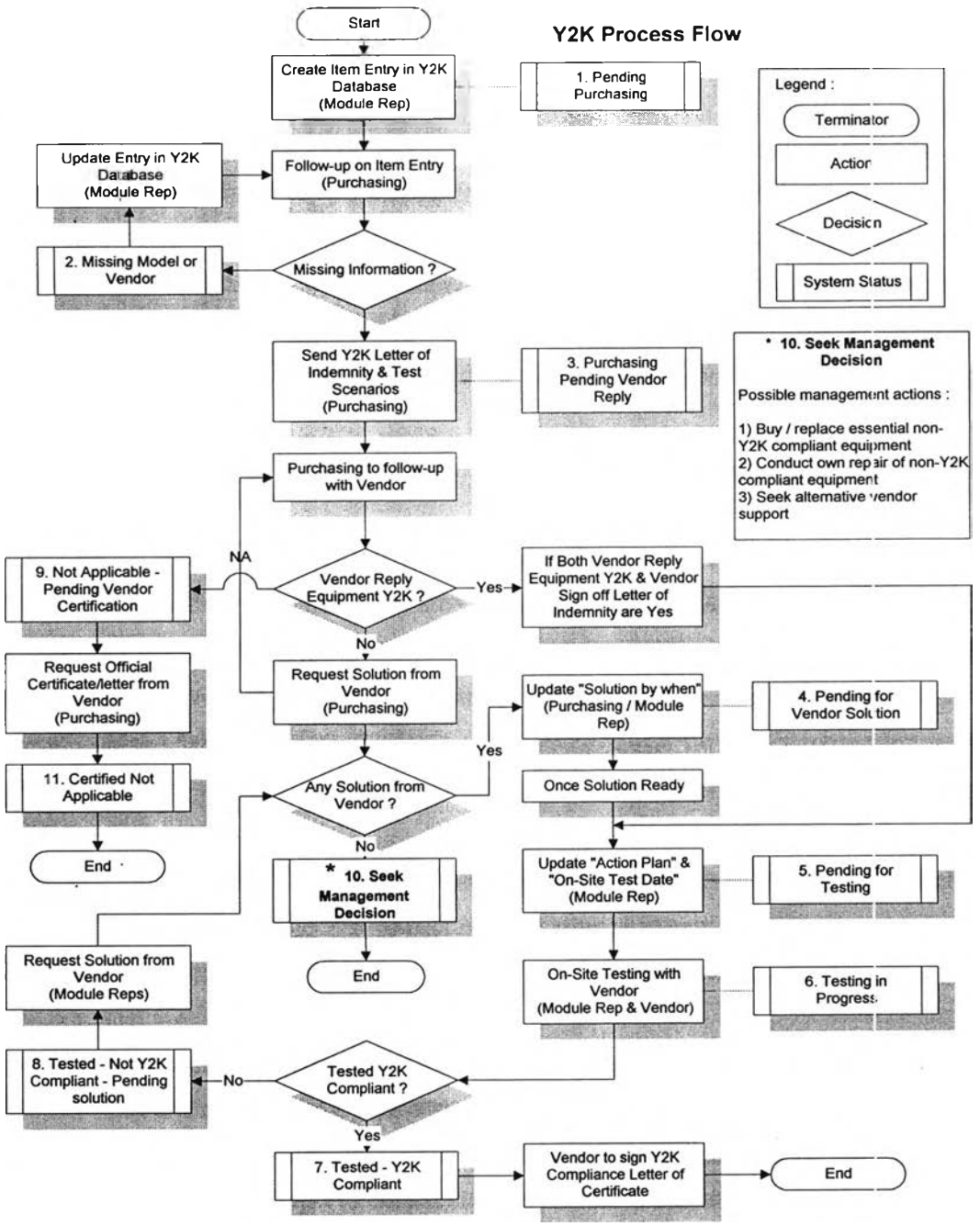

Figure 3.6 : Process Flow of the Y2K Compliant program

Project Lifecycle

A conversion model comprised of five phases each representing a major Y2K activity. Both private and public sectors have used this model in addressing their respective Y2K issues.

However, in Chartered Semiconductor Manufacturing, it has an initial stage to facilitate the whole of the Project. This stage called initial Study and preparation. At this stage, the IT and Purchasing Department are the team that will gather information from Vendors in term of their solution and cost for their customers. Additional study need to be carried out by IT Department to ensure that all the key operation and security are properly take into consideration. This research will carry out from this stage onward.

The rest of the five phases are :

- Awareness - At this stage, the main objective is to make it clear to all member to be fully aware of that the Project is all about. This means that the members will need to establish target for the Project. All members must have sufficient basic knowledge of the topic before they can start. This is the most important part of the project because it will determined the project necessary resources, like time, money, manpower, equipment, etc..

- Inventory Assessment – From the objectives of the project, the team member need to determine the realistic time, equipment, manpower, money, software, support from suppliers and customers.

- Implementation – With adequate resources and clear objectives of the Project, the next step is HOW the team should do to achieve the objectives. The develop process should emphasize on the risks of the organization faced and the prioritization of those risks. The test plans should consider focusing on the highest risks to reduce them down to manageable level. External Factor Consideration is also necessary for the team members to consider about what would affect the Software testing outcome as well as internal factor.

- Correction and Recovery – The actual testing should be focus on determining whether the high-risks software is achieving the objective of the project or not. The most effective use of the resources in the testing activities is to verify, rather than to validate. Verification is the static analysis of the changed software, which from expert experienced has proven to be much more effective in identifying the defects. Validation is physically ensures the operation by series of tests and this method should be focus on the internal and external interfaces software system.

- Final Audit – Testers should assume if the Software testing Project is not successful and business is interrupted. Therefore, the member of this project should develop a contingency plans to address potential interruptions in the mission-critical software system.

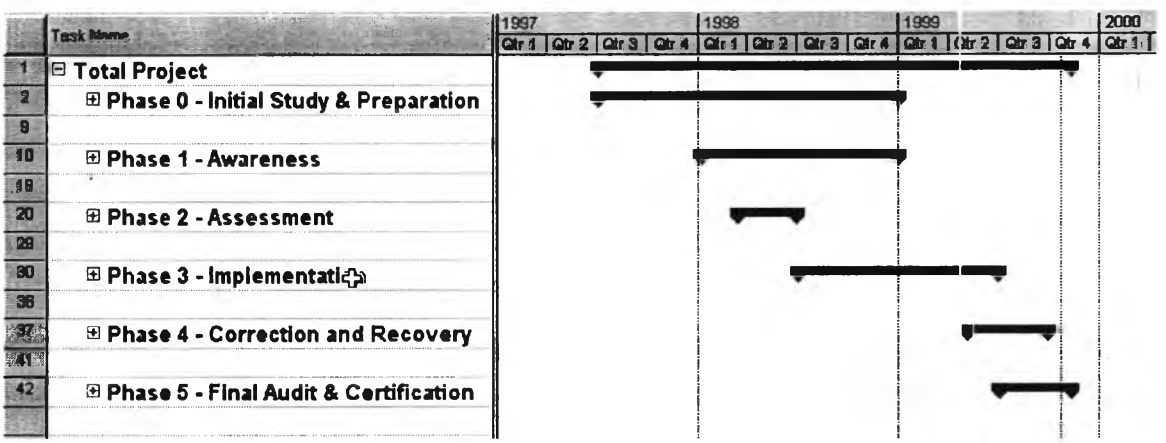

Figure 3.7 : Y2K Project Timeline