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ANALYSIS AND DESIGN OF A 3-STAGE CMOS CURRENT CONTROLLED RING OSCILLATOR

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A Thesis Submitted in Partial Fulfillment of the Requirements
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Thesis Title	ANALYSIS AND DESIGN OF A 3-STAGE CMOS CURRENT CONTROLLED RING OSCILLATOR
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Field of study	Electrical Engineering
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ปรับโต นโกลโฮ การวิเคราะห์และออกแบบวงจรซีมอสริงออสซิลเลเตอร์แบบ 3 ชั้น ควบคุมด้วยกระแส (ANALYSIS AND DESIGN OF A 3-STAGE CMOS CURRENT CONTROLLED RING OSCILLATOR) , อาจารย์ที่ปรึกษา: รองศาสตราจารย์ ดร. เอกชัย ลีลารัศมี

วิทยานิพนธ์นี้นำเสนอหลักการทำงานของวงจรริงออสซิลเลเตอร์ชนิดสามชั้นที่สร้างขึ้นจากเอ็นมอสขับกระแสโหลด และตัวเก็บประจุ วงจรนี้สามารถให้กำเนิดความถี่ ที่เป็นเชิงเส้นกับกระแสโหลด มีชื่อเรียกว่าวงจรซีมอสออสซิลเลเตอร์ควบคุมด้วยกระแส (ซีซีโอ) วงจรนี้ใช้เทคโนโลยีซีมอสขนาด 180 ไมโครเมตร/0.18 ไมโครเมตร กับ โหลดตัวเก็บประจุขนาด 1 พิโคฟารัด สามารถผลิตความถี่ได้ตั้งแต่ 468 เฮิรตซ์ ถึง 305 เมกะเฮิรตซ์ โดยการปรับกระแสโหลดจาก 1 นาโนแอมป์ ถึง 1 มิลลิแอมป์ วิทยานิพนธ์นี้ได้หาสมการที่แสดงความสัมพันธ์ของความถี่ และกระแสที่มีความถูกต้องสูง โดยมีความผิดพลาดเมื่อเทียบกับการจำลองการทำงานด้วยโปรแกรมคอมพิวเตอร์ไม่เกิน 1 % รวมทั้งได้มีการศึกษาผลกระทบของค่าแลมบ์ด้า แต่พบว่าต้องใช้วิธีแก้ปัญหาที่ยุ่งยากซับซ้อน วิทยานิพนธ์นี้จึงได้นำเสนอวงจรที่ดีกว่าเดิมโดยการเพิ่มบัฟเฟอร์ซึ่งจะให้ผลลัพธ์ความถี่ที่เป็นเชิงเส้นมากขึ้น จากนั้นได้ทำการสร้างต้นแบบวงจรซีมอสควบคุมด้วยกระแสที่ให้กำเนิดสัญญาณในช่วง 10 เมกะเฮิรตซ์ ทั้งแบบเดิมและแบบปรับปรุง

ภาควิชา.....วิศวกรรมไฟฟ้า.....ลายมือชื่อนิสิต.....

สาขาวิชา.....วิศวกรรมไฟฟ้า.....

ปีการศึกษา.....2549.....ลายมือชื่ออาจารย์ที่ปรึกษา.....

4870597721 : MAJOR ELECTRICAL ENGINEERING
KEY WORD: CMOS / OSCILLATOR / RING OSCILLATOR / CURRENT CONTROLLED OSCILLATOR (CCO)

PRAPTO NUGROHO, MR. : ANALYSIS AND DESIGN OF A 3-STAGE CMOS CURRENT CONTROLLED RING OSCILLATOR , THESIS ADVISOR: ASSOC. PROF. EKACHAI LEELARASMEE, PH.D, 57pp.

This thesis describes a ring oscillator using 3 stages of an NMOS driving a current load and a capacitor. Its frequency can be shown to increase monotonically with the load current giving rise to the name current controlled oscillator (CCO). The CCO circuit using 180μm/0.18μm NMOS with 1pF load can be tuned to oscillate from 468 Hz to 305 MHz using load current from 1nA to 1mA. An accurate derivation of the formulae relating the frequency with current has been derived. Its calculation result agrees with the simulation result to a high accuracy within 1 %. Then the effect of the channel length modulation has been attempted to derive using the same method, but it is too complicated to be solved.

Original and improved CCO are designed. They have output frequency of 10.02 MHz and 10 MHz respectively. The improved circuit employs additional buffers to make it is considerably more linear than the conventional one.

Department ….Electrical Engineering.. Student's signature .....
Field of study …Electrical Engineering..
Academic year …….2006..... Advisor's signature .....

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Terminology and Symbol

MOS	Metal Oxide Silicon
MOSFET	Metal Oxide Silicon Field Effect Transistor
CMOS	Complementary Metal Oxide Silicon
VCO	Voltage Controlled Oscillator
CCO	Current Controlled Oscillator
RCO	Resistor Controlled Oscillator
PLL	Phase Locked Loop
V_{GS}	Gate-Source Voltage
V_{TH}	Threshold Voltage
V_{DD}	Positive Supply Voltage
V_{SS}	Negative Supply Voltage
GND	Ground
T	Time or Period
I	Current
V	Volt
C	Capacitance
F	Frequency
F_{SIMP}	Frequency of simplified equation

CHAPTER I
INTRODUCTION

1.1 Motivation

An oscillator is a critical component in many electronic systems. It plays an important role in analog and digital circuit design, because it is widely used in communication, signal processing, control systems, sensors and clock generations.

A controlled oscillator is a key component in many communication devices and circuits, especially in this wireless communication era. As the markets emerge, the needs of small and multi function devices are important. A single-chip with capabilities of satisfying several communication standards can dramatically reduce the cost and increase the functionality for communication devices.

A controlled oscillator is usually embedded in a phase-locked system. It generates a clock signal with frequency varied according to its input voltage or current as shown in Fig 1.1.

Various types of controlled oscillator circuits have been extensively reported in the literature. They are based on ring, LC and relaxation oscillators [1].

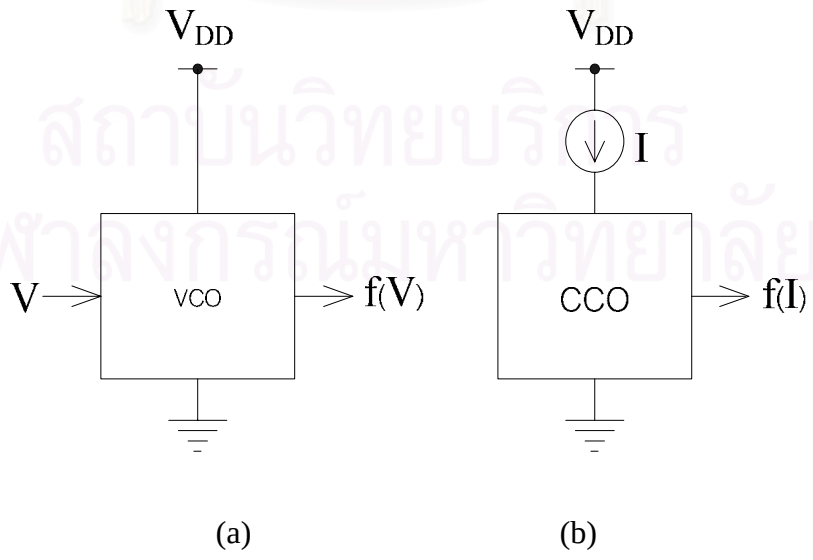


Figure 1.1 A block diagram of a VCO (a) and CCO (b).

LC resonant oscillator has particularly stable frequency. Its frequency of oscillation is defined by the LC resonance. An LC oscillator is also known to have low phase jitter, low tuning range and nonlinear sensitivity. This type of oscillator is more stable than ring or relaxation oscillators, but they are difficult to integrate successfully in bulk and there are limitations on integrated inductor design. With some difficulties, it can be converted to a VCO by replacing a fixed capacitor with a varactor. However, most varactors have limited tuning range, unless several volts can be applied [2]. In other words, typically LC oscillators require the use of either an off-chip inductor which will defeat the goal of integration, or the use of an on-chip inductor which yields poorer jitter performance at the cost of die area [3].

Relaxation oscillator or multivibrator operates by charging / discharging a capacitor. Its frequency varies with V- controlled current source as charging /discharging current but it is sensitive to thermal effect, supply voltage variation, and phase noise. However, temperature stabilized current supplies and controlled threshold voltages minimize these effects [2]. It is usually not a good choice for the present application due to the huge amount of phase noise as a result of positive feedback [4].

Ring Oscillator is very desirable in the VLSI environment because of its integration ability. It is easy to design and easily integrated. Without the need for inductors, the ring oscillator occupies far less die area than a harmonic LC oscillator. It is simple and can be operated at Low-DC level. Unfortunately, the jitter performance of the ring oscillator falls short of the jitter performance of an LC oscillator [5]. CMOS oscillators in today's technology are typically implemented as ring oscillators or LC Oscillators [1].

There are two topologies of ring oscillator, differential and single ended. The differential ring oscillator has higher phase-noise level than the single-ended ring oscillator, with equal power dissipation, frequency and number of stages. The single-ended topology dissipates power on a per transition basis only and therefore has a better phase noise for a given power dissipation. The difference in phase noise becomes even larger when the number of stages increases [3].

Among those types, single-ended ring oscillator is the most importance in digital circuit since they are less affected by supply and substrate noise [4].

We found very rare papers investigating about single-ended ring oscillator in detail. This motivates the needs of such contributions.

1.2 Objectives

This thesis has several objectives:

a) To study / evaluate a 3-stage single-ended CMOS ring oscillator controlled by current.
b) To derive expressions for the oscillation waveform and their periods in terms of the controlling current and size of MOS transistor.
c) To compare the analytical results with the simulated ones for actual MOS characteristics.
d) To design a prototype 10 MHz CMOS ring oscillator.

1.3 Literature Review

This section will present the state of the art and previous works that had been done in the ring oscillator.

There are some designs and analysis proposed using a ring oscillator but we can not find the one that gives detail analysis on Single-ended Current Controlled Ring Oscillator. Some works that have been done by people related to this thesis are listed below:

Basic analysis on 3-stages ring oscillator controlled by resistors is explained by Behzad Razavi [1] in his book, but he didn't give detail analysis.

Per Finnstam and Mikael Söderlune [3] designed and laid out a VCO based ring oscillator on a 0.5-μm BiCMOS process offered by Philips, using Cadence Analog Artist design tool. They used a 7-stage differential ring oscillator.

A current-frequency characteristic of a conventional relaxation oscillator, whose oscillation frequency is controlled by current, is analyzed by K. Yoshizaki, S. Takagi and N. Fujii [6]. They proposed technique to obtain a constant oscillation.

Voltage Controlled Ring Oscillator with wide tuning range and fast voltage swing is proposed by N. Retdian and his group [7] from TITECH, Japan. They are proposed a new design of a voltage controlled ring oscillator. Using the proposed method, a tuning range from 40Hz to 380MHz is achieved. They used single-ended inverter ring oscillator.

A current-controlled sinusoidal oscillator based on the Wien-bridge oscillator is presented by Hervé BARTHELEMY and Alain FABRE [8]. The circuit acts in current mode and uses a second generation current conveyor. Its oscillation frequency, which can be varied from 20 Hz to 90 MHz is adjustable from the bias current of a floating resistor.

Muhammad Taher and Husain Abdullah [9] presented a new current-mode sinusoidal oscillator circuits obtained from a voltage-mode two-operational-amplifier based oscillator circuit by replacing the operational amplifiers with four-terminal floating-nullors (FTFNs). The properties of the resulting oscillators are discussed and the theory is supported by SPICE simulation and experimental verification.

A current-controlled oscillator implemented in CMOS technology is presented by M.A.A. El Atta et al [10]. The oscillator utilizes a Schmitt-trigger, pass transistors, current mirrors and grounded capacitor with 3V power supplies.

A CCO as a part of PLL proposed by Behzad Razavi et al. [17] as part of PLL, It is used for high frequency (GHz) and fabricated in 0.1mm, but only a little explanation about the CCO.

A current controlled ring oscillator is utilized in a phase locked loop system was registered on US patent no.4091335 [18]. It use PNP current sources and Schottky clamped NPN transistors to provide a frequency range of 4 MHz at 50mA drive to 43 MHz at 1mA drive. The frequency of the ring oscillator is varied by varying the current injected into the ring.

A Multistage CCO is registered on US patent no.5028888, [19]. It use two current sources but doesn't provide detail analysis.

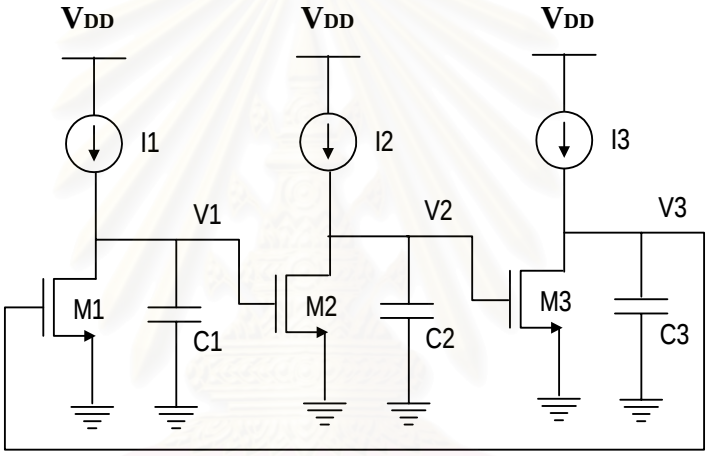
1.4 Scope of Thesis

1. Only CCOs are studied for period of oscillation.
2. Analysis assuming ideal switch will be first considered.

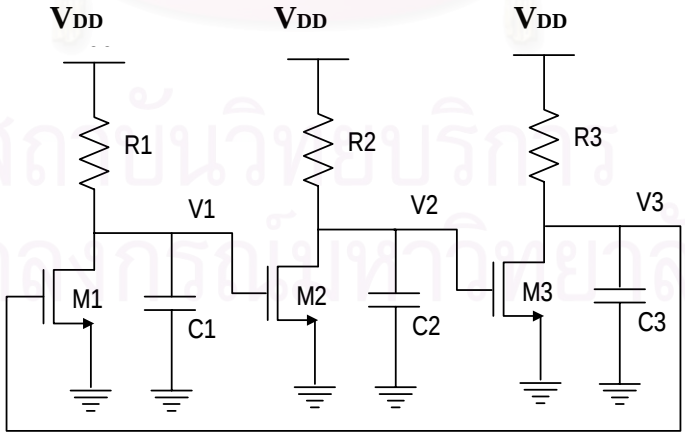
3. Effect of transistor size, i.e. W/L, and load current will be studied.
4. Computer simulation will be used to verify and compare its analytical result with actual MOS model.
5. A sample 10 MHz oscillator for 1.5 Volt DC supply will be demonstrated.

1.5 Research Procedure

The CMOS CCO proposed in this thesis is based on a 3-stage inverting ring oscillator [1]. However, rather than using a CMOS static inverter or an NMOS inverting device driving a PMOS resistive load, our inverting stage uses an NMOS device driving



(a)



(b)

Figure 1.2 A 3-stage ring CMOS ring oscillator using load current (a) and resistor (b).

a current source *I* together with an output capacitor *C* as shown in Fig. 1.2 (a). Thus its power consumption depends directly on *I* and there is no V_{DD} supply current spike typically found in a static inverter. As a comparison, another well known types controlled by resistor (RCO) is shown in Fig.1.2 (b).

There are some important properties we want to investigate from CCO in Fig.1.2:

1) Tuning range defined in term of its max/min frequency ratio.
2) Tuning linearity specifying how linear its frequency is with respect to load.
3) Derivation of their period in term of (I, W/L, C) or (R, W/L, C) as well as their waveform**.**
4) Analyze and simulate controlled oscillators in ideal and with the effect of λ
5) Analyze the results in term of
   a. Frequency of oscillation as a function of I, R or V_{DD}
   b. Maximum Amplitude
   c. Voltage Waveform

This thesis will be conducted in several steps, which are:

1. Studying Current Controlled Oscillator.

2. Preparing proposal and proposal defense.

3. Studying the effect of W/L and load current.

4. Simulating and verifying the result.

5. Designing a sample of 10 MHz oscillator.

6. Organizing all documents and writing the thesis.

1.6 Research Goals

The results or contributions from this work are summarized below:

- Detail analysis on a Current Controlled Oscillator circuit.
- Proposed better circuit in term of linearity.
- International conference paper.

1.7 Publications Included in the Thesis

Paper I:

P.Nugroho, E. Leelarasmee, N. Fujii, "**Tuning Analysis of a CMOS Current Controlled Ring Oscillator**", in *Proceedings of The 21th International Technical Conference on Circuits/System, Computer and Communication***,** Pang Suan Keaw Hotel, Chiang Mai, July 10-13, 2006 [11].

1.8 Thesis structure

This thesis is structured in the following chapters.

• Chapter 2 presents the basic theory related to these works.

• Chapter 3 presents the analyses of the CCO circuit.

• Chapter 4 describes the design of proposed circuit and 10 MHz Oscillator.

• Finally, Chapter 5 summarizes and recommend for future work.

CHAPTER II
BACKGROUND THEORY

2.1 Basic MOS

2.1.1 MOSFET as a switch

MOSFET is often considered as a switch to simplify the model of device before going into the actual operation. When operated as switch, the source and the drain is "ON", i.e. short circuit, if the gate is high ($V_{GS} > V_{TH}$), and "OFF", i.e. open circuit, if the gate is low ($V_{GS} < V_{TH}$) as can be seen in Fig.2.1. Another figure that use NMOS and PMOS as active "High" and active "Low" model is shown on Fig, 2.2.

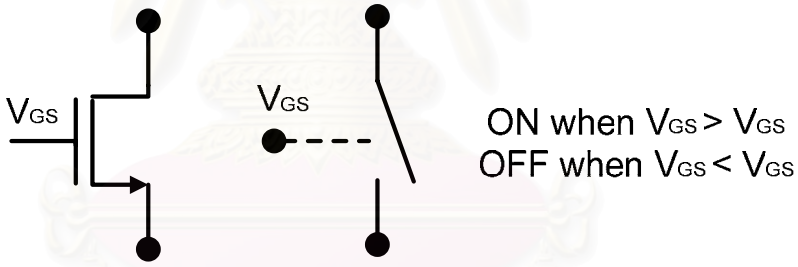


Figure 2.1 The switch model of an NMOS.

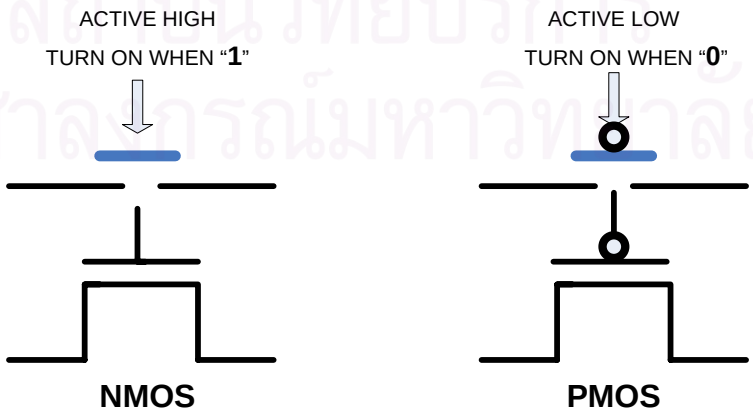


Figure 2.2 Active high and active low switch models.

2.1.2 MOS Characteristics

There are two things we should learn about this MOS characteristic; they are threshold voltage and *I/V* characteristics.

A. Threshold Voltage

To turn on an MOS, a minimum V_{GS} (Gate-Source Voltage) called V_{TH} (threshold voltage) must be applied. Typically V_{TH} is 0.4 to 0.8V. Even at $V_{GS} = V_{TH}$ conduction is poor. One needs a voltage many times higher to give a low channel resistance. Theoretically, the threshold voltage is simply the applied gate-to-source voltage needed to turn on a MOS device. The threshold voltage for a uniformly doped long channel device can be approximated by solving the one-dimensional Poisson's equation:

For an n-channel device

$$V_{TH} = V_{FB} + 2|\varphi_p| + \frac{1}{c_i}\sqrt{2\varepsilon_S q N_a \left(2|\varphi_p| - V_B\right)} \tag{2.1}$$

For a p channel device

$$V_{TH} = V_{FB} - 2|\varphi_N| - \frac{1}{c_i}\sqrt{2\varepsilon_S q N_d \left(2|\varphi_n| - V_B\right)} \tag{2.2}$$

Where V_{FB} is the flat-band voltage, c_i is the insulator capacitance, q is the charge carrier density, ε_s is the dielectric permittivity of the semiconductor and V_B is the bulk bias.

While

$$\varphi_n = \frac{kT}{q}\ln\left(\frac{N_d}{n_i}\right) \quad \text{and} \quad \varphi_n = -\frac{kT}{q}\ln\left(\frac{N_a}{n_i}\right) \tag{2.3}$$

are Fermi potentials of the *n*- and *p*-channel MOS device structures; N_a and N_d are the acceptor and donor dopant concentrations in the substrates respectively, *k* is Boltzmann constant, *T* is the absolute temperature and n_i is the intrinsic electron density.

Note that the threshold voltage is strongly dependent on doping concentration. As we increase the doping level, the threshold voltage becomes more positive for an *n*-channel and more negative in a *p*-channel device [12].

B. Channel-length modulation

Zeghbroeck [13] has described channel-length modulation as follows:

When the drain-source bias of a FET approaches the drain saturation voltage, a region of high electric field forms near the drain and the electron velocity in this region saturates.

In saturation, the length ΔL of the high-field region expands in the direction of the source with increasing drain-source voltage. The MOSFET behaves as if the effective channel length has been reduced by ΔL. This phenomenon is called channel-length modulation (CLM). The following simplified expression links V_{DS} to the length of the saturated region:

$$V_{DS} = V_p + V_\alpha \left[\exp\left(\frac{\Delta L}{\ell} \right) - 1 \right] \tag{2.4}$$

Where V_p and V_α and ℓ are parameters related to the electron saturation velocity, the field effect mobility, and the drain conductance in the saturation regime. In fact, it is the potential at the point of saturation in the channel, which is usually approximated by the saturation voltage (V_{DSAT}). The CLM effect can be modeled as an output conductance in saturation, which tends to remain constant over a wide range of drain biases. The output conductance decreases with increasing the nominal channel length.

C. *I/V* characteristics

Hussein [12] has described *I/V* characteristics as follows:

To obtain the relationships between the drain current of a MOSFET and its terminal voltages, we make two observations.

First, consider a semiconductor bar carrying current *I*. If the charge density along the direction of current is Q_d coulombs per meter with the velocity v meters per second, then

$$I = Q_d.v \tag{2.5}$$

Secondly, consider an NFET whose source and drain are connected to ground. Assuming the onside of inversion occurs at $V_{GS} = V_{TH}$, the inversion charge density produced by gate oxide capacitance is proportional to $V_{GS} - V_{TH}$. For $V_{GS} \geq V_{TH}$, the gate will mirror any charge placed on it by the charge in the channel that yields a uniform channel charge density (charge per unit length) according to

$$Q_d = WC_{ox}\left(V_{GS} - V_{TH}\right) \tag{2.6}$$

where C_{OX} is multiplied by the channel width to represent the total capacitance per unit length. Suppose the drain voltage is greater than zero. Since the channel potential varies from zero at the source to V_D at the drain, the difference between the gate and channel varies from V_G to V_G-V_D. Thus, the charge density at point *x* along channel can be written as

$$Q_d(x) = WC_{ox}\left[V_{GS} - V(x) - V_{TH}\right] \tag{2.7}$$

Combining with (2.5) we get

$$I = -WC_{ox}\left[V_{GS} - V(x) - V_{TH}\right]v \tag{2.8}$$

where the negative sign is inserted because the carrier is negative.

Since $v = \mu_n \frac{dV(x)}{dx}$, we have

$$I = -WC_{ox}\left[V_{GS} - V(x) - V_{TH}\right]\mu \frac{dV(x)}{dx} \tag{2.9}$$

Multiplying both sides by dx, and performing integration, we obtain

$$\int_{x=0}^{L} I_d\, dx = \int_{V=0}^{V_{DS}} WC_{ox}\mu_n\left[V_{GS} - V(x) - V_{TH}\right]dV \tag{2.2}$$

Because I_D is constant along the channel, the integration yields

$$I_D = \mu_n C_{ox} \frac{W}{L}\left[\left(V_{GS} - V_{TH}\right)V_{DS} - \frac{1}{2}V_{DS}^{\ 2}\right] \tag{2.11}$$

where L is the effective channel length.

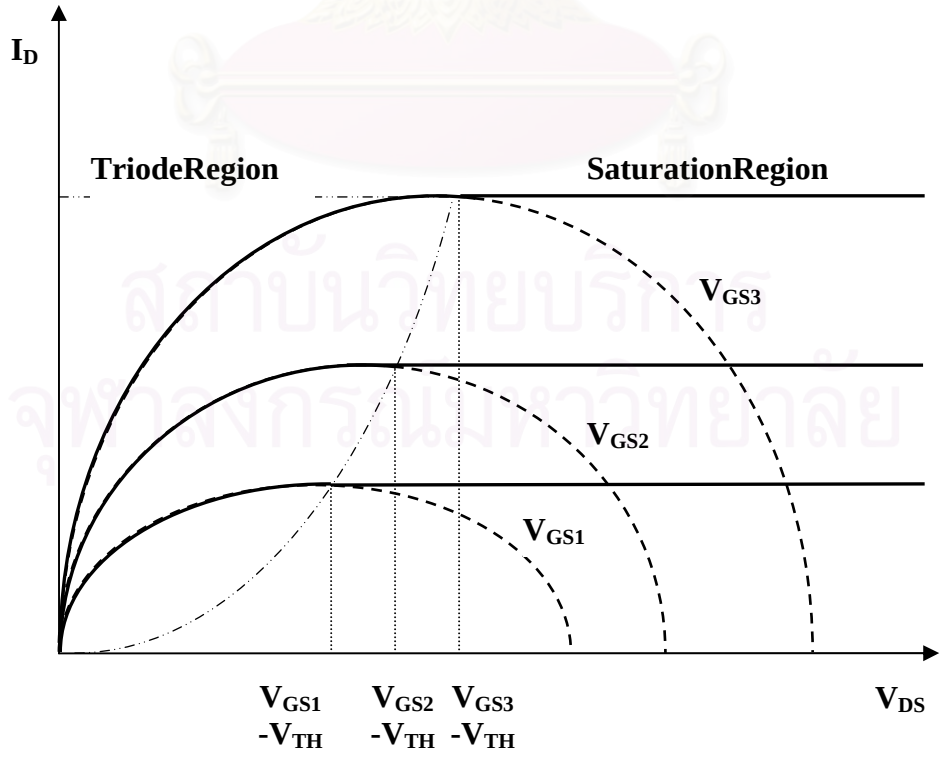


Figure 2.3 Drain current vs. drain-source voltages.

Fig. 2.3 plots the parabolas for different values of V_{GS}, indicating that the "current capabilities" of the device increases with V_{GS}.

We can show that the peak of the parabola occurs at $V_{DS} = V_{GS} - V_{TH}$ and the peak current is

$$I_{D,\max} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2 \tag{2.12}$$

$V_{GS} - V_{TH}$ is called "overdrive voltage" and W/L the "aspect ratio." If $V_{DS} \leq V_{GS} - V_{TH}$, it can be said the device operates in the "triode region". Since a MOSFET operating in saturation produces a current in response to its gate-source overdrive voltage, we may define figure of merit that indicates how well a device converts a voltage to current. More specifically we define the figure of merit as the change in the drain current divided by the change in the gate-source voltage. Called "transconductance" and denoted by g_m, it is expressed as:

$$g_m = \frac{\partial I_D}{\partial V_{GS}}\Big|_{V_{DS},const} \tag{2.13}$$

$$g_m = \mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH}) \tag{2.14}$$

If $V_{DS} << 2\,(V_{GS} - V_{TH})$

$$I_{D,\max} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})V_{DS} \tag{2.15}$$

The drain current is a linear function of V_{DS}. The linear relationships implies that the path from the source to the drain can be represented by a linear resistor equal to

$$R_{on} = \frac{1}{\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})} \tag{2.16}$$

On the channel length modulation, the current equation became

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2(1+\lambda V_{DS}) \tag{2.17}$$

So that

$$g_m = \sqrt{\frac{2\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})I_D}{1+\lambda V_{DS}}} \tag{2.18}$$

.

2.1.3 Basic MOSFET Current Mirror

A **current mirror** is a circuit designed to copy a current flowing through one active device by controlling the current in another active device of a circuit. The output current kept constant regardless of loading which could be different in amount.

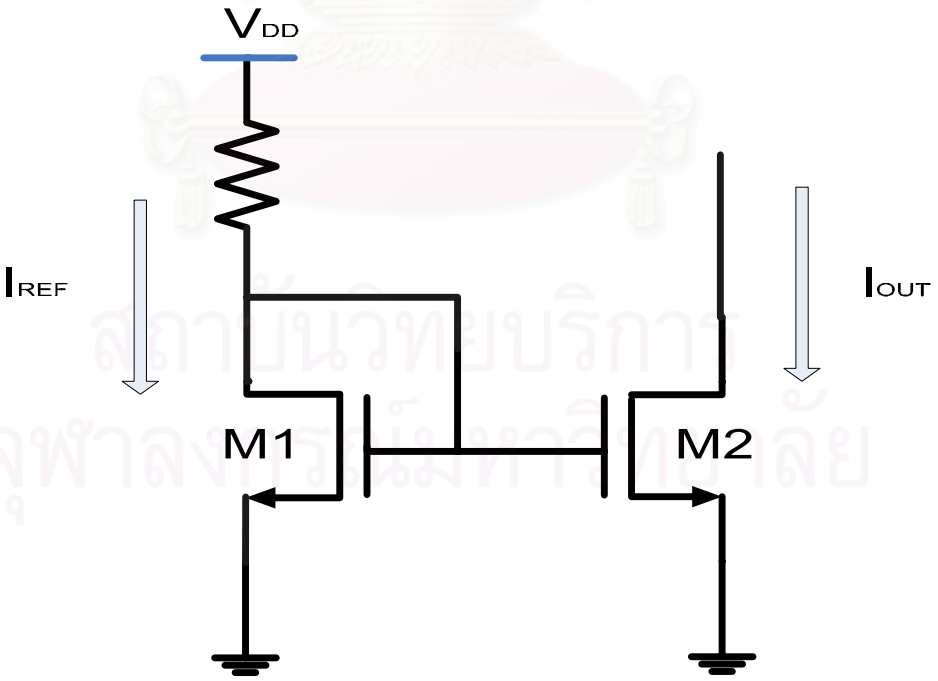


Figure 2.4 Simple current mirror.

A current mirror can be implemented with BJT or MOSFET. In this thesis we use a MOSFET current mirror as shown in Fig. 2.4.

The operation of current mirror can be described as follows. Transistor M1 with its Drain (D) and Gate (G) connected (or $V_{GS} = V_{DS}$) is operating in the saturation region. Since V_{GS} of M2 is equal to V_{GS} of M1 ($V_{GS1} = V_{GS2}$), ideally the current flows through M2 (I_{D2}) will be equal to the current flowing through M1 (I_{D1}). In this system, the output current I_{out} is flowing through M2 and I_{D1} will be input and is called I_{ref}. The circuit will work if other parameters on both transistors are equal or have the same values. The current I_D is given by

$$I_{D1} = \frac{\mu_n C_{ox}}{2}\frac{W_1}{L}\left(V_{GS1} - V_{THN}\right)^2 \tag{2.20}$$

$$I_{D2} = \frac{\mu_n C_{ox}}{2}\frac{W_2}{L}\left(V_{GS2} - V_{THN}\right)^2 \tag{2.21}$$

Since $V_{GS1} = V_{GS2}$, the ratio is given by

$$\frac{I_{D2}}{I_{D1}} = \frac{W_2 L_1}{W_1 L_2} \tag{2.22}$$

The reference drain current is determine by

$$I_{D1} = \frac{V_{DD} - V_{GS}}{R} = \frac{\mu_n C_{ox} W_1}{2L_1}\left(V_{GS} - V_{TH}\right)^2 \tag{2.23}$$

The minimum voltage (V_{MIN}) across the current sink is set by the requirement that M2 remains in saturation. That is $V_{MIN} = V_{DS,\,SAT} = V_{GS} - V_{TH}$.

By picking the same lengths for all MOSFETs in the current mirror, it will simplify Eq. (2.22) to

$$\frac{I_{D2}}{I_{D1}} = \frac{W_2}{W_1} \tag{2.24}$$

This simple current source can be developed to built more than one MOSFET mirrors so that $I_1 = I_2 = I_3 = \ldots\ldots = I_N$, as can be seen in Fig.2.5.

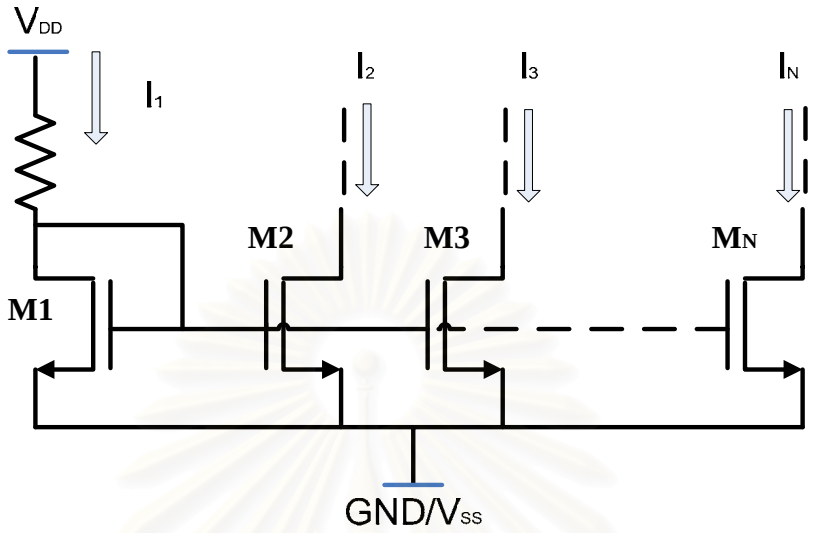


Figure 2.5 Current mirror arrays.

2.1.4 CMOS Inverter

There are a few kinds of CMOS inverters such as a pseudo NMOS inverter and a complementary CMOS inverter as shown in Fig 2.6.

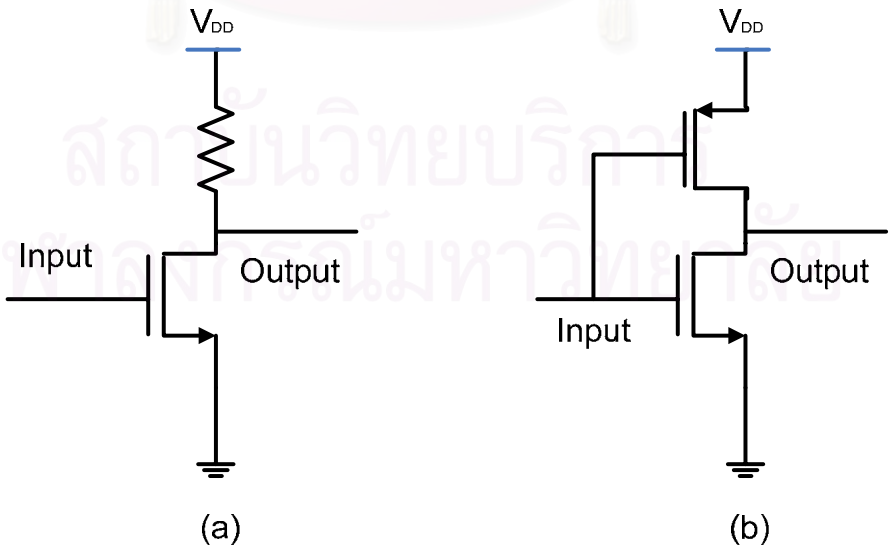


Figure 2.6 (a) Pseudo NMOS inverter (b) and Complementary CMOS inverter

2.2 Oscillator Theory

2.2.1 Barkhausen criteria

An oscillator is a circuit that produces a periodic signal, without any specific input signal except internal noise. An oscillator can be viewed as a feedback system, as shown in Fig.2.7. Its transfer function is given by:

$$\frac{V_{out}}{V_{in}}(s) = \frac{H(s)}{1+H(s)} \tag{2.25}$$

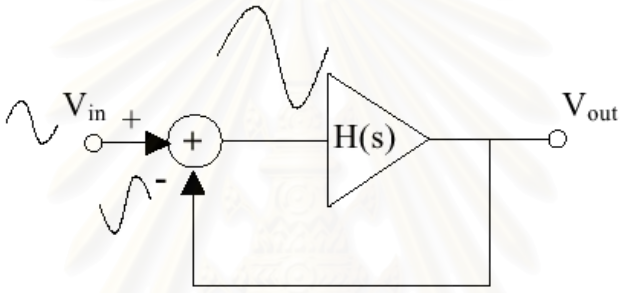


Figure 2.7 Feedback systems.

It can be seen that the close loop gain will approaches infinity at ω_o if $H(j\omega_o) = -1$. The circuit will oscillate if it satisfies two conditions:

$$|H(j\omega_o)| \geq 1 \tag{2.26}$$

$$\angle H(j\omega_o) = 180^o \tag{2.27}$$

These are called “Barkhausen criteria” [1].

These criteria mean that the returning signal is a negative replica of the input signal, which will give a larger difference between the input signal and the feedback signal when subtracting. The circuit is said to be regenerated.

Barkhausen criteria are not so accurate for all type of signal. It is mostly used for sinusoidal. However, ring oscillator is usually non-sinusoidal. Therefore, we can not use barkhausen criteria for determining the frequency of oscillation accurately.

2.2.2 LC oscillator

An LC oscillator is a resonance circuit. An inductor in parallel with a capacitor and a parasitic resistance constitute the resonator, also known as the LC tank. Electromagnetic oscillation occurs in the LC tank when energy is transferred between the capacitor and the inductor.

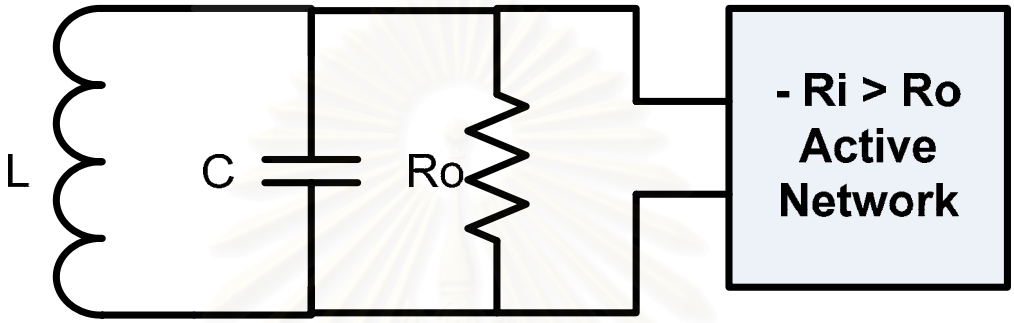


Figure 2.8 A simple LC oscillator model.

Part of the stored energy is dissipated in Ro when the LC tank oscillates. An active network is then introduced in the circuit to compensate for this loss. To ensure continuous oscillation, the active network is designed to generate a negative admittance smaller than Ro so that the total resistance in the circuit is negative. The oscillation frequency is set by the tank inductance and capacitance value.

2.2.3 Relaxation oscillator

A **relaxation oscillator** is an oscillator in which a capacitor is charged and discharged gradually. It is a circuit that repeatedly alternates between two states at a period that depends on the charging of a capacitor.

The capacitor is charged through the resistor, causing its voltage to rise exponentially. In parallel with the capacitor is the threshold device. Such device doesn't conduct at all until the voltage across them reaches some threshold (trigger) voltage. It then conducts heavily and discharges the capacitor. When the voltage across the capacitor drops to some lower threshold voltage, the device stops conducting and the

capacitor can begin charging again, repeating the cycle. If the threshold element is a neon lamp, the circuit also provides a flash of light with each discharge of the capacitor.

The electrical output of a relaxation oscillator is usually a triangular or sawtooth wave. If only a small portion of the exponential ramp is used (that is, if the triggering voltage of the threshold device is much lower than the charging voltage source), the ramp will approximate a linear ramp. However, if a truly linear sawtooth is required, the charging resistor should be replaced by some sort of constant current source [14].

2.2.4 Ring Oscillator

A ring oscillator consists of a number of amplifiers in a feedback loop. To get the ring oscillator to oscillate there needs to be at least three amplifiers. This is to fulfill the first criterion of a sufficient phase shift of 180°. The second criterion for oscillation is met if the closed loop gain is greater than 1 [1].

A. Topologies of Ring Oscillator

There are two main topologies for the ring oscillator. They are the differential and the single-ended ones as shown in Fig.2.9 where N = Number of Stages.

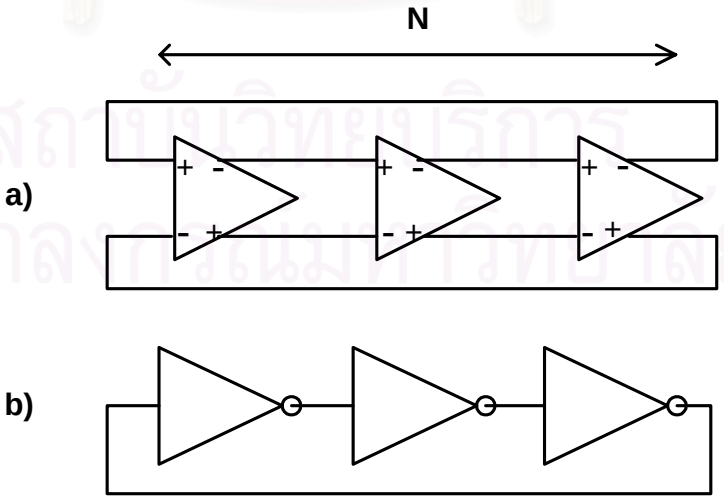


Figure 2.9 (a) Differential topology (b) Single-ended topology.

B. Single-ended Topology

The common basic single-ended topology consists of CMOS inverters, shown in the figure 2.10.

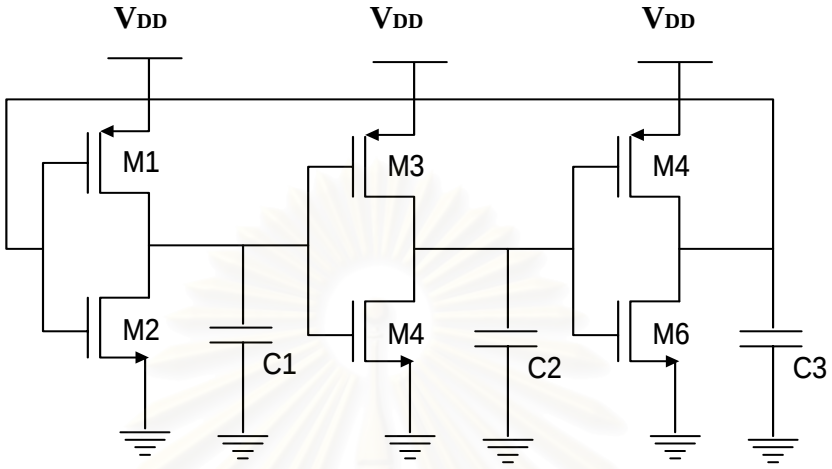


Figure 2.10 Single-ended 3-stage CMOS ring oscillator

The load PMOS can be replaced by resistors or current sources as we are going to do.

C. Differential Topology

The differential topology comprises a load and an NMOS differential pair, shown in Fig. 2.11. The load can consist of a resistor for fixed frequency or PMOS devices, which makes the oscillator tunable with a voltage.

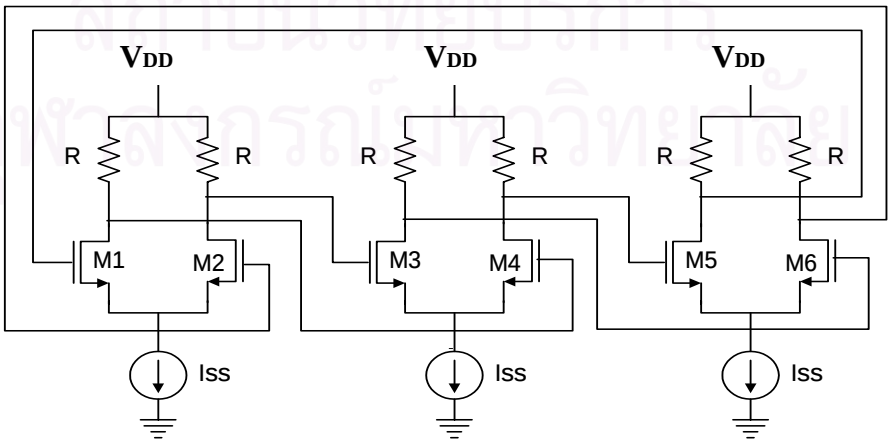


Figure 2.11 Differential CMOS ring oscillator

D. Single-ended vs. Differential Topology.

The differential ring oscillator has higher phase-noise level than the single-ended ring oscillator, with equal power dissipation, frequency and number of stages [3].

The single-ended topology dissipates power on a per transition basis only and therefore has a better phase noise for a given power dissipation. The difference in phase noise becomes even larger when the number of stages increases [3].

Single-ended ring oscillators are most importance in digital circuit since they are less affected by supply and substrate noise [15].

This motivates us to analyze CMOS ring oscillators. This thesis will present detailed analysis on two types of single-ended CMOS ring oscillator controlled by current and resistor.

CHAPTER III
ANALYZING CCO

3.1 Tuning Analysis of a CMOS CCO [11]

3.1.1 Introduction

A voltage controlled oscillator (VCO) is a key component in many communication devices and circuits. It generates a clock signal with frequency varied according to its input voltage.

Various types of VCO circuits have been extensively reported in the literature. They are ring [1], LC [1] and relaxation [2] oscillators. Three important properties of a controlled oscillator are:

1) Tuning range defined in term of its max/min frequency ratio. Due to process and temperature variations, a tuning range of more than a factor of 2 is preferred.
2) Phase jitter corresponding to the effect on its frequency due to the internal noise. A low jitter is preferred than a higher one.
3) Tuning linearity specifying how linear its frequency is with respect to V. A linear sensitivity is required if the VCO is to be implemented as a spread spectrum clock oscillator [3]. When implemented in a phase lock loop, nonlinearity is also shown to degrade its settling behavior [4].

In many cases, these properties impose conflicting design constraints. For example, an LC CMOS oscillator is known to have low phase jitter, low tuning range and nonlinear sensitivity, but it is difficult to integrate in bulk. A Ring Oscillator is more desirable in VLSI environment because of its integration ability, even though worse in jitter performance than the LC oscillator [5].

This chapter presents the analysis and design of another type of CMOS oscillator in which its frequency varies almost linearly with its load current source and is better referred to as a current controlled oscillator (CCO).

3.1.2 Circuit Architecture and Simplified Analysis

The CMOS CCO proposed in this paper is based on a 3-stage inverting ring oscillator [1]. However, rather than using a CMOS static inverter or a NMOS inverting device driving a PMOS resistive load, our inverting stage uses a NMOS device driving a current source *I* together with an output capacitor *C* as shown in Fig. 3.1. Thus its power consumption depends directly on *I* and there is no V_{DD} supply current spike typically found in a static inverter.

We shall first make a simplified analysis of this circuit by using a switch model of the NMOS, i.e. a NMOS becomes short circuited when its gate-source voltage V_{GS} exceeds its threshold voltage V_{TH}. This assumption is valid when the width (W) of the NMOS is sufficiently large compared with its length (L).

From the switch model, we note that only one NMOS can turn on at any given time. Since the three NMOS devices are identical, the total period *T* must be divided equally by the ON duration of each transistor and the transition from OFF to ON of a device must occur at the middle of the OFF interval of the preceding device as shown in Fig. 3.2. So a NMOS, e.g. M1, is ON for $T/3$ when its output V_1 is zero and OFF for another $2T/3$ during which its output capacitor is charged by the constant current *I*. Thus V_1 rises from zero at a slope of I/C as shown in the top waveform in Fig. 3.2 and will turn on M2 after ramping for $T/3$ when its value reaches V_{TH}.

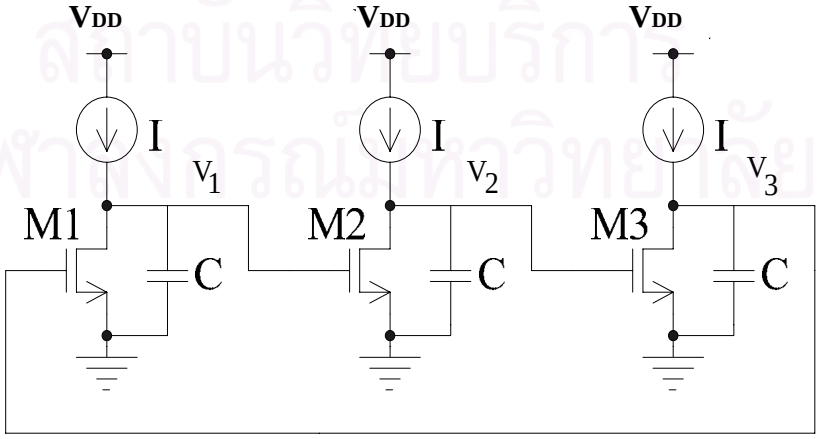


Figure 3.1 A CMOS 3-Stage Inverting Ring Oscillator Using Current Load

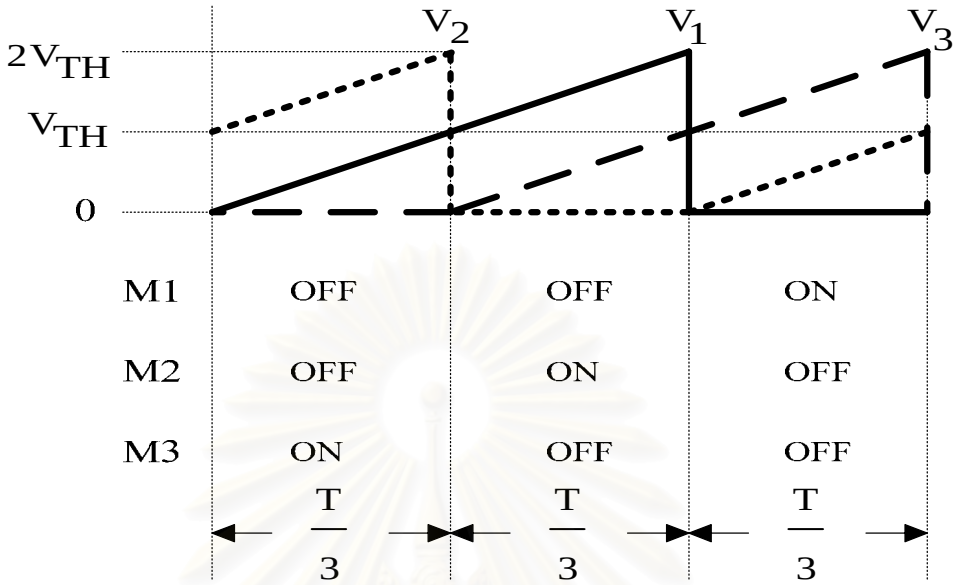


Figure 3.2 Simplified steady state oscillating waveforms

Therefore we now have the formulae for obtaining the period of oscillation as follows

$$\frac{I}{C}\times\frac{T}{3}=V_{TH} \quad \text{or} \quad T=3\frac{C}{I}V_{TH}$$

Thus $$f=\frac{1}{T}=\frac{I}{3CV_{TH}} \tag{3.1}$$

This shows that the frequency varies linearly with *I*. This is a desirable property for a Phase Lock Loop application. Also its power consumption $3V_{DD}$ *x I* depends linearly on *I* and there is no V_{DD} supply current spike. Since the OFF duration is $2T/3$, the maximum output voltage is $2V_{TH}$. Hence the minimum V_{DD} supply that the circuit can operate is

$$V_{DD}(\min)=2V_{TH}+V_{CS}$$

where V_{CS} is the minimum operating voltage of the current source. If the current source is implemented by a simple PMOS device, V_{CS} can be as low as its overdrive

voltage. Using a low threshold voltage CMOS technology, the circuit can operate at a low DC supply voltage of 1.5V.

3.1.3 The effect of the size of the NMOS

In practice, a NMOS with a finite width (W) and length (L) cannot behave as an ideal short circuit, i.e. having zero resistance when it turns on. This means that the circuit needs a small duration (δ) for discharging each output capacitor until its voltage is low enough to turn off the succeeding device as shown in Fig. 3.3, i.e. there are two ON devices during this interval. This will have an increasing effect on its period of oscillation (T) which is derived as follows

Note from the figure that each capacitor is charged by the constant current I from V_L at the beginning to V_{TH} after $T/3 - \delta$ interval and to V_H after another $T/3$ interval. Thus we have that

$$V_{TH} = V_L + \frac{I}{C}\left(\frac{T}{3} - \delta\right) \tag{3.2}$$

$$V_H = V_{TH} + \frac{I}{C}\frac{T}{3} \tag{3.3}$$

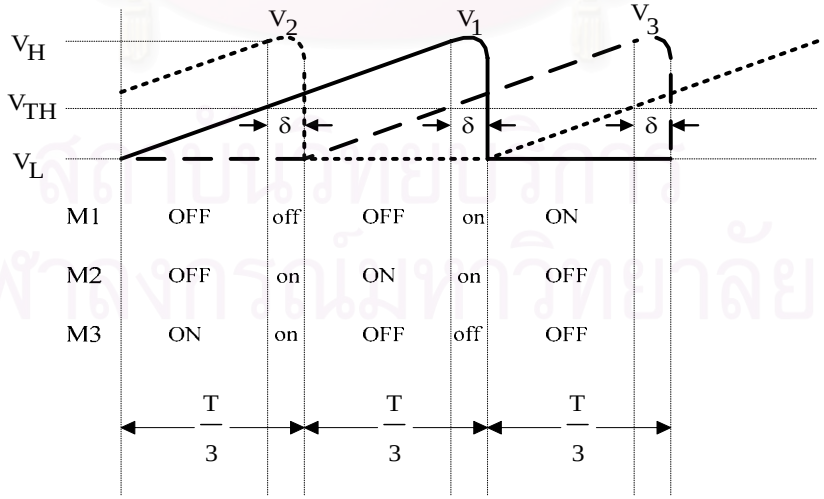


Figure 3.3 Steady state waveforms when each NMOS has finite W and L

where $V_L \approx 0$ is the minimum drain voltage of a NMOS to carry I.

After this, the NMOS is gradually turned on by its ramping input, i.e.

$$V_{GS} = V_{TH} + \frac{I}{C}t$$

Thus the capacitor voltage can still rise from V_H but will quickly decay to V_{TH} after duration of δ to start turning off the next device. The dynamic equation during this duration is

$$C\frac{dv}{dt} = I - \frac{\beta}{2}[V_{GS} - V_{TH}]^2 = I - \frac{1}{2}\beta\left[\frac{I}{C}t\right]^2 \tag{3.4}$$

Where $v(0) = V_H$, $v(\delta) = V_{TH}$ and $\beta = \mu_n C_{ox}\frac{W}{L}$.

Notice that the second term in the right hand side of the differential equation is the current due to the NMOS device and depends on its size. Integrating this equation from $t = 0$ to $t = \delta$, we get

$$V_{TH} - V_H = \frac{I}{C}\delta - \frac{\beta I^2}{6C^3}\delta^3 \tag{3.5}$$

After some algebraic manipulation with (3.2), (3.3) and (3.5), we have

$$x^3 + mx - n = 0 \tag{3.6}$$

Where $x = \frac{I}{C}\delta$, $m = -\frac{12I}{\beta}$, and $n = \frac{6I}{\beta}(V_{TH} - V_L)$.

This is a cubic equation with one real root given by [16]

Using viesta's substitution

$$x = w - \frac{m}{3w} - n = 0, \tag{3.7}$$

this reduces the cubic equation to the equation

$$w^3 - \frac{m^3}{27w^3} - n = 0 \tag{3.8}$$

It is turned to the quadratic equation again in w^3 by multiplying through by w^3

$$(w^3)^2 - n(w^3) - \frac{1}{27}m^3 = 0 \tag{3.9}$$

The result from the quadratic formula

$$w = \sqrt[3]{\frac{n}{2} + \sqrt{\frac{n^2}{4} + \frac{m^3}{27}}} + \sqrt[3]{\frac{n}{2} - \sqrt{\frac{n^2}{4} + \frac{m^3}{27}}} \tag{3.10}$$

Change it back to equation (3.7) we get

$$\frac{I}{C}\delta = x = \sqrt[3]{\frac{n}{2}+\sqrt{\frac{n^2}{4}+\frac{m^3}{27}}}+\sqrt[3]{\frac{n}{2}-\sqrt{\frac{n^2}{4}+\frac{m^3}{27}}}-\frac{m}{3\left[\sqrt[3]{\frac{n}{2}+\sqrt{\frac{n^2}{4}+\frac{m^3}{27}}}+\sqrt[3]{\frac{n}{2}-\sqrt{\frac{n^2}{4}+\frac{m^3}{27}}}\right]} \tag{3.11}$$

From (3.2) and (3.11), we have

$$\frac{I}{3C}T = (V_{TH}-V_L)+\frac{I}{C}\delta \tag{3.12}$$

Hence

$$T = \frac{3C}{I}\left[(V_{TH}-V_L)+\sqrt[3]{\frac{n}{2}+\sqrt{\frac{n^2}{4}+\frac{m^3}{27}}}+\sqrt[3]{\frac{n}{2}-\sqrt{\frac{n^2}{4}+\frac{m^3}{27}}}-\frac{m}{3\left[\sqrt[3]{\frac{n}{2}+\sqrt{\frac{n^2}{4}+\frac{m^3}{27}}}+\sqrt[3]{\frac{n}{2}-\sqrt{\frac{n^2}{4}+\frac{m^3}{27}}}\right]}\right] \tag{3.13}$$

And

$$F = \frac{I}{3C}\left[\frac{1}{(V_{TH}-V_L)+\sqrt[3]{\frac{n}{2}+\sqrt{\frac{n^2}{4}+\frac{m^3}{27}}}+\sqrt[3]{\frac{n}{2}-\sqrt{\frac{n^2}{4}+\frac{m^3}{27}}}-\frac{m}{3\left[\sqrt[3]{\frac{n}{2}+\sqrt{\frac{n^2}{4}+\frac{m^3}{27}}}+\sqrt[3]{\frac{n}{2}-\sqrt{\frac{n^2}{4}+\frac{m^3}{27}}}\right]}}\right] \tag{3.14}$$

These give an exact formula for determining *T* and *F*. However, we prefer to simplify it by assuming that W/L is large enough so as to make $V_L \approx 0$ and $n^2 >> m^3$. Thus we have

$$F_{SIMP} = \frac{1}{T} \approx \frac{I}{3C}\times\frac{1}{V_{TH}+\sqrt[3]{6IV_{TH}/\beta}}$$

$$\approx \frac{I}{3CV_{TH}}\left(1-\sqrt[3]{\frac{6I}{\beta V_{TH}^2}}\right) \tag{3.15}$$

We now see that the size of NMOS, or β, gives rise to a nonlinear term in F_{SIMP}. Where *F* is frequency using Eq.3.14 and F_{SIMP} is frequency as simplification of Eq.3.14.

3.1.4 Experimental Result

The circuit in Fig. 3.1 was simulated with the following parameters: Level = 1, V_{DD} = 3V, W = 180µm, L = 0.18µm, V_{TH} = 0.7Volt, C = 1pF and µCox = 120µA/V^2. Load current vary from 1nA to 1mA, with 0.1mA increment. The result waveform is shown in Fig.3.4 and Fig.3.5

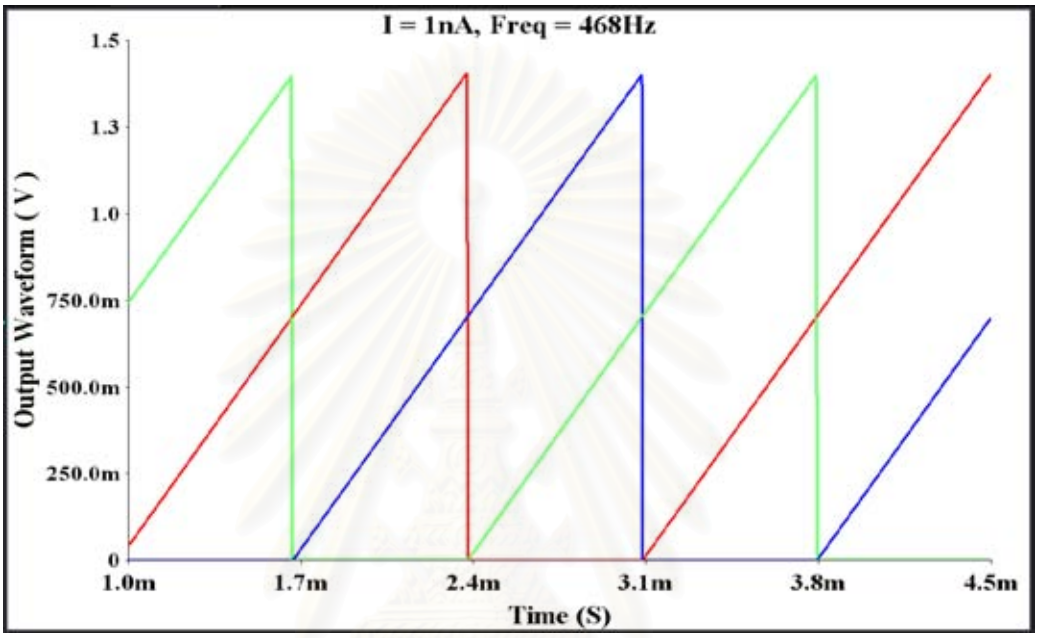


Figure 3.4 Output waveform, I = 1nA, Freq. = 468Hz

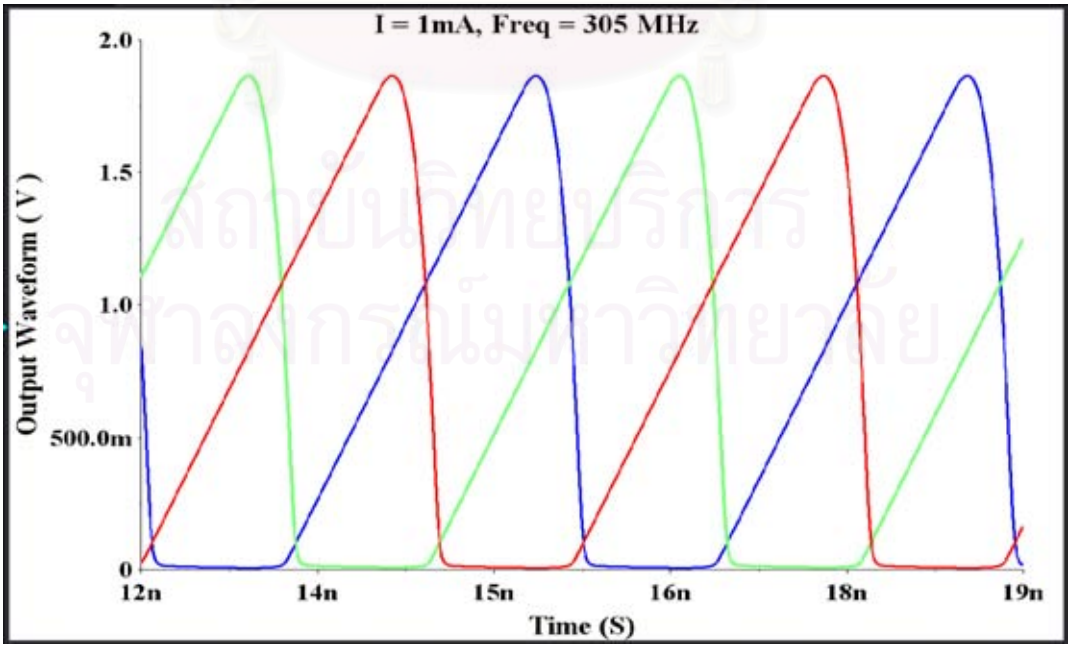


Figure 3.5 Output waveform, I = 1mA, Freq. = 305 MHz

The waveform shows that the higher the current, the higher the frequency and the higher delay we got. This shows the agreement with the theory mentioned in the previous pages.

The frequencies of the simulated waveform at different values of *I* are measured and plotted in Fig.3.6 compared with the predicted values from Eq.3.14 to show their relation. The result shows a very accurate comparison between prediction or calculation and the actual output frequency. In the same figure we can see also the comparison the graphic using Eq. 3.15, the graphic shows a small error when used W =180μm with current below 2mA, so that we can use this equation instead of Eq.3.14 that is more complicated then Eq.15, when used under the circumstance stated above.

The effects of the size of the NMOS are shown in Fig.3.7 and 3.8. In Fig 3.7, we use 3 size of W. They are W=18μm, W=180μm and W=1800μm. The graph of the biggest NMOS, i.e. W=1800μm shows the best linearity compared with the others. It shows that the bigger the size of the NMOS the more linear result we get. Fig. 3.8 shows that bigger NMOS produces smaller delay. If we compare the delay created in the output waveform between W=180μm and W=1800μm, we can see the smaller delay we got from W=1800μm. These show that bigger NMOS yields better result.

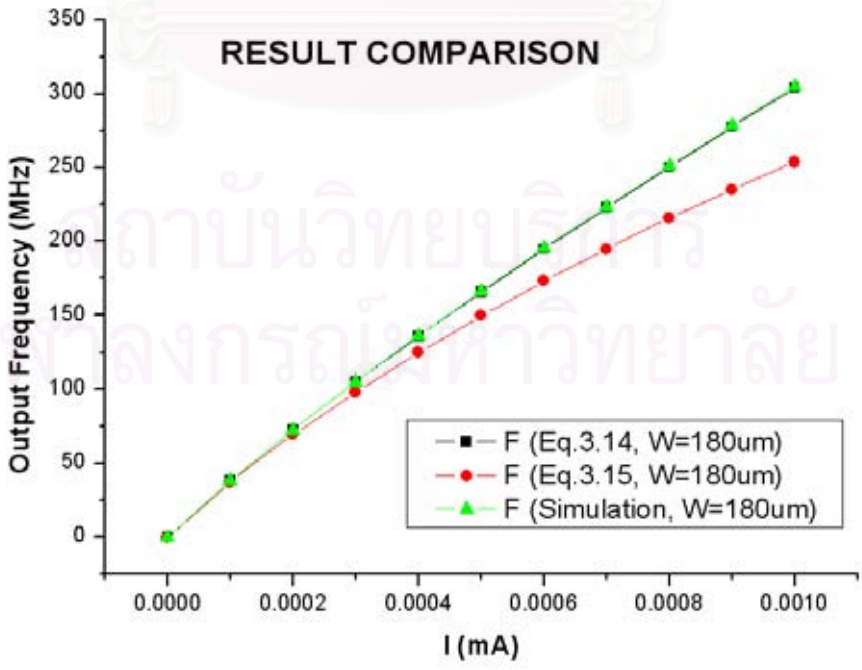


Figure 3.6 Frequency tuning using Eq.3.15, using Eq.3.14 and simulation result

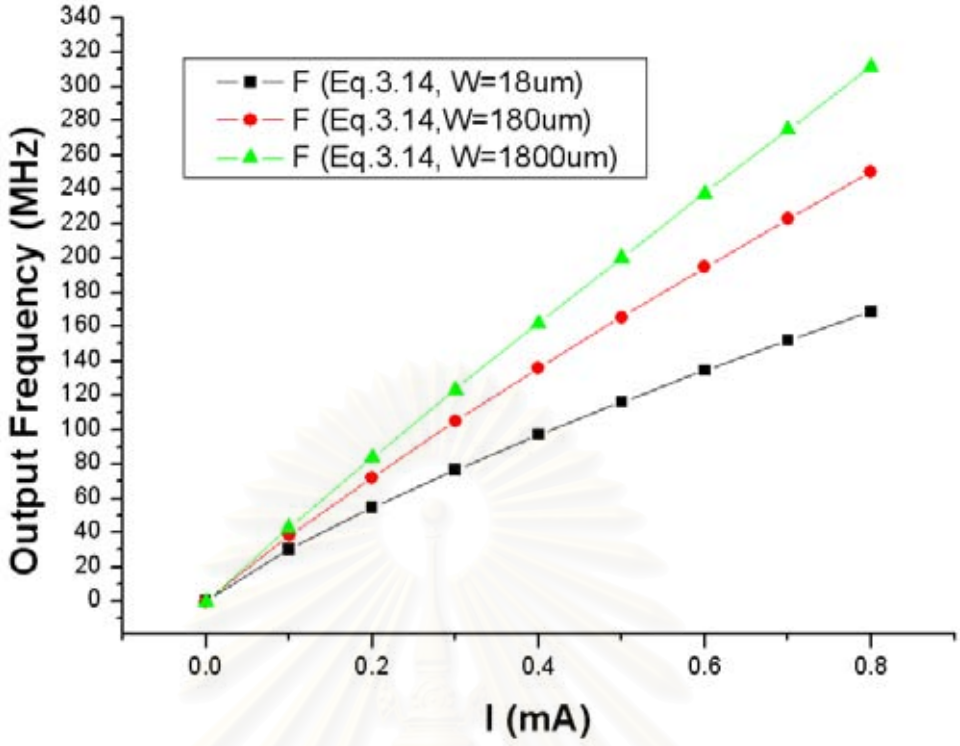


Figure 3.7 Linearity comparison W=18µm, 180µm and 1800µm

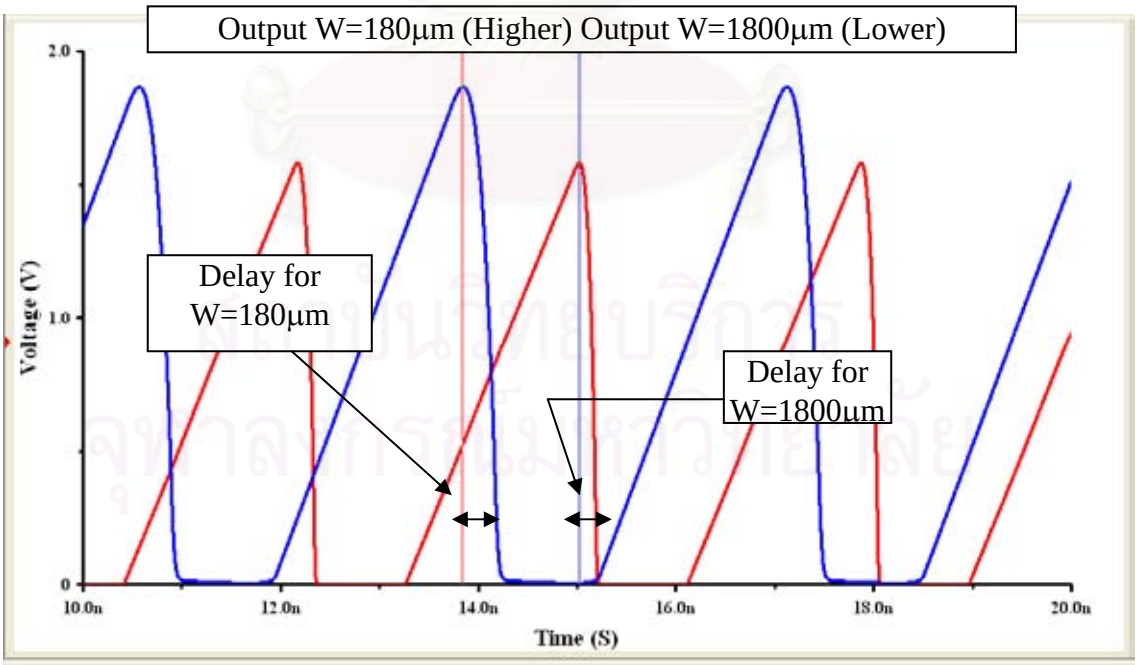


Figure 3.8 Output delay comparison with I=1mA

Fig.3.9 gives a nonlinearity error that shows the error percentage of the difference between prediction and simulation output frequency, showing that the error is below 1% in the little W (W = 180μm) but below 10 % in bigger W (W = 1800μm). This is because there is a parasitic capacitance contributed by bigger W that was not counted. We can prove it by using circuit as shown in Fig. 3.10. This circuit will show that the small capacitance in the bigger W will increase as can be seen in Fig 3.11, using different size of W, we get different time constant, the bigger W need longer time to reach V_{DD}. This meant the C has increased. We can predict the capacitance is about 0.08pF. It is shows by Fig. 3.12 where after we increase the capacitance of C2 to 0.18pF (we add 0.08pF), the time to reach the V_{DD} is now close between W=180μm and W=1800μm. And the error calculation of W=1800μm using Eq. 3.14 is now below 1%, except at I = 0.2 and 0.3mA as shown in Fig. 3.13. It should be better if we can calculate exactly the amount of the paracitic capacitance added by the size of the NMOS, because when we use bigger NMOS, we have better linearity and smaller delay as shown in Fig. 3.7 and 3.8 respectively.

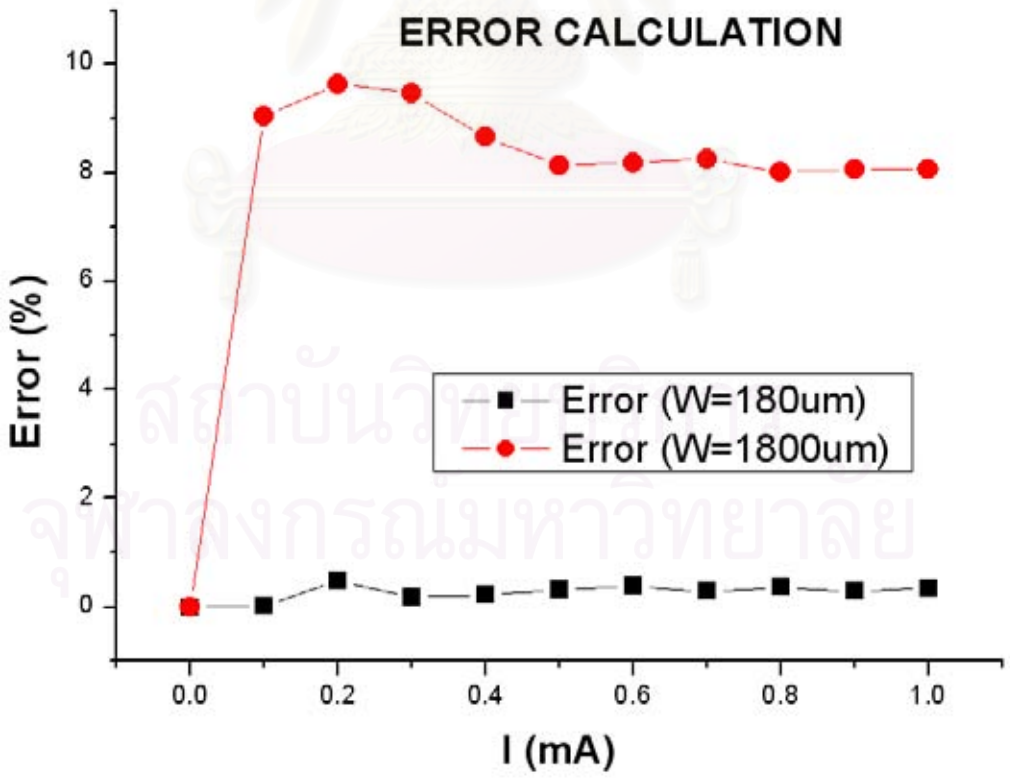


Figure 3.9 Calculation of error

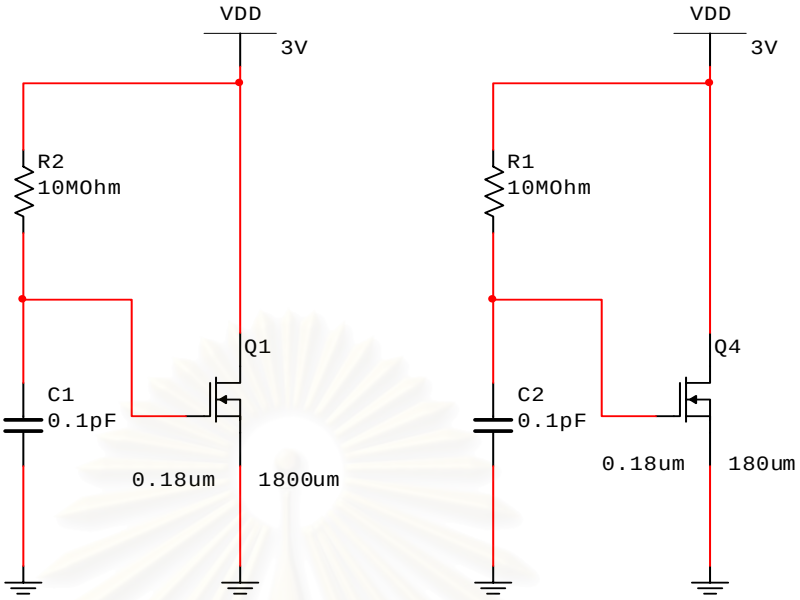


Figure 3.10 Circuit to prove parasitic capacitance

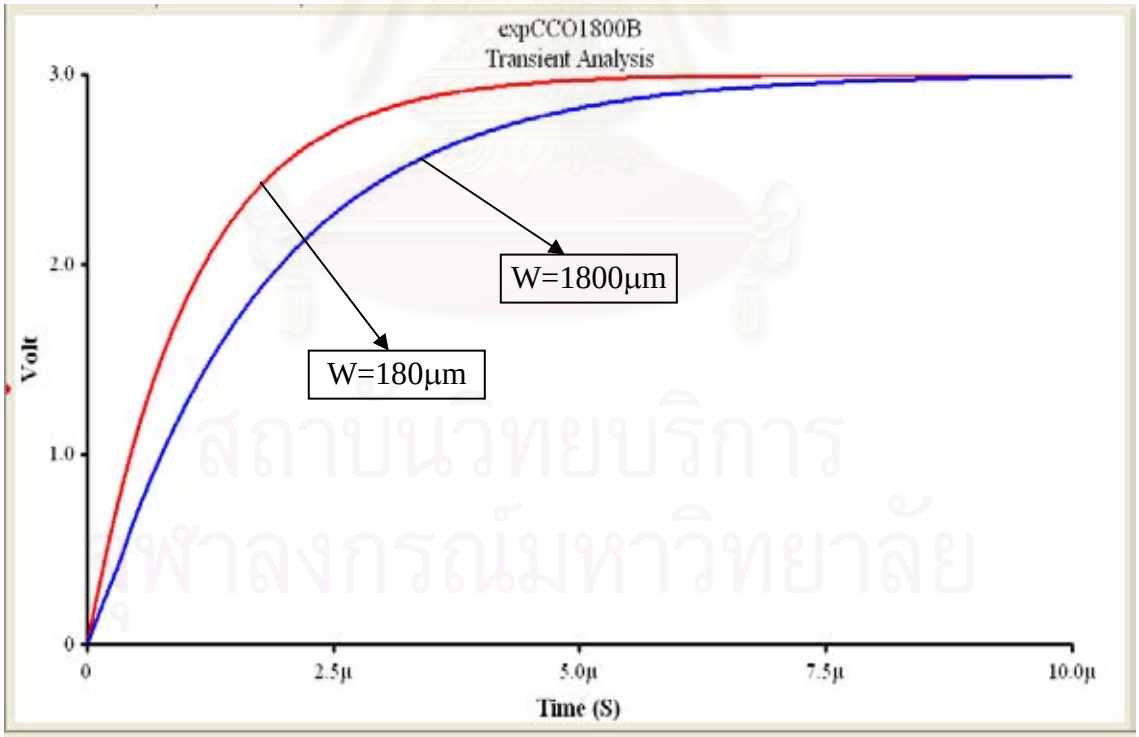


Figure 3.11 Time constant using C = 0.1pF

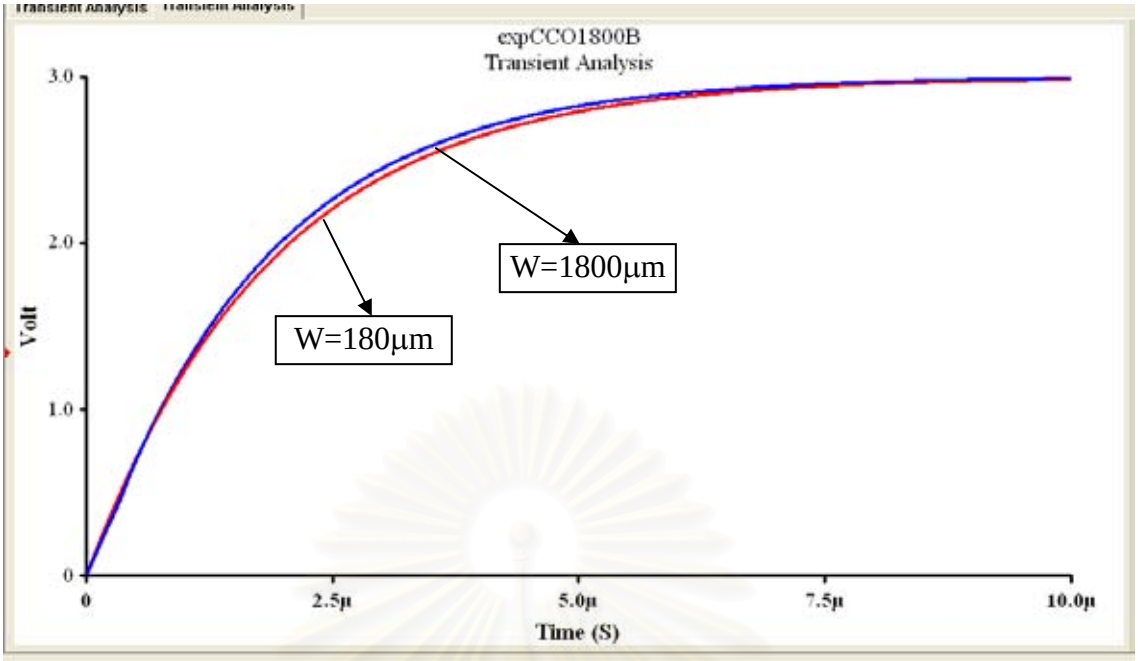


Figure 3.12 Time constant using C2 = 0.18pF

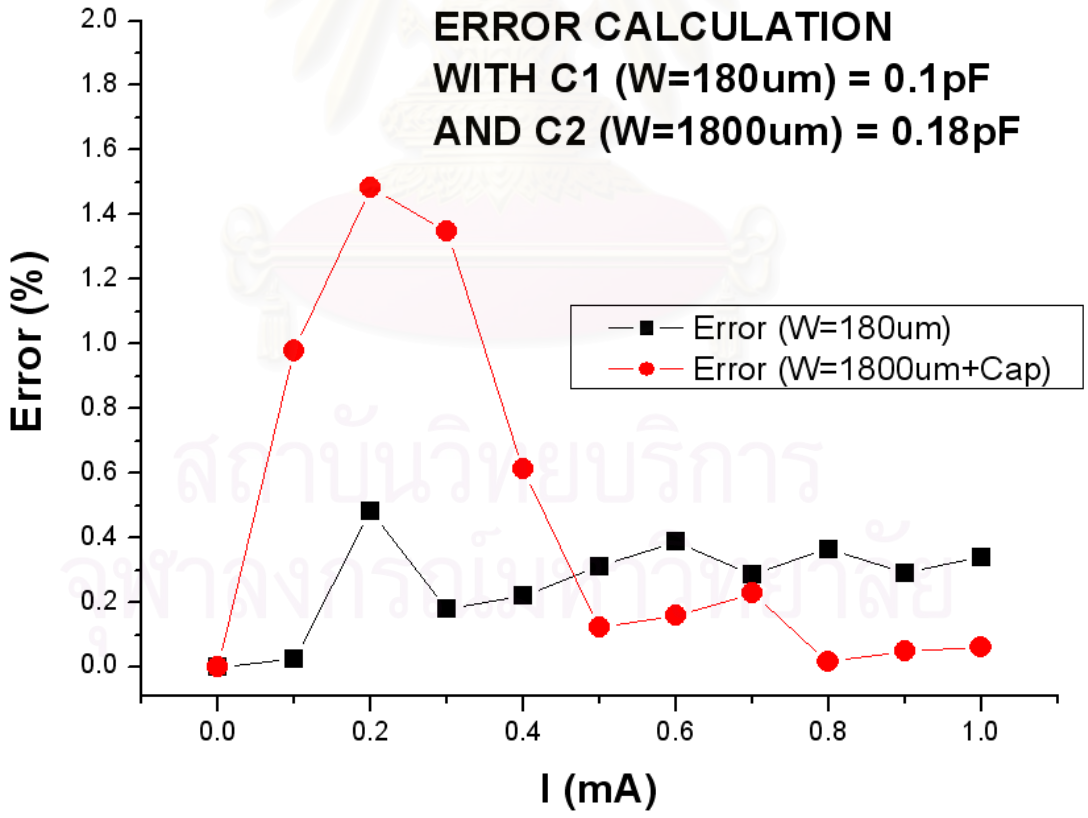


Figure 3.13 Measurement of error using C2=0.18pF

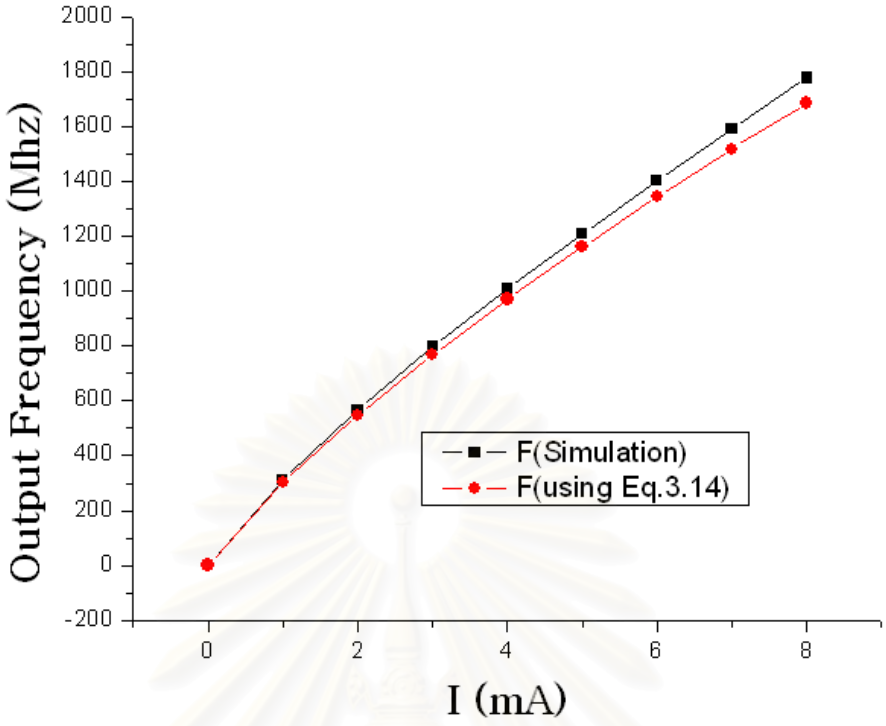


Figure 3.14 Expanding range measurement to 8mA

If we expand the current load to 8mA, the Result showed that the calculation or prediction result working accurately only at 0mA – 2mA. On 2mA-8mA the error is getting bigger. It is shown by Fig. 3.14.

Above 8mA the Calculation resulting in Error because the result is negative, so it's became error if we take the square root.

In conclusion, a CMOS 3-stage ring oscillator based on an inverting NMOS with current load is analyzed to obtain a formula for its frequency. The analysis shows that the frequency varies almost linearly with the load current.

This circuit has been simulated using load current from 1nA to 1mA, giving frequency output vary from 468-Hz ~ 305 MHz. The simulation result shows close agreements with the calculation analysis. It shows also that the size of the NMOS affects the result, showing that the bigger the size of the NMOS yields better result.

3.2 Effect of the lambda (λ)

3.2.1 Analysis

In the saturate region, drain current (I_D) assume as equal to drain current at saturate (I_{DS}), but in the practical world I_D is not precisely equal to I_{DS}.

$I_D=I_{DS}\ (1+\lambda V_{DS})$ in which I_{DS} is proportional to channel width (W) and depends on the Gate Voltage above threshold if $V_{GS} < V_{TH}$ then I_D =0 as shown in fig. 3.15.

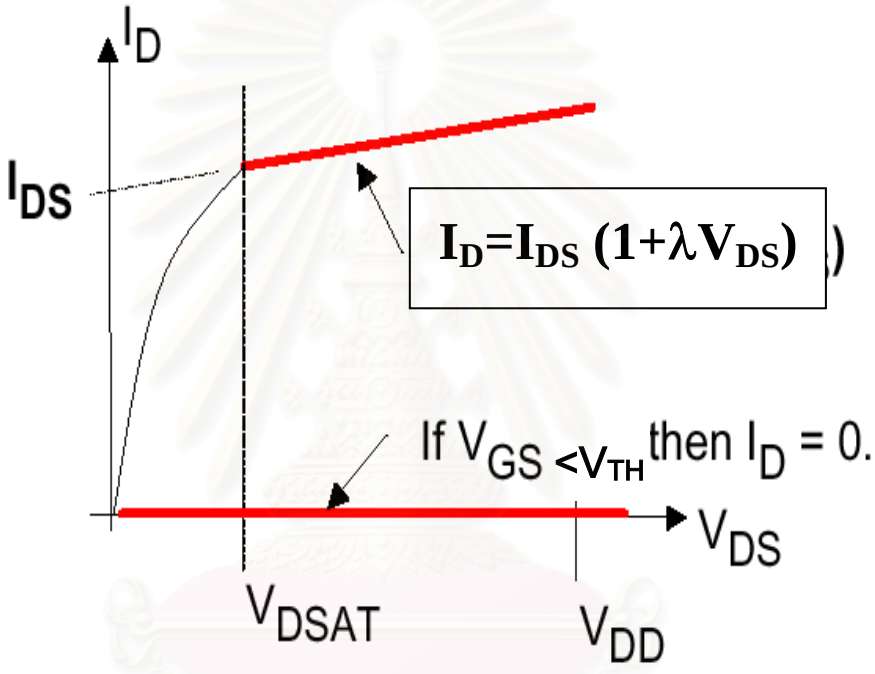


Figure 3.15 Effect of the lambda [10]

In the previous calculation, we use $\lambda = 0$. If λ is not equal to 0 the equation (3.4) became

$$C\frac{dv}{dt} = I - \frac{\beta}{2}\cdot\frac{I^2}{C^2}t^2(1+\lambda v) \qquad ;\ v(0) = v_H \tag{3.16}$$

Thus

$$\frac{dv}{dt} = \frac{I}{C} - \frac{\beta I^2}{2C^3}t^2 - \lambda\frac{\beta I^2}{2C^3}t^2 v \tag{3.17}$$

By considering the general equation

$$\frac{dx}{dt} = -\alpha(t)x + b(t) \tag{3.18}$$

This has the following solution

$$x(t) = e^{-\int_0^t \alpha(y)dy} x(0) + \int_0^t e^{-\int_0^{t-\tau} \alpha(y)dy} b(\tau)d\tau \tag{3.19}$$

If α(y) is small we can approximate

$$e^{-\int_0^t \alpha(y)dy} \approx 1 - \int_0^t \alpha(y)dy \tag{3.20}$$

Apply (3.19) and (3.20) to equation (3.17) we have

$$v(t) \approx \left[1 - \frac{\lambda\beta I^2}{6C^3}t^3\right]v(0) + \int_0^t \left[1 - \frac{\lambda\beta I^2}{6C^3}(t-\tau)^3\right]\left[\frac{I}{C} - \frac{\beta I^2}{2C^3}\tau^2\right]d\tau \tag{3.21}$$

or

$$\approx \left[1 - \frac{\lambda\beta I^2}{6C^3}t^3\right]v_H + \frac{I}{C}t - \frac{\lambda\beta I^3}{24C^4}t^4 - \frac{\beta I^2}{6C^3}t^3 + \frac{\lambda\beta^2 I^4}{720C^6}t^6 \tag{3.22}$$

At t = δ, we have v (δ) = V_{TH}, hence

$$V_{TH} = V_H - \frac{I}{C}\delta - \frac{\beta I^2\delta^3}{6C^3}(1 + \lambda V_H) - \frac{\lambda\beta I^3}{24C^4}\delta^4 + \frac{\lambda\beta^2 I^4}{720C^6}\delta^6 \tag{3.23}$$

moving V_H to the left side, it became

$$V_{TH} - V_H = -\frac{I}{C}\delta - \frac{\beta I^2\delta^3}{6C^3}(1 + \lambda V_H) - \frac{\lambda\beta I^3}{24C^4}\delta^4 + \frac{\lambda\beta^2 I^4}{720C^6}\delta^6 \tag{3.24}$$

This equation should be replacing Eq. 3.5, hence

$$\frac{I}{3C}T = (V_{TH} - V_L) + \frac{I}{C}\delta \tag{3.25}$$

or

$$V_{TH} = V_L + \frac{I}{C} \times (\frac{T}{3} - \delta) \tag{3.26}$$

Because

$$V_H = V_{TH} + \frac{I}{C} \times \frac{T}{3} \tag{3.27}$$

Combining (3.26) and (3.27), we obtain

$$V_H = V_L + \frac{2IT}{3C} - \frac{I}{C}\delta \tag{3.28}$$

Consider V_L=0 so that

$$V_H = \frac{2IT}{3C} - \frac{I}{C}\delta \tag{3.29}$$

Subtracting (3.26) by (3.27), we have

$$V_{TH} - V_H = V_L + \frac{I}{C} \times (\frac{T}{3} - \delta) - \left[V_{TH} + \frac{I}{C} \times \frac{T}{3} \right] \tag{3.30}$$

Or

$$V_{TH} - V_H = V_L - V_{TH} + \frac{IT}{3C} - (\frac{I}{C}\delta) - \frac{IT}{3C}$$

Or

$$V_{TH} - V_H = V_L - V_{TH} - (\frac{I}{C}\delta) \tag{3.31}$$

Combining (3.24) with (3.31), we obtain

$$V_L - V_{TH} - (\frac{I}{C}\delta) = -\frac{I}{C}\delta - \frac{\beta I^2 \delta^3}{6C^3}(1 + \lambda V_H) - \frac{\lambda \beta I^3}{24C^4}\delta^4 + \frac{\lambda \beta^2 I^4}{720C^6}\delta^6 \tag{3.32}$$

Replacing V_{TH} with (3.26) we have

$$V_L - V_L - \frac{IT}{3C} + (\frac{I}{C}\delta) - (\frac{I}{C}\delta) = -\frac{I}{C}\delta - \frac{\beta I^2 \delta^3}{6C^3}(1 + \lambda V_H) - \frac{\lambda \beta I^3}{24C^4}\delta^4 + \frac{\lambda \beta^2 I^4}{720C^6}\delta^6$$

After some manipulation, we have

$$T = 3\delta + \frac{\beta I\ \delta^3}{2C^2}(1+\lambda V_H) + \frac{\lambda\beta I^2}{8C^3}\delta^4 - \frac{\lambda\beta^2 I^3}{240C^5}\delta^6 \tag{3.33}$$

Or

$$T = 3\delta + \frac{\beta I\ \delta^3}{2C^2} + \frac{\beta I\ \delta^3}{2C^2}\lambda V_H + \frac{\lambda\beta I^2}{8C^3}\delta^4 - \frac{\lambda\beta^2 I^3}{240C^5}\delta^6 \tag{3.34}$$

Replacing V_H with (3.29) we get

$$T = 3\delta + \frac{\beta I\ \delta^3}{2C^2} + \frac{\beta I\ \delta^3}{2C^2}\lambda\left[\frac{2IT}{3C} - \frac{I}{C}\delta\right] + \frac{\lambda\beta I^2}{8C^3}\delta^4 - \frac{\lambda\beta^2 I^3}{240C^5}\delta^6 \tag{3.35}$$

Or

$$T = 3\delta + \frac{\beta I\ \delta^3}{2C^2} + \left[\frac{\beta I\ \delta^3}{2C^2}\left[\frac{2IT}{3C} - \frac{I}{C}\delta\right] + \frac{\beta I^2}{8C^3}\delta^4 - \frac{\beta^2 I^3}{240C^5}\delta^6\right]\lambda \tag{3.36}$$

We try to replacing λ by deriving it, we have

$$\frac{\partial T}{\partial\lambda} = \frac{\beta I\ \delta^3}{2C^2}\left[\frac{2IT}{3C} - \frac{I}{C}\delta\right] + \frac{\beta I^2}{8C^3}\delta^4 - \frac{\beta^2 I^3}{240C^5}\delta^6 \tag{3.37}$$

or

$$\frac{\partial T}{\partial\lambda} = \frac{\beta I^2 T}{3C^3}\delta^3 - \frac{\beta I^2}{3C^3}\delta^4 + \frac{\beta I^2}{8C^3}\delta^4 - \frac{\beta^2 I^3}{240C^5}\delta^6 \tag{3.38}$$

or

$$\frac{\partial T}{\partial\lambda} = \frac{\beta I^2 T}{3C^3}\delta^3 - \frac{5\beta I^2}{24C^3}\delta^4 - \frac{\beta^2 I^3}{240C^5}\delta^6 \tag{3.39}$$

Until this step the equation is not solved yet, but it's very complicated to manipulate this equation because we still have one unknown, i.e. δ. If we look at on (3.36) we have found the correlation between T and λ, but we have two unknowns λ and δ, so that we can use this equation easily. We tried to simplify it by using the form of Eq.3.6, in the same way we derive equation when assumed there is no effect of lambda, but it is so complicated because we found equation with power of six.

3.2.2 Experimental Result

In this case, we can only take the graphic of relation between lambda and the output frequency, see the effect of lambda in Fig. 3.16. It is shown that the higher lambda yields higher frequency. It is also shows effect of the lambda on the simulated frequency of oscillation. In this simulation we used **W=180μm, L=0.18μm and I=1mA**.

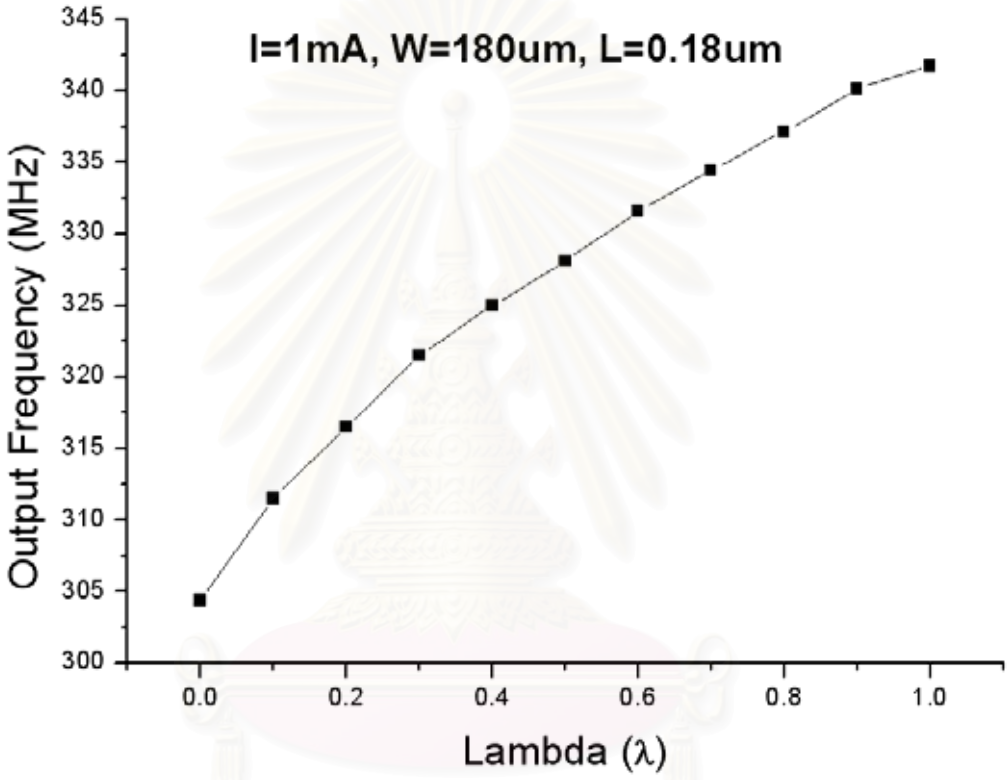


Figure 3.16 Effect of the lambda on the simulated frequency of oscillation.

CHAPTER IV
IMPROVED CIRCUIT

4.1 Introduction to circuit improvement

From the results in the previous chapter, it can be seen that the result graph deviates from linear, fairly large at higher frequencies as can be seen from the graph in Figure 4.1. Therefore, in this chapter we are going to propose a new circuit to improve the linearity.

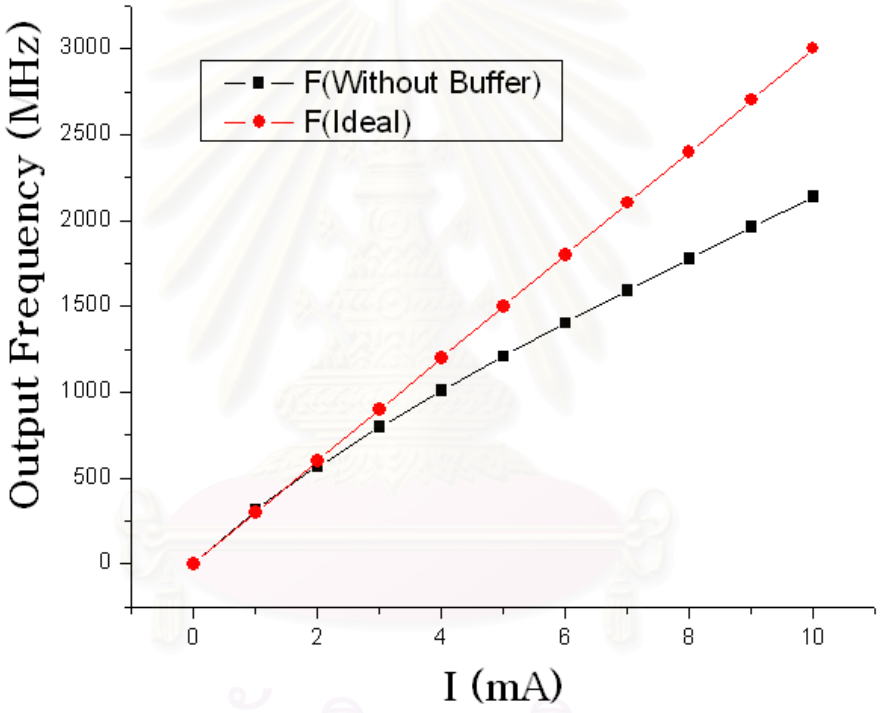


Figure 4.1 Ideal vs. simulation output graph.

It is quite possible that the cause of this is due to the switching delay between each inverter caused by a small duration for discharging each output capacitor. This means that the succeeding device cannot immediately turn off as shown in Fig 3.3.

We proposed one way to solve this by using an additional buffer between each step to make the succeeding inverter immediately turn off when the previous inverter output voltage reaches V_{TH} as shown from the graph in fig. 4.2.

The use of this additional buffer results in another delay. Therefore, there are three delays created because of the using of buffer. They are δ1, δ2, δ3.

Here δ1 is the delay from the first additional buffer, δ2 created by C2 when discharging and δ3 is the delay resulted from the second additional buffer. It will be repeated so that the delay made by third additional buffer will be the next cycle.

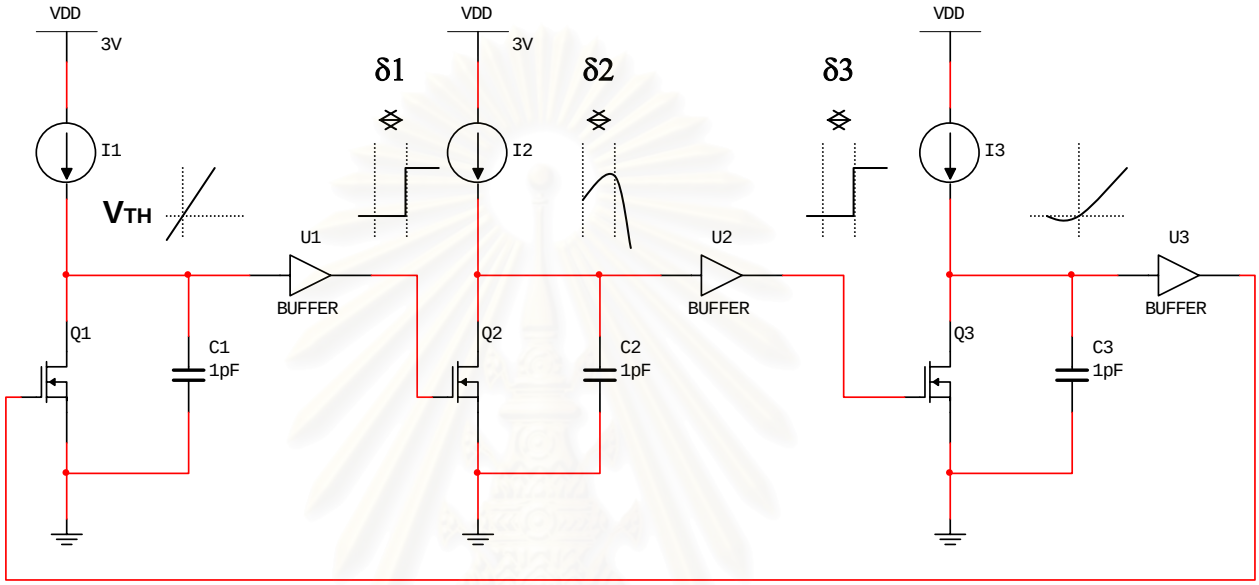


Figure 4.2 Delay occur on the circuit.

We can draw these delays in the following figure.

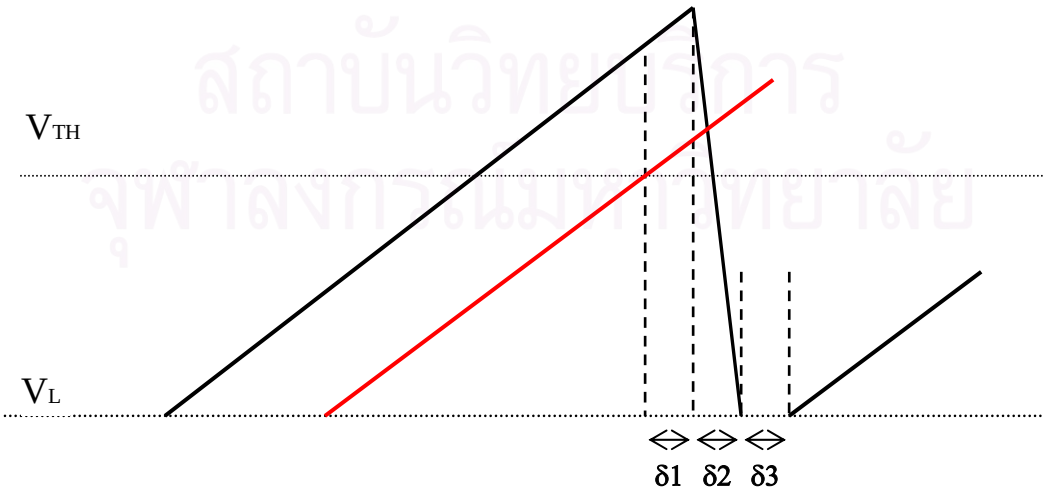


Figure 4.3 Total delays on circuit with additional buffer.

Addition of these three delays must be smaller than the delay when the circuit doesn't use additional buffer. Or we can write

$$\delta 1 + \delta 2 + \delta 3 < \delta$$

The delay without additional buffer can be seen on figure 4.4.

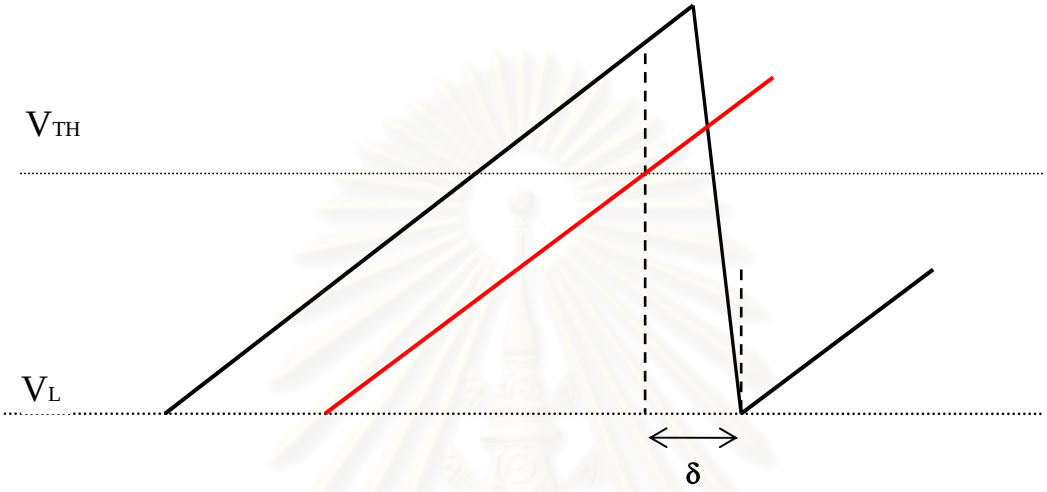


Figure 4.4 Total delays on circuit without additional buffer

4.2 Circuit architecture

We use a cascade of two inverters to obtain a buffer. The improved circuit is thus drawn as follows:

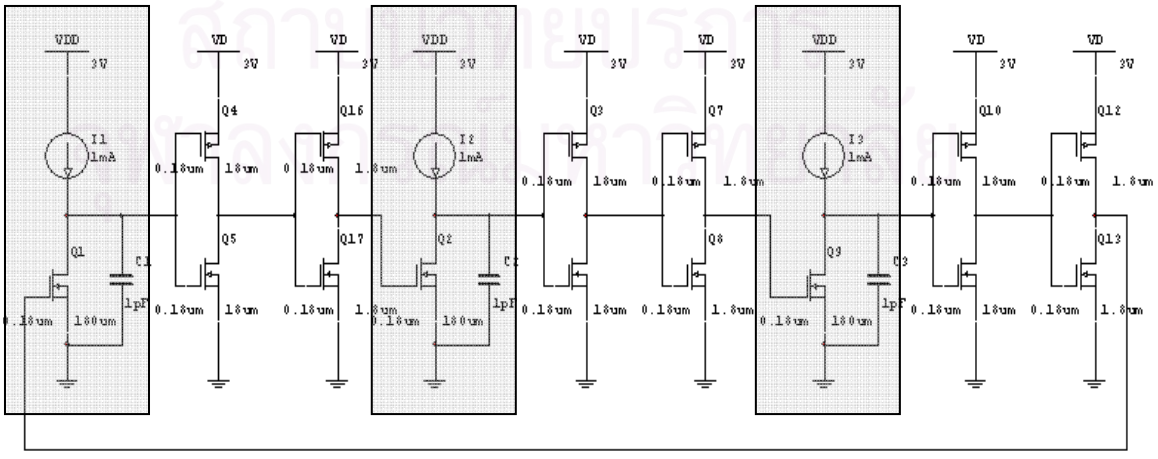


Figure 4.5 The CCO with additional buffer

It uses ideal current sources at first to simplify the analysis and design. The Current source is then changed with current sink and current mirrors after the simulation result as expected.

The figures of detail design using ideal current source can be seen in Fig. 4.6 and 4.7 on the next page. Fig. 4.6 shows the design of CCO and Fig. 4.7 shows the design of proposed CCO circuit.

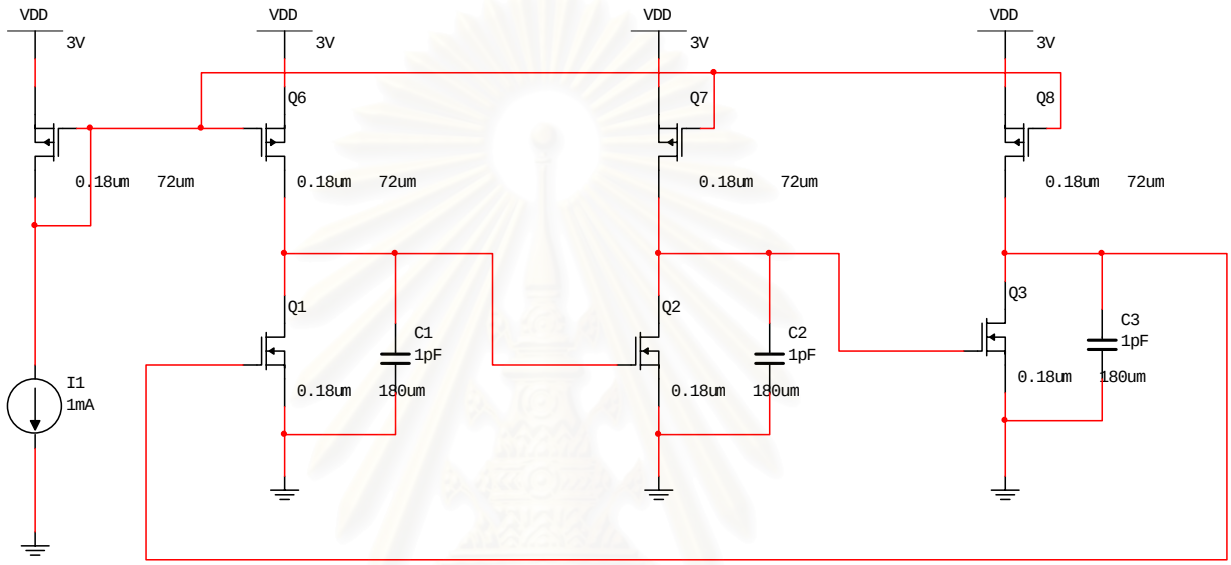


Figure 4.6 CCO with current sources obtained from current mirrors

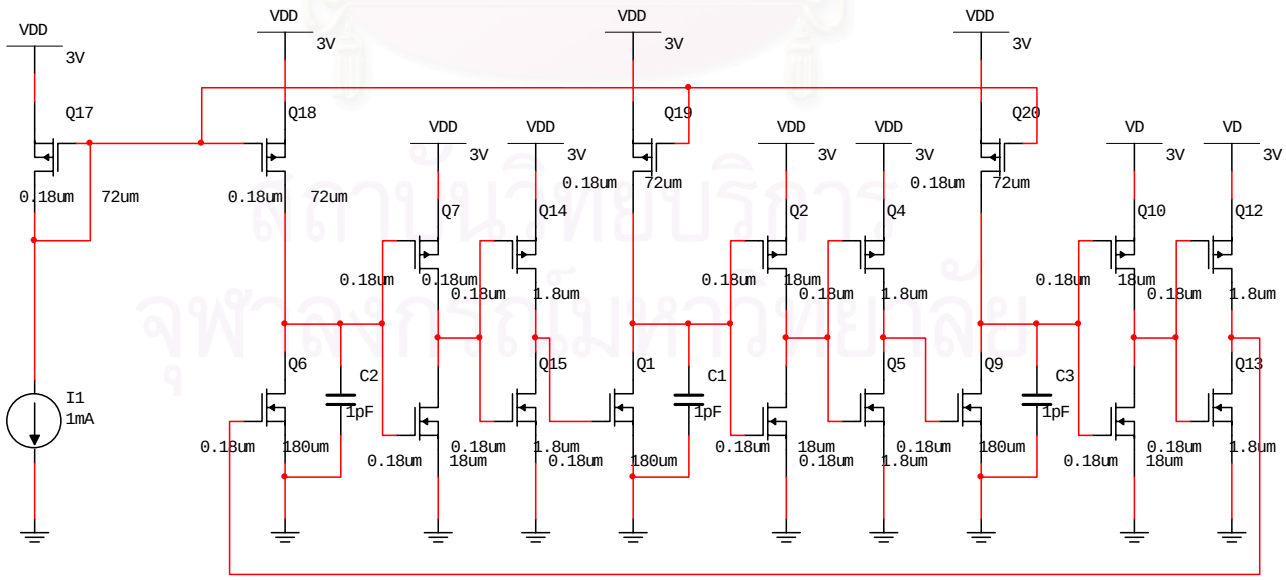


Figure 4.7 Improved CCO with current source obtained from current mirrors

To determine the W/L of the buffers, we simulate them and derive a table that shows which buffer has the smallest delay or which value of W/L that has the most linear frequency ranging. There are best 3 combinations (case) that are simulated by attaching them to the circuit to find the most linear one.

CASE 1

Buffer 1, 2 and 3

Inverter 1: PMOS → W=0.18μm, L=0.18μm, NMOS → W=18μm, L=0.18μm

Inverter 2: PMOS → W=1.8μm, L=0.18μm, NMOS → W=1.8μm, L=0.18μm

CASE 2

Buffer 1

Inverter 1: PMOS → W=0.18μm, L=0.18μm, NMOS → W=18μm, L=0.18μm

Inverter 2: PMOS → W=18μm, L=0.18μm, NMOS → W=1.8μm, L=0.18μm

Buffer 2 and 3

Inverter 1: PMOS → W=18μm, L=0.18μm, NMOS → W=18μm, L=0.18μm

Inverter 2: PMOS → W=1.8μm, L=0.18μm, NMOS → W=1.8μm, L=0.18μm

CASE 3

Buffer 1, 2 and 3

Inverter 1: PMOS → W=18μm, L=0.18μm, NMOS → W=18μm, L=0.18μm

Inverter 2: PMOS → W=1.8μm, L=0.18μm, NMOS → W=1.8μm, L=0.18μm

The result shows CASE 2 have the best linearity as shown in Fig. 4.8. We choose CASE 2's combination for the buffer.

We will use this combination for circuit in Fig. 4.6 and 4.7 to know the improvement that has been made by looking at the more linear graph as the result as shown in Fig.4.9. The circuit used in this graph using PMOS current mirror W = 72μm and L = 0.18μm as in Fig.4.6 and 4.7.

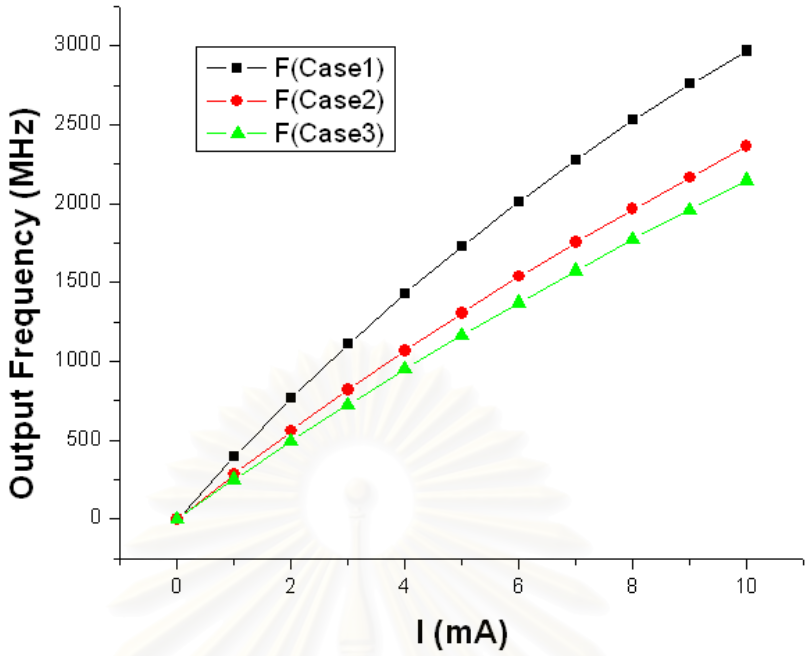


Figure 4.8 3 case comparison to find the best W/L for the buffer.

Fig.4.9 shows the result between output frequency without additional buffer (F (Without Buffer)) compared with the one with additional buffer (F (With Buffer)).

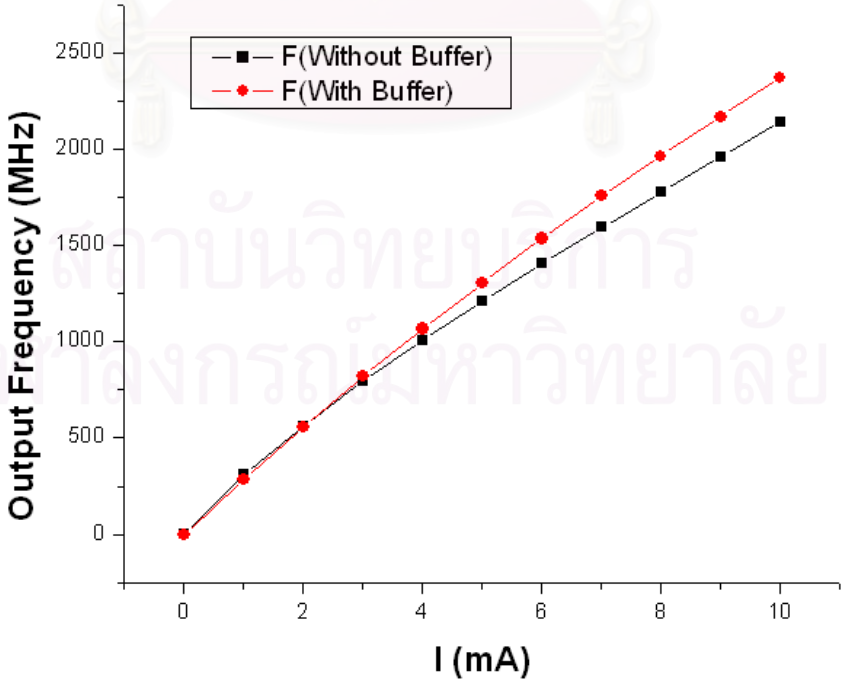


Figure 4.9 The graph of 3 condition of CCO

From this figure it can be shown that circuit with additional delay or improved circuit considerably more linear than the one without additional buffer.

4.3 A 10 MHz CMOS CCO design

To design a 10 MHz CMOS CCO, first we have to approximate by calculating the current we need to get 10 MHz by using Eq. (3.1), Thus we get

$$f = \frac{1}{T} = \frac{I}{3CV_{TH}} \rightarrow \quad I = 3fCV_{TH}$$

I = 3 x 10.10^{6} x 1.10^{-12} x 0.7

= 21 . 10^{6} = 21 μA

The next step is designing current mirror circuit to obtain that amount of current we need. Here we selected V_{DD} = 1.5 Volt, V_{GS} = 0.9 Volt, L = 0.18 μm , V_{SS} = 0 Volt. Assume I_{D1}=I_{D2} = 21 μA. R and W is determined by using Eq. (2.23)
After the calculation we have

W_{NMOS} = 6.3 μm

W_{PMOS} = 18.9 μμ

R = 28.57 KΩ

Using this parameter we simulate it and we have

T = 99.8 x 1.10^{9}

Or

$F = 1/T$ = 10.02 MHz

The result is not exactly 10 MHz possibly because there are some error in the manual reading and because we use ideal parameter in design calculation.

The design using improved circuit is drawn in the Fig. 4.11

This circuit has Output

$T = 100 \times 1.10^{9} \rightarrow F = 1/T = 10$ MHz

The simulation shows accurate result close to 10 MHz.

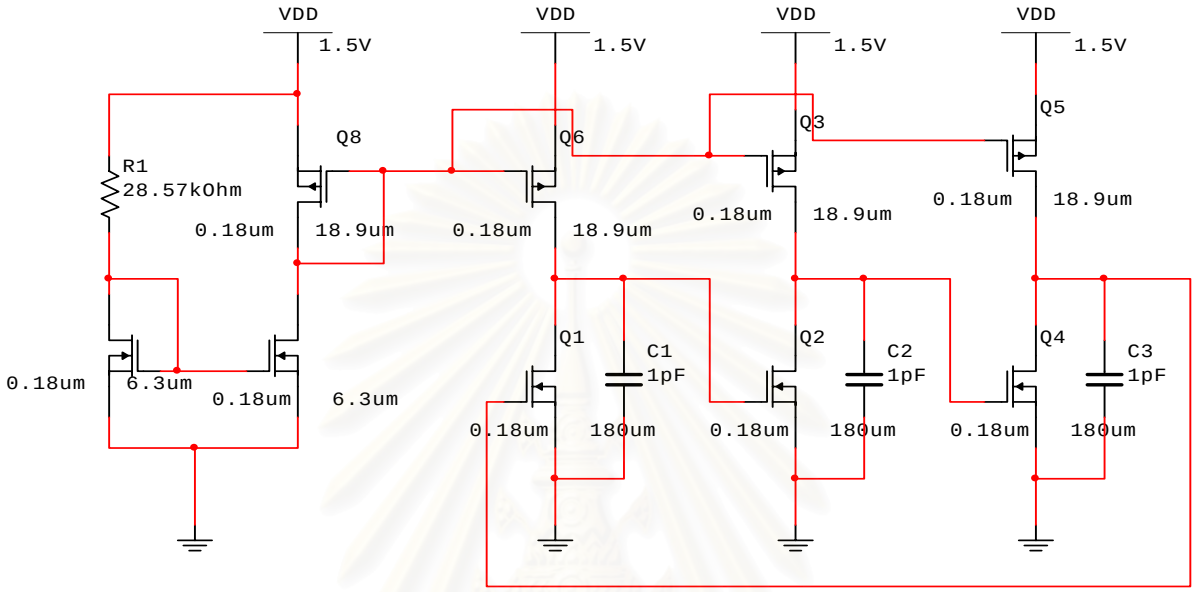


Figure 4.10 Final design of 10 MHz CCO

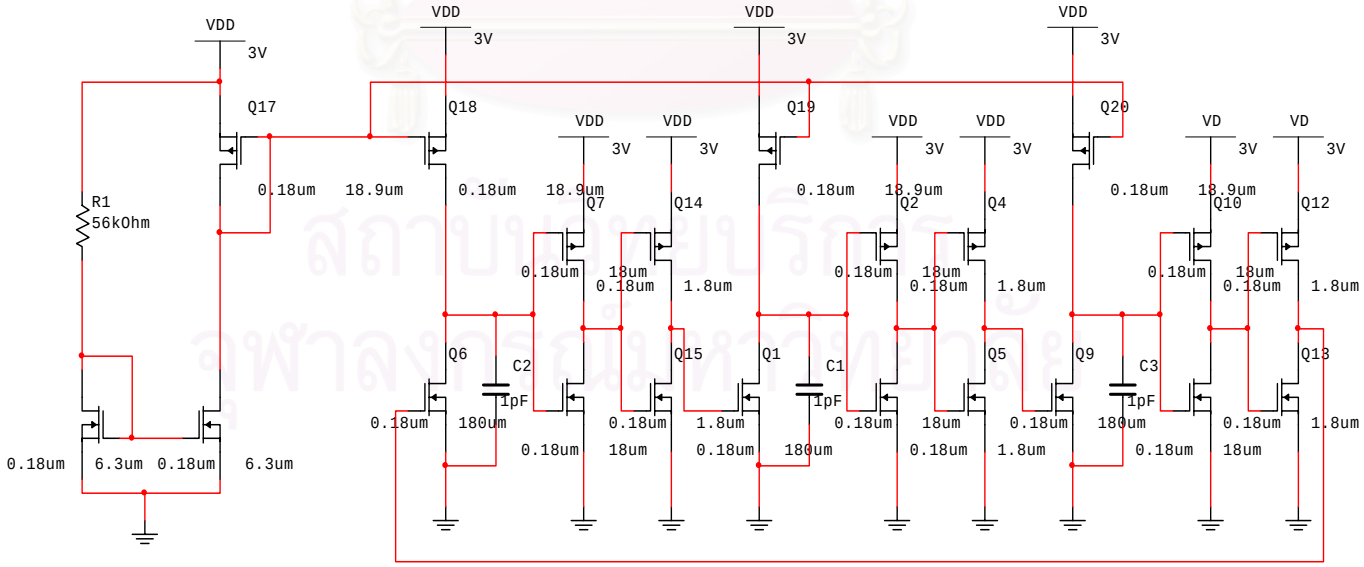


Figure 4.11 Final design of improved 10 MHz CCO.

4.4 Simulation result

Fig. 4.12 and 4.13 shows the output waveform of 10 MHz CCO and improved 10 MHz CCO. We can see in the circle the period (*T*). We use it to get output frequency.

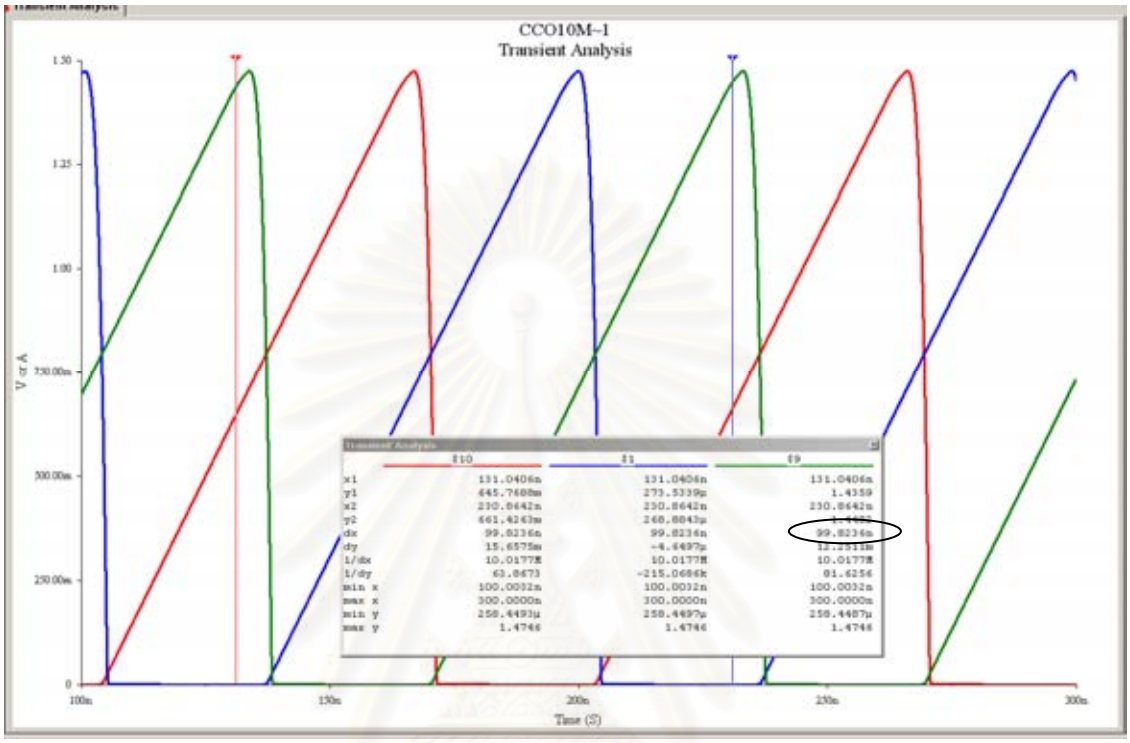


Figure 4.12 Output waveform of 10 MHz CCO

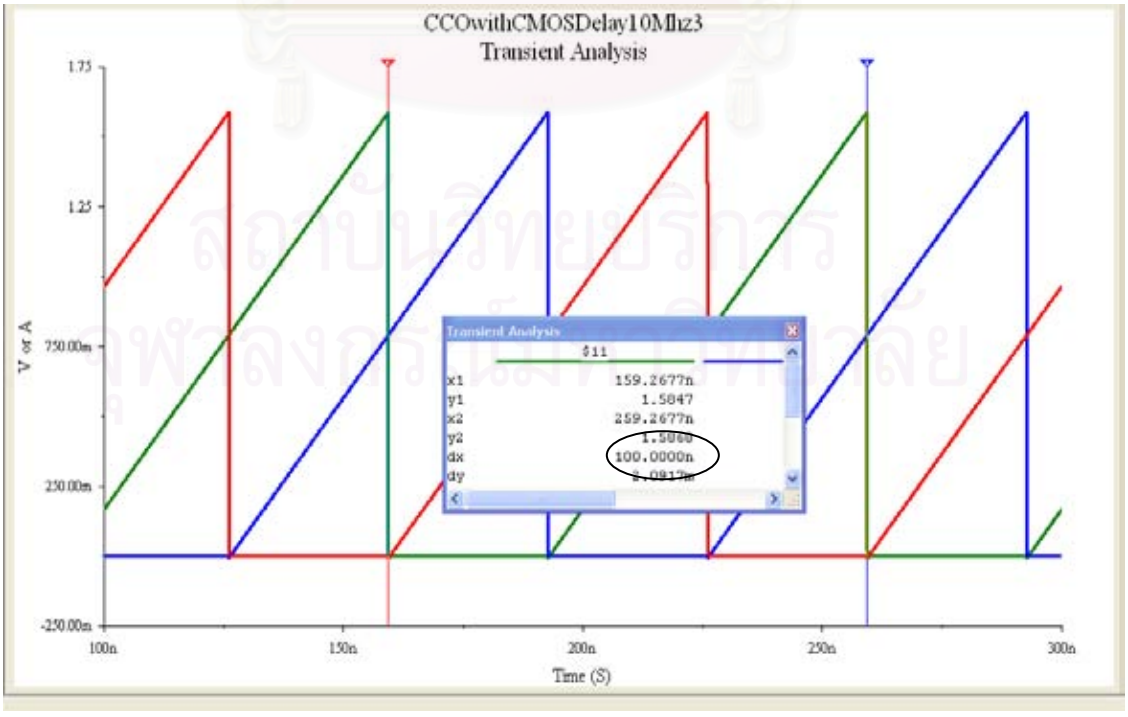


Figure 4.13 Output waveform of 10 MHz improved CCO

CHAPTER V
CONCLUSIONS

5.1 Summary

In this thesis there are 4 objectives and 3 goals we want to achieve as written in the objectives and research goals on Chapter I. For the first until the third objectives has been done in is written down in second until the third chapter. Forth objective is described on chapter forth.

Detail analysis as the first goal is presented on this thesis, followed by proposed better circuit in term of linearity and one international conference paper as the contributions and the third goal.

In Chapter 2, the basic theory is described briefly to support the analysis and design. There only the basic theories that related to this work were presented.

In Chapter 3, mostly the content is taken from the International conference paper that was presented on ITC-CSCC 2006. This chapter describes a ring oscillator using 3 stages of an NMOS driving a current load and a capacitor. Its frequency can be shown to increase monotonically with the load current giving rise to the name current controlled oscillator (CCO). An Accurate derivation of the formulae relating the frequency with the NMOS size and the current shows that nonlinearity error of its tuning characteristic is proportional to the cube root of the NMOS width/length ratio. The CCO circuit using 180 μm/0.18 μm NMOS with 1pF load can be tuned to oscillate from 468 Hz to 305 MHz using load current from 1nA to 1mA.

The error of the result between calculation and the simulation result is under 1 %, but it's became grater when we increase the current input above 10 mA. We can say that this formulae very accurate in the range of 0 to 10mA. The next subchapter, we analyze of the effects of the lambda (λ). It used the same way how we describe the tuning analysis of CMOS CCO, but we found complicated equation to solve. It is still a challenge to know the effect of the lambda.

In Chapter 4, we proposed a new circuit that better in a way with the previous one, it has more linear output. The way we designed and the circuit architecture were described, followed by the simulation result that showing the output wave forms of two circuits and the graph of the comparison between the previous circuit and the proposed

one. The final design of the proposed circuit can has precisely 10MHz output, while the previous CCO circuit can not achieved, it have 10.02 MHz. It is still on the tolerance since there are some works that are done manually.

5.2 Recommendation for The Future Works

- Tuning analysis of RCO

  I can not found the detail analysis about this RCO in the internet and any literature source. This is a challenge to derive the formulae and give detail analysis on RCO.
- Solving the Effect of the lambda on the CCO

  There may be a way to solve the complexity of the effect of the lambda, we can solved the lambda as the function of frequency, current or conversely.
- Prototyping the CCO and proposed CCO on a chip respectively.

  Because the limit of time we can not prototyping these CCOs into a single chip, this is a challenge to make it and then compare the result with the simulated one.
- Applications of CCO

  Using this CCO result as a part of some applications, such as on PLL or wide spectrum signal generator.

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APPENDICES

Tuning Analysis of a CMOS Current Controlled Ring Oscillator

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ABSTRACT

A ring oscillator using 3 stages of an NMOS driving a current load and a capacitor is described. Its frequency can be shown to increase monotonically with the load current giving rise to the name current controlled oscillator (CCO). An Accurate derivation of the formulae relating the frequency with the NMOS size and the current shows that nonlinearity error of its tuning characteristic is proportional to the cube root of the NMOS width/length ratio. The CCO circuit using 180um/0.18um NMOS with 1pF load can be tuned to oscillate from 468 Hz to 305 MHz using load current from 1nA to 1mA.

Keywords: Tuning Analysis, Current Controlled Oscillator, Ring Oscillator, Voltage Controlled Oscillator.

1. INTRODUCTION

A voltage controlled oscillator (VCO) is a key component in many communication devices and circuits. It generates a clock signal with frequency varied according to its input voltage as shown in fig. 1a.

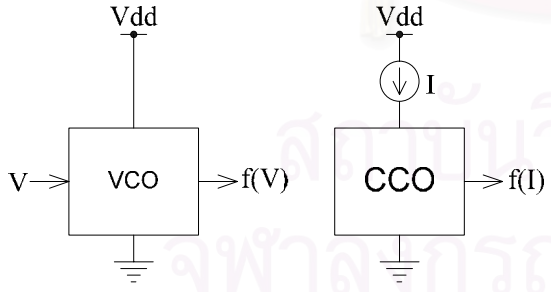

Fig. 1: *A Block Diagram of A VCO (a) and CCO (b)*

Various types of VCO circuits have been extensively reported in the literature. They are ring [1], LC [1] and relaxation [7] oscillators. Three important properties of a VCO are

1) Tuning range defined in term of its max/min frequency ratio. Due to process and temperature variations, a tuning range of more than a factor of 2 is preferred.
2) Phase jitter corresponding to the effect on its frequency due to the internal noise. A low jitter is preferred than a higher one.
3) Tuning linearity specifying how linear its frequency is with respect to V. A linear sensitivity is required if the VCO is to be implemented as a spread spectrum clock oscillator [3]. When implemented in a phase lock loop [4, 6], nonlinearity is also shown to degrade [2, 5] its settling behaviour.

In many cases, these properties impose conflicting design constraints. For example, an LC CMOS oscillator is known to have low phase jitter, low tuning range and nonlinear sensitivity.

This paper presents the analysis and design of another type of CMOS oscillator in which its frequency varies almost linearly with its load current source and is better referred to as a current controlled oscillator (CCO) as shown in Fig. 1b. The circuit topology is described in Section II along with a simplified analysis for its frequency of oscillation. Section III provides a detail analysis about how the size of the NMOS affects the tuning nonlinearity. Section IV described a designed CCO circuit and its simulated result.

2. CIRCUIT ARCHITECTURE AND SIMPLIFIED ANALYSIS

The CMOS CCO proposed in this paper is based on a 3-stage inverting ring oscillator [1]. However, rather than using a CMOS static inverter or an NMOS inverting device driving a PMOS resistive load, our inverting stage uses an NMOS device driving a current source I together with an output capacitor C as shown in Fig. 2. Thus its power consumption depends directly on I and there is no Vdd supply current spike typically found in a static inverter.

We shall first make a simplified analysis of this circuit by using a switch model of the NMOS as shown in Fig. 3, i.e. an NMOS becomes short circuited when its gate-source voltage V_{GS} exceeds its threshold voltage V_{TH}. This assumption is valid when the width (W) of the NMOS is sufficiently large compared with its length (L).

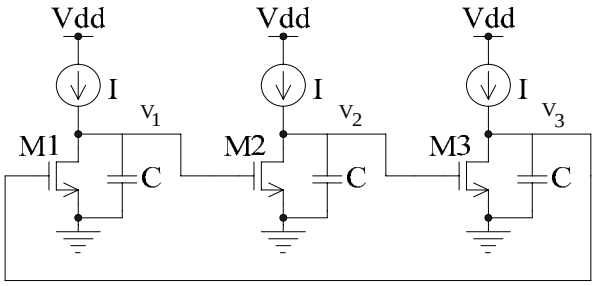

Fig.2: *A CMOS 3-Stage Inverting Ring Oscillator Using Current Load.*

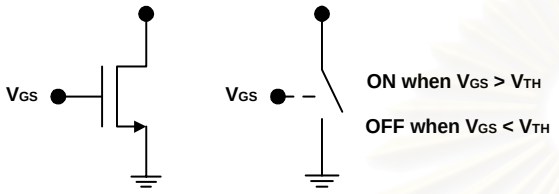

Fig. 3: *The Switch Model of Tthe NMOS*

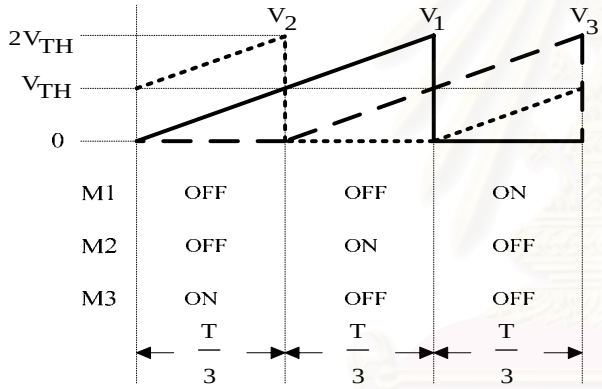

Fig. 4: *Simplified Steady State Oscillating Waveforms*

From the switch model, we note that only one NMOS can turn on at any given time. Since the three NMOS devices are identical, the total period T must be divided equally by the ON duration of each transistor and the transition from OFF to ON of a device must occur at the middle of the OFF interval of the preceding device as shown in Fig. 4. So an NMOS, e.g. M1, is ON for T/3 when its output $\mathbf{V_1}$ is zero and OFF for another 2T/3 during which its output capacitor is charged by the constant current I. Thus $\mathbf{V_1}$ rises from zero at a slope of I/C as shown in the top waveform in Fig. 4 and will turn on M2 after ramping for T/3 when its value reaches $\mathbf{V_{TH}}$. Therefore we now have the formulae for obtaining the period of oscillation as follows

$$\frac{I}{C}\times\frac{T}{3}=V_{TH} \quad \text{or} \quad T=3\frac{C}{I}V_{TH}$$

$$\text{Thus } f=\frac{1}{T}=\frac{I}{3\cdot C\cdot V_{TH}} \qquad (1)$$

Which shows that the frequency varies linearly with I. This is a desirable property for a Phase Lock Loop application. Also its power consumption $3V_{DD}\,I$ depends linearly on I and there is no V_{DD} supply current spike. Since the OFF duration is *2T/3*, the maximum output voltage is $2V_{TH}$. Hence the minimum V_{DD} supply that the circuit can operate is

$$V_{DD}(\min)=2V_{TH}+V_I$$

where V_I is the minimum operating voltage of the current source. If the current source is implemented by a simple PMOS device, V_I can be as low as its overdrive voltage. Using a low threshold voltage CMOS technology, the circuit can operate at a low DC supply of 1.5V.

3. EFFECT OF THE SIZE OF THE NMOS

In practice, an NMOS with a finite width (W) and length (L) cannot behave as an ideal short circuit, i.e. having zero resistance when it turns on. This means that the circuit needs a small duration (δ) for discharging each output capacitor until its voltage is low enough to turn off the succeeding device as shown in Fig. 5, i.e. there are two ON devices during this interval. This will have an increasing effect on its period of oscillation (T) which is derived as follows.

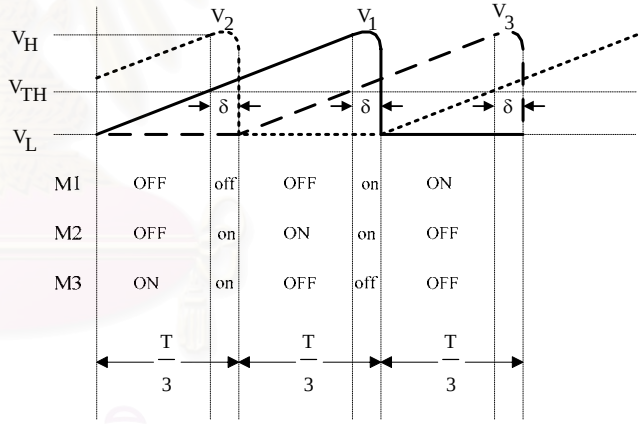

Fig. 5: *Steady State Waveforms When Each NMOS Has Finite W and L*

Note from the figure that each capacitor is charged by the constant current I from $\mathbf{V_L}$ at the beginning to $\mathbf{V_{TH}}$ after $\boldsymbol{T/3-\delta}$ interval and to $\mathbf{V_H}$ after another **T**/3 interval. Thus we have that

$$V_{TH}=V_L+\frac{I}{C}\times\left(\frac{T}{3}-\delta\right) \qquad (2)$$

$$V_H=V_{TH}+\frac{I}{C}\times\frac{T}{3} \qquad (3)$$

where $\mathbf{V_L \approx 0}$ is the minimum drain voltage of an NMOS to carry I. After this, the NMOS is gradually turned on by its ramping input, i.e.

$$V_{GS} = V_{TH} + \frac{I}{C}t$$

Thus the capacitor voltage can still rise from $\mathbf{V_H}$ but will quickly decay to $\mathbf{V_{TH}}$ after duration of δ to start turning off the next device. The dynamic equation during this duration is

$$C\frac{dv}{dt} = I - \frac{\beta}{2}[V_{GS} - V_{TH}]^2 = I - \frac{1}{2}\beta\left[\frac{I}{C}t\right]^2 \quad (4)$$

Where $v(0) = V_H$, $v(\delta) = V_{TH}$ and $\beta = \mu_n C_{ox}\frac{W}{L}$.

Notice that the second term in the right hand side of the differential equation is the current due to the NMOS device and depends on its size. Integrating this equation from $\boldsymbol{t = 0}$ to $\boldsymbol{t = \delta}$, we get

$$V_{TH} - V_H = \frac{I}{C}\delta - \frac{\beta \cdot I^2}{6 \cdot C^3}\delta^3 \quad (5)$$

After some algebraic manipulation with (2), (3) and (5), we have

$$x^3 + mx - n = 0 \quad (6)$$

where $x = \frac{I}{C}\delta$, $m = -\frac{12I}{\beta}$ and $n = \frac{6I}{\beta}(V_{TH} - V_L)$.

This is a cubic equation with one real root given by

$$\frac{I}{C}\delta = x = \sqrt[3]{\frac{n}{2} + \sqrt{\frac{n^2}{4} + \frac{m^3}{27}}} + \sqrt[3]{\frac{n}{2} - \sqrt{\frac{n^2}{4} + \frac{m^3}{27}}} \quad (7)$$

From (2) and (7), we have

$$\frac{I}{3 \cdot C}T = (V_{TH} - V_L) + \frac{I}{C}\delta =$$
$$(V_{TH} - V_L) + \sqrt[3]{\frac{n}{2} + \sqrt{\frac{n^2}{4} + \frac{m^3}{27}}} + \sqrt[3]{\frac{n}{2} - \sqrt{\frac{n^2}{4} + \frac{m^3}{27}}} \quad (8)$$

These give an exact formula for determining T. However, we prefer to simplify it by assuming that W/L is large enough so as to make $\boldsymbol{V_L \approx 0}$ and $\boldsymbol{n^2 >> m^3}$. Thus we have

$$f = \frac{1}{T} \approx \frac{I}{3 \cdot C} \times \frac{1}{V_{TH} + \sqrt[3]{6 \cdot I \cdot V_{TH} / \beta}}$$
$$\approx \frac{I}{3 \cdot C \cdot V_{TH}}\left(1 - \sqrt[3]{\frac{6I}{\beta \cdot V_{TH}^2}}\right) \quad (9)$$

We now see that the size of NMOS, or $\boldsymbol{\beta}$, gives rise to a nonlinear term in $\boldsymbol{f}$.

4. EXPERIMENTATION RESULT AND CONCLUSION

The circuit in Fig. 3 is simulated using Multisim Ver.7 with the following parameters: Level = 1, Vdd = 3V, W = 180um, L = 0.18um, V_{Th} = 0.7Volt, C = 1pF and Kp = 120u. Load current vary from 1nA to 1mA, with 0.1mA increment. The result waveform is shown in Fig.6 and Fig.7, indicating a good agreement with the theoretical analysis given in Section III.

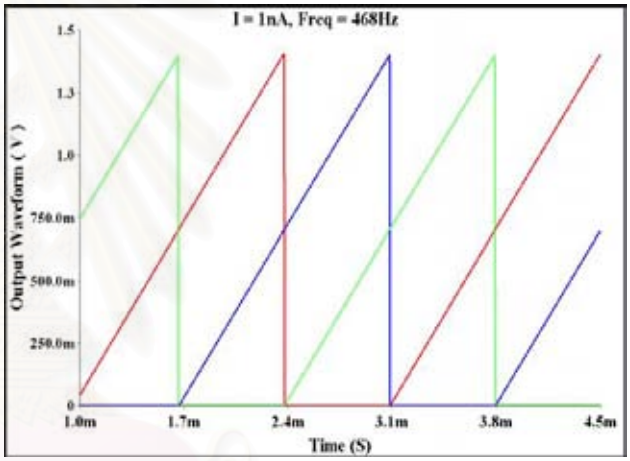

Fig. 6: *OutputWaveform, I = 1nA, Freq. = 468Hz.*

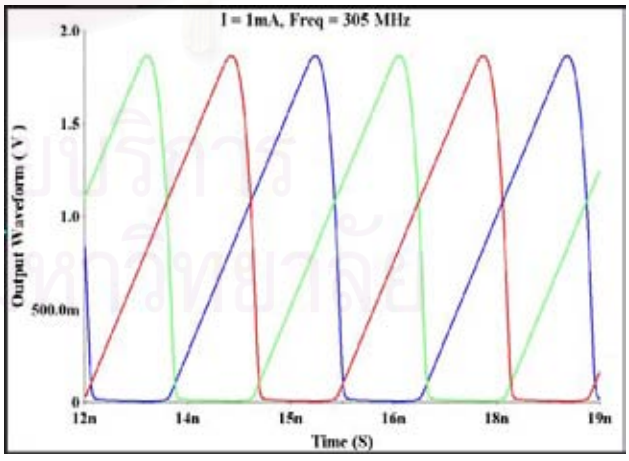

Fig.7: *Output Waveform, I = 1mA, Freq. = 305 MHz.*

The frequencies of the simulated waveform at different values of I are measured and plotted in Fig.8 compared with the predicted values from Eq. (1) and Eq. (9) to show their relation. The result showed a close

agreement with the analysis in the circle area or in the small load current.

Fig.9 gives a nonlinearity error that shows the error persentage of the difference between oscillating and prediction frequency, showing that the error increases linearly when load current increases. It shows also that the error decreases for higher W.

The effects of the size of the NMOS are shown in Fig.10. The result is getting closer to the prediction on the higher W or higher size.

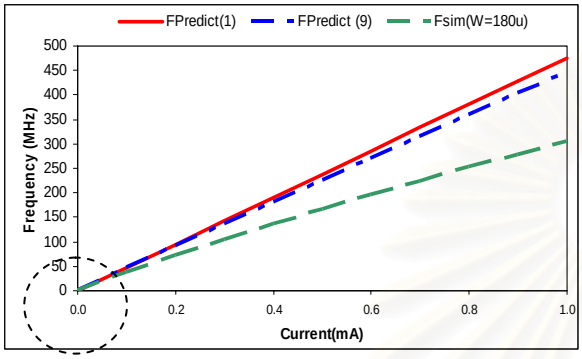

Fig. 8: *Measured Frequency Vs Predicted Frequency.*

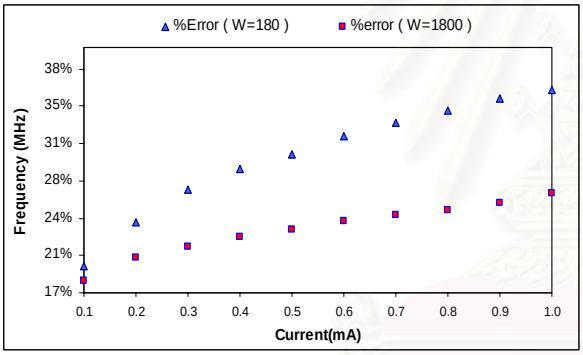

Fig. 9: *Measured Linearity of Error.*

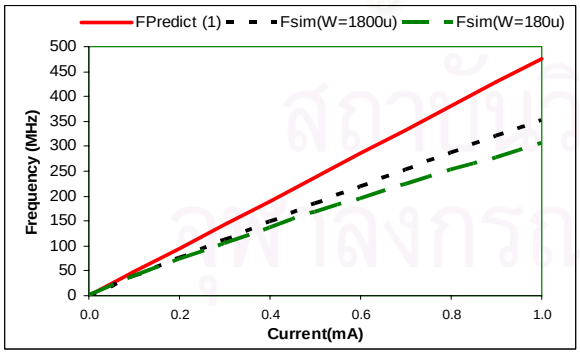

Fig. 10: *Effect of the Size of the NMOS.*

In conclusion, a CMOS 3-stage ring oscillator based on an inverting NMOS with current load is analyzed to obtain a formula for its frequency. The analysis shows that for large NMOS or small current, the frequency varies almost linearly with the load current.

This circuit has been simulated using load current from 1nA to 1mA, giving frequency output vary from 468-Hz ~ 305-MHz. The simulation result shows close agreements with the theoritical analysis. It shows that the error is bigger on the higher frequency / current, forming a linear plot. It shows also that the size of the NMOS affects the result, showing that the error is smaller on the higher NMOS size as predicted.

For the future work, considering other parameters in NMOS model is needed for simulation to obtain higher accuracy compared with analysis result.

5. ACKNOWLEDGEMENT

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BIOGRAPHY

Prapto Nugroho received the Bachelor degree in electrical engineering from Gadjah Mada University, Yogyakarta, Indonesia, in 2000, and is currently is an M.Eng student at Chulalongkorn University, Bangkok, Thailand.

From 2000 to 2002, he was a Test Engineer with the Yoshikawa Electronics Bintan, Indonesia where he was involved with IC Testing for OKI semiconductor and Texas Instruments's logic and mixed signal products.

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